

MERUS™ 400V Class D Audio Amplifier Controller

Features

- Single channel integrated analog input Class D audio amplifier driver
- 400V high voltage gate driver stage
- Differential or single-ended input
- Versatile protection control enabling latched, non-latched, or host-controlled shutdown function
- Programmable over current protection
- Programmable dead-time generation
- External thermal sensor input
- Click noise reduction
- Under voltage protection
- High noise immunity

Product summary

Product feature	Key Specification
Topology	Half-Bridge/ Full-Bridge
$V_{\text{OFFSET (max)}}$	+/- 200 V
$I_{\text{O+}}$ & $I_{\text{O-}}$ (typical)	0.5 A & 0.6 A
Selectable deadtime	165/225/280/340 ns
DC offset	<18 mV
OC protection delay	500 ns (max)
Shutdown propagation delay	250 ns (max)
Error amplifier open loop gain	>60 dB

Potential applications

- High voltage high power Class D audio amplifier
- High voltage high power PWM amplifier

Product validation

Qualified for industrial applications according to the relevant JEDEC47/20/22

Ordering information

Base Part Number	Package Type	Standard Pack Form and Quantity	
IRS2461S	20 Lead SOICWB	Tape and Reel	1000

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1 Description

The IRS2461S integrates high voltage, high performance Class D audio amplifier drivers with PWM modulator and protections. In conjunction with external MOSFET, the IRS2461S forms a single channel Class D audio amplifier. The IRS2461S is designed with floating analog inputs and protection control interface pins convenient for half bridge applications. High and low side MOSFETs are protected from over current conditions by a programmable over current protection. Essential elements of PWM modulator section allow flexible system design. The IRS2461S is a lead-free, ROHS compliant. The typical application diagram is shown in Figure 1.

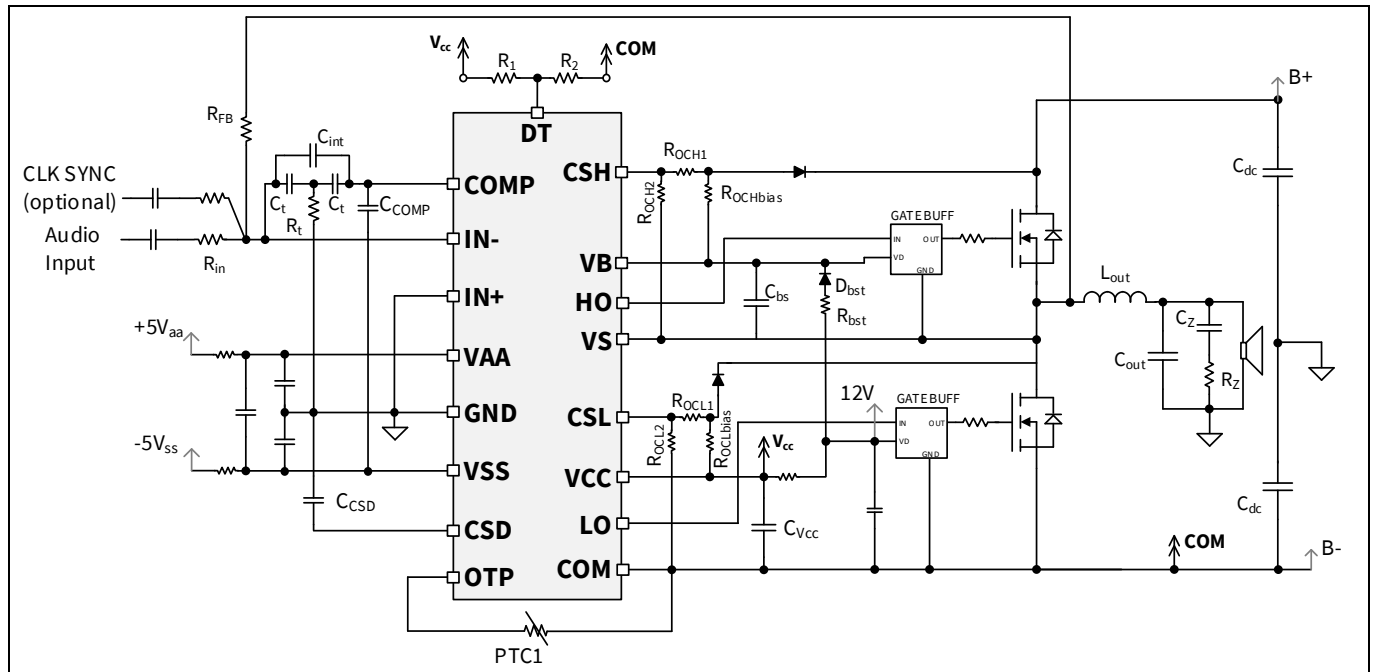


Figure 1 Typical application diagram

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2 Pin configuration and functionality

The pin configuration is shown in Figure 2 and the functions are described in Table 1.

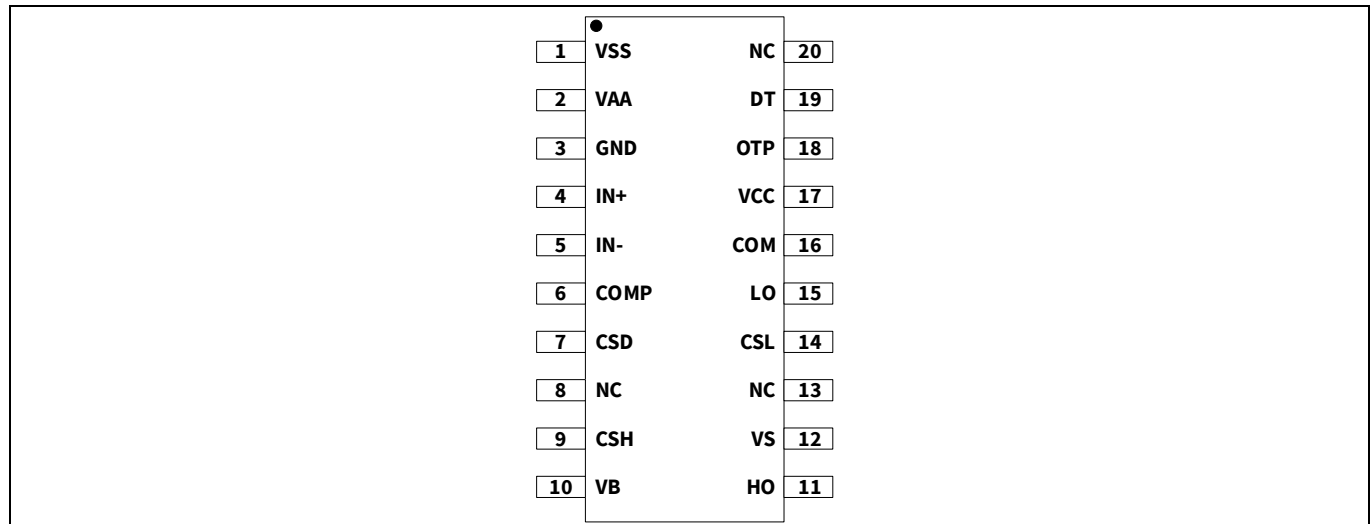


Figure 2 Pin configuration

Table 1 Pin definitions and functions

Pin	Symbol	Pin type	Function
1	VSS	Input	Floating input negative supply
2	VAA	Input	Floating input positive supply
3	GND	Input	Input reference GND
4	IN+	Input	Non-inverting analog input
5	IN-	Input	Inverting analog input
6	COMP	Input/output	PWM comparator input
7	CSD	Input/output	Protection control
8	NC	-	
9	CSH	Input	High side over current sensing input, referenced to VS
10	VB	Input	High side floating supply
11	HO	Output	High side output
12	VS	Input	High side floating supply return
13	NC	-	
14	CSL	Input	Low side over current sensing input, referenced to COM
15	LO	Output	Low side output
16	COM	Input	Low side gate drive supply return
17	VCC	Input	Low side gate drive supply
18	OTP	Input	OTP sensor input
19	DT	Input	Deadtime program, reference to COM
20	NC	-	

3 Functional block diagram

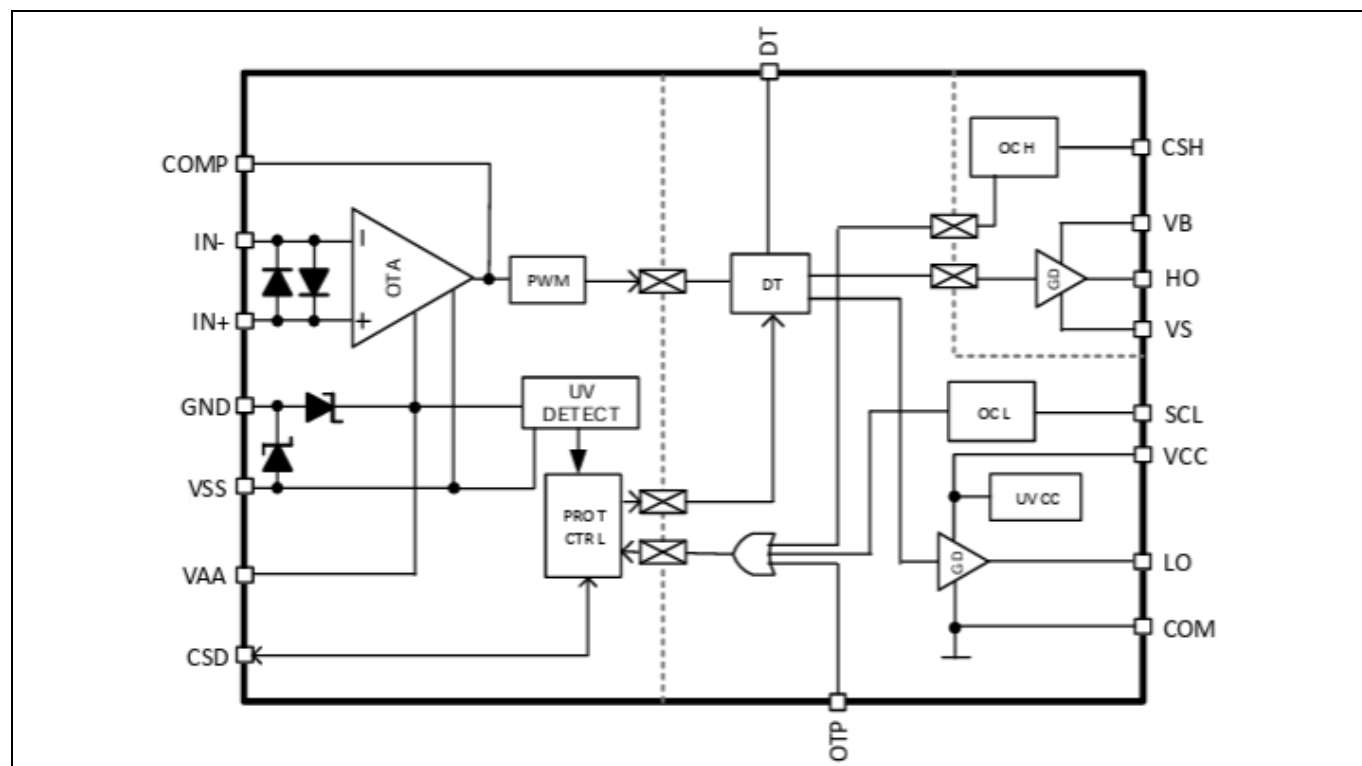


Figure 3 Functional block diagram

4 Qualification Information

Qualification Level		Industrial
Moisture Sensitivity Level		MSL3 (per IPC/JEDEC J-STD-020C)
ESD	Machine Model	Class B (per JEDEC standard EIA/JESD22-A115)
	Human Body Model	Class 1B (per EIA/JEDEC standard JESD22-A114)
	Charge Device Model	Class 0B (per EIA/JEDEC standard JESD22-C101)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

5 Characteristics

5.1 Package Characteristics

Symbol	Definition	Min	Max	Units
Pd	Maximum power dissipation @ $T_A \leq +25^{\circ}\text{C}^{\dagger\dagger\dagger}$	-	1.14	W
Rth _{JA}	Thermal resistance, Junction to ambient ^{†††}	-	65.8	$^{\circ}\text{C}/\text{W}$
T _J	Junction Temperature	-	150	$^{\circ}\text{C}$
T _S	Storage Temperature	-55	150	$^{\circ}\text{C}$
T _L	Lead temperature (Soldering, 10 seconds)	-	300	$^{\circ}\text{C}$

††† According to JESD51-5. JEDEC still air chamber.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM=VN; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V _B	High side floating supply voltage	-0.3	415	V
V _S	High side floating supply voltage ^{††}	V _{Bn} -15	V _{Bn} +0.3	V
V _{HO}	High side floating output voltage	V _{Sn} -0.3	V _{Bn} +0.3	V
V _{CSH}	CSH pin input voltage	V _{Sn} -0.3	V _{Bn} +0.3	V
V _{CC}	VCC low side fixed supply voltage ^{††}	-0.3	15.5	V
V _{LO}	Low side output voltage	-0.3	V _{CC} +0.3	V
V _{AA}	Floating input positive supply voltage ^{††}	(See I _{AAZ})	210	V
V _{SS}	Floating input negative supply voltage ^{††}	-1 (See I _{SSZ})	V _{AA} +0.3	V
V _{GND}	Floating input supply ground voltage	V _{SS} -0.3	V _{AA} +0.3	V
I _{IN-}	Inverting input current [†]	-	±3	mA
V _{CSD}	SD pin input voltage	V _{SS} -0.3	V _{AA} +0.3	V
V _{COMP}	COMP pin input voltage	V _{SS} -0.3	V _{AA} +0.3	V
V _{CLK}	CLK pin input voltage	V _{SS} -0.3	V _{AA} +0.3	V
V _{DT}	DT pin input voltage	-0.3	V _{CC} +0.3	V
V _{OTP}	OTP pin input voltage	-0.3	V _{CC} +0.3	V
V _{CSL}	CSL pin input voltage	-0.3	V _{CC} +0.3	V
I _{AAZ}	Floating input positive supply zener clamp current ^{††}	-	10	mA
I _{CCZ}	Low side VCC supply zener clamp current ^{††}	-	10	mA
I _{BSZ}	Floating supply zener clamp current ^{††}	-	10	mA
dV _S /dt	Allowable V _S voltage slew rate	-	50	V/ns
dV _{SS} /dt	Allowable V _{SS} voltage slew rate ^{†††}	-	50	V/ms

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† IN- contains clamping diode to GND.

†† VAA-VSS, VCC-COM, VCC2-COM2, VB-VS contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.

††† For the rising and falling edges of step signal of 10V. VSS=15V to 200V.

5.3 Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at VAA-VSS=10V, VCC =12V, and VB-VS=12V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition	Min	Max	Units
V_B	High side floating supply absolute voltage	$V_{Sn} + 10$	$V_{Sn} + 14$	V
V_S	High side floating supply offset voltage	(Note1)	400	V
V_{AA}	Floating input supply voltage	$V_{SS} + 4.5$	$V_{SS} + 15$	V
I_{AAZ}	Floating input positive supply zener clamp current	1	11	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	14	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{GND}	GND pin input voltage	V_{SS} (Note2)	V_{AA} (Note2)	V
V_{IN-}	Inverting input voltage	$V_{GND} - 0.5$ (Note2)	$V_{GND} + 0.5$ (Note2)	V
V_{CSD}	CSD pin input voltage	V_{SS}	V_{AA}	V
V_{COMP}	COMP pin input voltage	V_{SS}	V_{AA}	V
C_{COMP}	COMP pin phase compensation capacitor to GND	2.2	-	nF
V_{CLK}	CLK pin input voltage	V_{SS}	V_{AA}	V
V_{DT}	DT pin input voltage	0	V_{CC}	V
V_{OTP}	OTP pin input voltage	0	V_{CC}	V
V_{CSH}	CSH pin input voltage	V_{Sn}	V_{Bn}	V
V_{CSL}	CSL pin input voltage	0	V_{CC}	V
dV_{SS}/dt	Allowable V_{SS} voltage slew rate upon power-up (Note3)	-	50	V/ms
f_{SW}	Switching frequency	-	800	kHz
f_{CLK}	CLK frequency (Note4)	-	800	kHz
T_A	Ambient Temperature	-40	125	°C

(Note 1) Logic operational for Vs equal to -5V to +400V. Logic state held for Vs equal to -5V to -VBS.

(Note 2) GND input voltage is limited by IIN-n.

(Note 3) Vss ramps up from 0V to 200V.

(Note 4) The CLK input frequency needs to be within +/-10% of self-oscillating frequency in order to synchronize PWM in a typical self-oscillating application.

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5.4 Electrical Characteristics

VCC=VBS=VDT=12V, VSS=VS=COM=0V, VGND=5V, VAA=10V, CL=1nF and TA=25°C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply						
UV _{CC+}	V _{CC} supply UVLO positive threshold	8.4	8.9	9.4	V	
UV _{CC-}	V _{CC} supply UVLO negative threshold	8.2	8.7	9.2	V	
UV _{CCHYS}	UV _{CC} hysteresis	-	0.2	-	V	
I _{QCC}	Low side quiescent current	-	-	6	mA	V _{DT} =V _{CC}
V _{CLAMPL}	Low side zener diode clamp voltage	14.7	15.3	16.2	V	I _{CC} =5mA
High Side Floating Supply						
UV _{BS+}	High side well UVLO positive threshold	8.0	8.5	9.0	V	
UV _{BS-}	High side well UVLO negative threshold	7.8	8.3	8.8	V	
UV _{BSHYS}	UV _{BS} hysteresis	-	0.2	-	V	
I _{QBS}	High side quiescent current	-	-	1	mA	
I _{LKH}	High to Low side leakage current	-	-	50	μA	V _B =V _S =400V
V _{CLAMPH}	High side zener diode clamp voltage	14.7	15.3	16.2	V	I _{BS} =5mA
Floating Input Supply						
UV _{AA+}	V _{AA} floating supply UVLO positive threshold from V _{SS}	8.2	8.7	9.2	V	GND pin floating
UV _{AA-}	V _{AA} floating supply UVLO negative threshold from V _{SS}	7.7	8.2	8.7	V	GND pin floating
UV _{AAHYS}	UV _{AA} hysteresis	-	0.5	-	V	GND pin floating
I _{QAASD}	Floating Input positive quiescent supply current in shutdown mode	-	2	3	mA	V _{CSD} =V _{GND}
I _{QAA0}	Floating Input positive quiescent supply current, positive input	-	4	6	mA	V _{IN-} =V _{SS} +5.2V
I _{QAA1}	Floating Input positive quiescent supply current, negative input	-	3	4	mA	V _{IN-} =V _{SS} +4.8V
I _{QAAST}	Floating Input positive quiescent supply current in start-up mode	-	3	4	mA	V _{CSD} =V _{GND} +2.5V
I _{LKM}	Floating input side to Low side leakage current	-	-	50	μA	V _{AA} =V _{SS} =V _{GND} =100V
V _{CLAMPM}	Floating supply zener diode clamp voltage	14.7	15.3	16.2	V	I _{AA} =5mA, V _{CSD} =V _{GND}

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Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Audio Input (GND=0V, V _{AA} =5V, V _{SS} =-5V, COM =V _{CC} =-5V, V _S =CSH=-5V, DT=-5V)						
V _{Os}	Input offset voltage	-18	0	18	mV	
I _{BIN}	Input bias current	-	-	40	nA	
GBW	Small signal bandwidth	-	5 Note 1	-	MHz	C _{COMPn} =2.2nF, R _f =10k, Note 1
V _{COMP}	OTA Output voltage	V _{AA} -1	-	V _{SS} +1	V	
g _m	OTA transconductance	80	200	260	mS	V _{IN} =10mV
G _V	OTA gain	60	-	-	dB	
V _{Nrms}	OTA input noise voltage	-	250	-	mVrms	BW=20kHz, Resolution BW=22Hz Fig.8
SR	Slew rate	-	±5	-	V/us	C _{COMP} =2.2nF
CMRR	Common-mode rejection ratio	-	60	-	dB	
PSRR	Supply voltage rejection ratio	-	65	-	dB	
PWM Comparator						
V _{thPWM}	PWM comparator threshold in COMP	-	(V _{AA} - V _{SS})/2	-	V	
f _{OTA}	COMP pin star-up local oscillation frequency	-	0.6	-	MHz	V _{CSD} =V _{GND} +2.5V
Protection						
V _{thOCL}	Low side OC threshold in V _{CSL}	1.1	1.2	1.3	V	
V _{thOCH}	High side OC threshold in V _{CSH}	1.1+ V _S	1.2+ V _S	1.3+ V _S	V	V _S =400V
V _{th1}	CSD pin shutdown release threshold	0.52xV _{AA-GND}	0.68xV _{AA-GND}	0.84xV _{AA-GND}	V	
V _{th2}	CSD pin self reset threshold	0.26xV _{AA-GND}	0.30xV _{AA-GND}	0.34xV _{AA-GND}	V	
I _{CSD+}	CSD pin discharge current	70	100	130	μA	V _{CSD} = V _{GND} + 2.4V
I _{CSD-}	CSD pin charge current	70	100	130	μA	V _{CSD} = V _{GND} + 2.4V
t _{SSD}	Shutdown propagation delay from V _{CSD} < V _{GND} + V _{th1} to Shutdown	-	140	250	ns	
t _{OCH}	Propagation delay time from V _{CSHn} > V _{thOCHn} to Shutdown	-	400	500	ns	
t _{OCL}	Propagation delay time from V _{sn} > V _{thOCL} to Shutdown	-	270	350	ns	
V _{OTP}	OTP pin input threshold	-	2.8	-	V	
I _{OTP}	OTP bias sourcing current	-	0.6	-	mA	OTP=0V

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Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver						
I _{o+}	Output high short circuit current (Source)	-	0.5	-	A	V _o =0V, PW≤10μS, Note 1
I _{o-}	Output low short circuit current (Sink)	-	0.6	-	A	V _o =12V, PW≤10μS, Note 1
V _{OL}	Low level output voltage LO – COM, HO – VS	-	-	0.1	V	I _o =0A
V _{OH}	High level output voltage VCC – LO, VB – HO	-	-	1.4	V	
Ton0	High and low side turn-on propagation delay	-	505	-	ns	V _{DT} = V _{CC}
Toff0	High and low side turn-off propagation delay	270	340	410	ns	
t _r	Turn-on rise time	-	12	25	ns	
t _f	Turn-off fall time	-	12	25	ns	
DT1	Deadtime: LOn turn-off to HOn turn-on (DT _{LO-HO}) & HOn turn-off to LOn turn-on (DT _{HO-LO})	130	165	200	ns	V _{DT} >V _{DT1} , V _{DTM} =COM
DT2	Deadtime: LOn turn-off to HOn turn-on (DT _{LO-HO}) & HOn turn-off to LOn turn-on (DT _{HO-LO})	180	225	270	ns	V _{DT1} >V _{DT} >V _{DT2} , V _{DTM} =COM
DT3	Deadtime: LOn turn-off to HOn turn-on (DT _{LO-HO}) & HOn turn-off to LOn turn-on (DT _{HO-LO})	225	280	335	ns	V _{DT2} >V _{DT} >V _{DT3} , V _{DTM} =COM
DT4	Deadtime: LOn turn-off to HOn turn-on (DT _{LO-HO}) & HO turn-off to LOn turn-on (DT _{HO-LO}) V _{DT} = V _{DT4}	275	340	405	ns	V _{DT} <V _{DT3} , V _{DTM} =COM
V _{DT1}	DT mode select threshold 1	0.51xV _{CC}	0.57xV _{CC}	0.63xV _{CC}	V	V _{DTM} =COM
V _{DT2}	DT mode select threshold 2	0.32xV _{CC}	0.36xV _{CC}	0.40xV _{CC}	V	
V _{DT3}	DT mode select threshold 3	0.21xV _{CC}	0.23xV _{CC}	0.25xV _{CC}	V	

Note 1 Guaranteed by design, but not tested in production.

5.5 Waveform definitions

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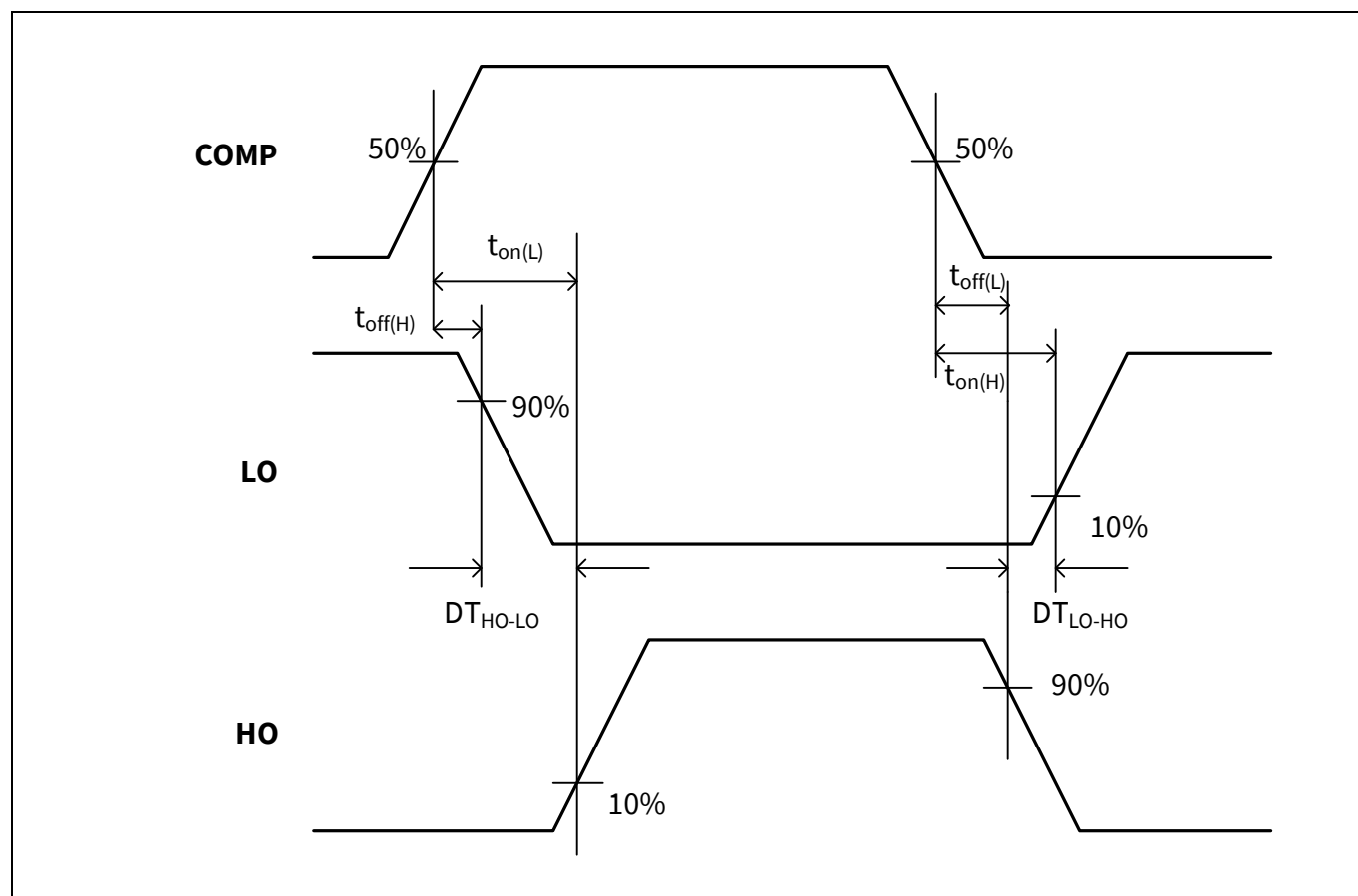


Figure 4 Switching time waveform definitions

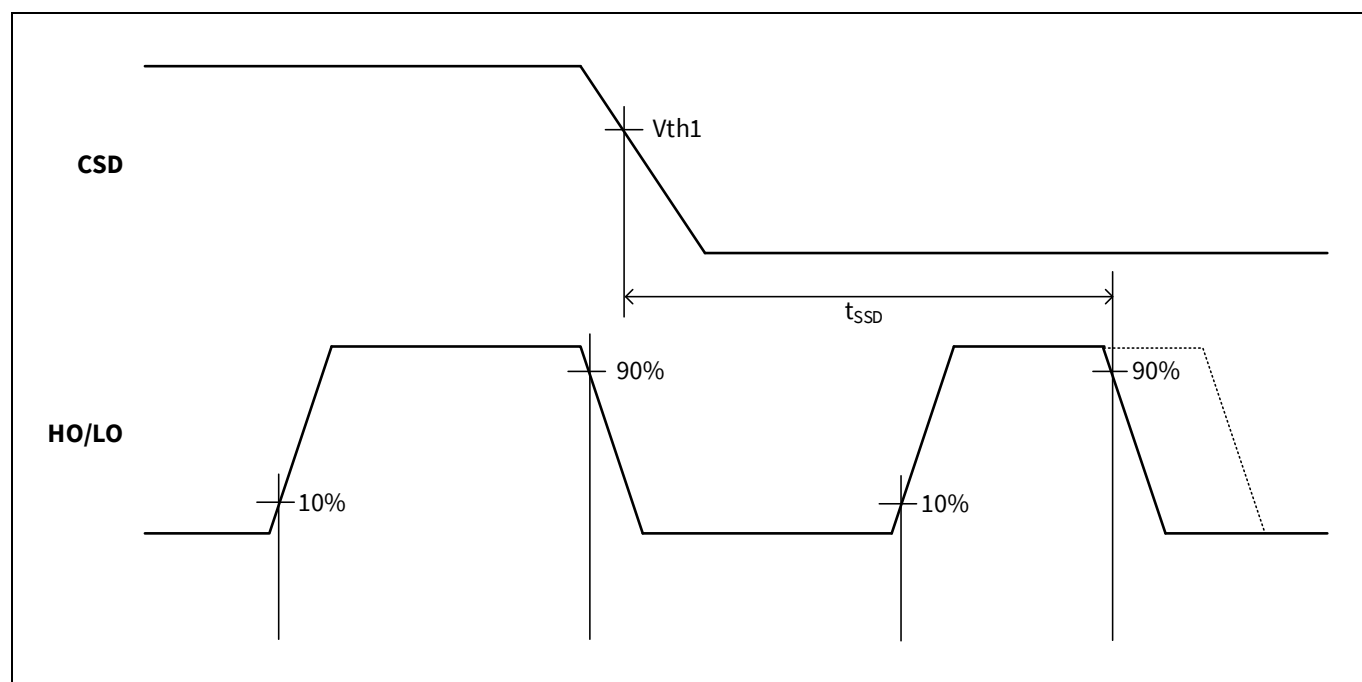
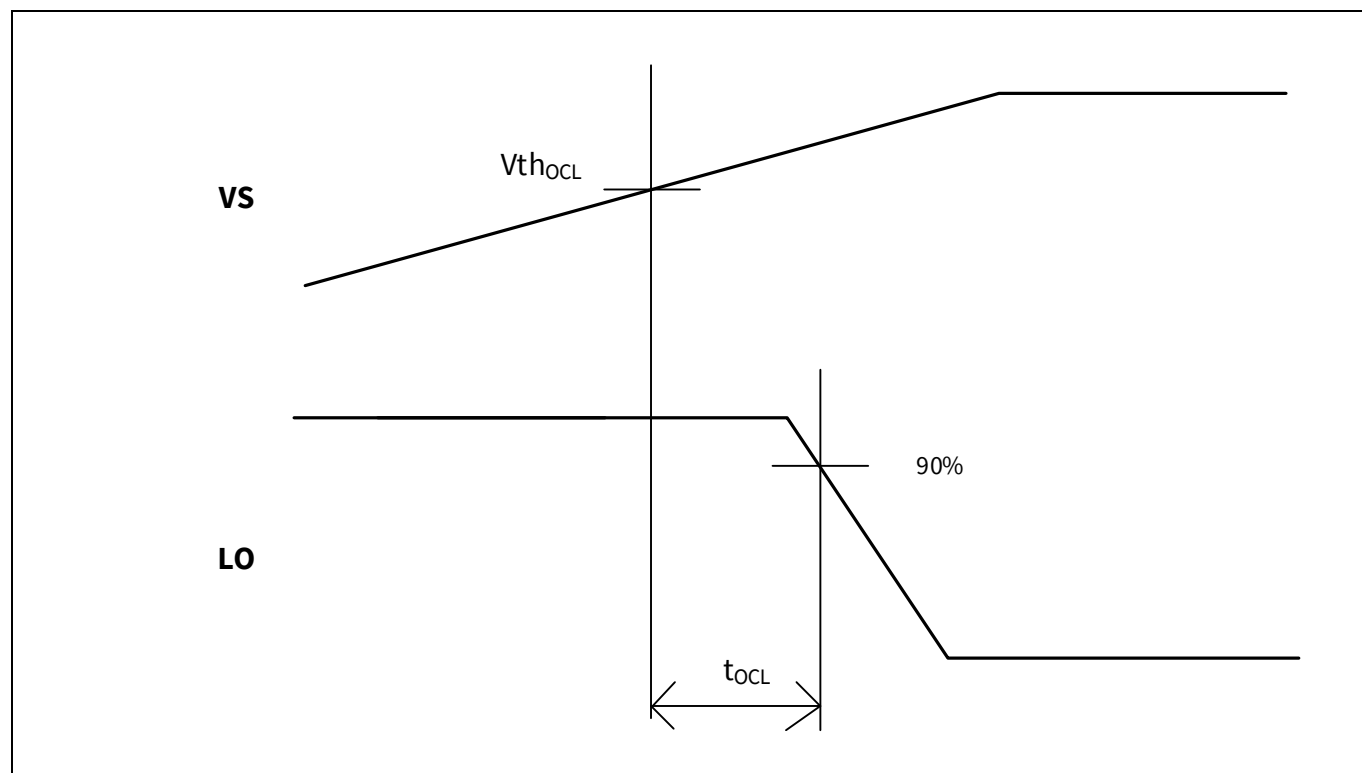
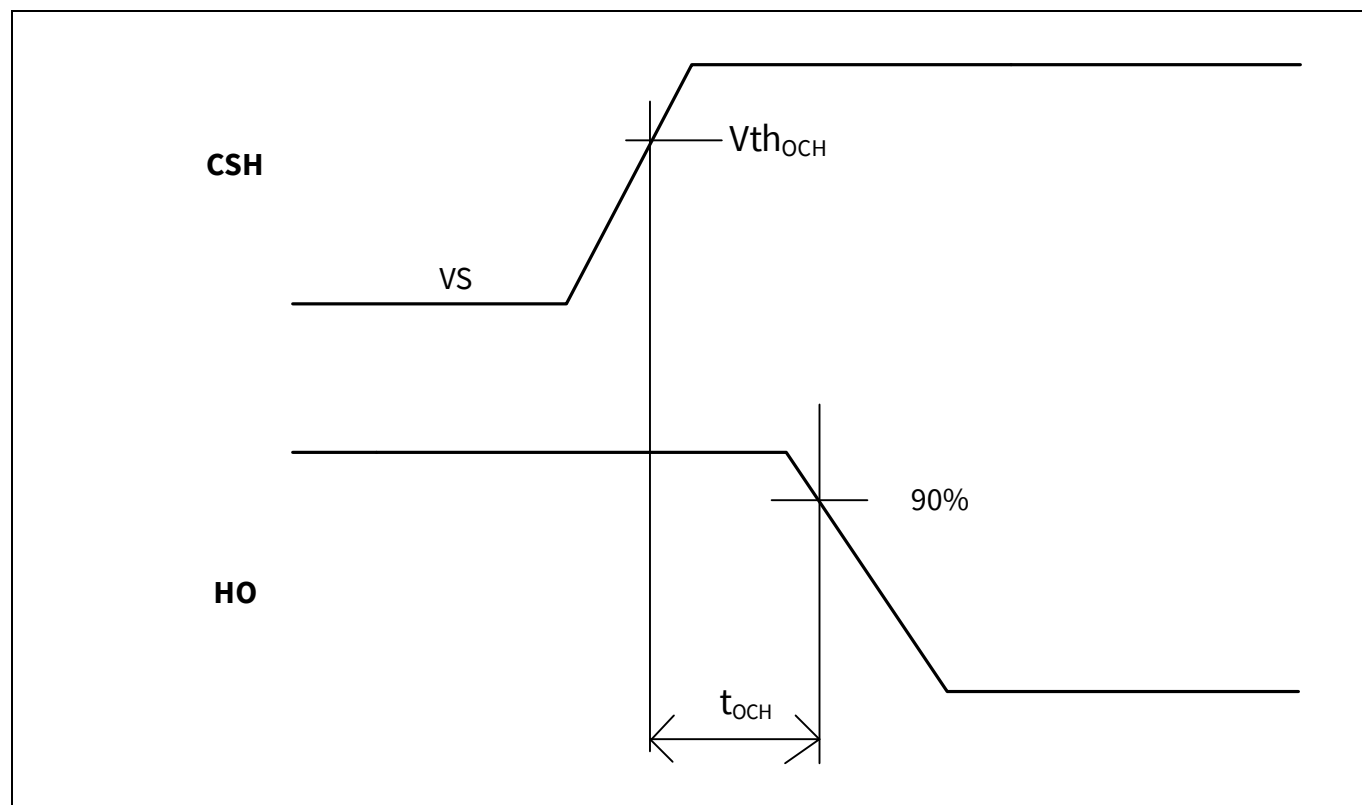


Figure 5 CSD to shutdown waveform definitions

**Figure 6** $V_S > V_{th_{OCL}}$ to shutdown waveform**Figure 7** $V_{CSH} > V_{th_{OCH}}$ to shutdown waveform

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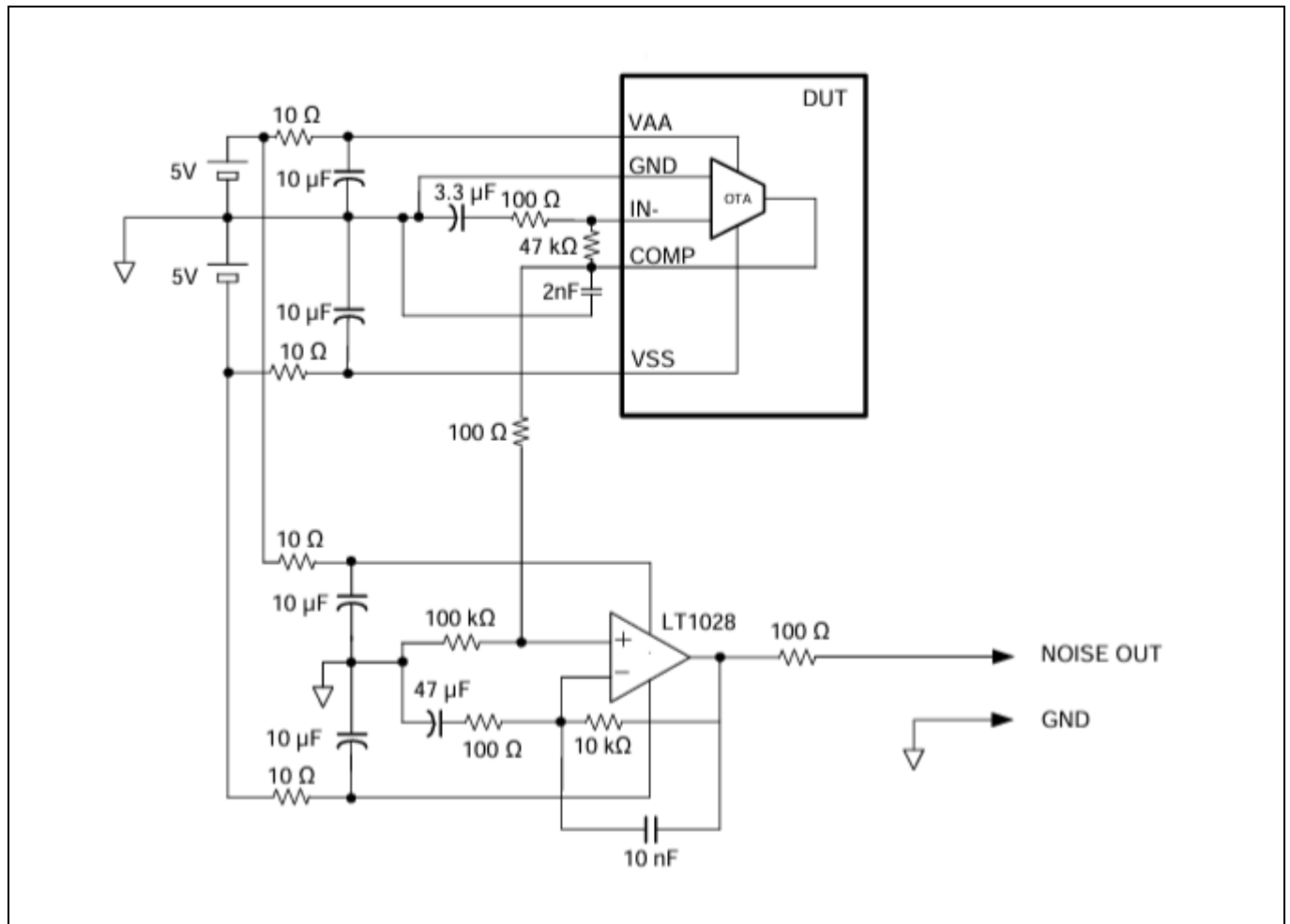


Figure 8 **OTA input noise voltage measurement circuit**

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6 General description

The IRS2461S is a single channel Class D audio amplifier driver rated at 400V with integrated PWM modulators and over current protection. Combined with four external MOSFETs and passive components, the IRS2461S forms a high voltage analog input Class D amplifier. The versatile structure of the analog input section with an error amplifier and a PWM comparator offer flexibility for implementing different types of PWM modulator schemes.

Loss-less current sensing utilizes the RDS(on) of the MOSFETs. The protection control logic monitors the status of the power supplies and load current through each MOSFET.

With the convenience of a half bridge configuration, the differential input analog PWM modulator and protection logic interface are floated from the main power supply.

The IRS2461S, shown in Figure 9, is equipped with start-up click noise reduction to suppress unwanted audible noise during PWM start-up and shutdown. A 20 lead SOIC package enhances the benefits realized by a small size Class D topology. To evaluate IRS2461S in a design, please refer to Reference Design REF_IRS2461S_5KW.

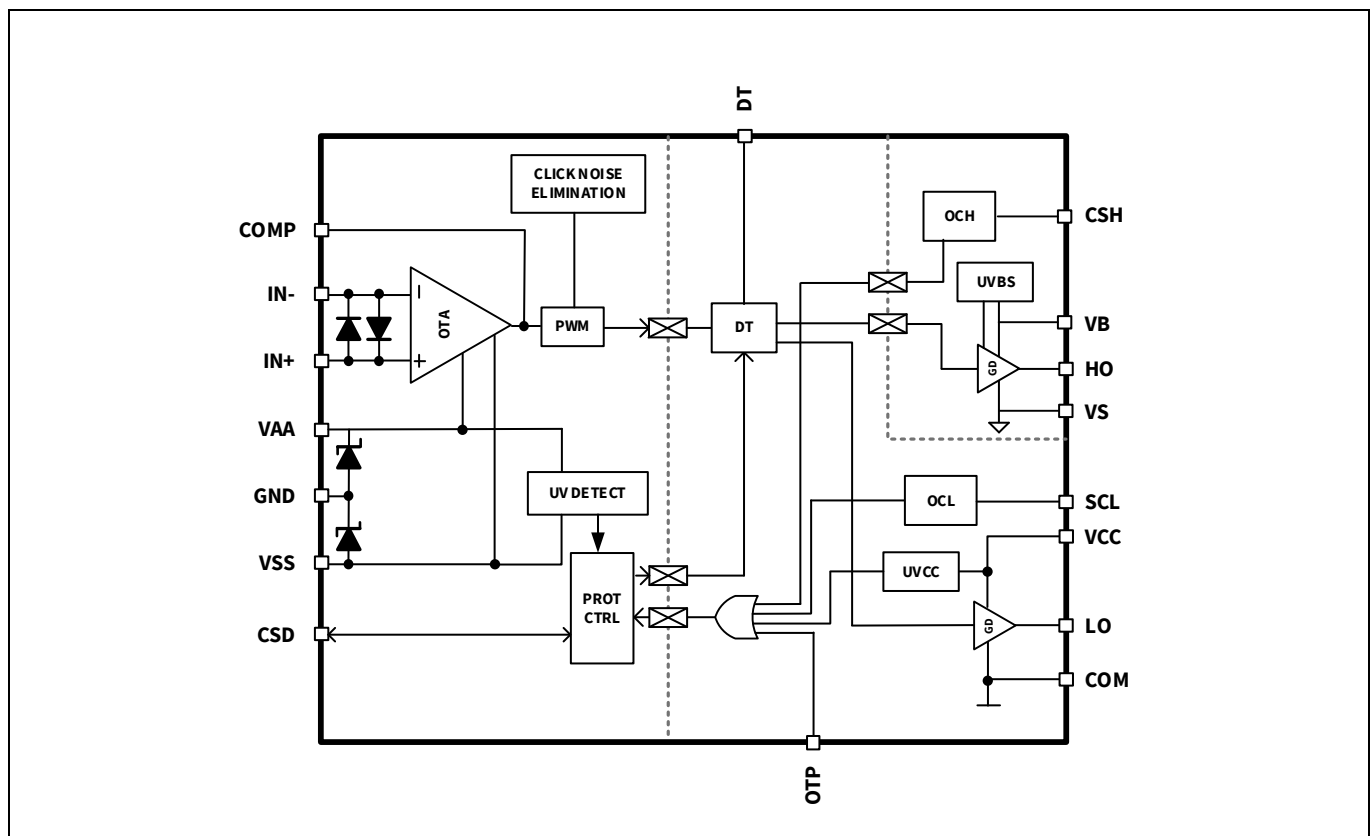


Figure 9 Functional block diagram of IRS2461S

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7 PWM modulator design

The open access frontend structure of the IRS2461S offers many ways to implement a PWM modulator. The following explanations are based on a typical application circuit with self-oscillating PWM topology shown in figure 2. For further information on the design, refer to the REF_IRS2461S_5KW.

7.1 Input section

7.1.1 Unbalanced input

The audio input stage forms an inverting error amplifier as shown in Figure 10. The voltage gain of the amplifier, G_V , is determined by the ratio between input resistor R_{IN} and feedback resistor R_{FB} .

$$G_V = \frac{R_{FB}}{R_{IN}}$$

Since the feedback resistor R_{FB} is part of an integrator time constant, which determines switching frequency, changing the overall voltage gain by R_{IN} is simpler and therefore recommended. Note that the input impedance of the amplifier is equal to the input resistor R_{IN} .

A DC blocking capacitor $C3$ should be connected in series with R_{IN} to minimize the DC offset voltage in the output. Due to potential distortion, a ceramic capacitor is not recommended. Reducing the DC offset is essential to minimize the audible noise during power ON and OFF.

The connection of the non-inverting input $IN+$ is a reference for the error amplifier, and thus is crucial for audio performance. Connect $IN+$ to the signal reference ground in the system, which has the same potential as the negative terminal of the speaker output.

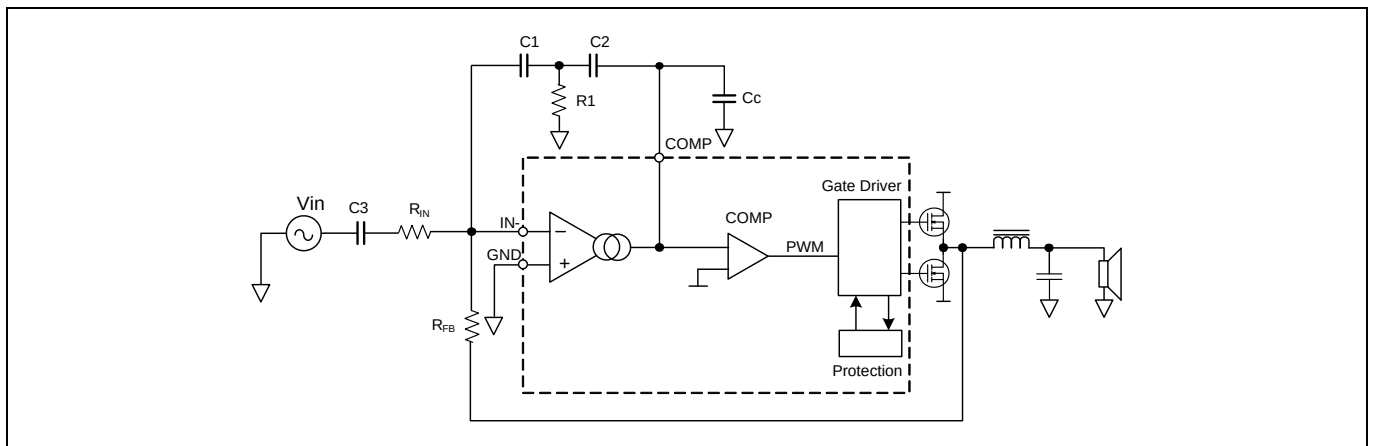


Figure 10 IRS2461S typical control loop design

7.1.2 Differential input

Figure 11 shows an example of a differential input configuration. This design is useful in a single supply configuration. Use $R_{IN1}=R_{IN2}$, $R_{FB1}=R_{FB2}$, $C3=C4$.

Voltage gain is given by a ratio between R_{IN} and R_{FB} .

$$G_V = \frac{R_{FB}}{R_{IN}}$$

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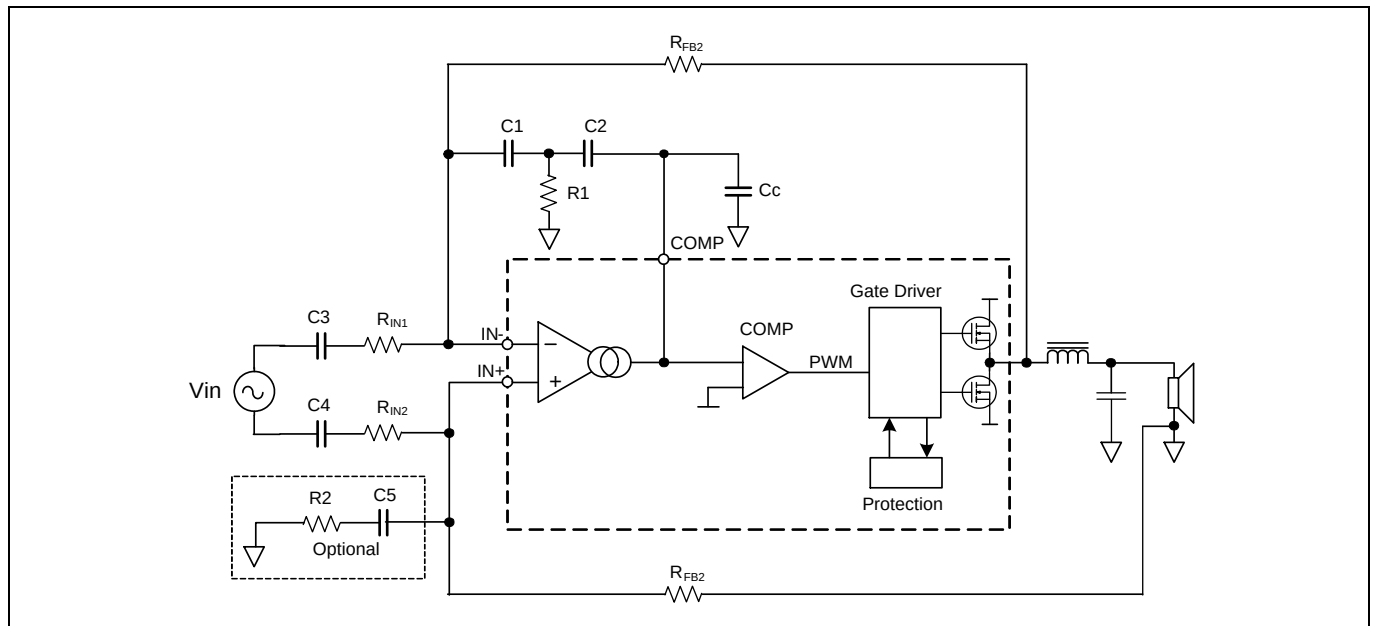


Figure 11 Differential input

Although component values in the feedback network are balanced between inverting and non-inverting inputs, the integration capacitor path in the non-inverting input creates an unbalance at high frequencies, causing slightly higher distortion compared to an unbalanced input configuration. To improve the THD degradation, place an optional RC network $R2=R1$ and $C5=C1$.

7.1.3 OTA (Operational Transconductance Amplifier)

The front-end error amplifier of the IRS2461S features an operational transconductance amplifier (OTA), which is designed to obtain optimal audio performance. The OTA outputs a current to the COMP pin, unlike a voltage output in an operational amplifier (OPA).

The inverting and non-inverting inputs have clamping diodes to improve recovery from clipping as well as ensuring stable start up. The OTA output COMP is internally connected to the PWM comparator with a threshold of $(V_{AA}-V_{SS})/2$.

For stable operation of the OTA, a compensation capacitor C_c of minimum 2.2 nF is required. The OTA shuts down when $V_{CSD} < V_{th2}$.

7.1.4 Pop-less startup

The IRS2461S has a unique feature that minimizes the audible click noise at start and stop. When CSD is in between V_{th1} and V_{th2} during start up, an internal closed loop around the OTA enables an oscillation that generates voltages at COMP and IN-, bringing them to steady state values. It runs at around 1 MHz, independent from the switching oscillation.

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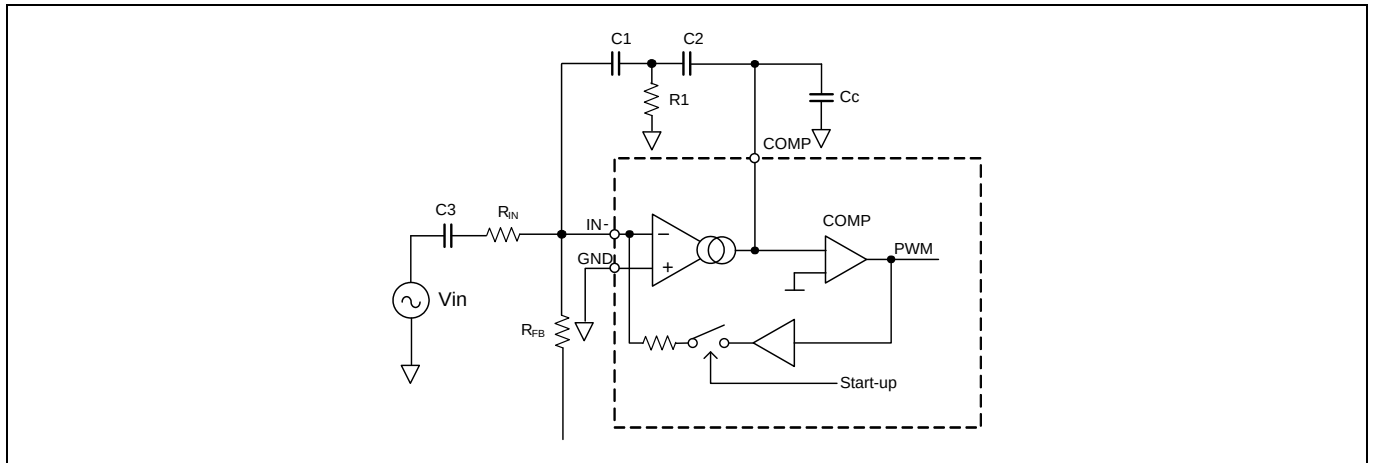


Figure 12 Audible click noise elimination

As a result, all capacitive components connected to COMP and IN- pins, such as C1, C2, C3 and Cc in Figure 12, are pre-charged to their steady state values during the startup sequence. This allows instant settling of PWM operation.

To utilize the click noise reduction function, the following conditions must be met:

1. The CSD pin has slow enough ramp up from Vth1 to Vth2 such that the voltages in the capacitors can settle to their target values.
2. The high-side bootstrap power supply needs to be charged up prior to starting oscillation.
3. The audio input has to be zero.
4. For the internal local loop to override external feedback during the startup period, DC offset at the speaker output prior to shutdown release has to satisfy the following condition:

$$DCoffset < 30\mu A \cdot R_{FB}$$

For minimum click noise it is recommended not to start synchronous clock during pop-less startup period.

7.2 Control loop design

The IRS2461S allows the user to choose from numerous ways of PWM modulator implementations. In this section, all the explanations are based on typical application circuits of a self-oscillating PWM.

7.3 PWM frequency

Choosing idling switching frequency entails making a tradeoff between many aspects. At lower switching frequencies, the conduction losses in the MOSFET stage increases due to higher inductor ripple current. The output carrier leakage in the speaker output increases. At higher switching frequency, the efficiency degrades due to higher switching losses. Higher switching frequency supports wider audio bandwidth. The reduced inductor ripple current slows down the zero-volt switching (ZVS) operation therefore increasing the minimum deadtime required for efficient idling operation. For these reasons, 320 kHz is chosen as a typical design example in the REF_IRS2461S_5KW.

Self-oscillating frequency is determined mainly by the following items in Figure 10.

- Integration capacitors, C1 and C2
- Integration resistor, R1
- Propagation delay in the gate driver
- Feedback resistor, RFB

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- Duty cycle

Note that the nature of a self-oscillating PWM is for the switching frequency to decrease as the PWM modulation deviates from idling.

Table 2 summarizes suggested values of components for a given target self-oscillating frequency. The front-end operational transconductance amplifier (OTA) output has limited voltage and current compliances. This set of component values ensures that OTA operates within its linear region for optimal THD+N performance. In case the target frequency is somewhere in between the frequencies listed in Table 2, simply adjust the frequency by tuning R1.

Table 2 External component values vs. self-oscillation frequency

Target self-oscillation frequency (kHz)	C1 = C2 (nF)	Cc (nF)	R1 (Ohms)
400	3.3	2.2	131
350	3.3	2.2	97
300	3.3	2.2	78
250	3.3	2.2	69
200	3.3	2.2	64

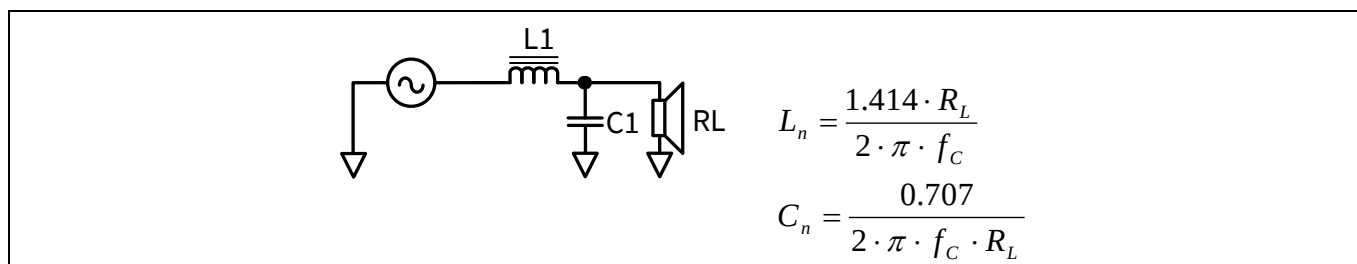
7.4 Output LPF

The output low pass filter (LPF) demodulates the amplified audio signal. It is also necessary for efficient operation of a Class D amplifier; therefore, selecting the right components is critical for both audio performance and system efficiency.

A typical output LPF uses a second order Butterworth LC filter designed to achieve maximum flat frequency response up to a corner frequency with nominal load impedance. Figure 13 explains how to calculate the component values for a load impedance. The corner frequency should be set according to the bandwidth requirement. A corner frequency of 40 kHz would be a good tradeoff point between 20 kHz bandwidth, inductor ripple current, and inductance in other words the size of the inductor and the PWM carrier leak amplitude in the output. Note that the higher the corner frequency the higher the switching carrier leakage, and the lower the corner frequency the bigger the inductor size.

The inductance of the inductor changes with load current bias, which causes distortion in audio output. Core saturation increases the inductor ripple significantly which could trigger the over current protection immediately. Use an inductor with a saturation point that is higher than the peak load current. Consider the I_{RMS} rating of an inductor for temperature rise condition with 1/8 rated power and peak current for maximum load current.

Use a capacitor which meets AC voltage ratings at the highest audio frequency output. Use a film capacitor with lower series inductance structure type. Ceramic capacitors could add audio distortion from the strong bias voltage dependency in capacitance; this is especially demonstrated in high dielectric coefficient ceramic capacitors such as Y5V.

**Figure 13** Output LPF design

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8 Operational mode

The CSD pin determines the operational mode of the IRS2461S as shown in Figure 14. The OTA has three operational modes: cut off, local oscillation and normal operation; while the gate driver section has two modes: shutdown and normal operation.

When $V_{CSD} < V_{th2}$, the IC is in shutdown mode and the OTA is cut off. When $V_{th2} < V_{CSD} < V_{th1}$, the HO and LO outputs are still in shutdown mode. The OTA is activated and starts local oscillation for pop-less start-up which pre-biases all the capacitive components in the error amplifier. When $V_{CSD} > V_{th1}$, the shutdown is released and PWM operation starts.

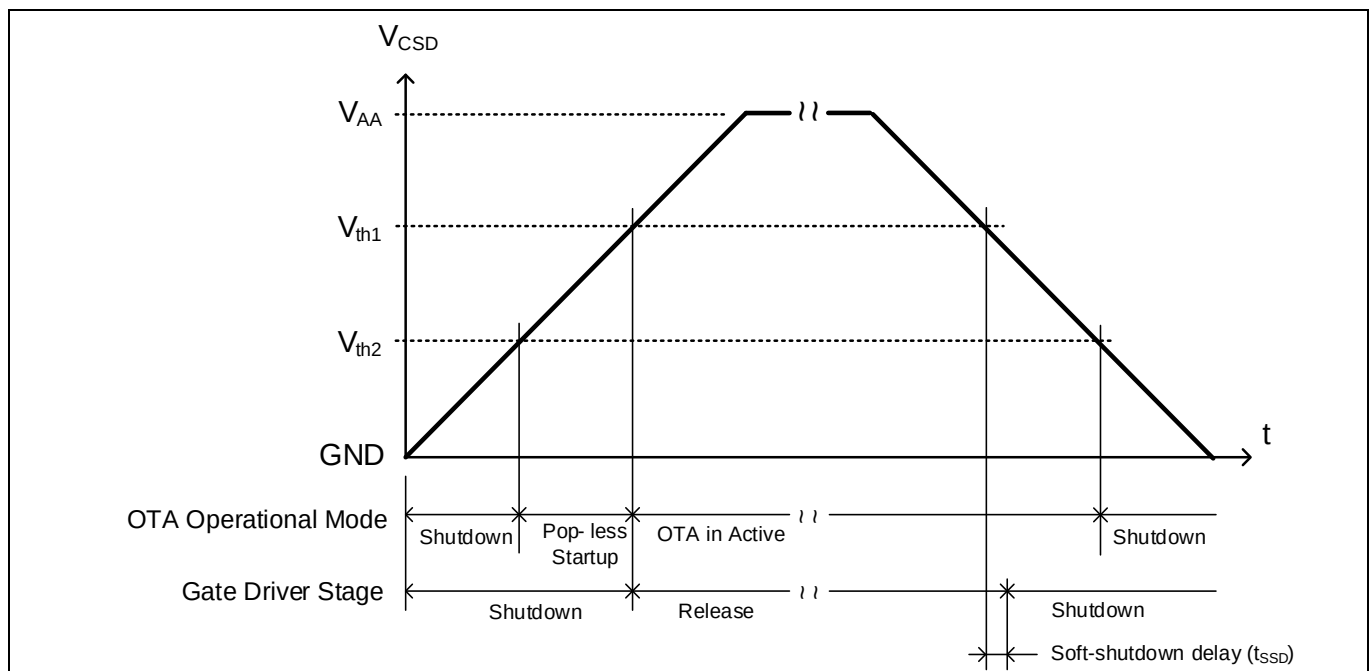


Figure 14 V_{CSD} and operational mode

8.1 Self-oscillation start-up condition

The IRS2461S requires the following conditions be met in order for pop-less startup to work properly.

- All the control power supplies (V_{AA}, V_{SS}, V_{CC} and V_{BS}) are above the under-voltage lockout thresholds.
- The CSD pin voltage is over the V_{th1} threshold.
- $|i_{IN}| < |i_{FB}|$

$$\text{Where } i_{IN} = \frac{V_{IN}}{R_{IN}}, i_{FB} = \frac{V_{+B}}{R_{FB}}.$$

- The duration of the CSD voltage transitioning from V_{th2} to V_{th1} is long enough to pre-charge the input and integration capacitors around OTA section.

9 Deadtime setting

9.1 Determining required deadtime

Deadtime is the blanking period inserted between high-side and low-side ON duration. Deadtime serves two purposes: to prevent shoot-through at any time and to ensure zero voltage switching (ZVS) at idling.

The internal dead time generation block allows the user to select the optimum dead time from a range of preset values. An external voltage divider selects a preset dead time through the DT pin voltage. The selectable dead time setting prevents incoming noise modulating the switching timing, which is critical to the audio performance.

An effective deadtime in MOSFET gate bias voltage differs from the deadtime specified in the datasheet. The deadtime value in the datasheet is defined as the time period between the beginning of transition on one side of the output to the other side as shown in Figure 15. The fall time of the MOSFET gate voltage must be subtracted from the deadtime value in the datasheet to determine the effective deadtime of a Class D audio amplifier.

$$(\text{Effective deadtime}) = (\text{Deadtime in datasheet}) - t_f$$

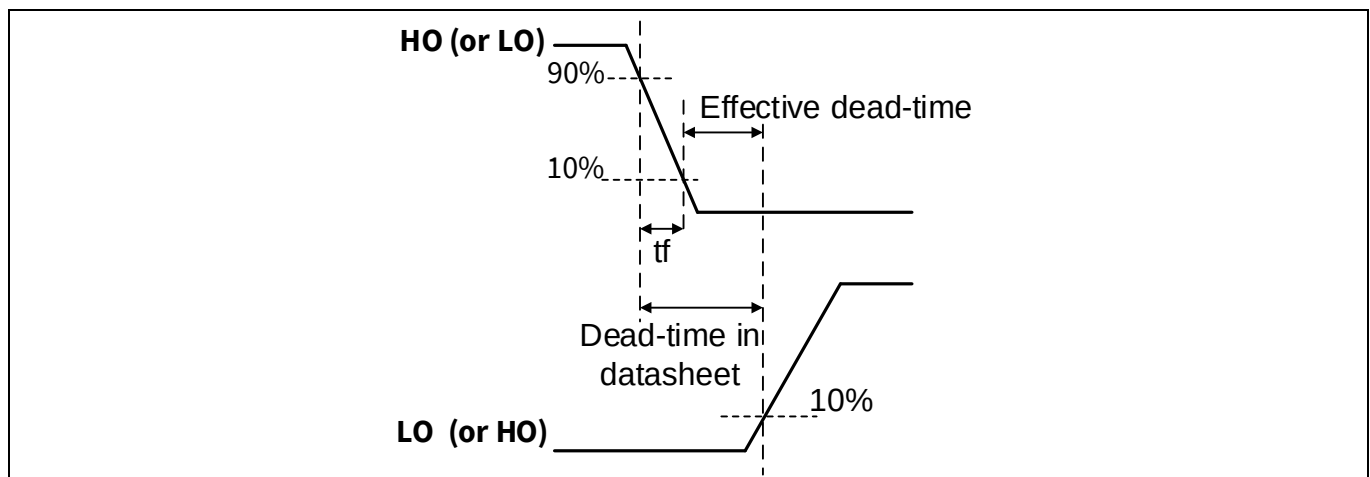


Figure 15 Effective dead-time

A longer deadtime period is required for a MOSFET with a larger gate charge value because of the longer t_f . Negative values of effective deadtime cause excessive heat dissipation in the MOSFETs, leading to potential damage so they should always be avoided. Therefore, effective deadtime determines the minimum deadtime a design can take.

In a practical design, efficient operation at idling is important to minimize idling power loss. Setting a deadtime for zero volt switching (ZVS) operation ensures minimum idling power consumption. A time duration required to complete the voltage transition, t_{ZVS} , is a function of output inductor current, total MOSFET output capacitance in VS node, C_o , and output inductance in the LC LPF.

$$t_{ZVS} = 8 \cdot C_o \cdot f_{sw} \cdot L$$

where C_o : total capacitance in VS node = $2 \cdot C_{oss}$, use time constant equivalent C_{oss}

f_{sw} : PWM frequency

L : output inductor inductance

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Select a deadtime window such that minimum effective deadtime is longer than t_{ZVS} as shown in Figure 16.

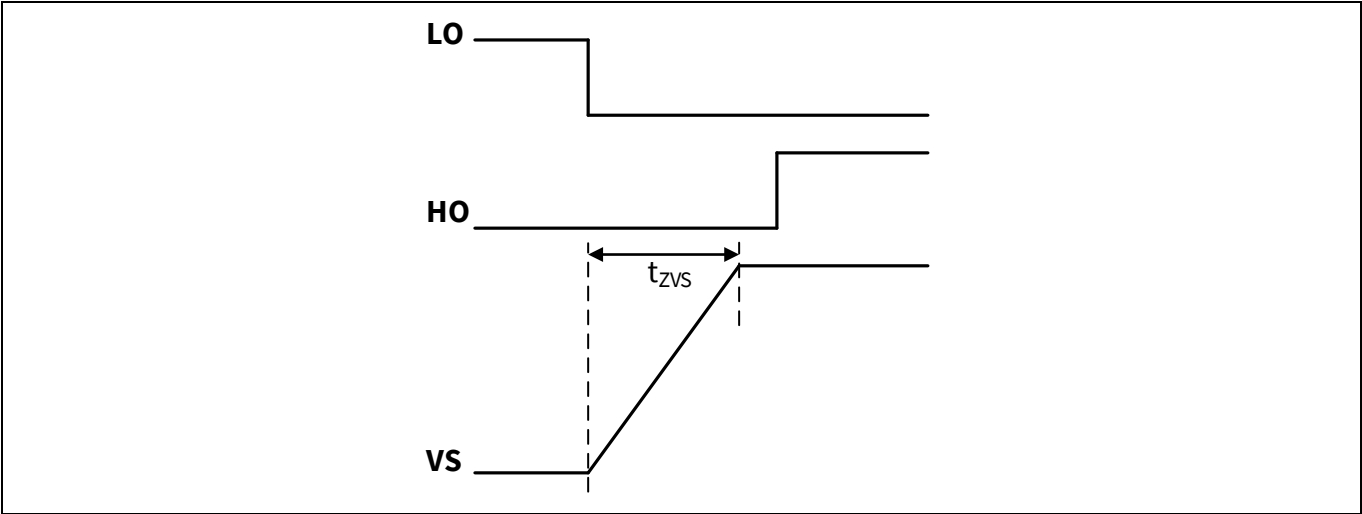


Figure 16 ZVS during dead-time (deadtime > t_{ZVS})

9.2 Programming deadtime

The IRS2461S selects the deadtime from a range of preset deadtime values based on the voltage applied at the DT pin. An internal comparator translates the DT input to a predetermined deadtime by comparing the input with internal reference voltages. These internal reference voltages are set in the IC through a resistive voltage divider using VCC. The relationship between the operation mode and the voltage at DT pin is illustrated in Figure 17 below.

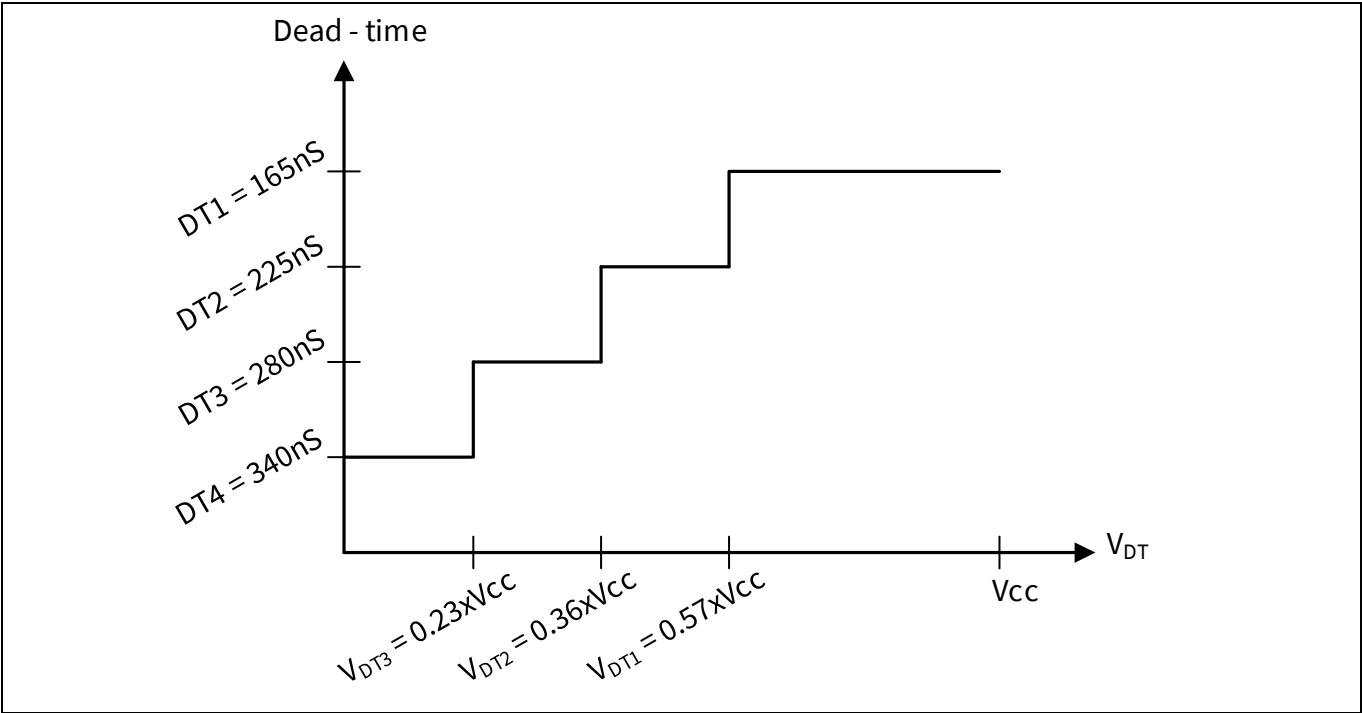


Figure 17 Dead-time vs. V_{DT}

Table 3 suggests pairs of resistor values used in the voltage divider for selecting deadtime. Resistors with up to 5% tolerance are acceptable when using these values.

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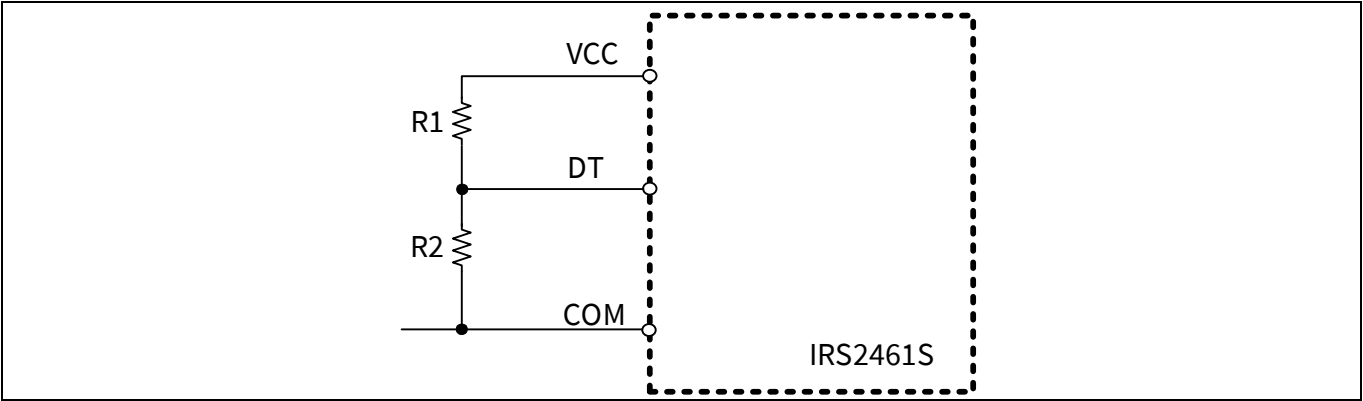


Figure 18 External voltage divider for DT pin

Table 3 Recommended resistor values for dead-time selection

Deadtime mode	R1	R2	DT voltage
DT1	<10k	Open	Vcc
DT2	5.6 kΩ	4.7 kΩ	0.46 x Vcc
DT3	8.2 kΩ	3.3 kΩ	0.29 x Vcc
DT4	Open	<10 kΩ	COM

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10 Adding gate drive buffer

The built-in gate driver with 0.5A output can drive a MOSFET with $Q_g < 20$ nC. In order to drive a MOSFET with a larger Q_g , it is recommended to use a gate drive buffer to boost the output current. Due to the over current sensing monitoring the V_{DS} when the MOSFET is on, propagation delay in the gate buffer needs to be less than 50 ns to prevent false triggering.

Figure 19 explains how to add a buffer using BJTs.

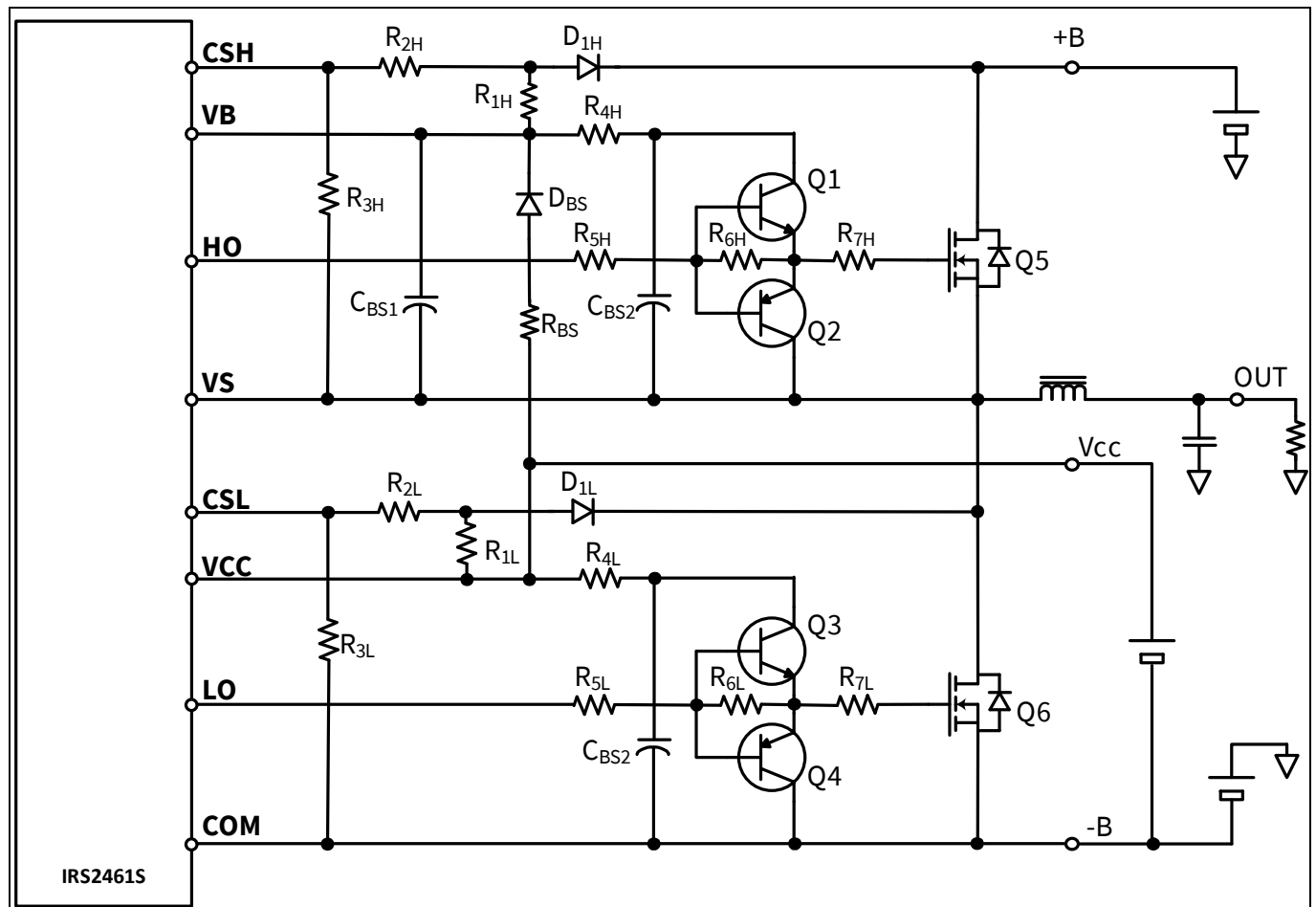


Figure 19 IRS2461S with gate drive buffer

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11 Protection features

11.1 Protection control

The internal protection control block dictates the operational mode, normal or shutdown, using the input of the CSD pin. In shutdown mode, the IC forces LO and HO to output 0 V with respect to COM and VS respectively to turn off the power MOSFETs.

The CSD pin provides five functions:

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

The CSD pin of one IRS2461S IC cannot be tied with another IRS2461S directly. The protection logic block diagram is shown in Figure 20.

The operating statuses of the protection features are shown in Table 4.

Table 4 Events and actions of CSD

Event	CSD	Fault
UVCC, rising edge	Recycle*	L until CSD > Vth1
UVCC, falling edge	n/a	n/a
UVAA, rising edge	n/a	L at VAA < UVAA
UVAA, falling edge	n/a	L at VAA < UVAA
UVBS, rising edge	n/a	n/a
UVBS, falling edge	n/a	n/a
Over Current Protection (OCP)	Keep recycling until OCP is reset	Held L until OCP is reset
OTP input	Keep recycling until OTP is reset	Held L until OTP is reset

Note: *CSD recycle: CSD pin voltage discharges down to Vth2 and charges back to VAA, if CSD pin is configured as self reset protection.

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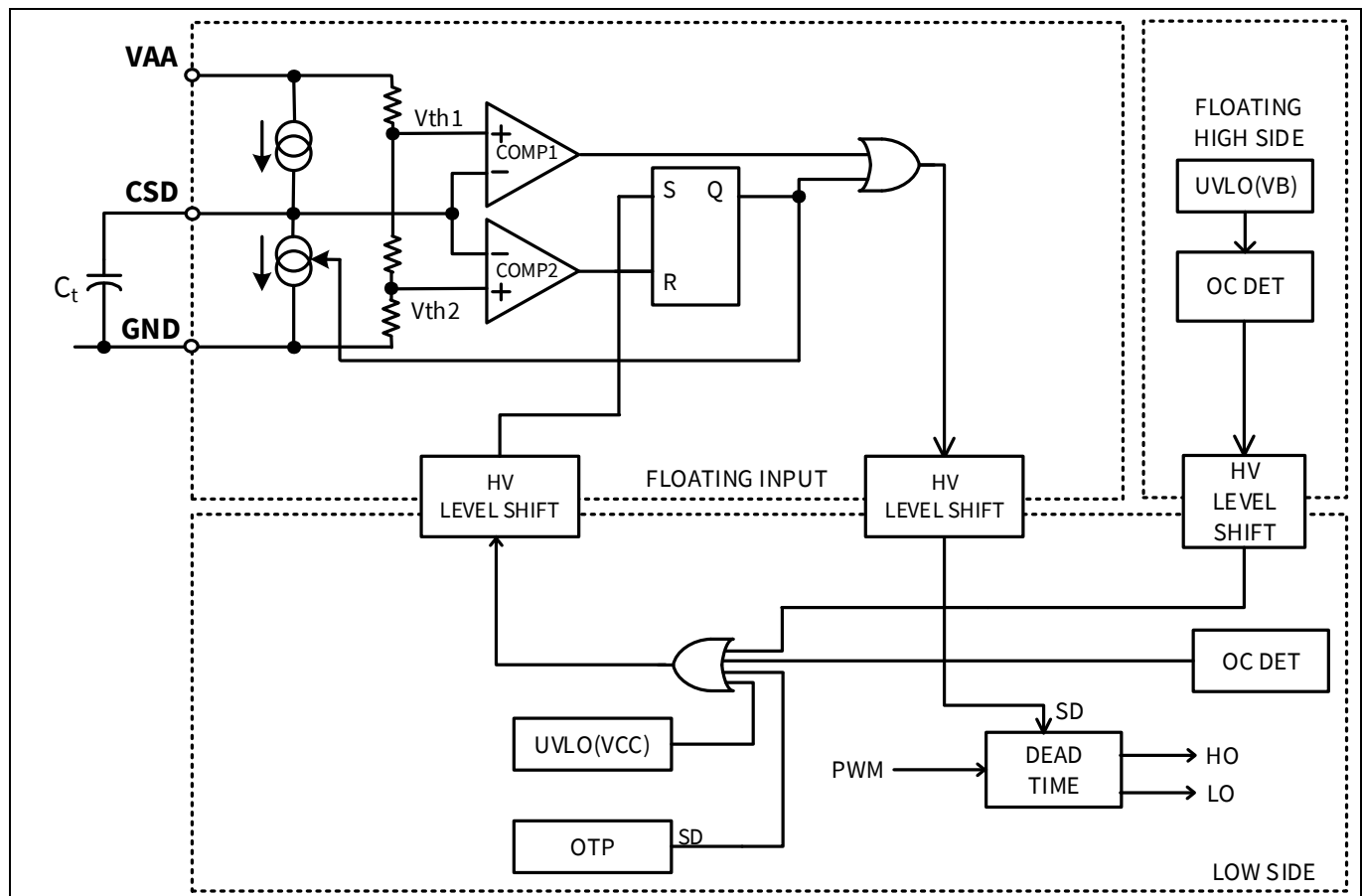


Figure 20 Protection functional block diagram

11.1.1 Self-reset protection

Attaching a capacitor between CSD and VSS configures the IRS2461S self-reset protection mode (Figure 21).

Upon an OCP event, the CSD pin discharges the external capacitor voltage, VCSD, down to the lower threshold Vth2 to reset the internal shutdown latch. Then, the CSD pin begins to charge the external capacitor, Ct, in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold, Vth1, the IC resumes normal operation.

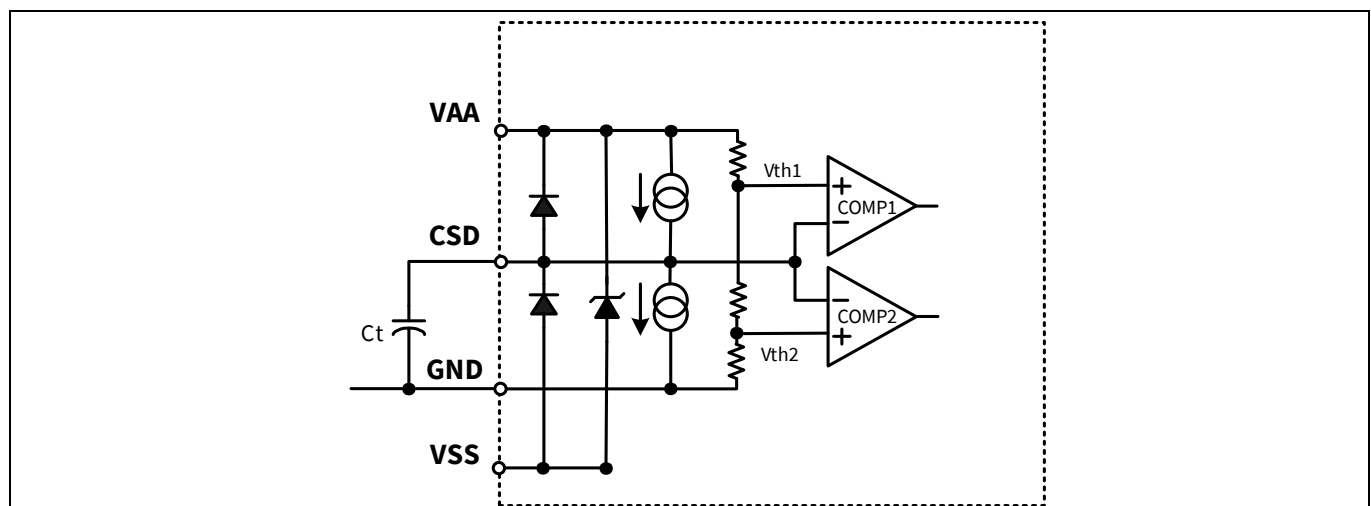


Figure 21 Self-reset protection configuration

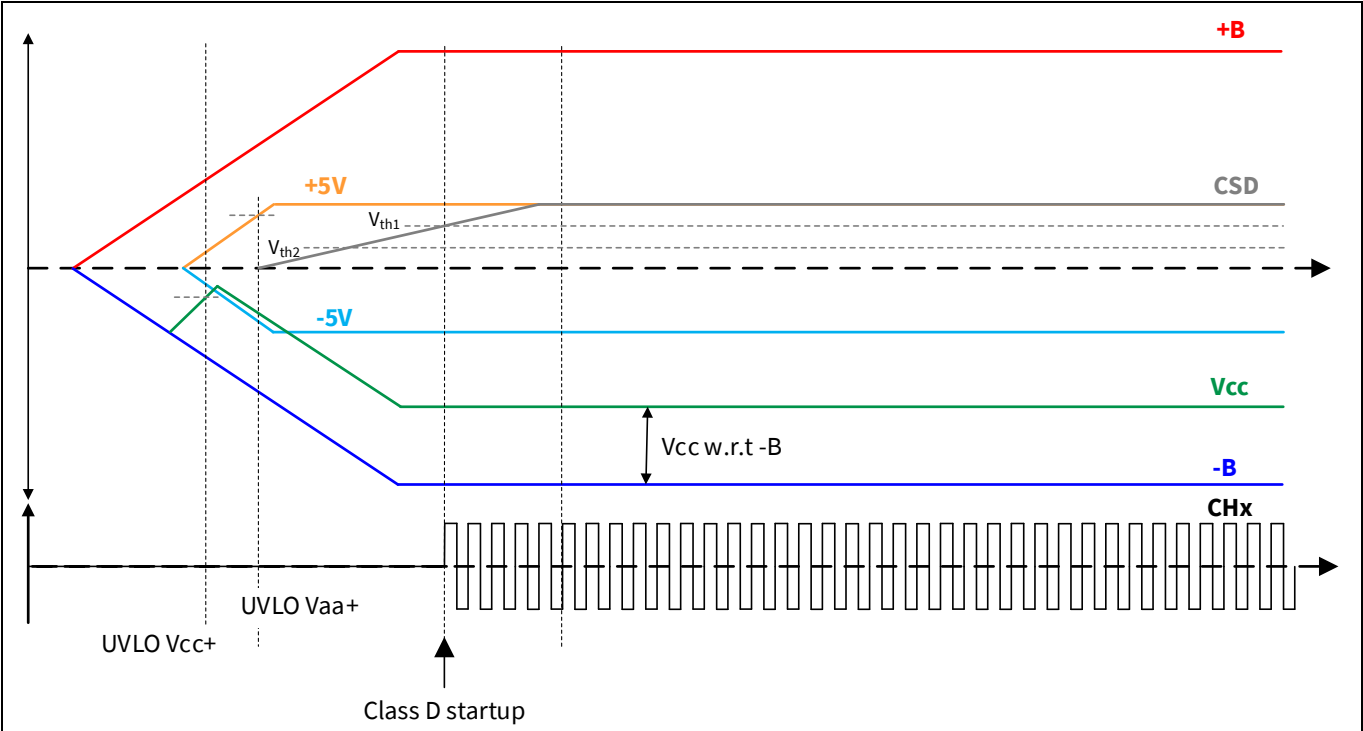


Figure 22 Self-reset protection start-up

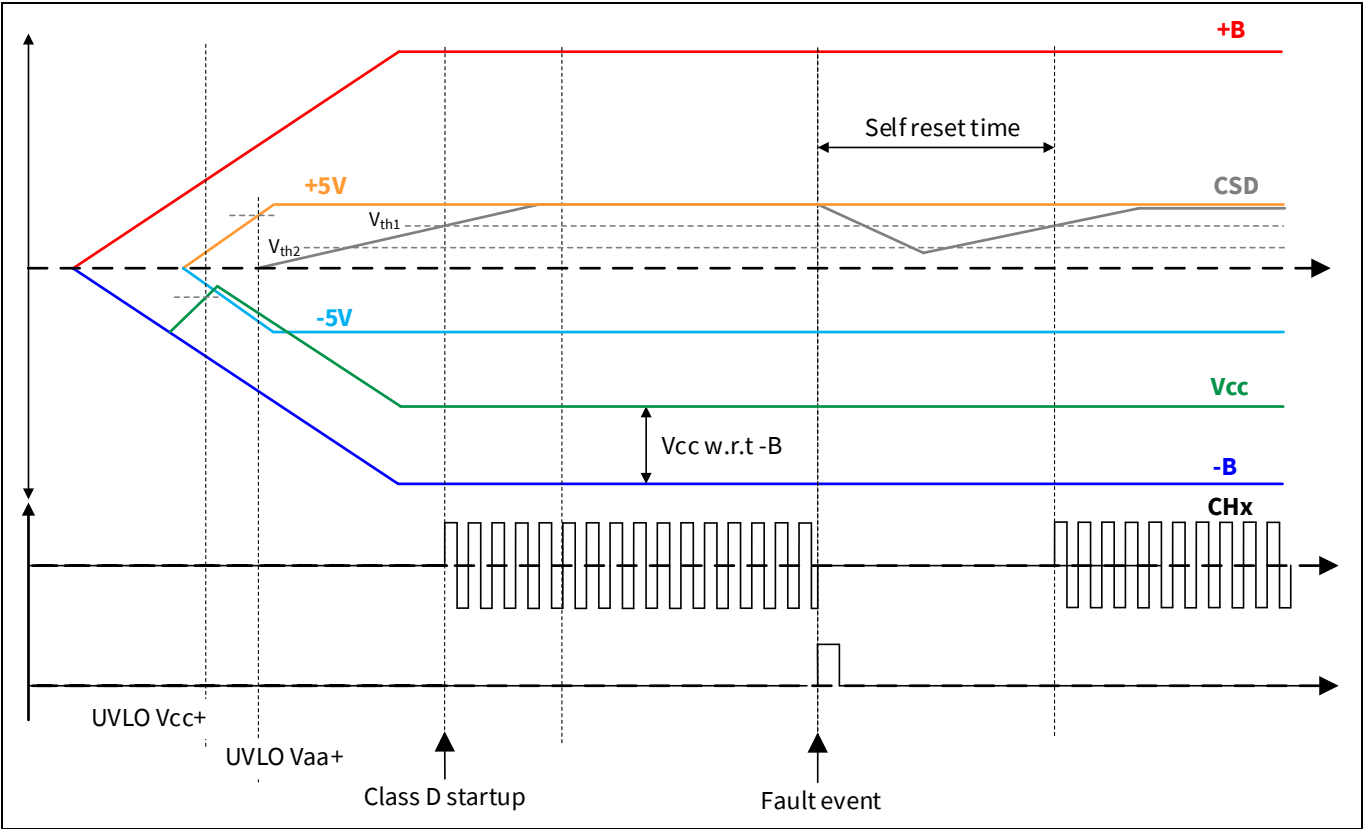


Figure 23 Self-reset protection fault recovery

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11.1.2 Designing Ct

The external timing capacitor, C_t , programs self-reset timings, t_{RESET} and t_{SU} .

- The t_{RESET} is the time that elapses from when the IC enters the shutdown mode to the time when the IC resumes operation. The t_{RESET} should be long enough to avoid over heating the MOSFETs from the repetitive sequence of shutting down and resuming operation during over-current conditions. In most applications, the minimum recommended time for t_{RESET} is 0.1 seconds.
- The t_{SU} is the time between powering up the IC in shutdown mode to the moment the IC releases shutdown to begin normal operation.

The C_t determines t_{RESET} and t_{SU} as shown in the following equations:

$$t_{RESET} = \frac{C_t \cdot V_{AA}}{1.1 \cdot I_{CSD}} \quad [s]$$

$$t_{SU} = \frac{C_t \cdot V_{AA}}{0.7 \cdot I_{CSD}} \quad [s]$$

where I_{CSD} = the charge/discharge current at the CSD pin
 V_{AA} = the input supply voltage with respect to GND

11.1.3 Shutdown input

During normal operation, pulling the CSD pin below the upper threshold V_{th1} forces the IC into shutdown mode. Figure 24 shows how to add an external discharging path to shut down the PWM.

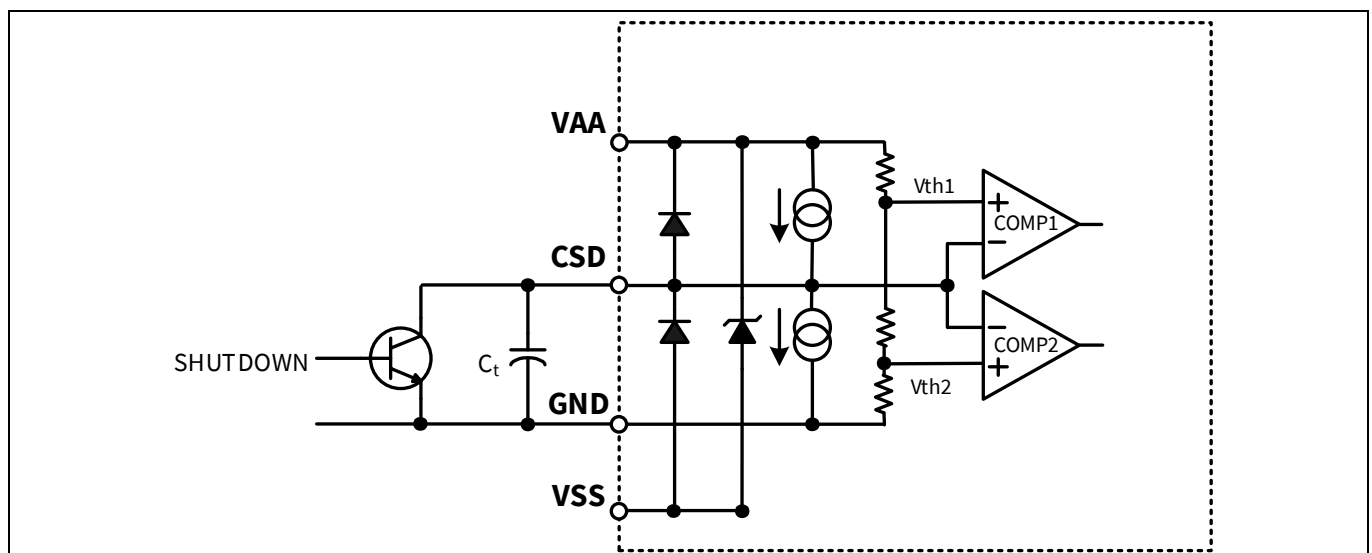


Figure 24 Shutdown input

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11.1.4 Latched Protection

Connecting CSD to VAA through a 10 kΩ or less configures the latched protection mode (Figure 25). The internal shutdown latch stays in shutdown mode after over current is detected. An external reset switch brings CSD below the lower threshold V_{th2} for a minimum of 200 ns and resets the latch. Until then, the system remains in the soft-start state. Also, at first power up, a reset signal to the CSD pin is required to release the IC from shutdown mode.

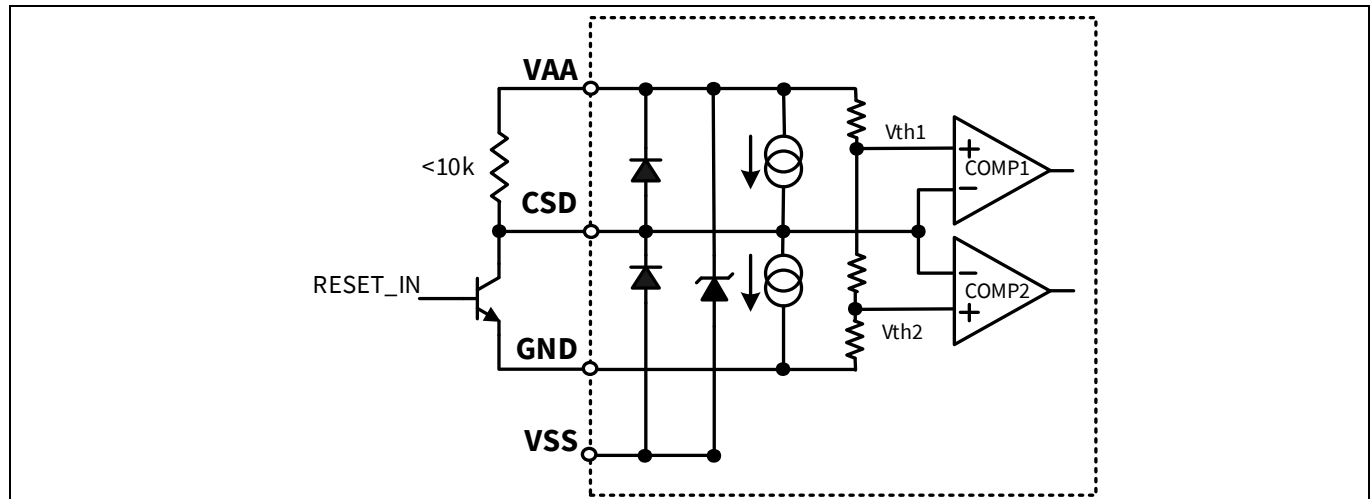


Figure 25 Latched protection with reset input

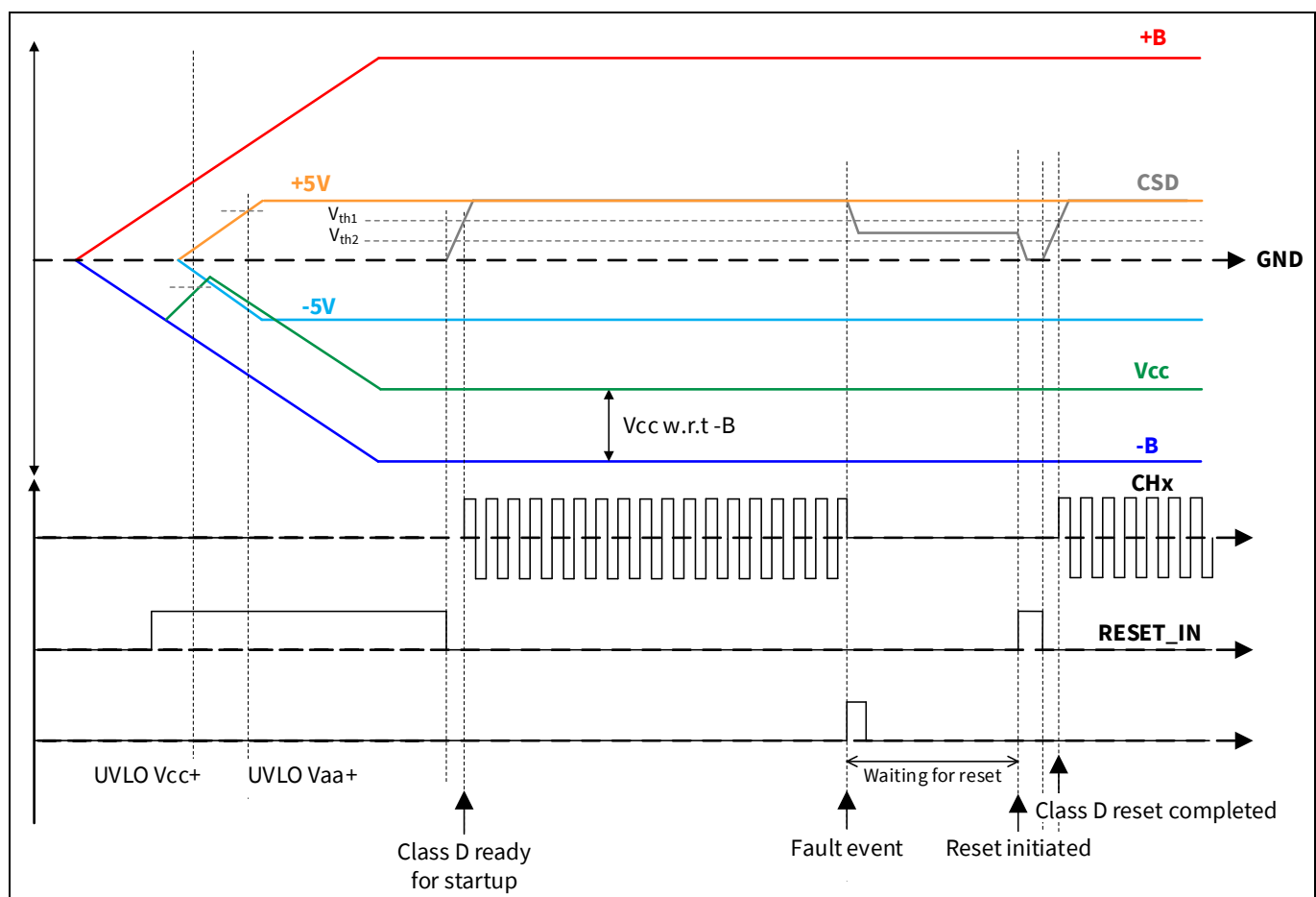


Figure 26 Latched protection with reset input: Fault recovery

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11.1.5 Interfacing with system controller

The IRS2461S can communicate with an external system controller through a simple interfacing circuit shown in Figure 27. A generic PNP transistor, U1, detects the sink current at the CSD pin during protection event and outputs a shutdown flag signal to an external system controller.

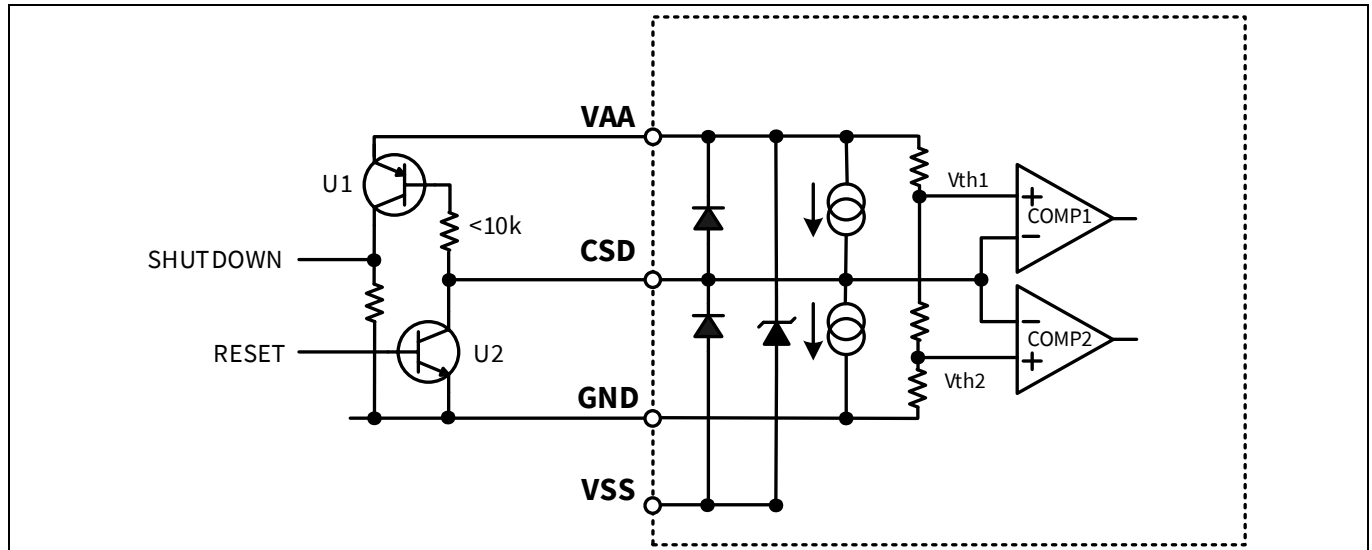


Figure 27 Interfacing CSD with system controller

Another generic NPN transistor, U2, can then reset the internal protection logic by pulling the CSD voltage below the lower threshold V_{th2} . After the first power up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

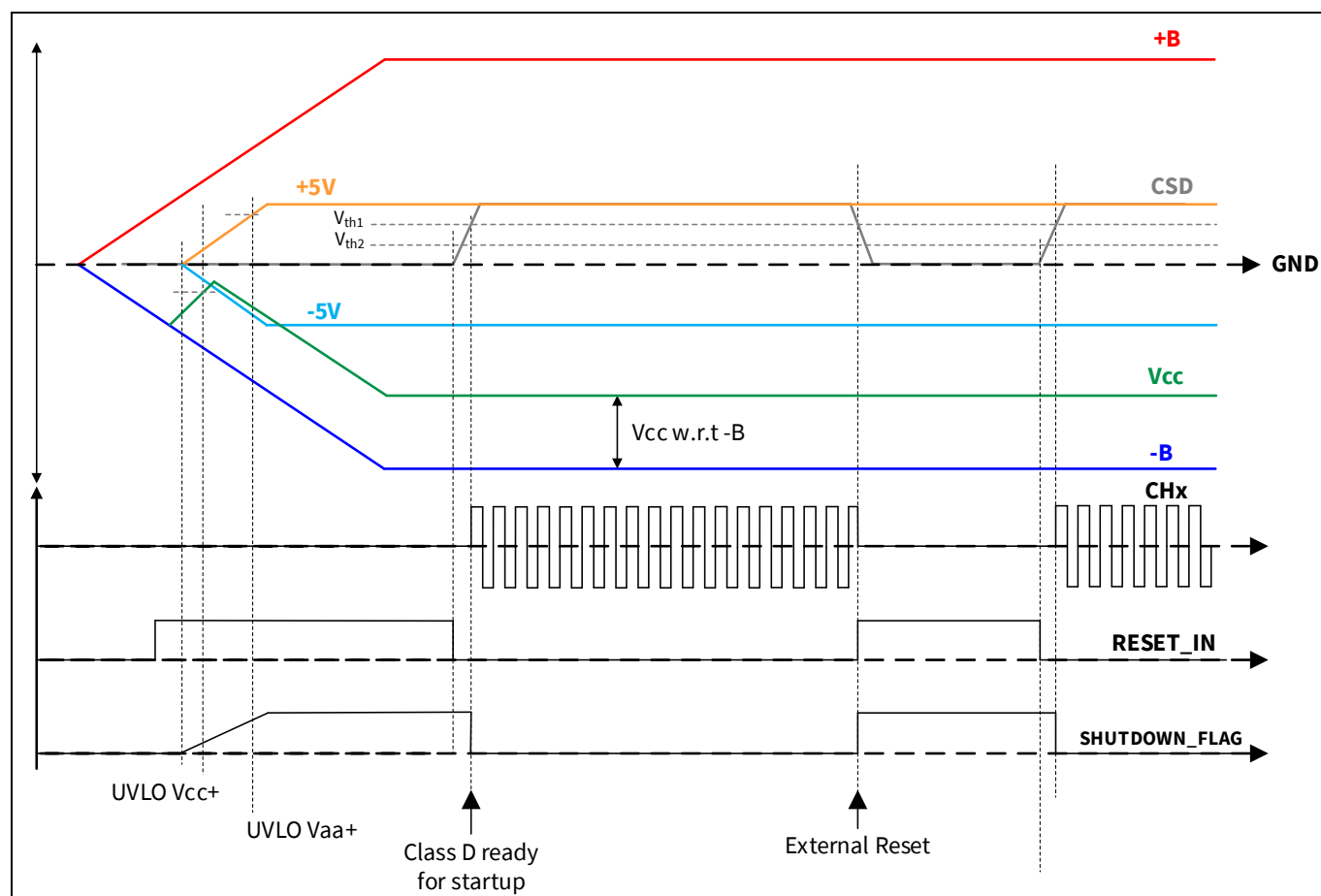


Figure 28 System controller – External reset behavior

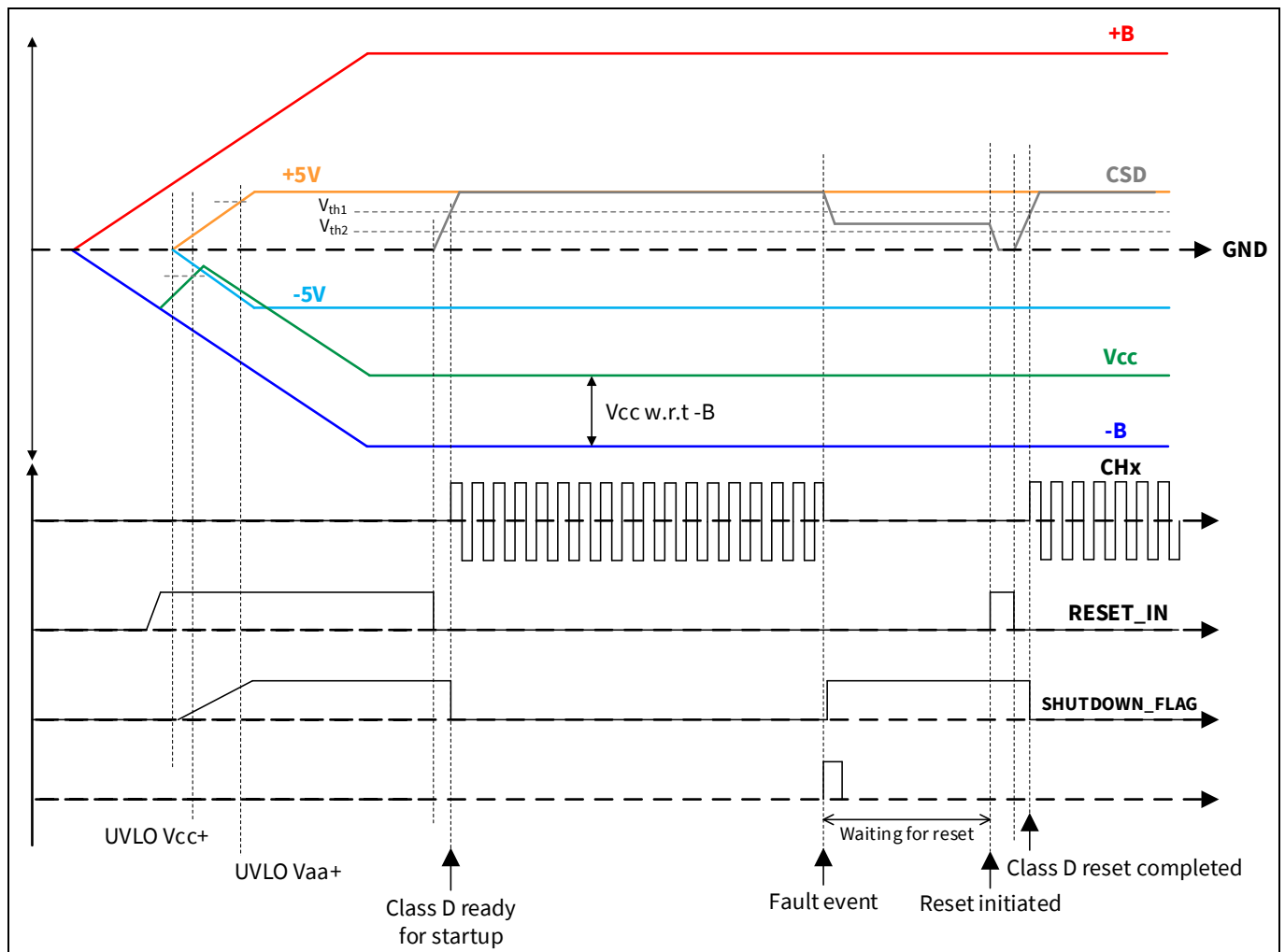


Figure 29 System controller – Fault recovery

11.2 Over Current Protection (OCP)

The IRS2461S features over current protection to protect the external power MOSFETs during abnormal load conditions. The control logic diagrams are in Figure 25. As soon as either the high-side or low-side current sensing block detects over current the following sequence will occur:

1. The shutdown latch flips its logic state from normal operational mode to shutdown mode.
2. The low-side and high-side MOSFETs go into an off-state condition.
3. The CSD pin starts discharging the external capacitor Ct.
4. When the voltage across Ct falls below the lower threshold V_{th2} , the COMP2 resets the shutdown latch to normal mode.
5. The CSD pin starts charging the external capacitor Ct.
6. When VCSD goes above the upper threshold V_{th1} , the logic on COMP1 toggles and the IC resumes operation.

Figure 30 summarizes the above. As long as the over current condition exists, the IC will repeat the over current protection sequence at a repetitive rate set by the CSD capacitor.

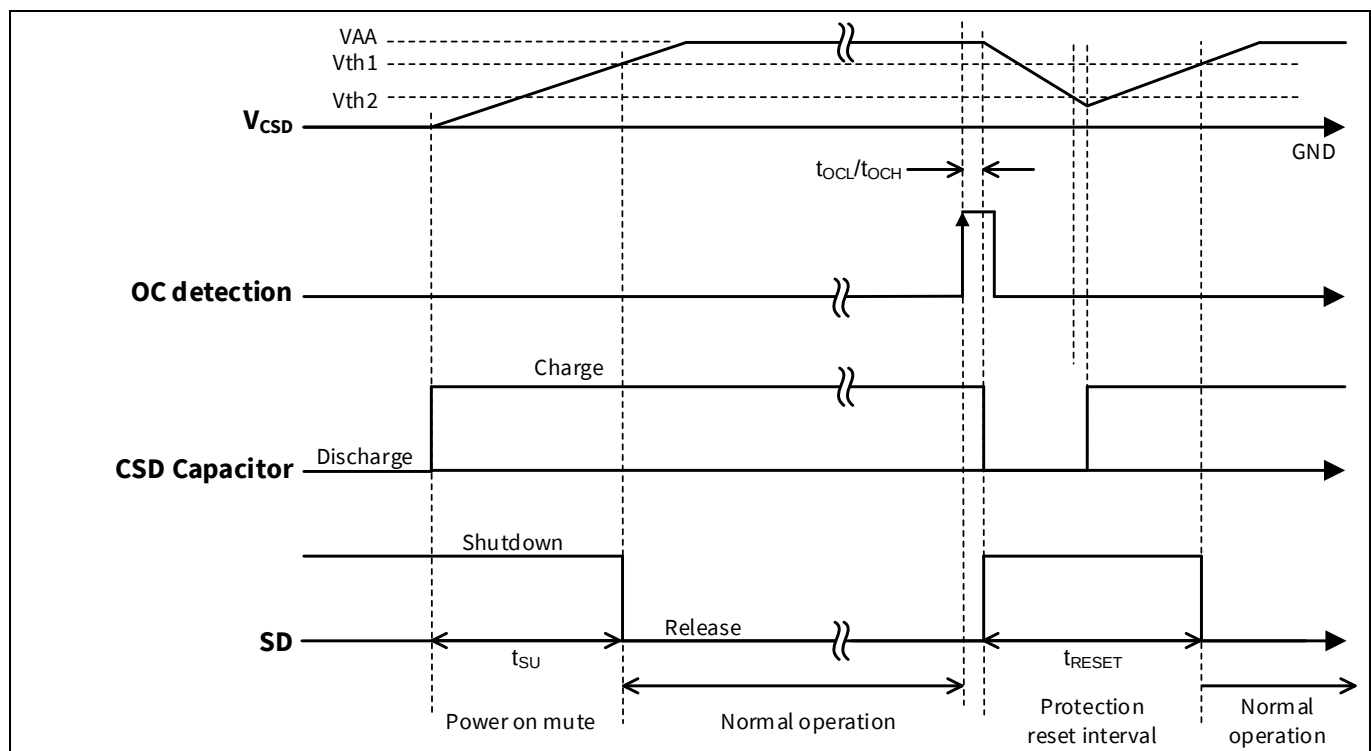


Figure 30 Overcurrent protection timing chart

11.2.1 Programming OCP trip level

In a Class D audio amplifier, the direction of the load current alternates with the audio input signal. An over-current condition can therefore occur during either a positive current cycle or a negative current cycle. The IRS2461S uses the $R_{DS(on)}$ of the output MOSFETs as current sensing resistors. If the measured current exceeds a predetermined threshold, the OCP block outputs a signal to the protection block, forcing HO and LO low and protecting the MOSFETs. The IRS2461S provides an identical over-current sensing signal to both high-side and low-side MOSFETs (Figure 31).

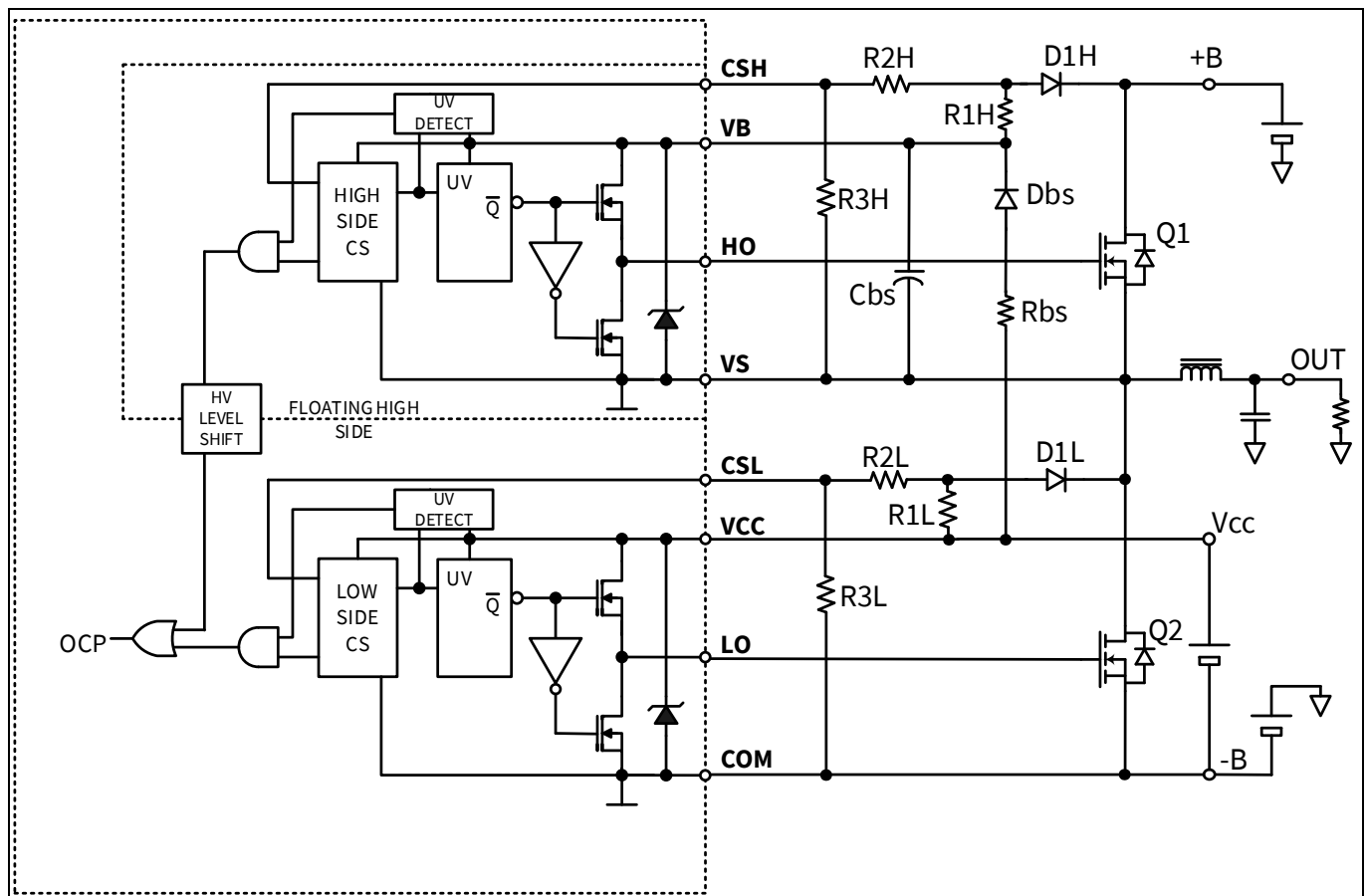


Figure 31 Bi-directional over current protection

11.2.2 Over-current sensing

Over current sensing block monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level. Current sensing uses the drain to source voltage, V_{DS} , across the MOSFET during the turn on period via CSH and CSL pins.

As shown in Figure 32, an external diode, D1, blocks the high voltage from the drain of the MOSFET from feeding into the CSL/CSH pin while the MOSFET is off. A 10 kohms resistor, R1, forward biases D1.

The detection thresholds of the OCP, $V_{th_{OCL}}$ and $V_{th_{OCH}}$, are internally fixed at 1.2 V. An external resistive divider, R2 and R3, set the threshold. Due to a forward voltage drop of $V_{F(D1)}$ across the D1, the minimum threshold required for high-side over current protection therefore is $V_{th_{OCL}}$ or $V_{th_{OCH}}$ minus $V_{F(D1)}$, which is typically 0.6 V.

Sensing voltage for high side CSH pin is:

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot (V_{DS} + V_{F(D1)})$$

where V_{DS} = the drain to source voltage of the high-side MOSFET during on state

$V_{F(D1)}$ = the forward drop voltage of D1

Since the V_{DS} is the product of drain current I_D and $R_{DS(on)}$ of the high side MOSFET. V_{CSH} can be rewritten as:

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot (R_{DS(on)} \cdot I_D + V_{F(D1)})$$

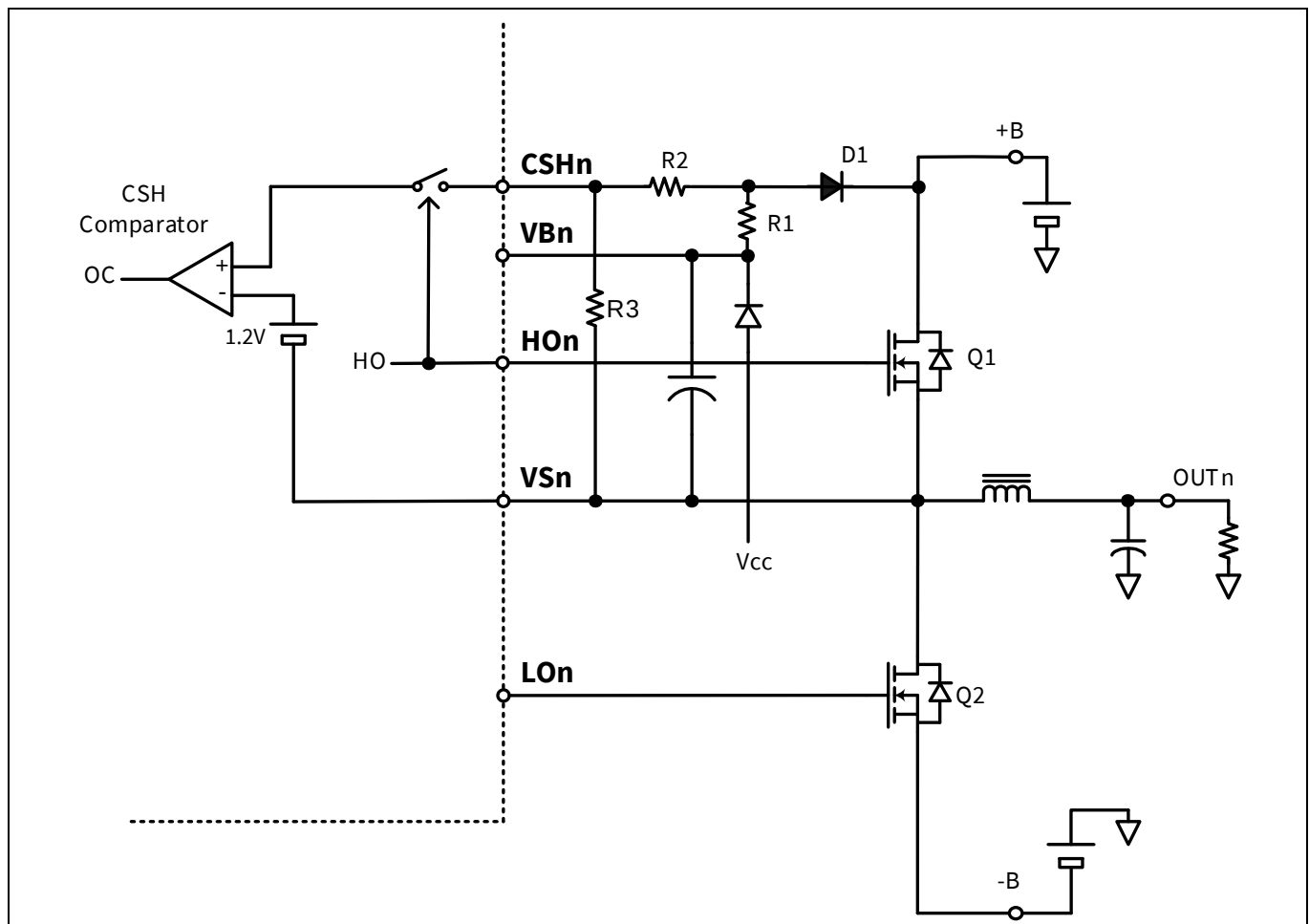


Figure 32 Programming high side current threshold

An OCP trip point of $R_{DS(on)}$ based current sensing changes according to the junction temperature T_J of the sensing MOSFET. The OCP threshold reduces at higher T_J . Therefore, consider operating T_J and set a threshold not to trigger within normal operating conditions. The current sensing in the IRS2461S is designed to handle output inductor core saturation. Setting a trip threshold above output inductor saturation current is to set the OCP threshold at the inductor saturation point.

In the following example, the over current protection level is set to trip at 30 A using a MOSFET with an $R_{DS(on)} = 100 \text{ m}\Omega$. The component values of R2 and R3 can be calculated using the following formula:

Let $R_2 + R_3 = 10 \text{ k}\Omega$.

$$R_3 = 10 \text{ k}\Omega \cdot \frac{V_{th_{OCH}}}{V_{DS} + V_F}$$

where $V_{th_{OCL}} = 1.2 \text{ V}$

V_F = the forward voltage of reverse blocking diode D1 = 0.6 V.

V_{DS} at $I_D = 30 \text{ A}$ = the voltage drop across the high side MOSFET when the MOSFET current is 30 A.

Therefore, V_{DS} at $I_D = 30 \text{ A} = I_D \times R_{DS(on)} = 30 \text{ A} \times 100 \text{ m}\Omega = 3 \text{ V}$

Based on the formulas above, closest resistor values in E12 series are $R_2 = 6.8 \text{ k}\Omega$ and $R_3 = 3.3 \text{ k}\Omega$.

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11.2.3 Choosing the reverse blocking diode

The CSL and CSH sensing diodes require a reverse voltage higher than the supply voltage between +B and –B. The reverse recovery time must be less than 100 ns. A diode such as the ON Semiconductor's MURA140T3G, rated at 400 V, $t_{rr}=65$ ns high speed switching diode or equivalent fits well.

11.3 Over Temperature Protection (OTP) input

The over temperature protection OTP input uses an external PTC Thermistor or thermostat to monitor the temperature of the MOSFET. The OTP pin sources a 0.6 mA internal current to the external thermal sensor. Over temperature protection activates when the voltage at any of OTP input pin reaches higher than 2.8 V, that makes the typical threshold sensor resistance 4.7 kohms.

The OTP pin of IRS2461S is designed for connecting a PTC Thermistor with characteristics shown in Figure 33. Recommended PTC Thermistor includes PRF15**471QB1RC, PRF18**471QB1RB or PRF21**471QB1RA series from Murata Manufacturing co., Ltd or similar (Figure 34). A mechanical thermostat switch or a thermostat IC with open drain output, such as LM26 from National Semiconductor, can also be used as a temperature sensor for better accuracy as shown in Figure 35.

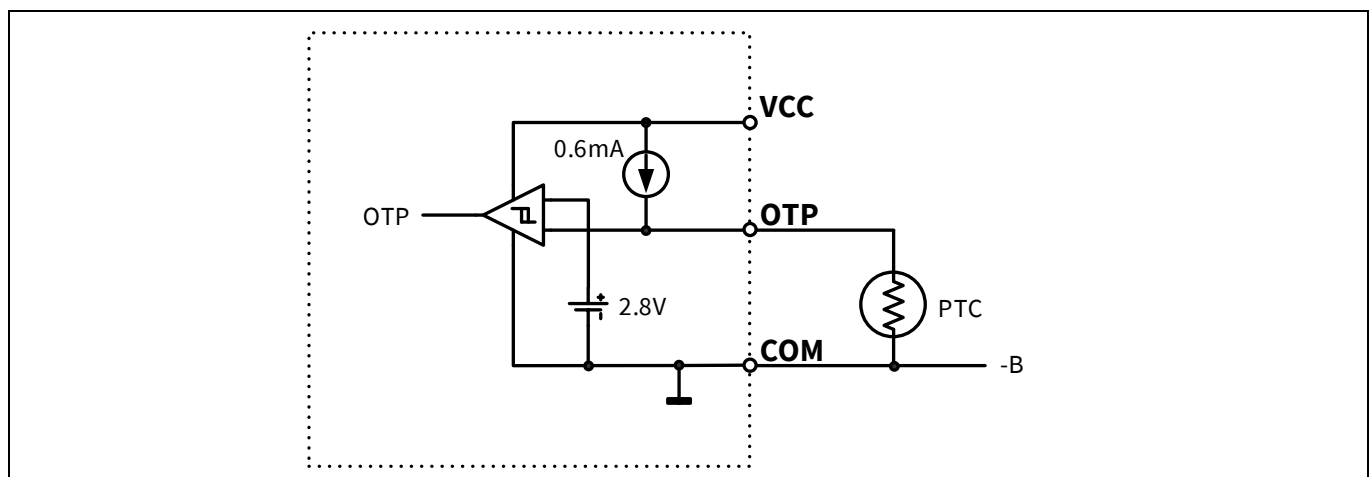


Figure 33 Over Temperature Protection (OTP) input structure

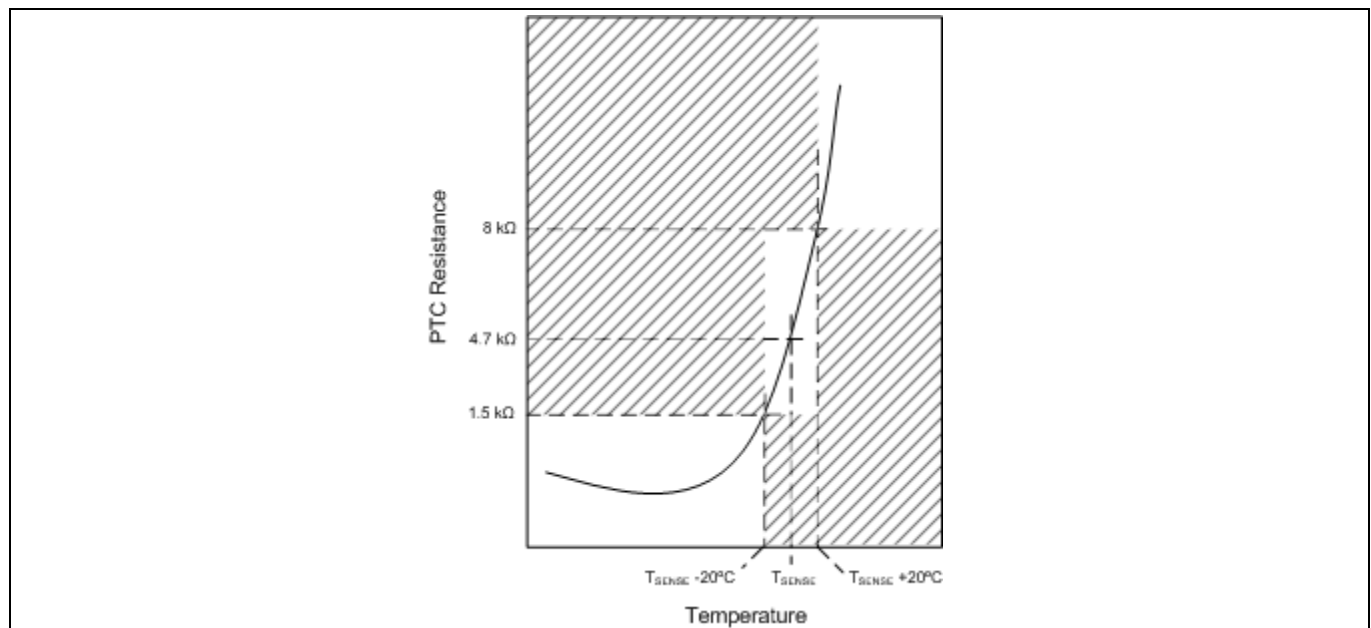


Figure 34 Recommended PTC sensor characteristics

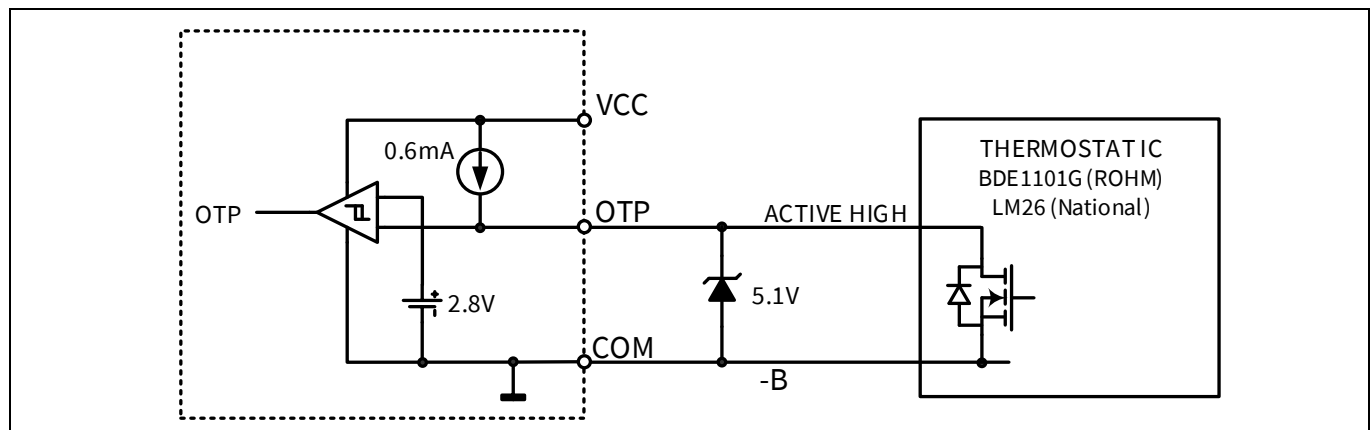


Figure 35 OTP pin with thermostat IC

11.4 Under Voltage Protection (UVP)

In order to prevent a partial on state of the external MOSFET, under voltage protection monitors the low side and high side gate bias supplies, VCC and VB. When VCC is below UVLO, both high and low side MOSFETs are turned off. When the high side supply V_{BS} is below the UVLO threshold, the high side output is disabled, while the low side works normally.

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12 Power supply design

12.1 Supplying VAA and VSS

VAA and VSS are supply voltages at the front-end of the analog section, hence noise sensitive. For best audio performance, use regulated power supplies for VAA and VSS as shown in Figure 35.

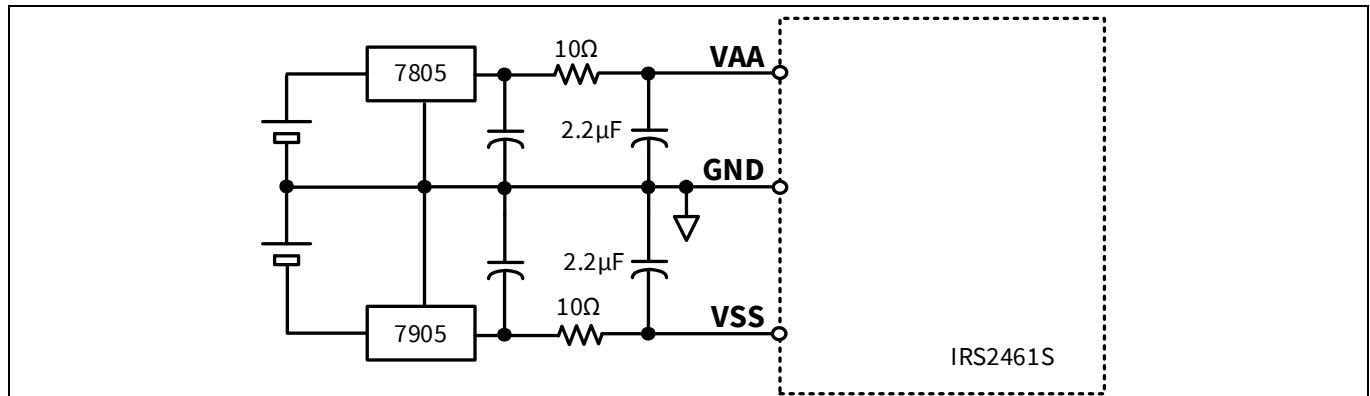


Figure 36 Supplying VAA and VSS with external voltage regulators

When switched mode regulators are used as power supply voltages for VAA and VSS, place a two-stage R-C noise filter in the supply lines as shown in Figure 36.

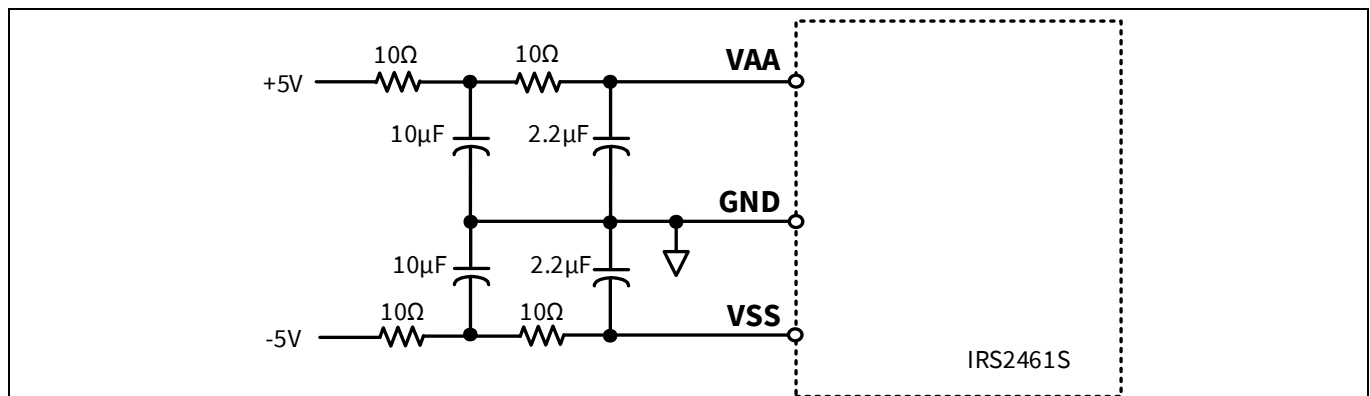


Figure 37 Supplying VAA and VSS from switched mode power supply

12.2 Supplying VCC and VB

Figure 38 shows the recommended power supply configuration for gate driver power supplies. The gate driver stage has two power supply inputs:

1. VB-VS: High side gate drive supply
2. VCC-COM: Low side gate drive supply

The low-side power supply, VCC, feeds the internal gate drive logic and low side gate driver. In order to protect VCC from switching noise generated by the VS node, it is recommended to insert a few ohms of R_{BS} in the bootstrap charging path.

The high-side driver requires a floating supply VB referenced to the respective switching node VS where the source of the output MOSFET is connected. A charge pump method (floating bootstrap power supply) eliminates the need for a floating power supply and thus is used in the typical application circuit. The floating

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C_{BS} retains its voltage as a floating power supply referenced to V_S . Before C_{BS} discharges and V_{BS} crosses the under voltage lock out threshold UV_{BS} , the next charging cycle should start by turning on the low-side MOSFET.

Figure 39 depicts the low-side MOSFET ON state. I_1 turns off the high-side MOSFET first, then I_2 turns on the low side MOSFET. As soon as the switching node V_S reaches the negative supply $-B$, the bootstrap diode, D_{BS} , turns on and starts charging C_{BS} with current I_3 from V_{CC} . Note that $V_{BS} = V_{CC} -$ (forward drop voltage of D_{BS}).

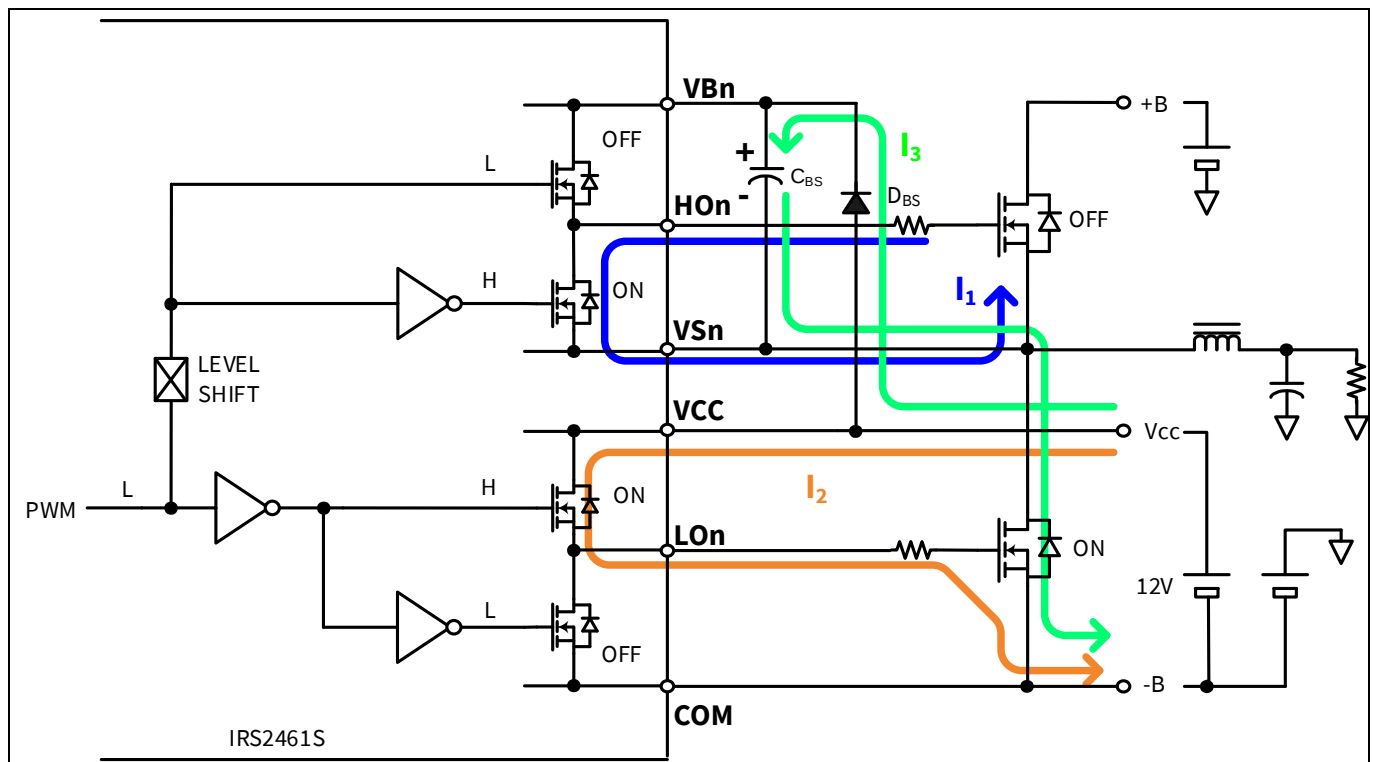


Figure 39 Charging V_{BS} : low-side ON period

After the low-side conduction period, I_4 in Figure 40 turns off the low-side MOSFET. Then I_5 turns on the high-side MOSFET, increasing V_S up to $+B$. As long as the high side is ON, the bootstrap diode, D_{BS} , isolates the floating power supply V_{BS} .

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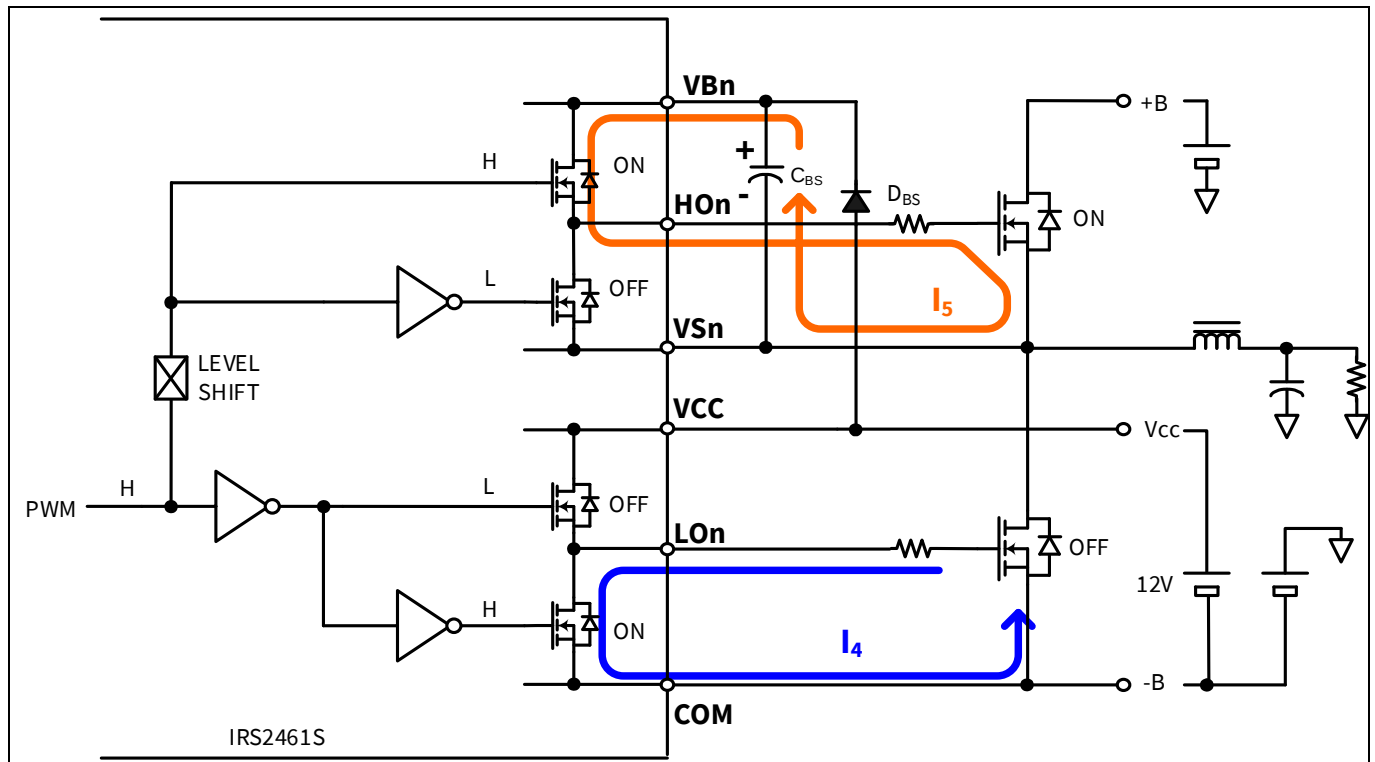


Figure 40 High-side ON period

12.2.1 Choosing bootstrap capacitance

During high side on period, the bootstrap capacitor, C_{BS} , holds the high-side supply voltage. Quiescent current I_{QBS} in the high-side gate driver, precharging resistor ($R_{PRE-CHARGE}$) discharging current I_{R2} , and I_{R1} a current through high-side current sensing resistor $R1$ discharge the C_{BS} . (Figure 42) The I_{QBS} and I_{R1} are the most significant contributors and the others are negligible.

The minimum bootstrap capacitance is determined as follows:

$$C_{BS} >> \frac{(I_{QBS} + I_{R1}) \cdot t_{ON}}{VCC - 1.5 - UVBS}$$

Where C_{BS} : floating bootstrap capacitance [F]

I_{QBS} : high-side quiescent current [A]

I_{R1} : high-side current sensing bias current [A]

t_{ON} : longest high-side MOSFET conduction time [s]

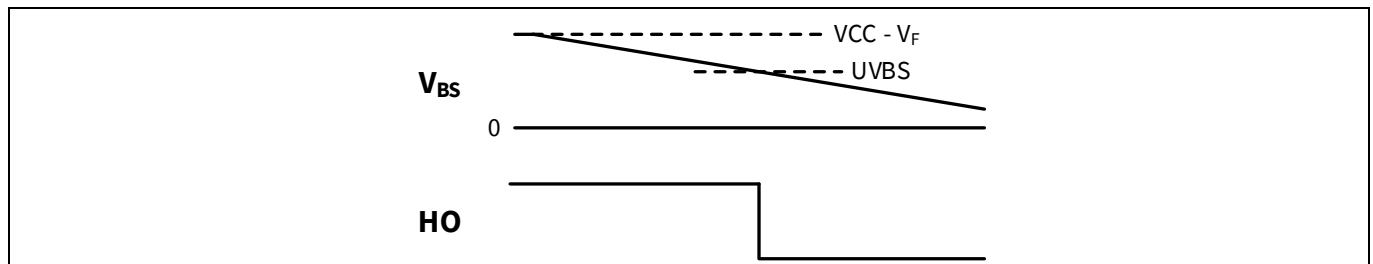
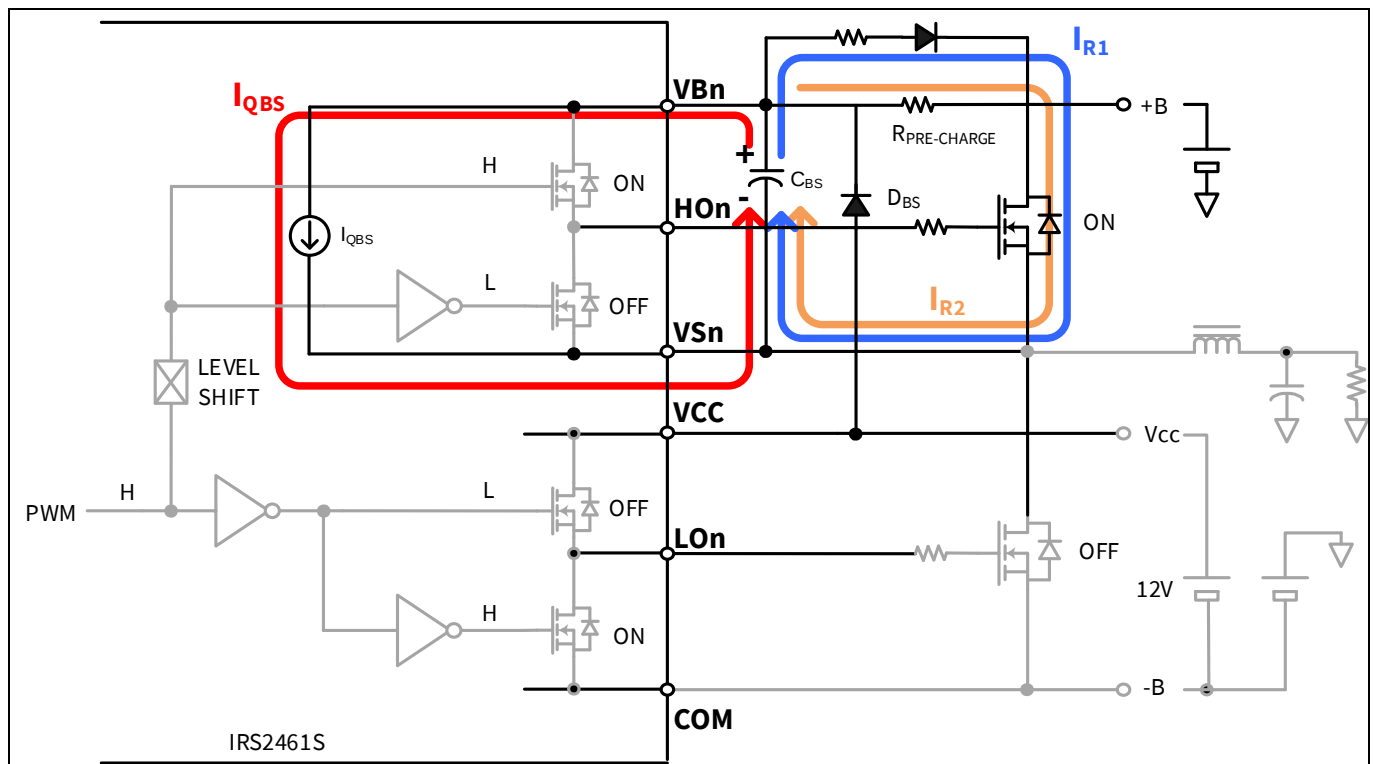
VCC : low-side power supply voltage [V]

$UVBS$: high-side under voltage lockout threshold [V]

1.5: voltage drop in the bootstrap charging diode D_{BS}

Often the IRS261S operates in hard clipping condition. The continuous high-side ON duration could last as long as it is half of the lowest audio frequency, tens of milliseconds. A typical application uses a 22 μF C_{BS} to support this low audio frequency clipping condition. A ceramic capacitor (X7R, X5R or X5S type) or aluminum electrolytic capacitor with 25 V or higher voltage rating is recommended. Since the bootstrap capacitor sees the VCC supply voltage, a ceramic capacitor (X7R, X5R or X5S type) or aluminum electrolytic capacitor with 25 V or higher voltage rating is recommended.

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Figure 41 V_{BS} dischargingFigure 42 C_{BS} discharging during high-side ON period

12.2.2 Choosing bootstrap diode

Use a bootstrap charging diode with voltage rating of 1.5 x the maximum bus voltage. In order to charge the bootstrap capacitor a very short low-side ON period with a high PWM modulation ratio and a fast recovery diode type ($t_{rr} < 50$ ns) is recommended.

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12.2.3 Charging V_{BS} prior to start

For proper start-up in a self-oscillating PWM configuration, precharging the bootstrap supply VBS prior to PWM start-up ensures that the oscillation can start with either high side or low side first. A charging resistor R_{CHARGE} , inserted between the positive supply bus and VB, charges CBS prior to switching as shown in Figure 43. The minimum resistance of R_{CHARGE} is limited by the maximum continuous ON duration of the high side MOSFET. When the high-side MOSFET is on, R_{CHARGE} drains the bootstrap power supply together with the quiescent current I_{QBS} so it reduces holding up time.

The maximum resistance of R_{CHARGE} is limited by the current charge capability of the resistor during startup:

$$I_{CHARGE} > I_{QBS}$$

where

I_{CHARGE} = the current through R_{CHARGE}

I_{QBS} = the high side supply quiescent current, 1 mA

The pre-charging current flows into the speaker load. A balancing resistor $R_{BALANCE}$ and a dummy load R_{DUMMY} reduces the DC current flows in to the load.

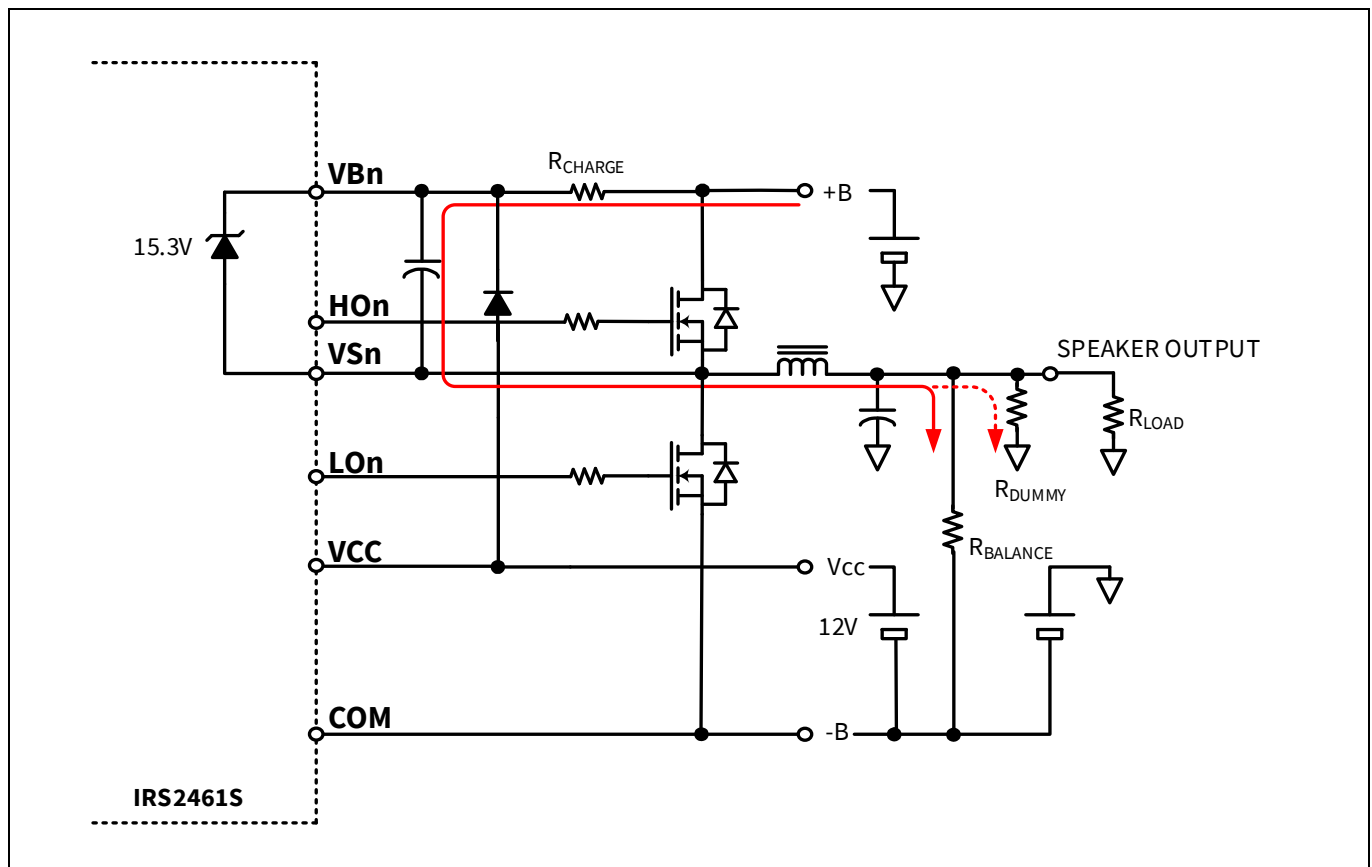


Figure 43 Pre-charging bootstrap supply

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12.3 Start-up/power-down sequence (UVLO)

The protection control block in the IRS2461S monitors the status of V_{AA} and V_{CC} to ensure that both voltage supplies are above their respective UVLO (under-voltage lockout) thresholds before beginning normal operation. If either V_{AA} or V_{CC} is below the under-voltage threshold, LO and HO are disabled in shutdown mode until both V_{AA} and V_{CC} rise above their voltage thresholds.

As soon as V_{AA} or V_{CC} falls below its UVLO threshold, protection logic in the IRS2461S turns off LO and HO, shutting off the power MOSFETs.

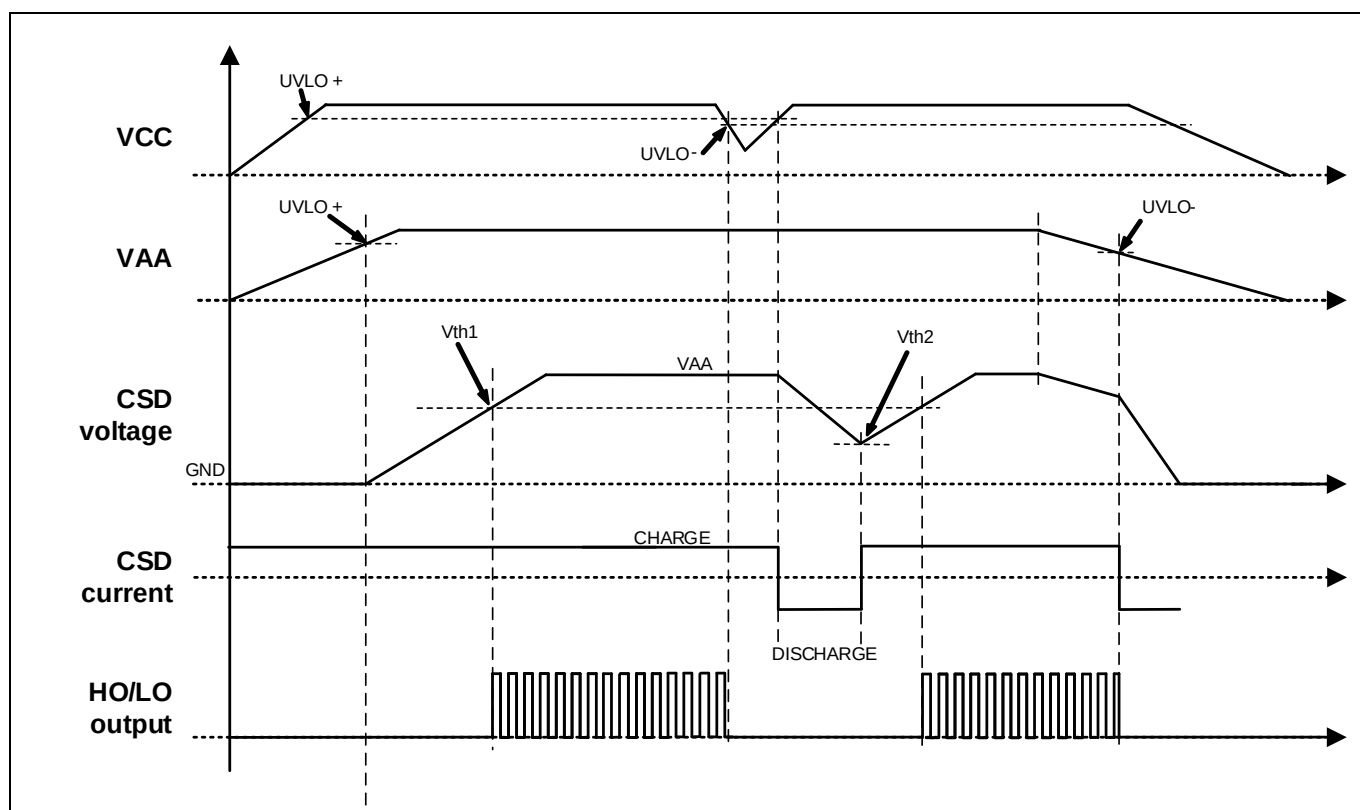


Figure 44 IRS2461S UVLO timing chart

12.4 Power supply decoupling

Due to the analog circuitry in the IRS2461S, careful attention must be given to decoupling the power supplies for proper operation of the IC. Ceramic capacitors (minimum of 0.1 μF) or aluminum capacitors (minimum of 1 μF) should be placed close to the power supply pins of the IC on the board. Due to large capacitance variations, Y5V dielectric or similar type ceramic capacitors are not recommended.

Please refer to the application note AN-978 for general design considerations of a high voltage gate driver IC.

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13 Board layout considerations

13.1 Board layout plan

There are functional blocks that generate noise and there are functional blocks that are sensitive to noise. The PCB designer should identify them and find out the best component placement based on these facts as well as mechanical and thermal requirements.

Noise sensitive functions:

- The audio input circuitry, especially IN+ and IN-
- Clock input

Noise generating functions:

- The gate driver stage, especially VB, CSH and VS
- The MOSFET stage

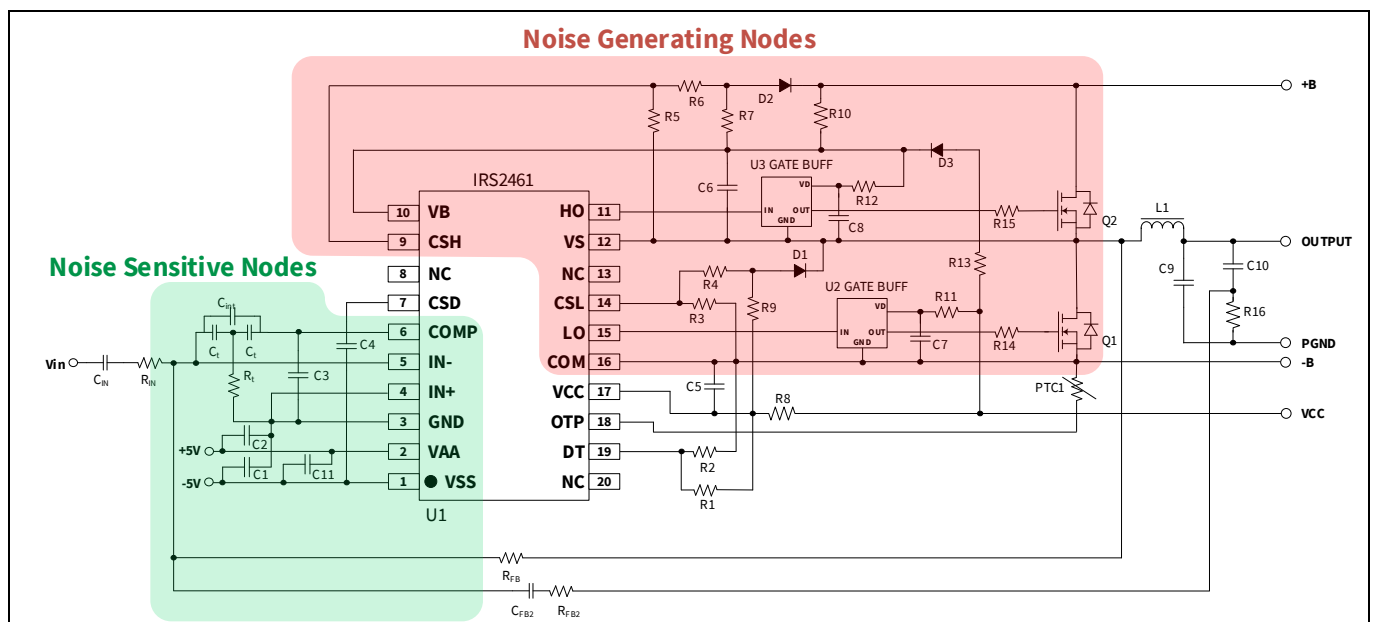


Figure 45 Noise mapping of IRS2461S application

It is important to properly locate the ground planes to obtain good audio performance. Since each functional block within the IRS2461S refers to different potentials, it is recommended to apply three reference potentials, analog, gate drive and power grounds.

Figure 46 is a PCB layout example used with the IRAUDAMP26 reference design. Note that there is no overlap between the input GND plane and the noisy switching nodes: VS and high side components. Stray inductance in the VS connection is less influential than VP and VN so prioritize these power supply traces. Prioritize +B to -B power traces for minimum impedance.

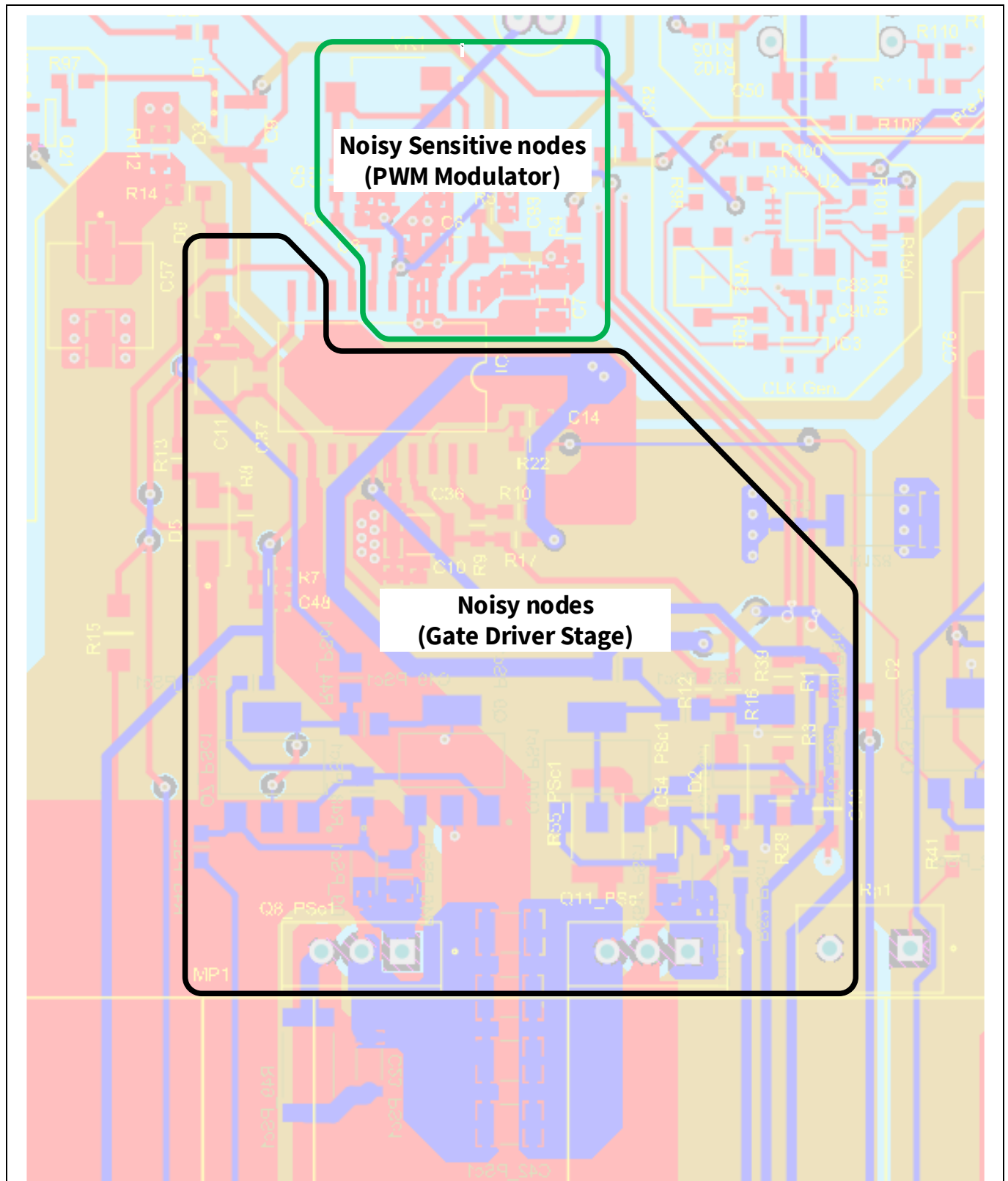


Figure 46 Noise mapping of IRS2461S PCB design example

13.2 Analog ground

The input analog section is referenced to the signal ground, or GND, which should be a quiet reference node for the audio input signal. The peripheral circuits in the floating input section such as CSD and COM pins refer to this ground. These nodes should all be separated from the switching stages of the system. In order to prevent

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potential capacitive coupling to the switching nodes, use a ground plane only in this part of the circuit. Do not share the signal ground plane with the gate driver or power stages unless there is a dedicated layer for GND plane.

13.3 Gate driver reference

The gate driver stage of the IRS2461S is located between pins 13 and 30 and is referenced to the negative bus voltage, COM. This is the substrate of the IC and acts as ground. Although the negative bus is a noisy node in the system, both of the gate drivers refer to this node. Therefore, it is important to shield the gate drive stages with the negative bus voltage so that all the noise currents due to stray capacitances flow back to the power supply without degrading signal ground.

13.4 Power ground

Power ground is the ground connection that closes the loops of the bus capacitors and inductor ripple current circuits. Separate the power ground and input signal grounds from each other as much as possible to avoid common stray impedances.

Figure 47 illustrates how to lay out reference planes. The power GND plane should include a negative bus capacitor. The power reference plane should include Vcc. Also, use distinctly different symbols for the different grounds.

For further board layout information, refer to AN-1135, PCB Layout with Infineon Class D Audio Gate Drivers.

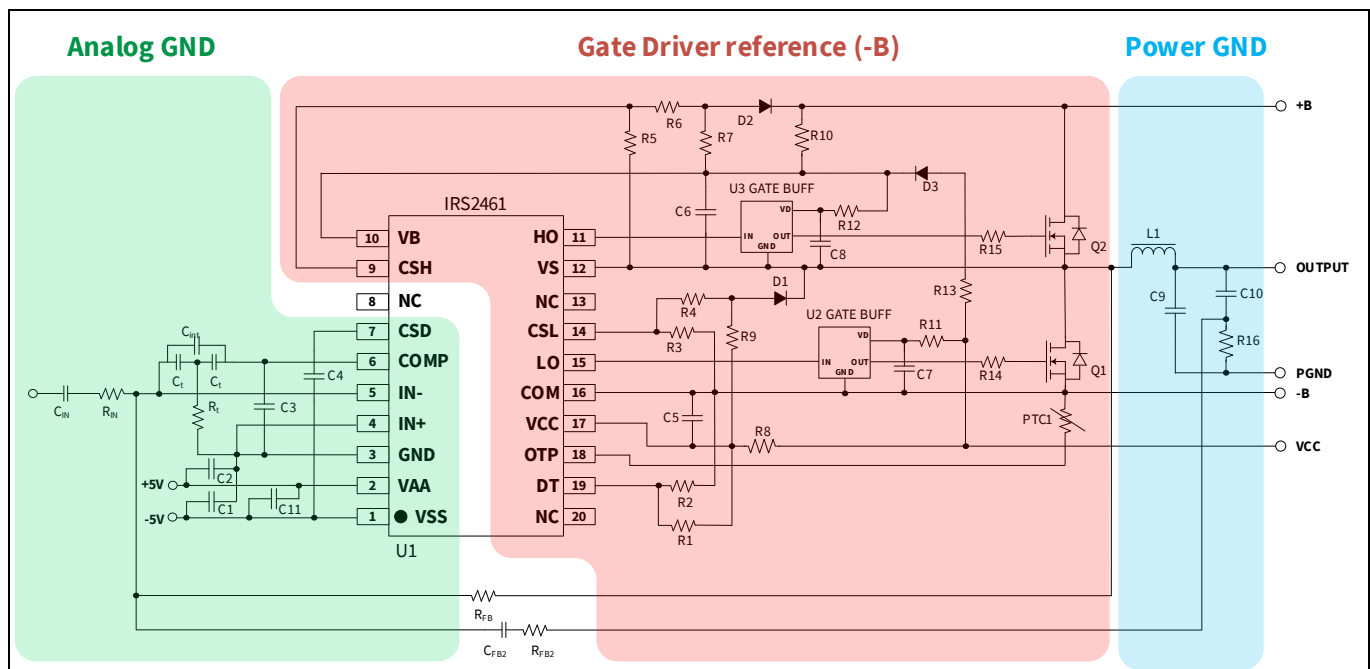


Figure 47 Applying ground planes

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14 Package dimensions

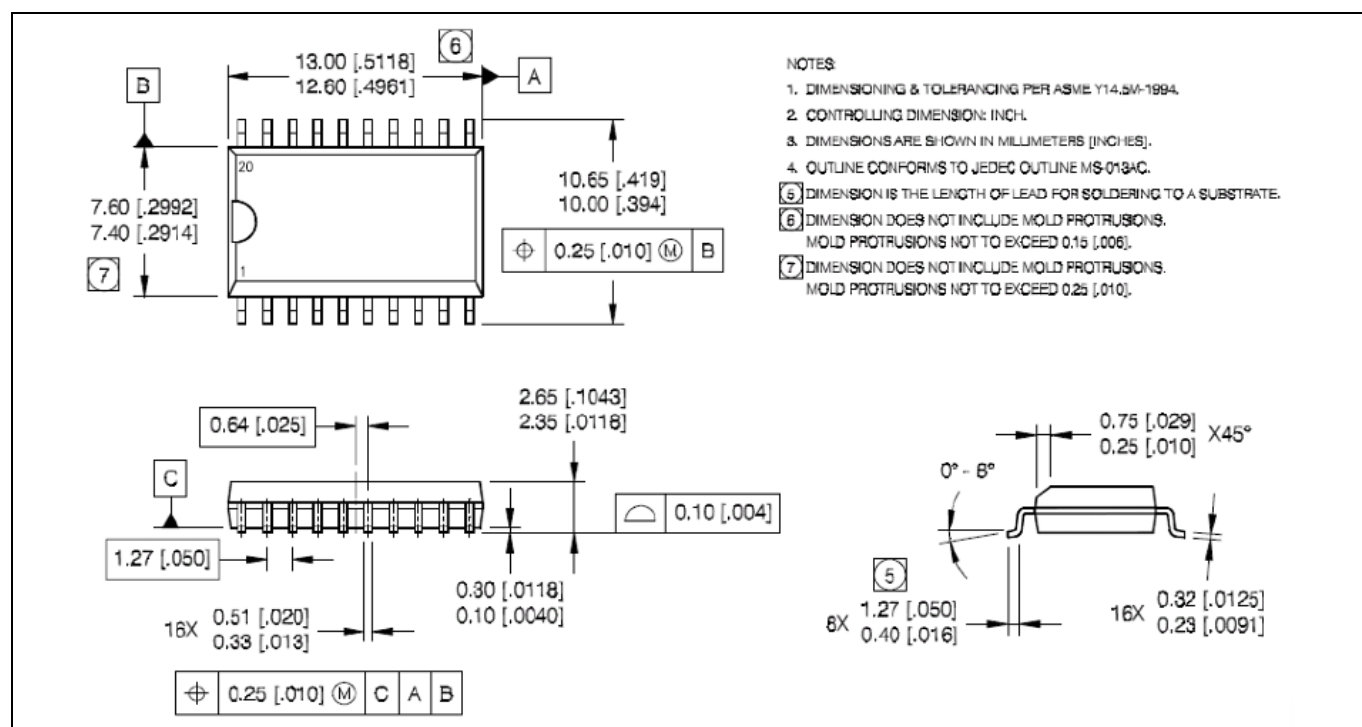


Figure 48 20 Lead SOIC (wide body)

15 Marking

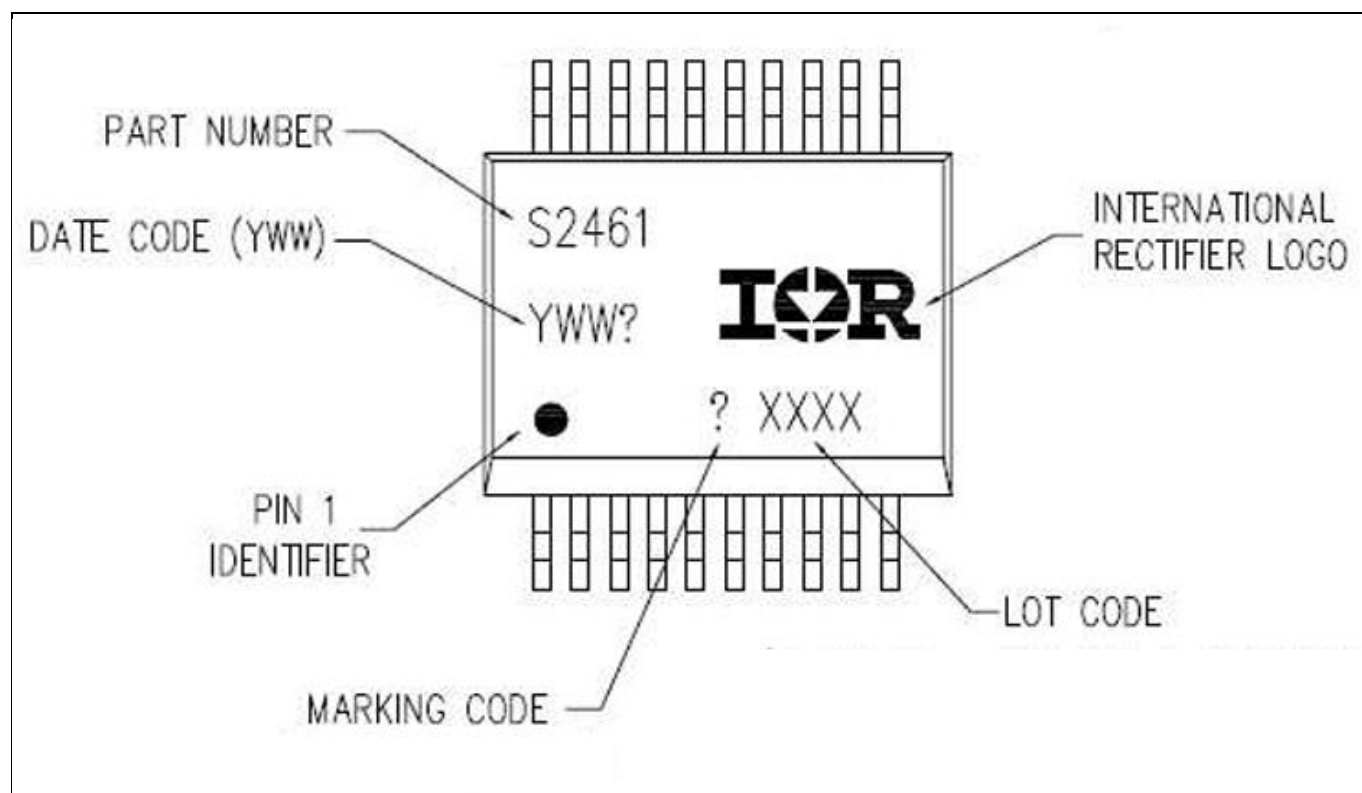


Figure 49 Top marking (laser)

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Revision history

IRS2461S

Revision 2026-05-19, Rev. 2.4

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.3	2019-06-04	added ton(typ)
2.4	2026-05-19	Included functional description and application notes

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