

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _c = +25°C
-20V	5.5mΩ @V _{GS} = -4.5V	-71A
	7.5mΩ @V _{GS} = -2.5V	-60A

Description

This MOSFET is designed to minimize on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

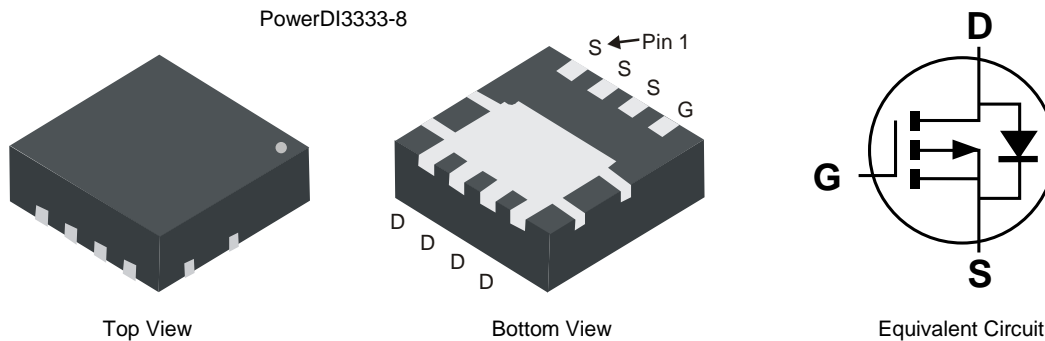
- Load switches
- Power management functions

Features

- Low R_{DS(ON)} – Ensures On-State Losses are Minimized
- Small Form Factor, Thermally Efficient Package Enables Higher Density End Products
- Occupies Just 33% of the Board Area Occupied by SO-8 Enabling Smaller End Product
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

Mechanical Data

- Package: PowerDI[®]3333-8
- Package Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish—Matte Tin Annealed over Copper Lead-Frame; Solderable per MIL-STD-202, Method 208
- Weight: 0.030 grams (Approximate)



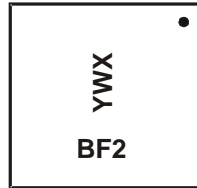
Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP26M1UFG-7	PowerDI3333-8	2,000	Tape & Reel
DMP26M1UFG-13	PowerDI3333-8	3,000	Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

PowerDI3333-8



BF2 = Product Type Marking Code
 YWX = Date Code Marking
 Y = Year (ex: 2 = 2022)
 W = Week (ex: a = week 27; z represents week 52 and 53)
 X = Internal Code (ex: U = Monday)

Date Code Key

Year	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
Code	1	2	3	4	5	6	7	8	9	0	1	2

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-Source Voltage	V_{GSS}	± 10	V
Continuous Drain Current (Note 7) $V_{GS} = -4.5\text{V}$	I_D	$T_C = +25^\circ\text{C}$	-71
		$T_C = +70^\circ\text{C}$	-56
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	-110	A
Maximum Continuous Body Diode Forward Current (Note 5)	I_S	-2	A
Avalanche Current $L = 0.1\text{mH}$ (Note 8)	I_{AS}	-37	A
Avalanche Energy $L = 0.1\text{mH}$ (Note 8)	E_{AS}	-71	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	1.67	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	P_D	3.0	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	41	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case (Note 7)	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - Thermal resistance from junction to soldering point (on the exposed drain pad).
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	-20	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1	μA	V _{DS} = -16V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	V _{GS(TH)}	-0.4	—	-1.0	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	4.7	5.5	mΩ	V _{GS} = -4.5V, I _D = -15A
		—	5.8	7.5		V _{GS} = -2.5V, I _D = -10A
		—	7.8	12		V _{GS} = -1.8V, I _D = -1A
		—	11	17		V _{GS} = -1.5V, I _D = -1A
Diode Forward Voltage	V _{SD}	—	-0.7	-1.1	V	V _{GS} = 0V, I _S = -10A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C _{iSS}	—	5392	—	pF	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oSS}	—	608	—		
Reverse Transfer Capacitance	C _{rSS}	—	564	—		
Gate Resistance	R _G	—	2.05	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = -4.5V)	Q _g	—	75	—	nC	V _{DD} = -10V, I _D = -20A
Total Gate Charge (V _{GS} = -10V)	Q _g	—	164	—		
Gate-Source Charge	Q _{gs}	—	6.9	—		
Gate-Drain Charge	Q _{gd}	—	19.8	—		
Turn-On Delay Time	t _{D(on)}	—	9	—	ns	V _{DD} = -10V, V _{GEN} = -4.5V, R _{GEN} = 1Ω, I _D = -10A
Turn-On Rise Time	t _R	—	24	—		
Turn-Off Delay Time	t _{D(off)}	—	69	—		
Turn-Off Fall Time	t _F	—	107	—		
Reverse Recovery Time	t _{RR}	—	54	—	ns	I _F = -10A, di/dt = 100A/μs
Reverse Recovery Charge	Q _{RR}	—	55	—	nC	

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

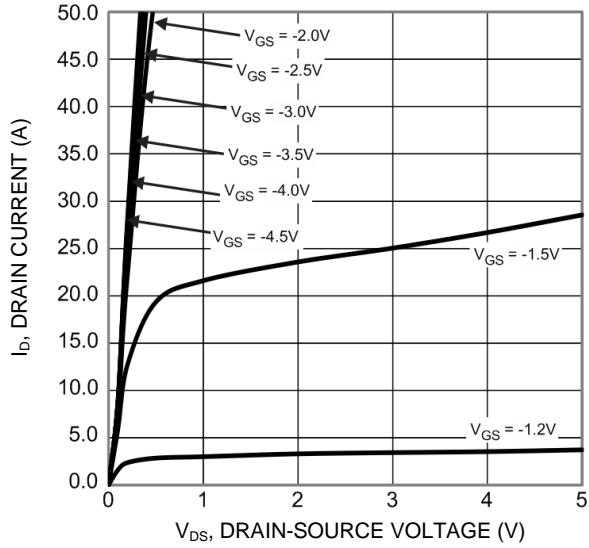


Figure 1. Typical Output Characteristic

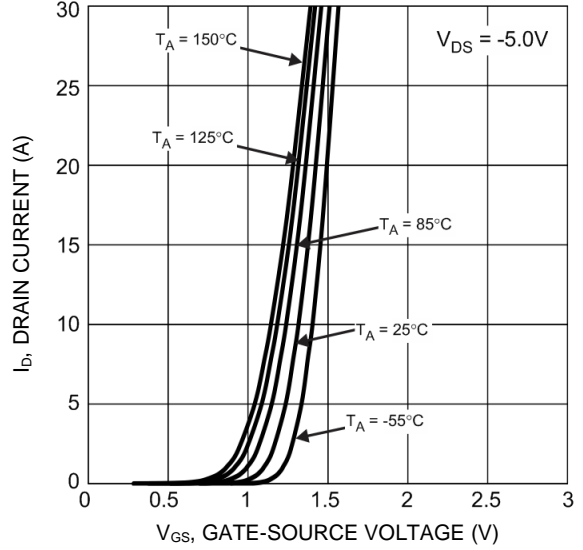


Figure 2. Typical Transfer Characteristic

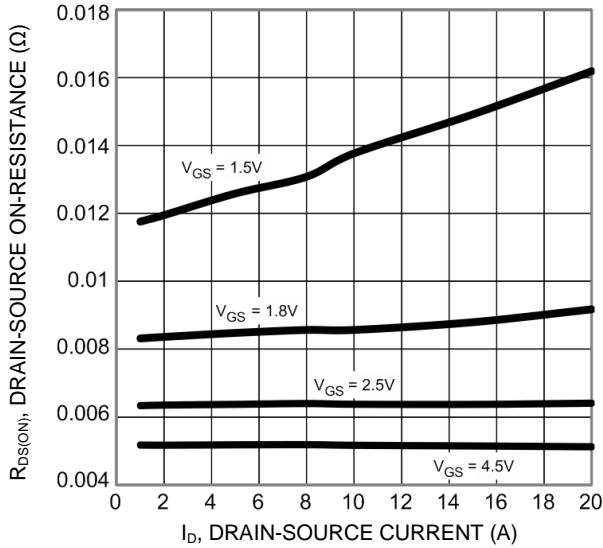


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

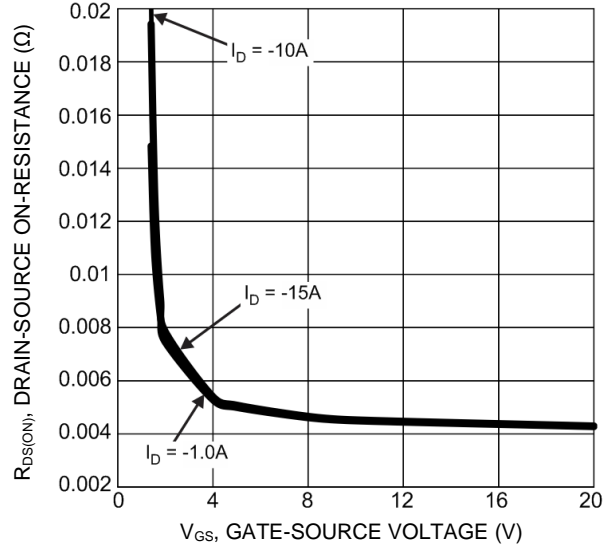


Figure 4. Typical Transfer Characteristic

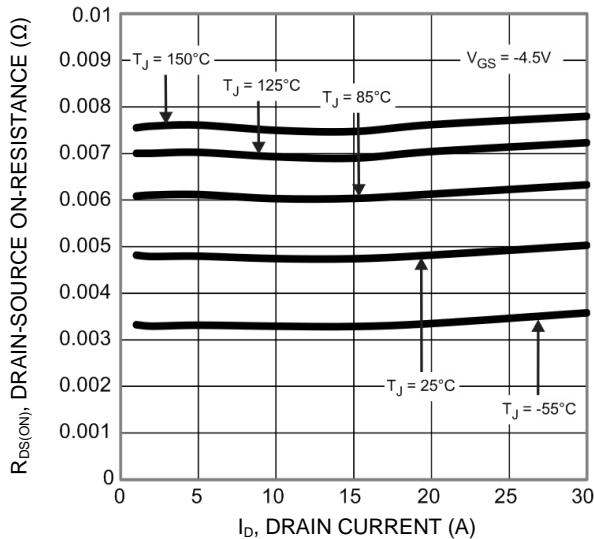


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

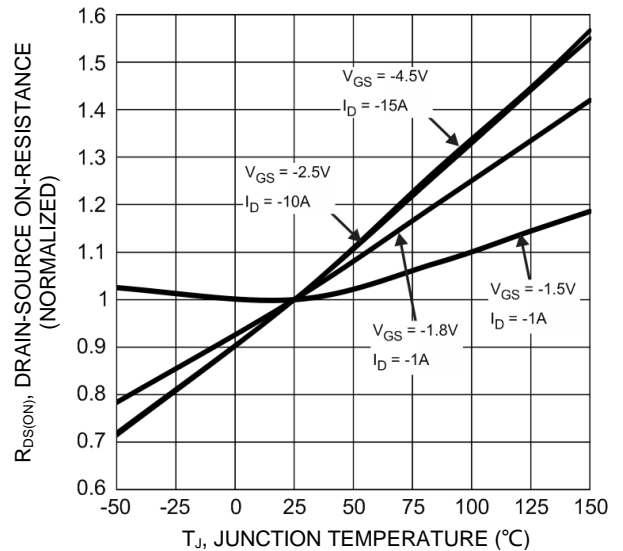


Figure 6. On-Resistance Variation with Junction Temperature

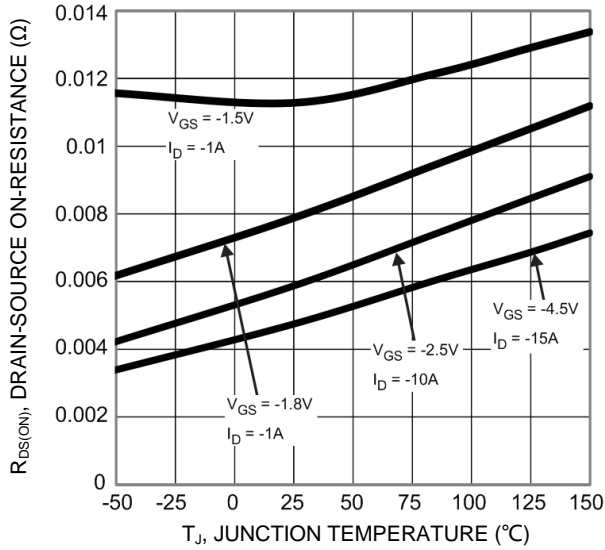


Figure 7. On-Resistance Variation with Junction Temperature

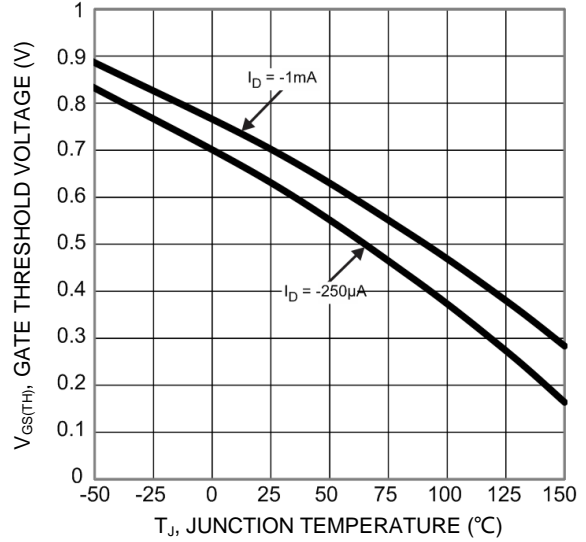


Figure 8. Gate Threshold Variation vs. Junction Temperature

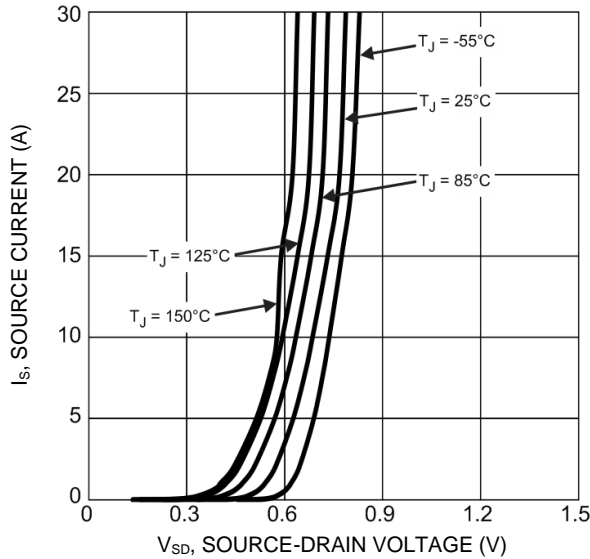


Figure 9. Diode Forward Voltage vs. Current

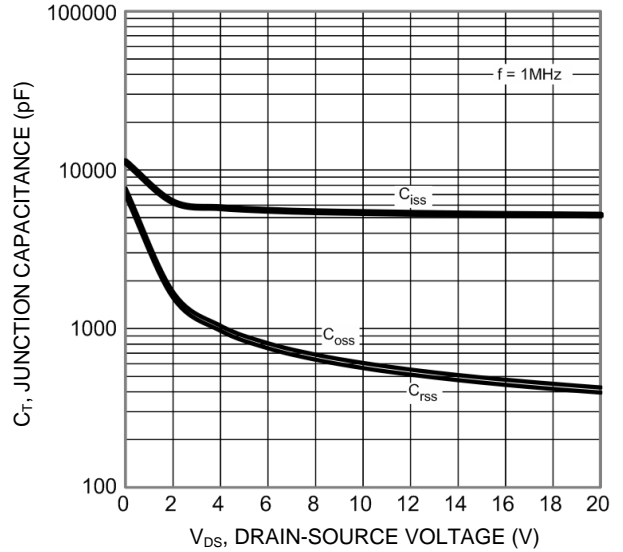


Figure 10. Typical Junction Capacitance

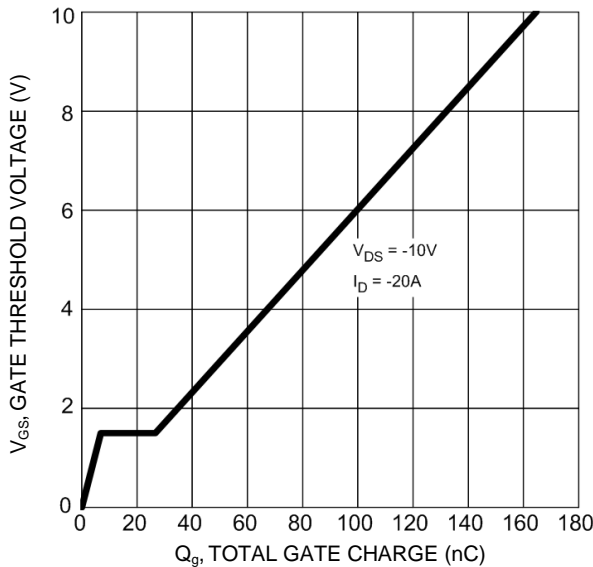


Figure 11. Gate Charge

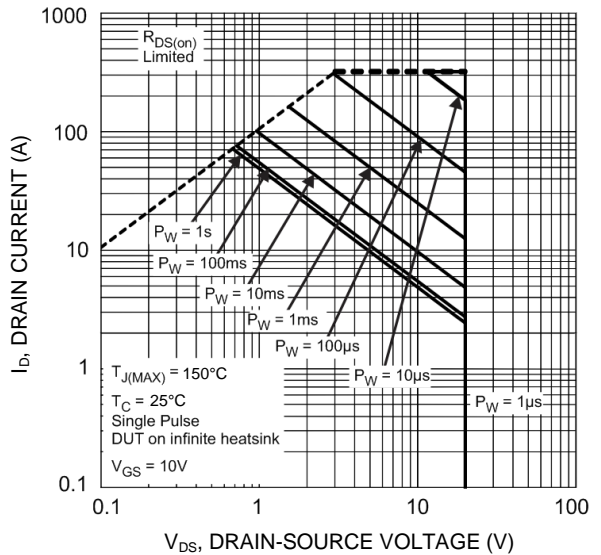


Figure 12. SOA, Safe Operation Area

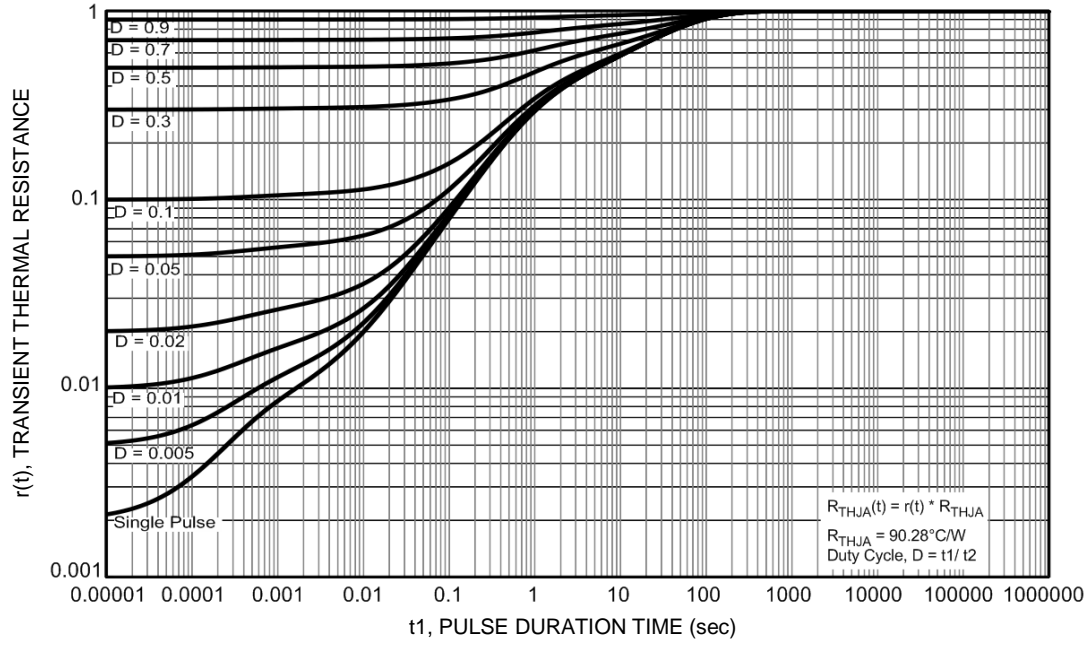
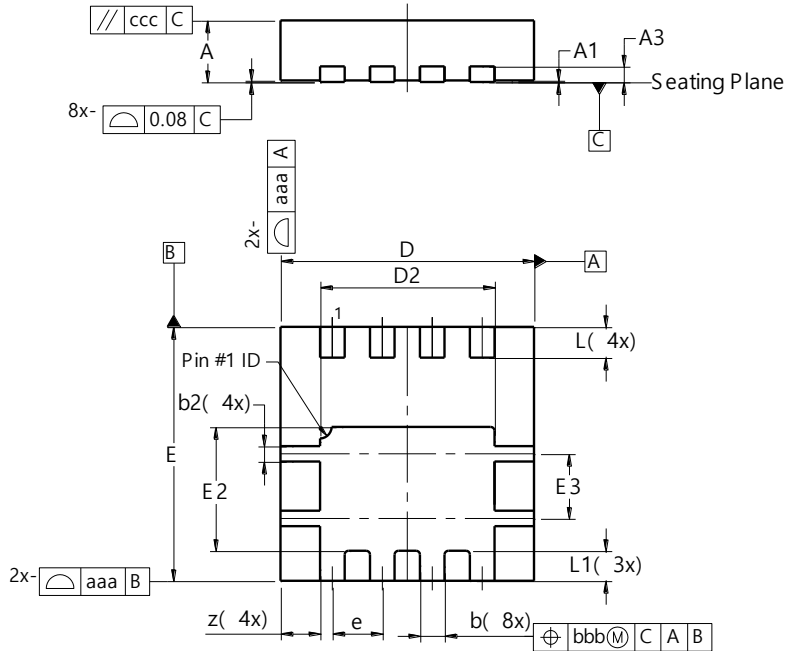


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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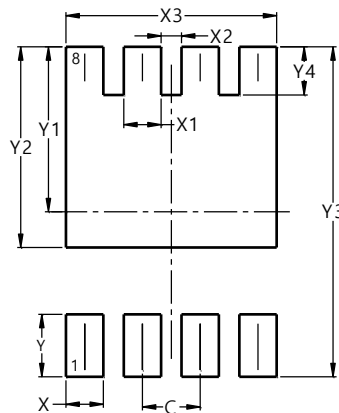


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Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.27	0.37	0.32
b2	-	-	0.20
D	3.25	3.35	3.30
D2	2.22	2.32	2.27
E	3.25	3.35	3.30
E2	1.56	1.66	1.61
E3	0.79	0.89	0.84
e	-	-	0.65
L	0.35	0.45	0.40
L1	-	-	0.39
z	-	-	0.515
aaa	0.25		
bbb	0.10		
ccc	0.10		
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.370
Y	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Y4	0.540

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