

MOSFET
OptiMOS™ 6 Power-Transistor, 150 V

Features

- N-channel, normal level
- Very low on-resistance R_DS(on)
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Table with 3 columns: Parameter, Value, Unit. Rows include V_DS (150 V), R_DS(on),max (3.4 mΩ), I_D (194 A), Q_oss (205 nC), Q_G (69 nC), and Q_rr (500A/μs) (156 nC).

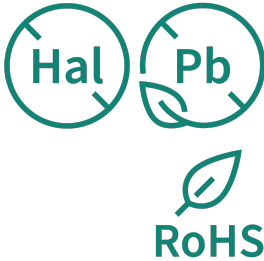
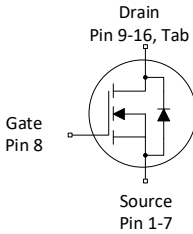
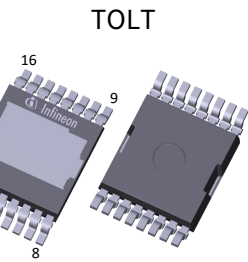


Table with 4 columns: Type / Ordering code, Package, Marking, Related links. Row 1: IPTC034N15NM6, PG-HDSOP-16, 034N15N6, -



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1 Maximum ratings

at $T_A=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	194 137 125 22	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ }^{\circ}\text{C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ }^{\circ}\text{C}$ $V_{GS}=8\text{ V}$, $T_C=100\text{ }^{\circ}\text{C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ }^{\circ}\text{C}$, $R_{thJA}=40\text{ }^{\circ}\text{C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	776	A	$T_C=25\text{ }^{\circ}\text{C}$
Avalanche current, single pulse ⁴⁾	I_{AS}	-	-	84	A	
Avalanche energy, single pulse	E_{AS}	-	-	484	mJ	$I_D=53\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	294 3.8	W	$T_C=25\text{ }^{\circ}\text{C}$ $T_A=25\text{ }^{\circ}\text{C}$, $R_{thJA}=40\text{ }^{\circ}\text{C/W}$ ²⁾
Operating and storage temperature	T_j , T_{stg}	-55	-	175	$^{\circ}\text{C}$	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.51	$^{\circ}\text{C/W}$	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	40	$^{\circ}\text{C/W}$	
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	$^{\circ}\text{C/W}$	

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.5	4.0	V	$V_{DS}=V_{GS}$, $I_D=179\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.9 3.1 3.5	3.2 3.4 4.1	$\text{m}\Omega$	$V_{GS}=15\text{ V}$, $I_D=84\text{ A}$ $V_{GS}=10\text{ V}$, $I_D=84\text{ A}$ $V_{GS}=8\text{ V}$, $I_D=42\text{ A}$
Gate resistance	R_G	-	0.98	1.47	Ω	-
Transconductance	g_{fs}	70	140	-	S	$ V_{DS} \geq 2 I_D $, $R_{DS(on)max}$, $I_D=84\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁶⁾	C_{iss}	-	4900	6400	pF	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}	-	1500	2000	pF	
Reverse transfer capacitance ⁶⁾	C_{rss}	-	19	33	pF	
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=42\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	9	-	ns	
Turn-off delay time	$t_{d(off)}$	-	26	-	ns	
Fall time	t_f	-	12	-	ns	

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge ⁸⁾	Q_{gs}	-	27	36	nC	$V_{DD}=75\text{ V}$, $I_D=42\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	17.3	-	nC	
Gate to drain charge ⁸⁾	Q_{gd}	-	15.7	24	nC	
Switching charge	Q_{sw}	-	25	-	nC	
Gate charge total ⁸⁾	Q_g	-	69	86	nC	
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	58	-	nC	
Output charge ⁸⁾	Q_{oss}	-	205	273	nC	$V_{DS}=75\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

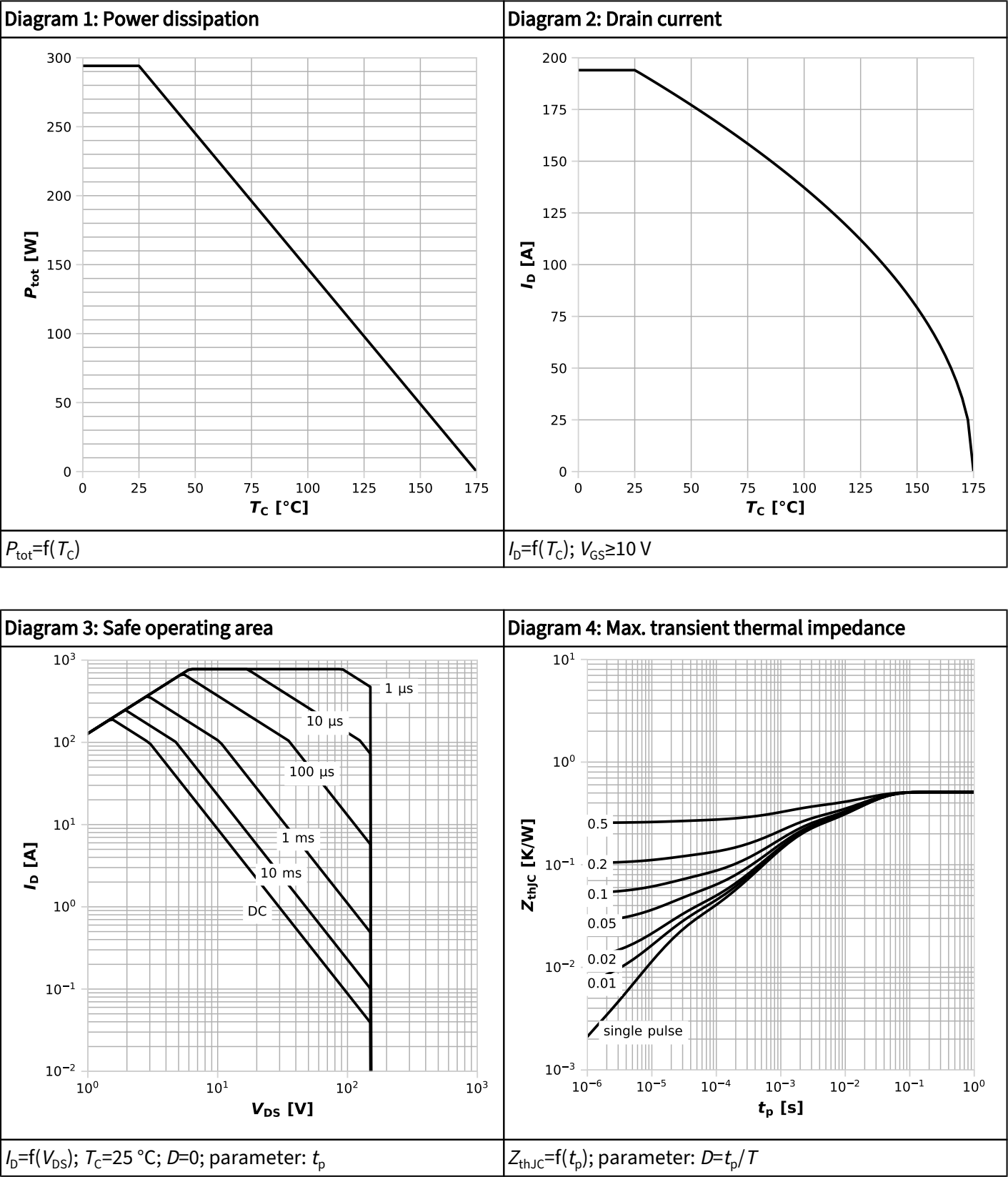
⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	194	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	776	A	
Diode forward voltage	V_{SD}	-	0.86	1.0	V	$V_{GS}=0\text{ V}$, $I_F=84\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	36	72	ns	$V_R=75\text{ V}$, $I_F=42\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	156	312	nC	
Reverse recovery time ⁹⁾	t_{rr}	-	33	66	ns	$V_R=75\text{ V}$, $I_F=42\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	277	554	nC	

⁹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams



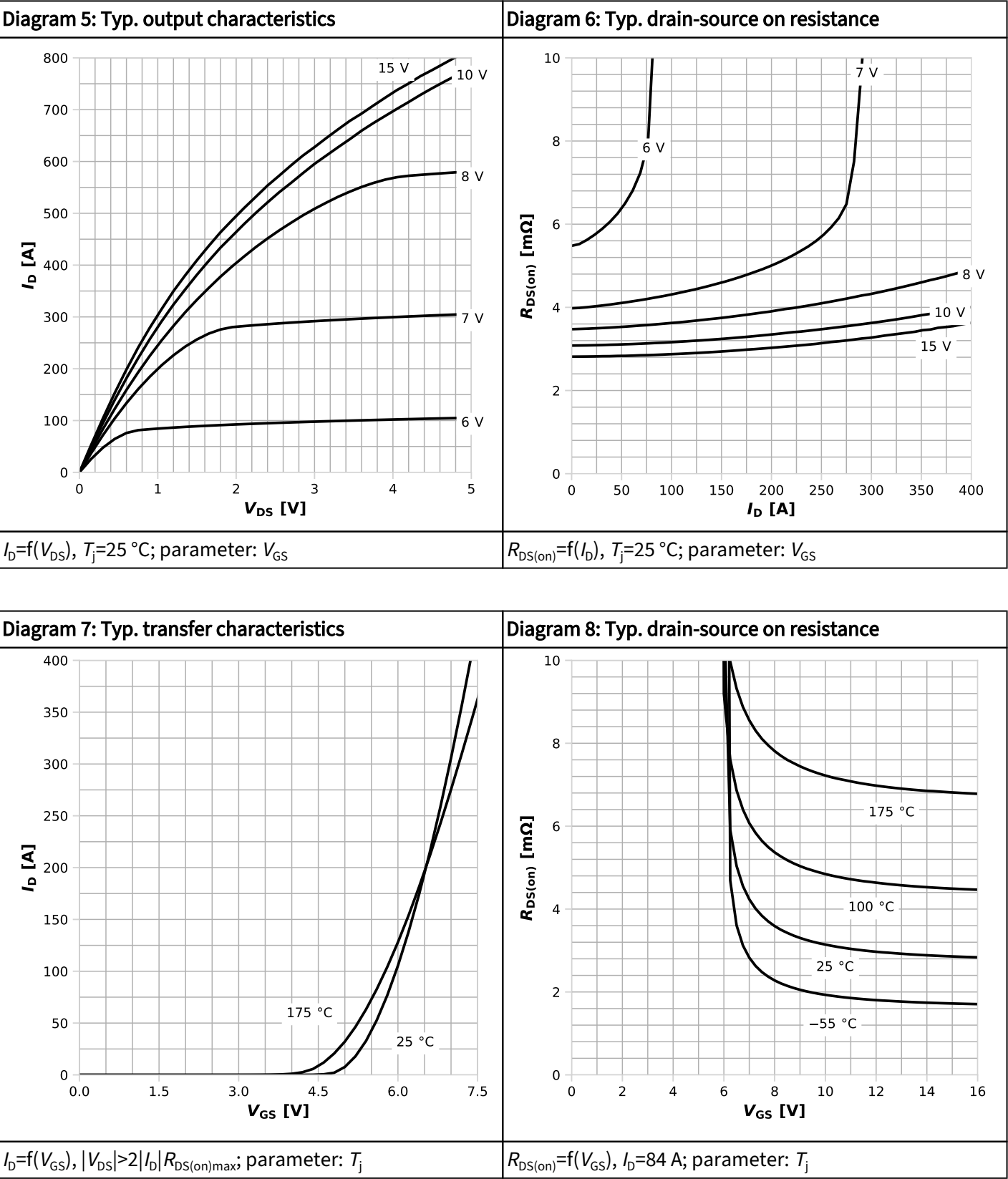
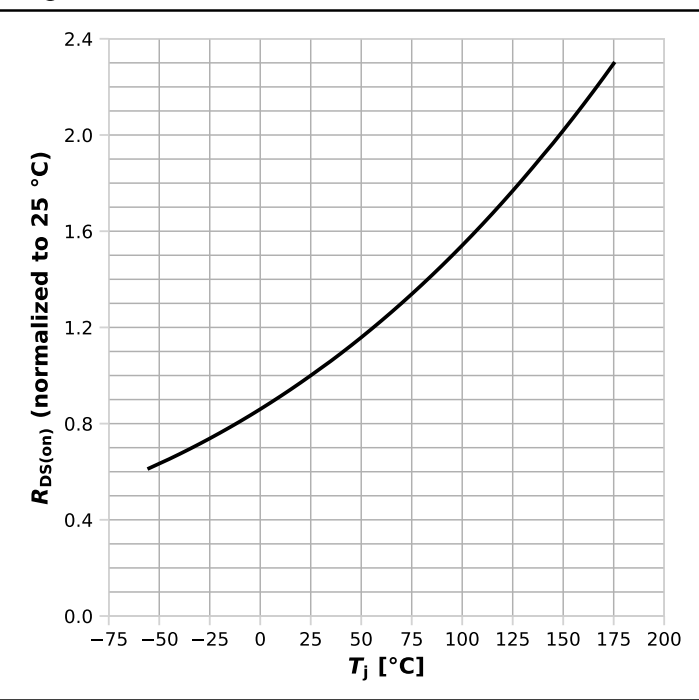
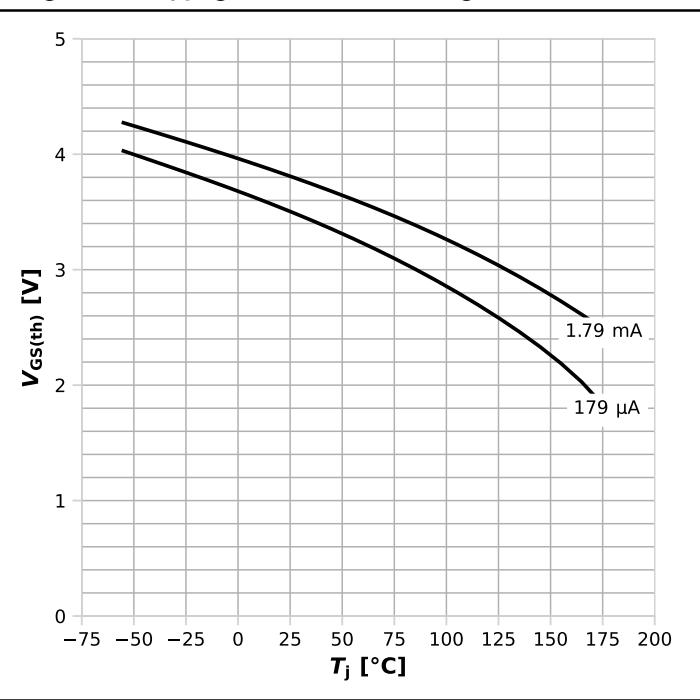


Diagram 9: Normalized drain-source on resistance



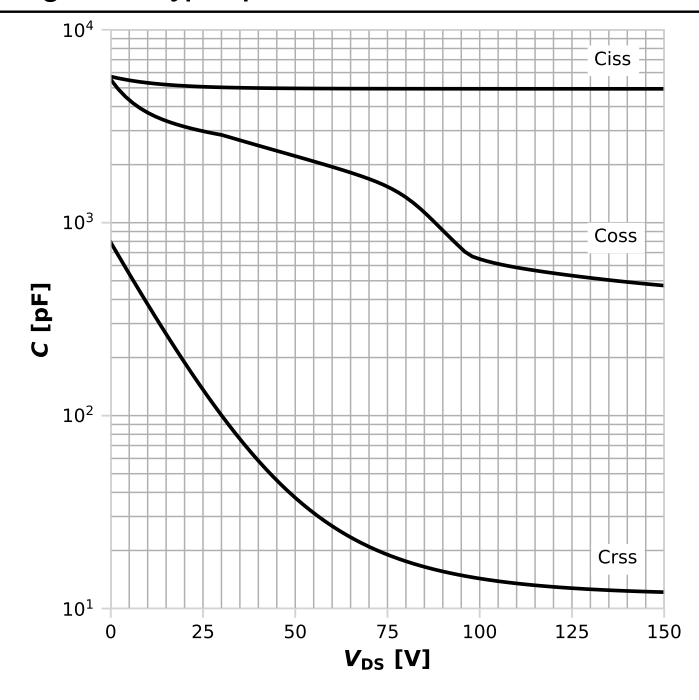
$R_{DS(on)}=f(T_j)$, $I_D=84$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



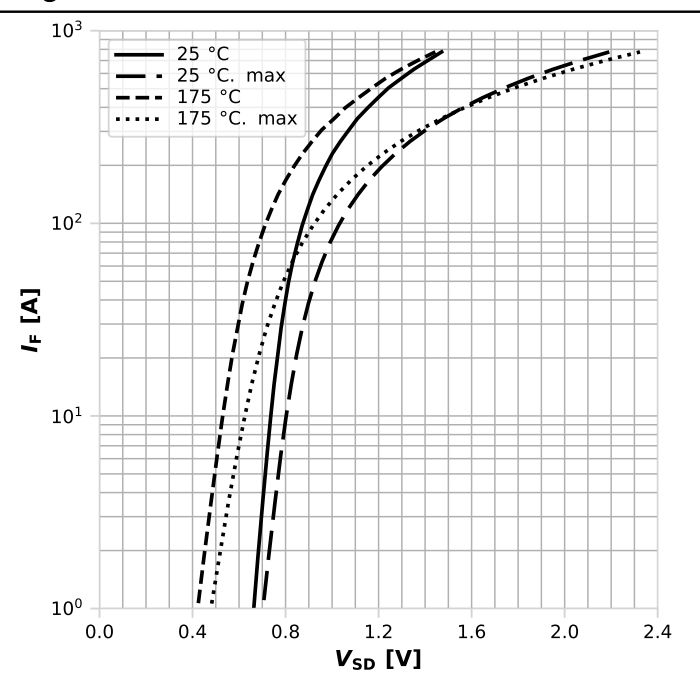
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



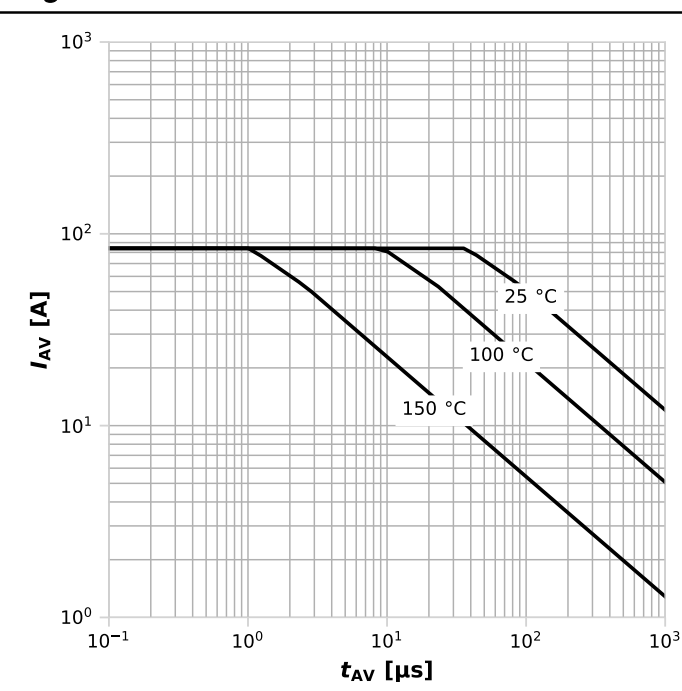
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



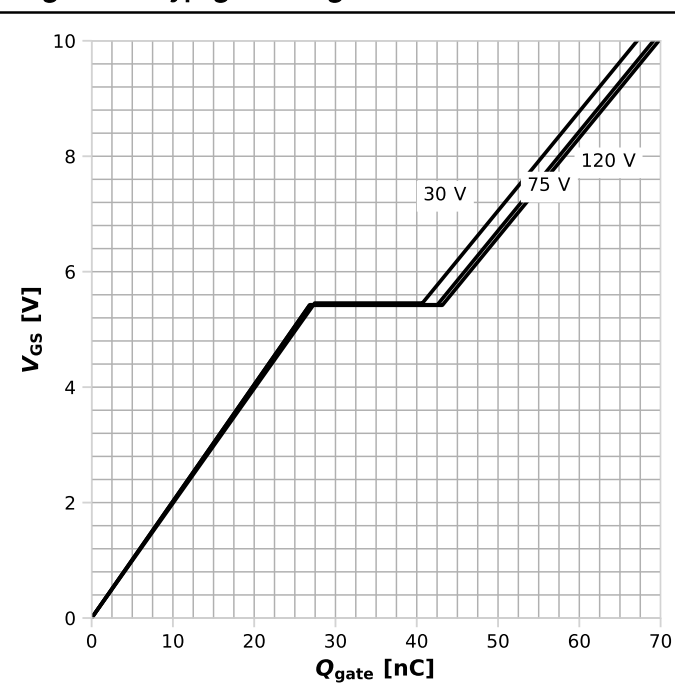
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



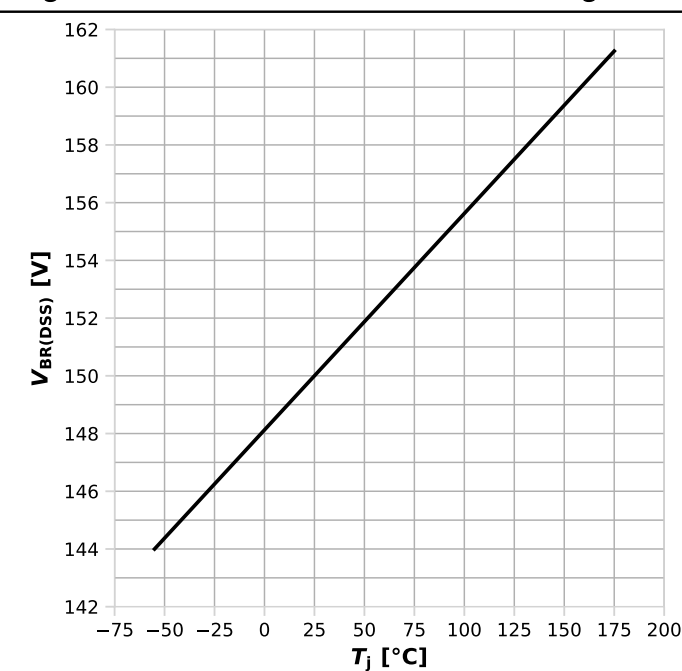
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



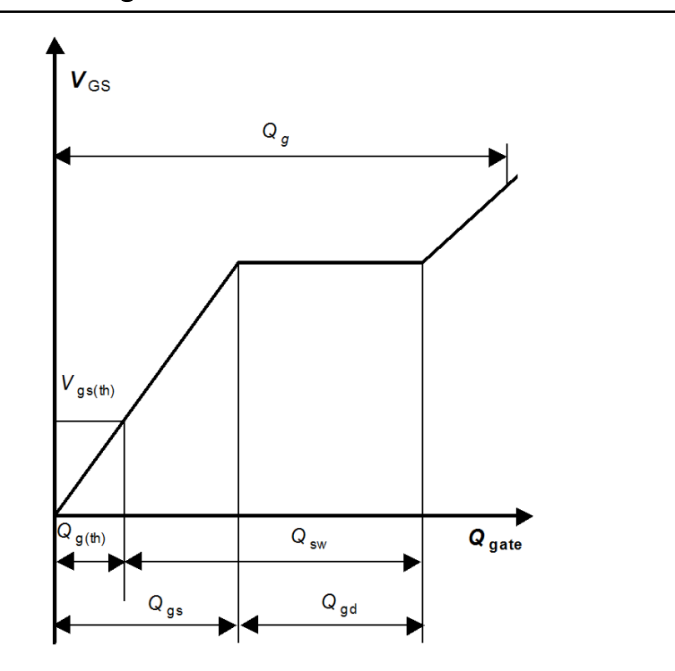
$V_{GS}=f(Q_{gate})$, $I_D=42\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



5 Package outlines

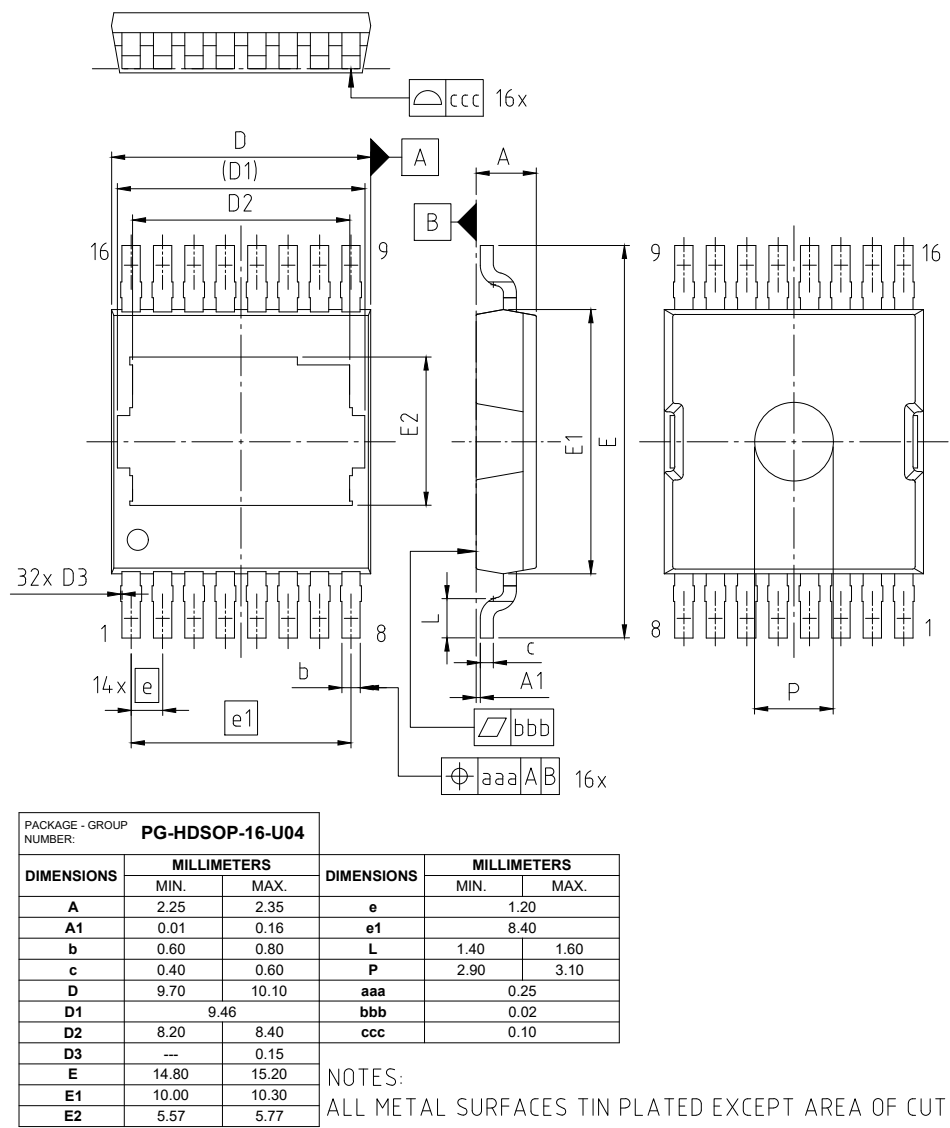


Figure 1 Outline PG-HDSOP-16, dimensions in mm

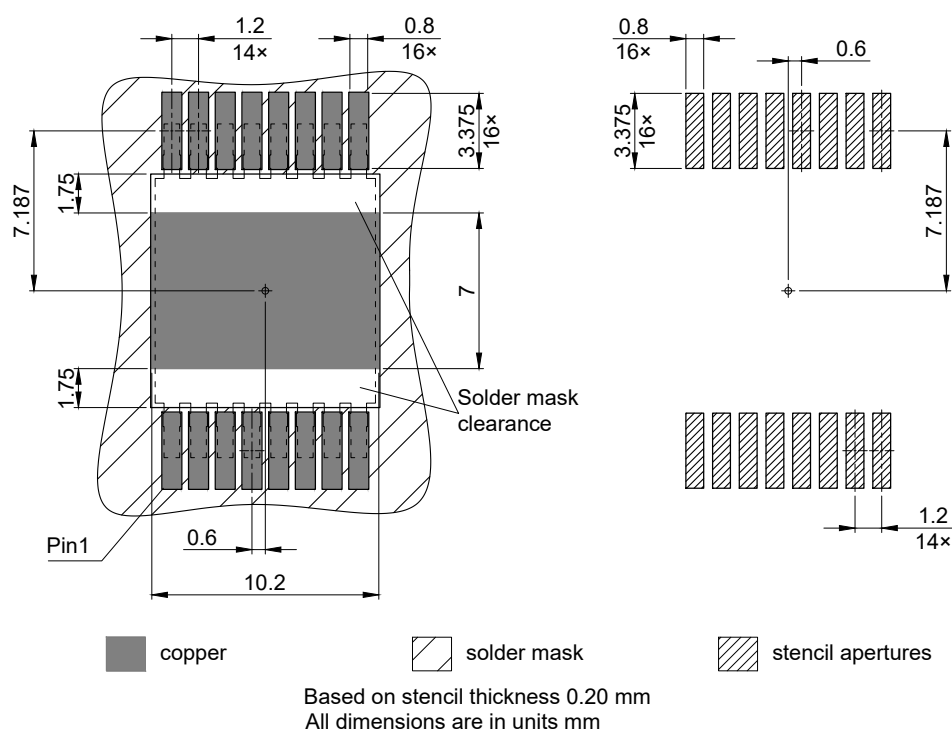
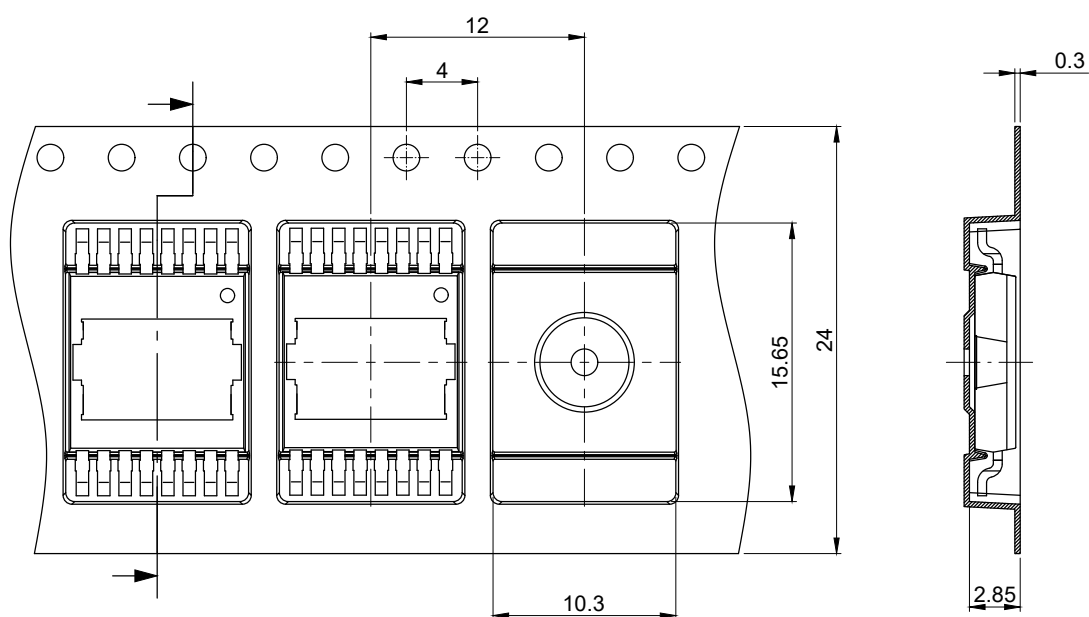


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HDSOP-16, dimensions in mm



Revision history

IPTC034N15NM6

Revision 2024-12-09, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-12-09	Release of final datasheet

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