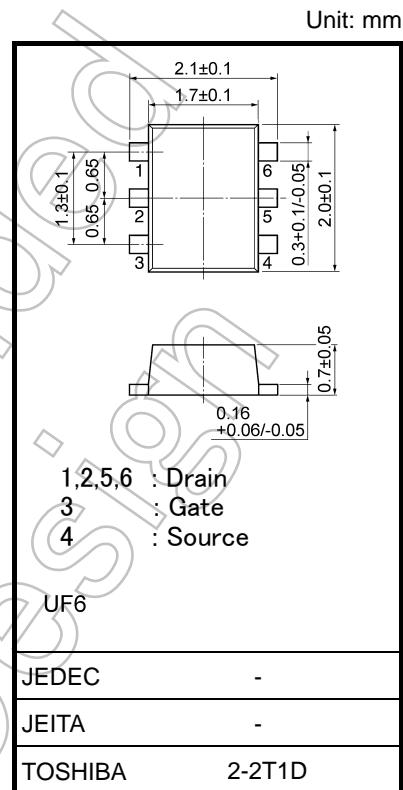


TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSIV)

# SSM6J51TU

## High Current Switching Applications

- Suitable for high-density mounting due to compact package
- Low on-resistance:  $R_{on} = 54 \text{ m}\Omega$  (max) (@ $V_{GS} = -2.5 \text{ V}$ )  
 $85 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.8 \text{ V}$ )  
 $150 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.5 \text{ V}$ )



Weight: 7 mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e.

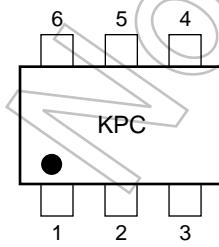
operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

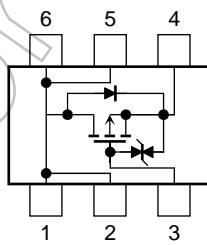
Note 1: Mounted on an FR4 board.

(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm<sup>2</sup>)

## Marking



## Equivalent Circuit (top view)



## Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

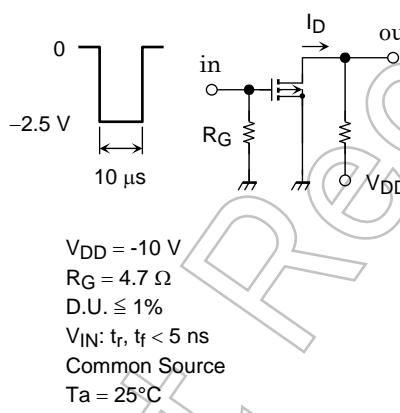
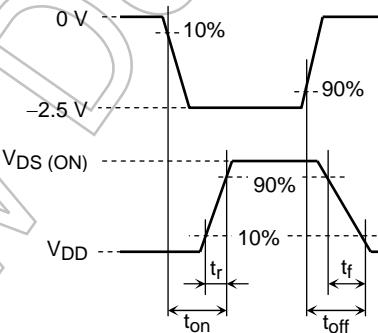
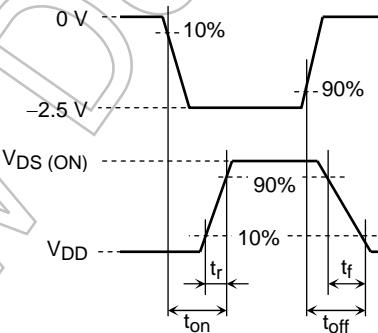
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0	—	—	±10	μA	
Drain-Source breakdown voltage	V <sub>(BR)</sub> DSS	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0	-12	—	—	V	
	V <sub>(BR)</sub> DSX	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = +8 V	-4	—	—		
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = -12 V, V <sub>GS</sub> = 0	—	—	-10	μA	
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1 mA	-0.3	—	-1.0	V	
Forward transfer admittance	Y <sub>fs</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -2.0 A (Note 2)	6.0	12.0	—	S	
Drain-Source on-resistance	R <sub>DS</sub> (ON)	I <sub>D</sub> = -2.0 A, V <sub>GS</sub> = -2.5 V (Note 2)	—	38	54	mΩ	
		I <sub>D</sub> = -1.0 A, V <sub>GS</sub> = -1.8 V (Note 2)	—	48	85		
		I <sub>D</sub> = -0.3 A, V <sub>GS</sub> = -1.5 V (Note 2)	—	60	150		
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1 MHz	—	1700	—		
Reverse transfer capacitance	C <sub>rss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1 MHz	—	190	—	pF	
Output capacitance	C <sub>oss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1 MHz	—	210	—	pF	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2.0 A, V <sub>GS</sub> = 0~ -2.5 V, R <sub>G</sub> = 4.7 Ω	—	57	—	ns
	Turn-off time	t <sub>off</sub>		—	120	—	

Note 2: Pulse test

## Switching Time Test Circuit

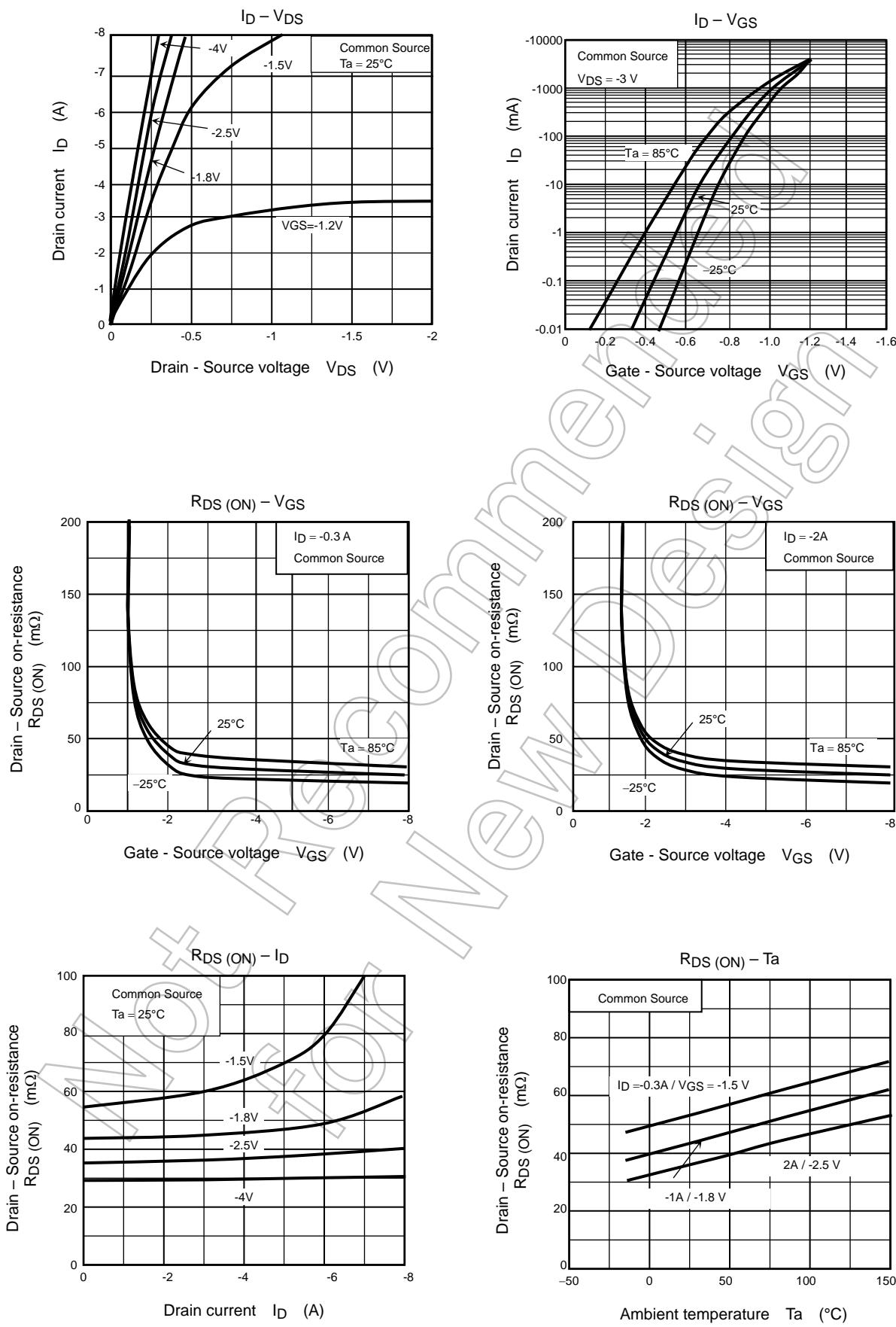
## (a) Test Circuit

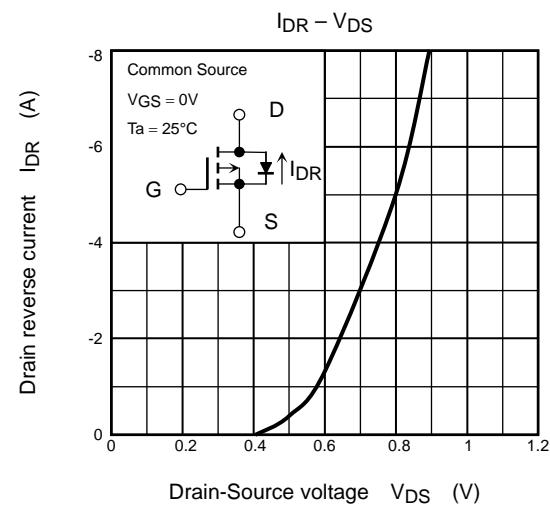
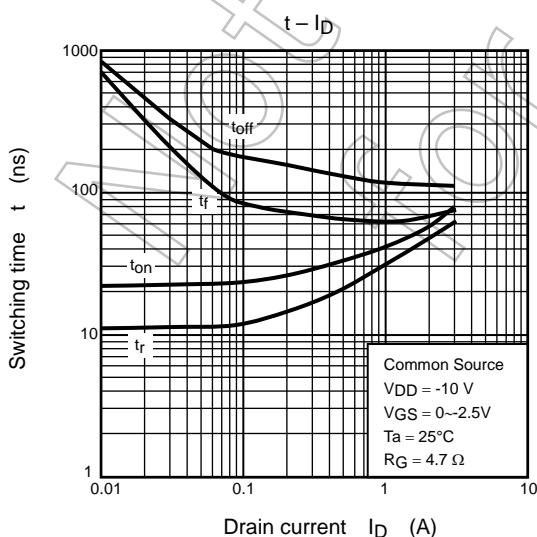
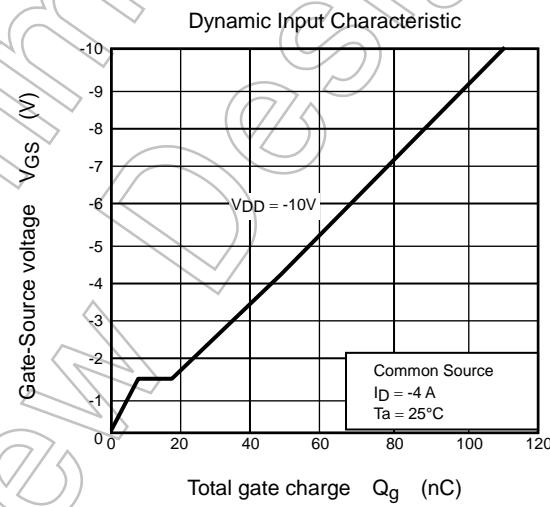
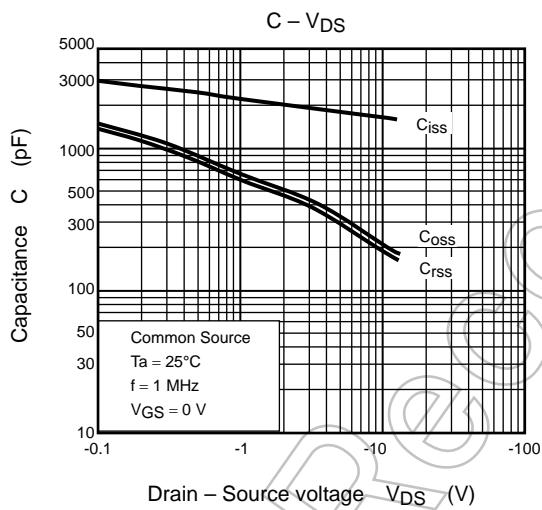
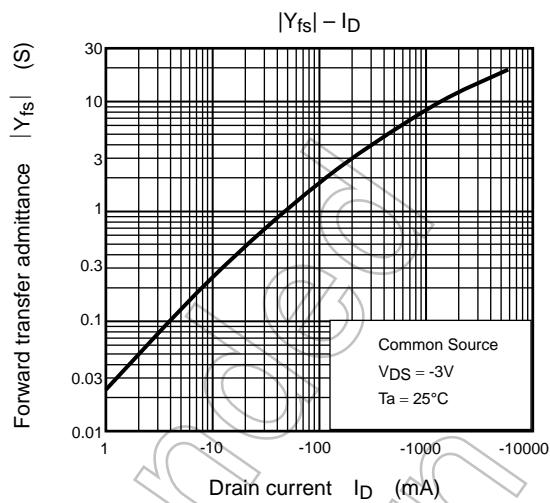
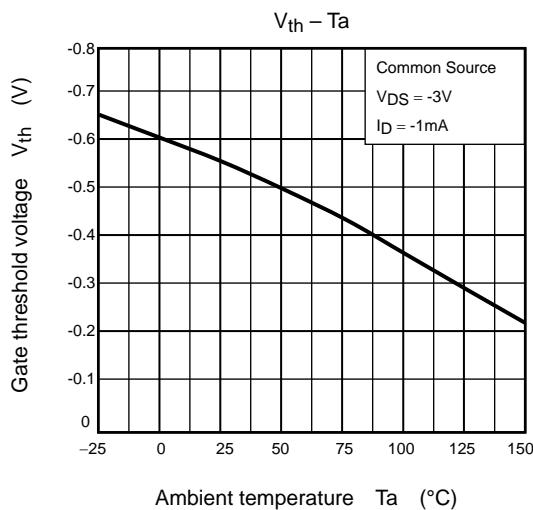
(b) V<sub>IN</sub>(c) V<sub>OUT</sub>

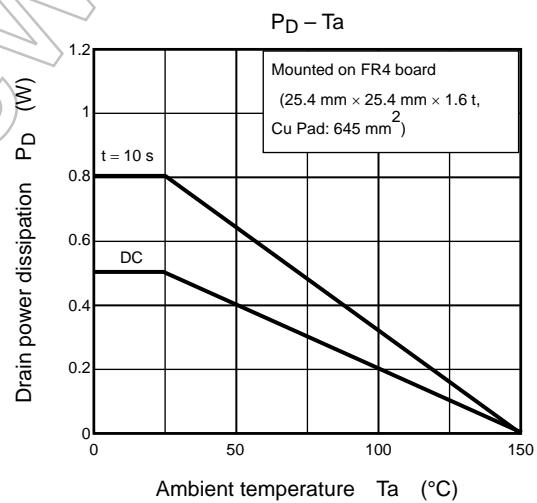
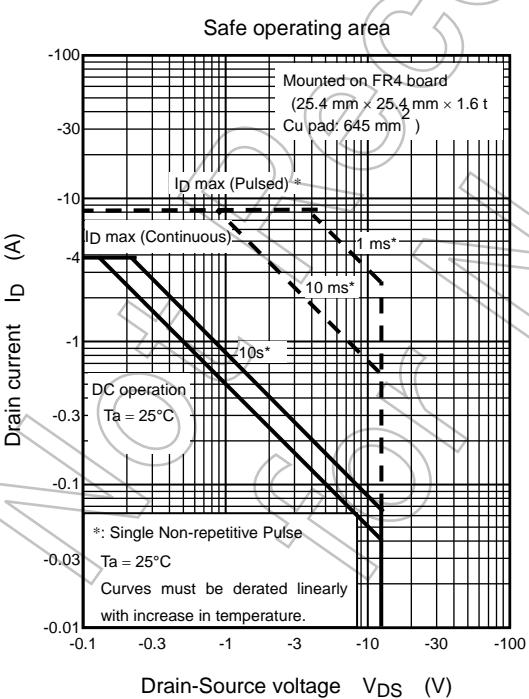
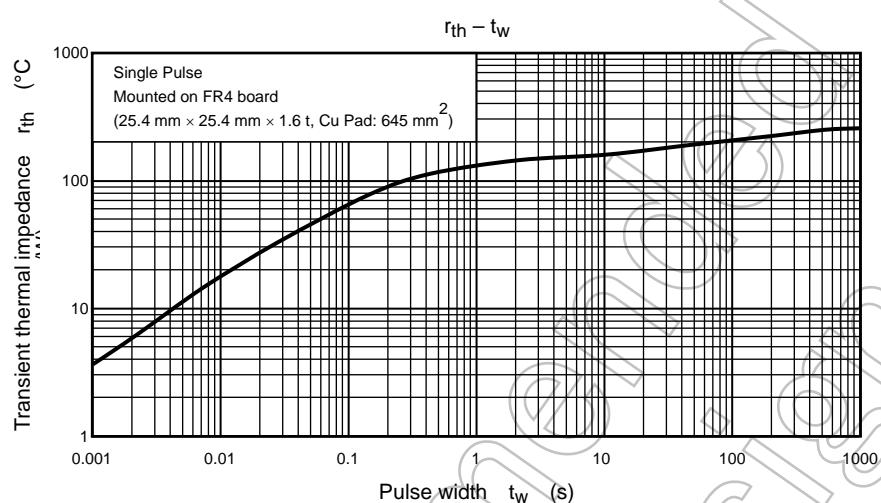
## Precaution

V<sub>th</sub> can be expressed as the voltage between the gate and source when the low operating current value is I<sub>D</sub> = -1mA for this product. For normal switching operation, V<sub>GS</sub> (on) requires a higher voltage than V<sub>th</sub> and V<sub>GS</sub> (off) requires a lower voltage than V<sub>th</sub>. (The relationship can be established as follows: V<sub>GS</sub> (off) < V<sub>th</sub> < V<sub>GS</sub> (on).)

Be sure to take this into consideration when using the device.







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