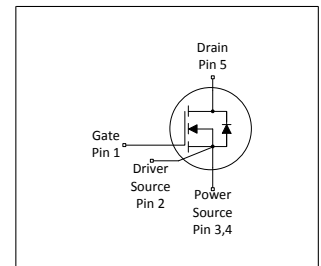
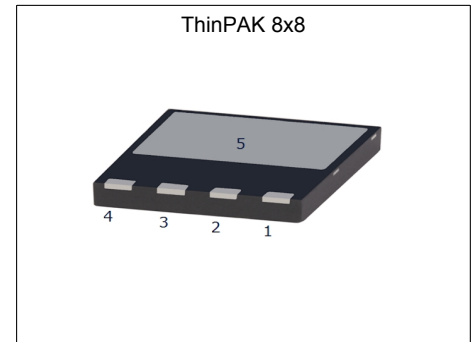


MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.



Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_f/dt ruggedness
- Lowest FOM $R_{DS(on)} \cdot Q_g$ and $R_{DS(on)} \cdot E_{oss}$
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product Validation: Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	140	mΩ
$Q_{g,typ}$	35	nC
$I_{D,pulse}$	66	A
$E_{oss} @ 400V$	4.1	μJ
Body diode di_f/dt	1300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPL60R140CFD7	PG-VSON-4	60R140F7	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	18 12.0	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	66	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	78	mJ	$I_D=4.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.39	mJ	$I_D=4.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	4.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	106	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	18	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	66	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 18\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	diF/dt	-	-	1300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 18\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_θ .

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.18	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL2A

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}$, $I_D=0.39mA$
Zero gate voltage drain current ¹⁾	I_{DSS}	-	-	1	μA	$V_{DS}=600V$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=600V$, $V_{GS}=0V$, $T_j=125^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.112 0.253	0.14 -	Ω	$V_{GS}=10V$, $I_D=7.8A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=7.8A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	8.8	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1503	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	28	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ²⁾	$C_{o(er)}$	-	51	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ³⁾	$C_{o(tr)}$	-	520	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.9A$, $R_G=9.0\Omega$; see table 9
Rise time	t_r	-	11	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.9A$, $R_G=9.0\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	80	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.9A$, $R_G=9.0\Omega$; see table 9
Fall time	t_f	-	4.5	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=7.9A$, $R_G=9.0\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	9	-	nC	$V_{DD}=400V$, $I_D=7.9A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	12	-	nC	$V_{DD}=400V$, $I_D=7.9A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	35	-	nC	$V_{DD}=400V$, $I_D=7.9A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.6	-	V	$V_{DD}=400V$, $I_D=7.9A$, $V_{GS}=0$ to $10V$

¹⁾ Maximum specification is defined by calculated six sigma upper confidence bound

²⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

³⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	$V_{GS}=0V$, $I_F=7.8A$, $T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	103	155	ns	$V_R=400V$, $I_F=7.9A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.42	0.84	μC	$V_R=400V$, $I_F=7.9A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	7.3	-	A	$V_R=400V$, $I_F=7.9A$, $di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

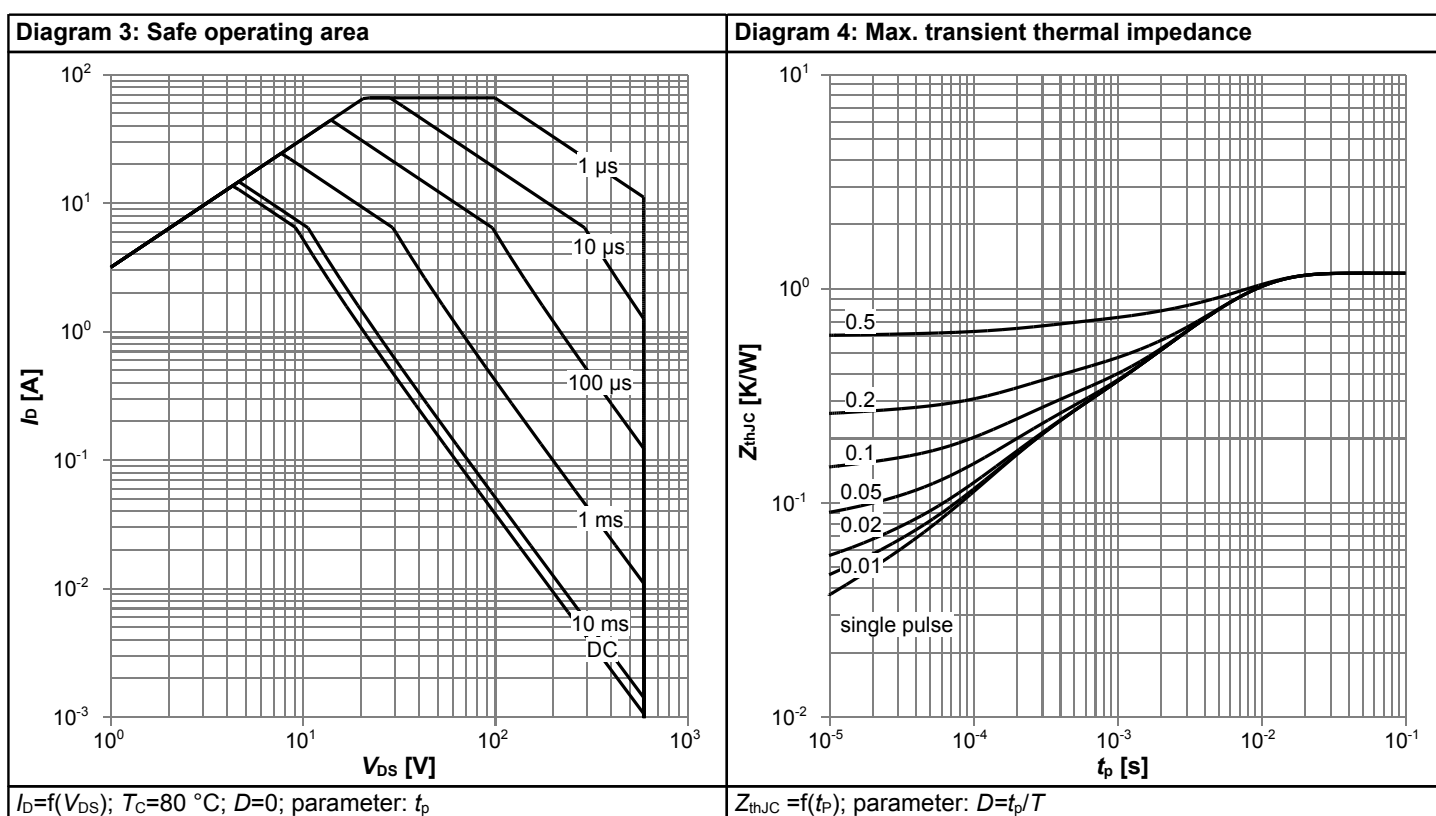
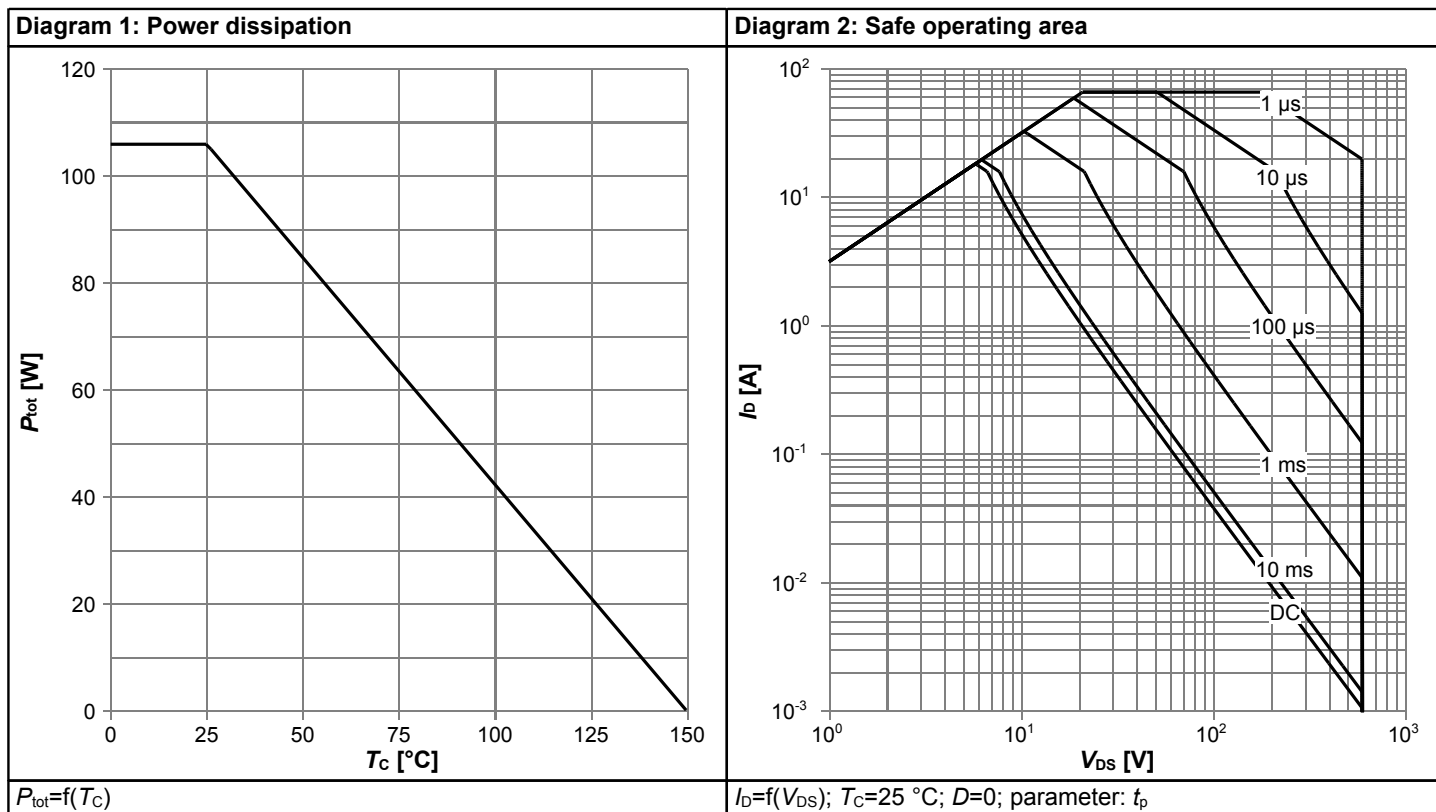
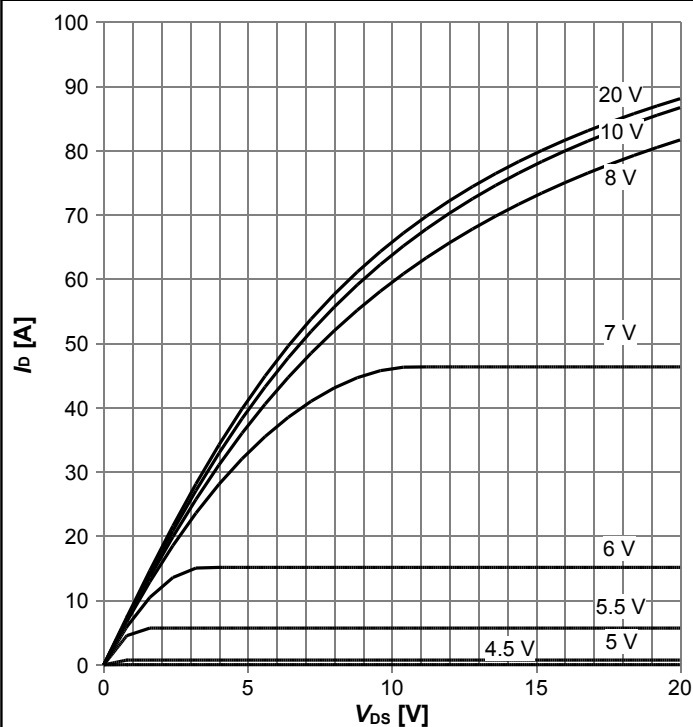
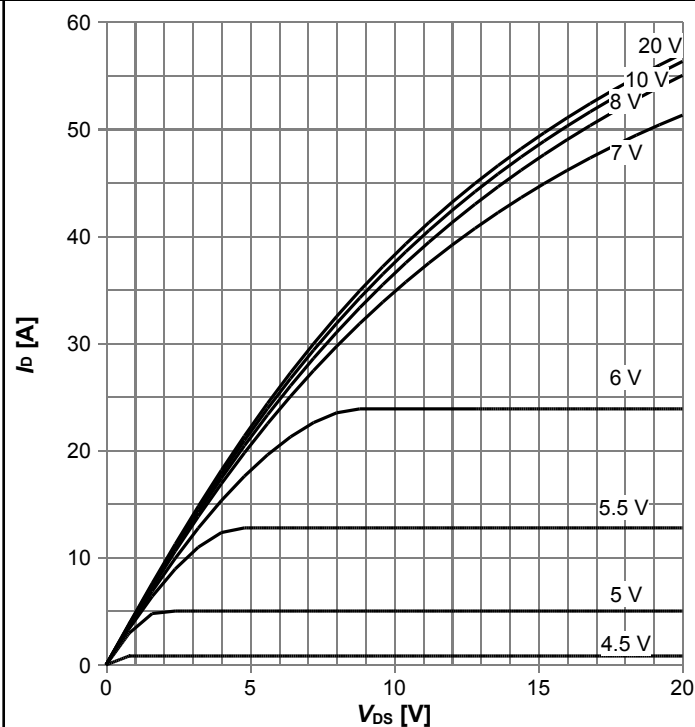


Diagram 5: Typ. output characteristics



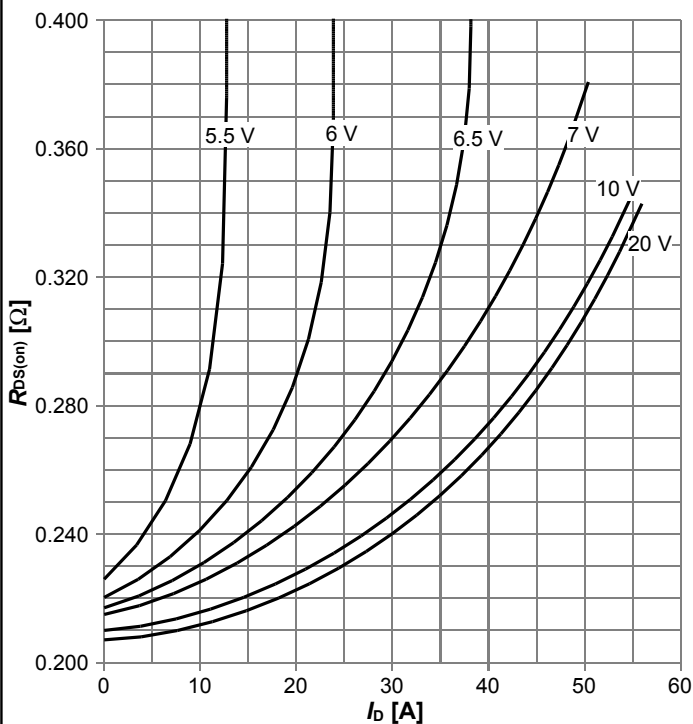
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



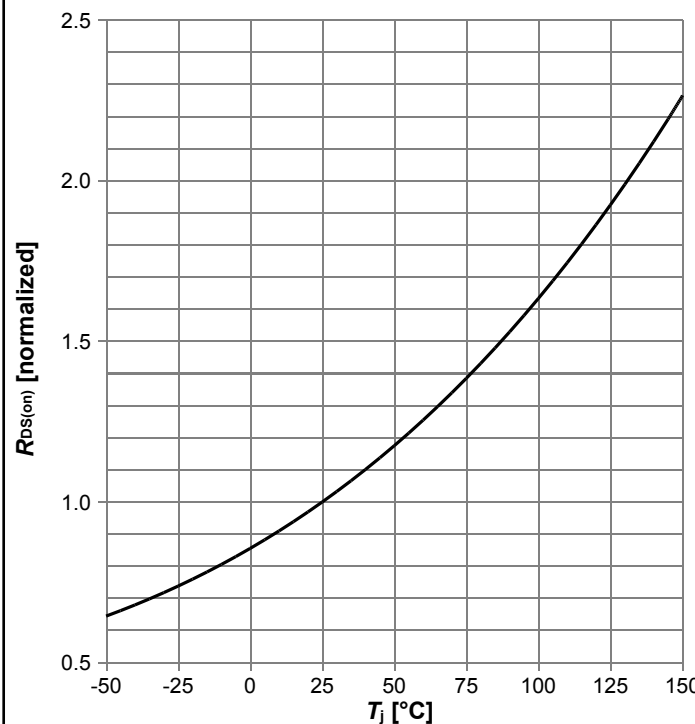
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



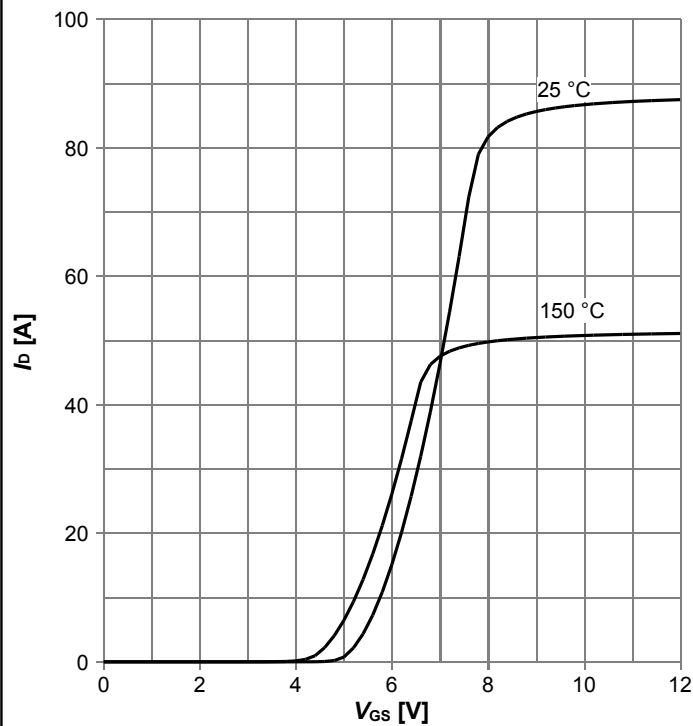
$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



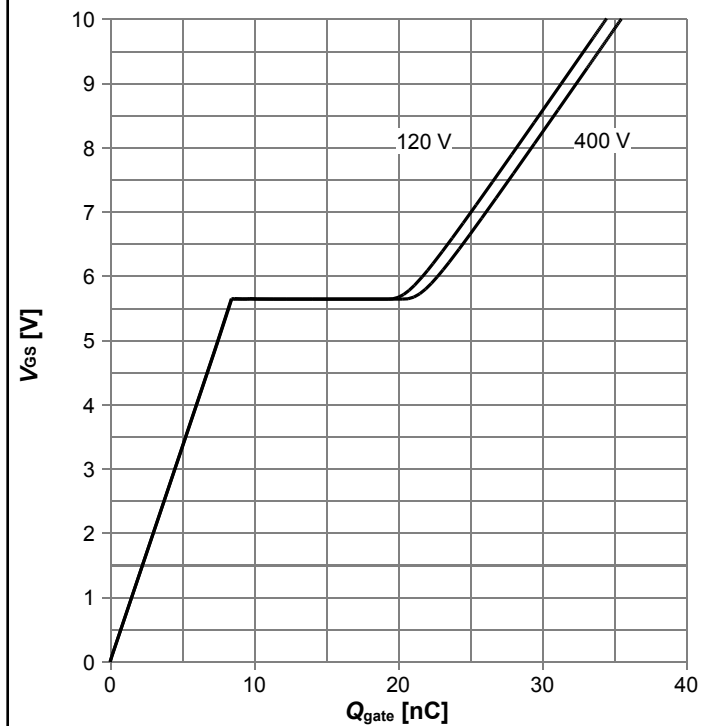
$R_{DS(on)} = f(T_j)$; $I_D = 7.8\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



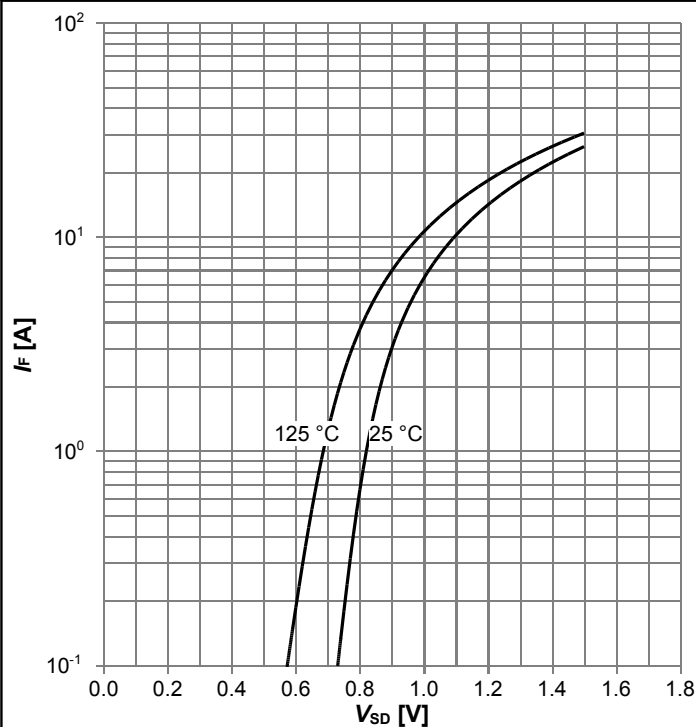
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



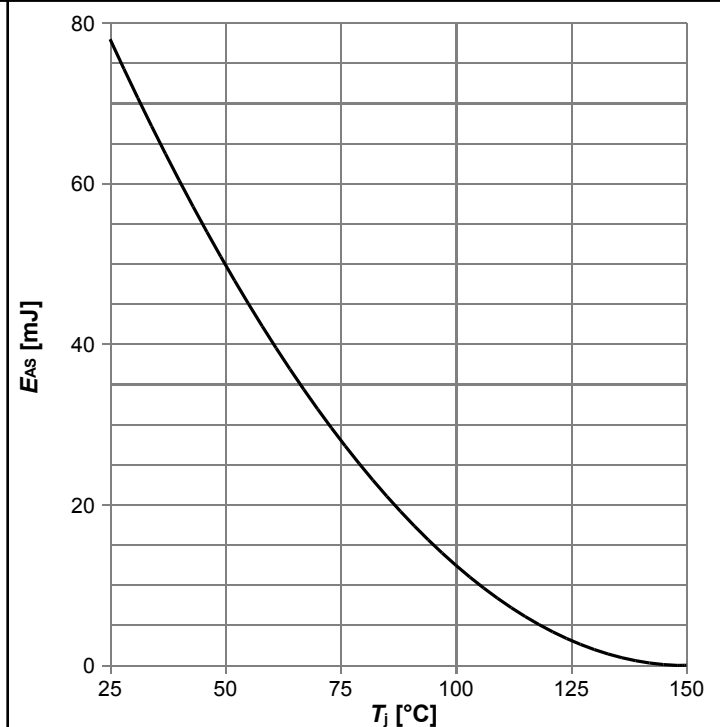
$V_{GS} = f(Q_{gate})$; $I_D = 7.9$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



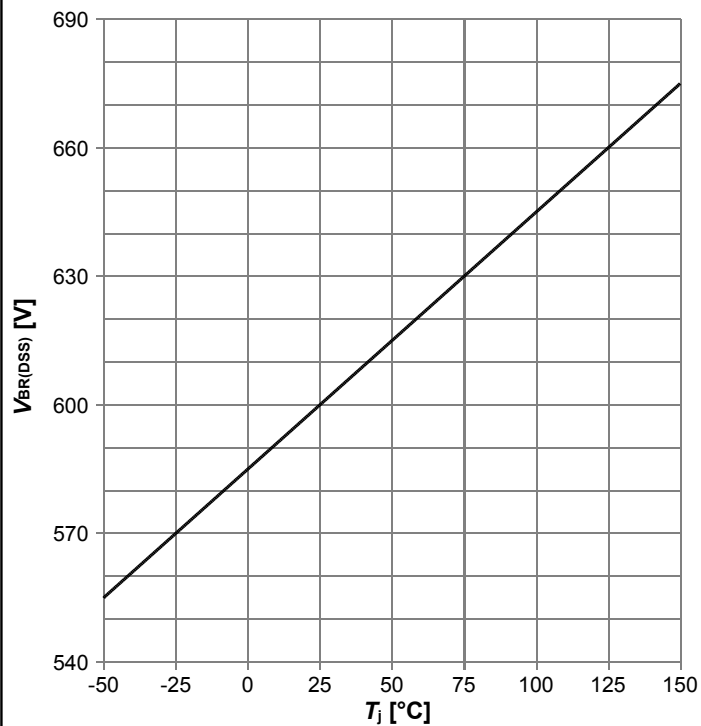
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



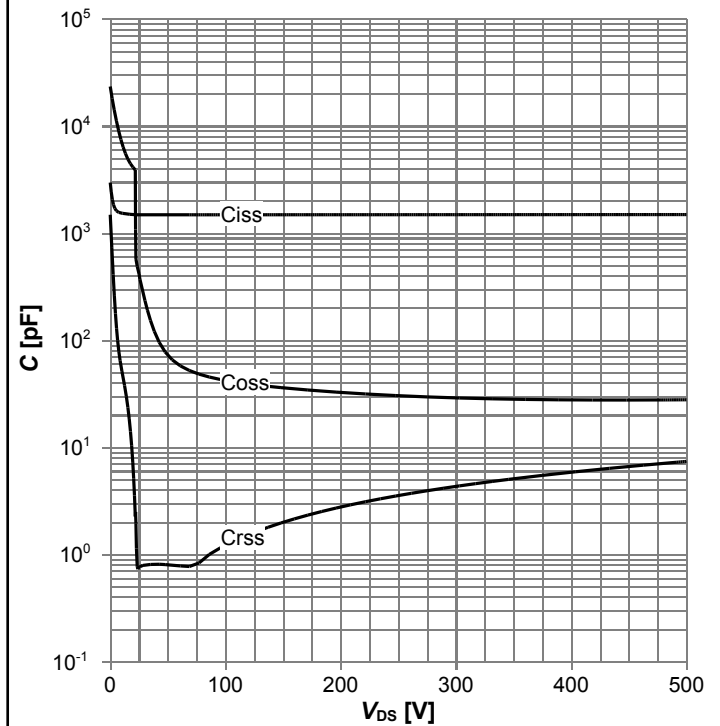
$E_{AS} = f(T_j)$; $I_D = 4.4$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



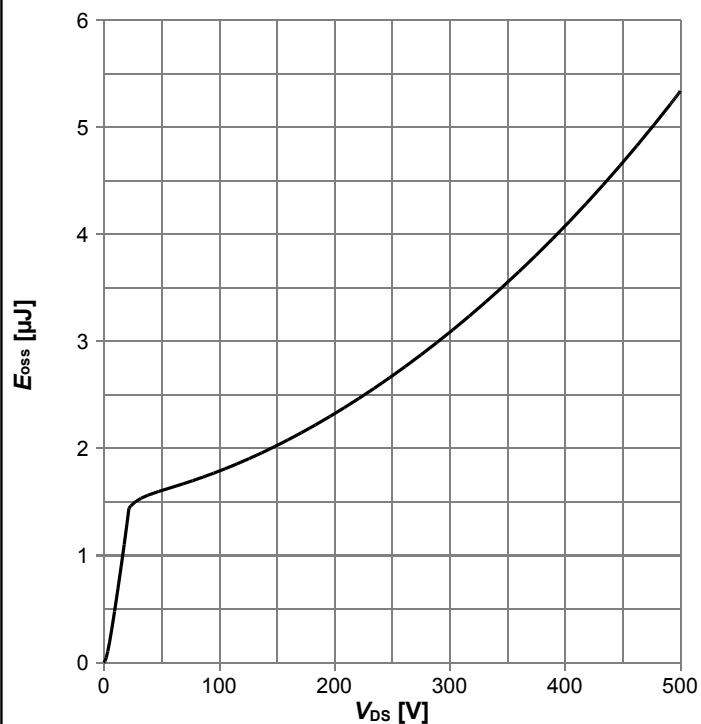
$V_{BR(DSS)} = f(T_J); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

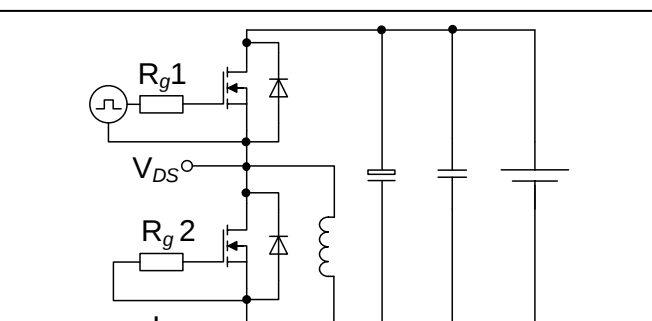
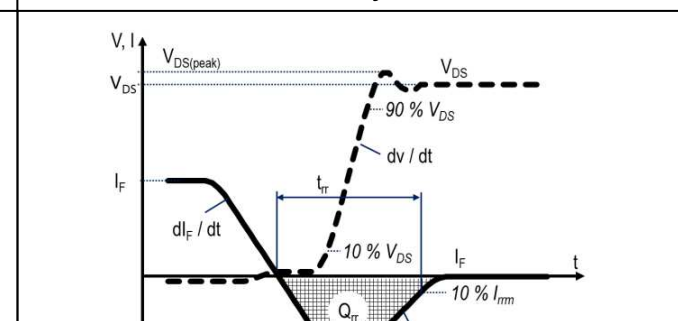
Test circuit for diode characteristics  $R_{g1} = R_{g2}$	Diode recovery waveform 
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Table 9 Switching times

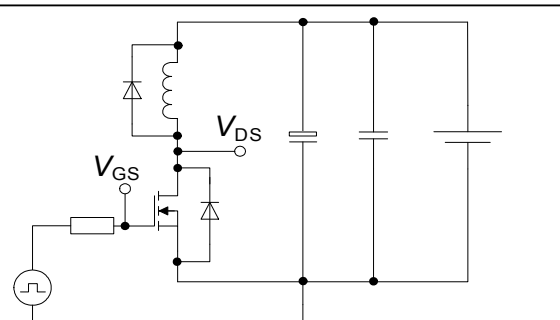
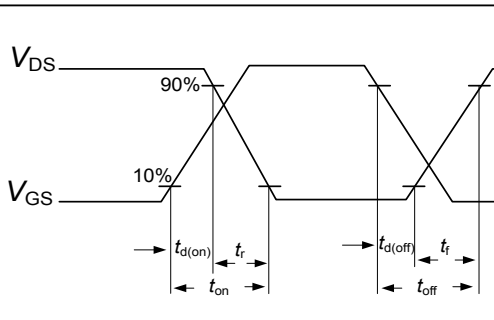
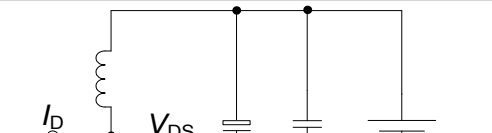
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a MOSFET switching an inductive load. A pulse source is connected to the MOSFET gate through a resistor. The MOSFET's drain is connected to an inductor, which is in series with a load capacitor. A freewheeling diode is connected in parallel with the inductor and capacitor. The MOSFET's source is grounded. The drain-source voltage is labeled V_{DS} and the gate-source voltage is labeled V_{GS}.	 The timing diagram shows the switching waveforms for V_{DS} and V_{GS}. The V_{GS} signal is a square wave that transitions between a low level and a high level. The V_{DS} signal shows the voltage across the MOSFET during these transitions. Key time intervals are marked: $t_{d(on)}$: Delay time from the start of the V_{GS} rise to the 10% point of the V_{DS} fall. t_r: Rise time of V_{DS} from 90% to 10% during the V_{GS} fall. $t_{d(off)}$: Delay time from the start of the V_{GS} fall to the 90% point of the V_{DS} rise. t_f: Fall time of V_{DS} from 90% to 10% during the V_{GS} rise. t_{on}: Total on-time from the start of V_{GS} rise to the start of V_{GS} fall. t_{off}: Total off-time from the start of V_{GS} fall to the start of V_{GS} rise.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 application note:** www.infineon.com
- **IFX CoolMOS CFD7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPL60R140CFD7

Revision: 2018-11-13, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-04-20	Release of final version
2.1	2018-11-13	Table 7: Reduced trr,max value; Change of qualification grade nomenclature

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