Precision Instrumentation Amplifier with Level Shift and Output Clamping

FEATURES

- **Single Gain Set Resistor: G = 1 to >1000**
- **Excellent DC Precision**
  - **Input Offset Voltage: 60µV Max**
  - **Input Offset Voltage Drift: 0.6µV/°C Max**
  - **Low Gain Error: 0.01% Max (G = 1)**
  - **Low Gain Drift: 35ppm/°C Max (G > 1)**
  - **High DC CMRR: 86dB Min (G = 1)**
- **Integrated Output Clamps**
- **Integrated Output Level Shift**
- Input Bias Current: 800pA Max
- 3.1MHz –3dB Bandwidth (G = 1)
- Low Noise:
  - 0.1Hz to 10Hz Noise: $0.2µV_{P-P}$
  - 1kHz Voltage Noise: $7nV/\sqrt{Hz}$
- Integrated Input RFI Filter
- Wide Supply Range 4.75V to 35V
- Temperature Ranges: –40°C to 85°C and –40°C to 125°C
- MS16E and 20-Lead 3mm × 4mm QFN Packages

APPLICATIONS

- Bridge Amplifier
- Data Acquisition
- Thermocouple Amplifier
- Strain Gauge Amplifier
- Medical Instrumentation
- Transducer Interfaces
- Differential to Single-Ended Conversion

DESCRIPTION

The LT®6372-1 is a gain programmable, high precision instrumentation amplifier that delivers industry leading DC precision. This high precision enables smaller signals to be sensed and eases calibration requirements, particularly over temperature. The LT6372-1 incorporates features into the LT6370 which further improve accuracy and simplify interfacing to an ADC.

The LT6372-1 uses a proprietary high performance bipolar process which enables industry leading accuracy coupled with exceptional long-term stability. The LT6372-1 is laser trimmed for very low input offset voltage (60µV) and high CMRR (86dB, G = 1). Proprietary on-chip test capability allows the gain drift (35ppm/°C) to be guaranteed with automated testing.

The LT6372-1's difference amplifier uses a split reference configuration which simplifies level shifting the amplifier's output to the center of the ADC's input range. Output clamp pins are also provided to limit the voltage which can be applied to an ADC's input. EMI filtering is integrated on the LT6372-1's inputs to maintain accuracy in the presence of harsh RF interference.
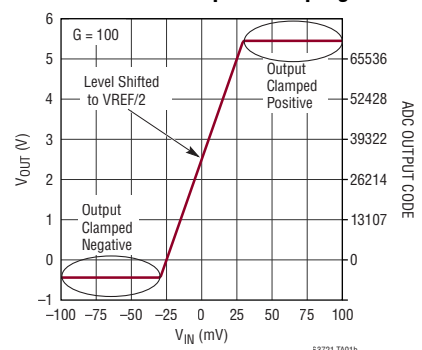
The LT6372-1 is available in a compact MS16E or a 20-pin 3mm x 4mm QFN. The LT6372-1 is fully specified over the –40°C to 85°C and –40°C to 125°C temperature ranges.

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TYPICAL APPLICATION

GAIN OF 100 BRIDGE AMPLIFIER

6372-1 TA01a
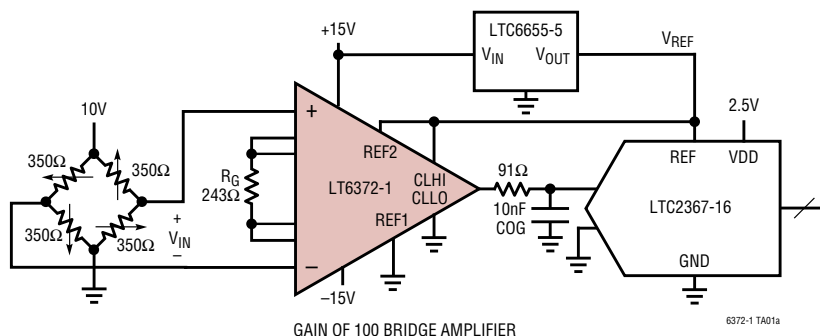
LT6372–1 Driving LTC2367–16 with Level Shift and Output Clamping

53721 TA01b

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V⁺ to V⁻) 36V
Input Voltage (+IN, −IN, +$R_{G,S}$, +$R_{G,F}$, −$R_{G,S}$, −$R_{G,F}$,
   REF1, REF2, CLHI, CLLO)... (V^- − 0.3V) to (V^+ + 0.3V)
Differential Input Voltage
   (+IN to −IN)..±36V
   (REF1 to REF2) .... ±15V
Input Current (+$R_{G,S}$, +$R_{G,F}$, −$R_{G,S}$, −$R_{G,F}$)............±2mA
Input Current (+IN, −IN, CLLO) .... ±10mA
Input Current (REF1, REF2, CLHI) ....−10mA

Output Short-Circuit Duration ....Thermally Limited
Output Current 80mA
Operating and Specified Temperature Range
   I-Grade..−40°C to 85°C
   H-Grade ....−40°C to 125°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range ....−65°C to 150°C
Lead Temperature (Soldering, 10 sec)...................300°C

PIN CONFIGURATION

TOP VIEW

```
        −R_G,F  1 ┌───────────┐ 16  +R_G,F
        −R_G,S  2 │           │ 15  +R_G,S
           NIC  3 │           │ 14  NIC
           −IN  4 │    17     │ 13  REF2
           +IN  5 │           │ 12  V⁺
           NIC  6 │           │ 11  OUTPUT
          CLLO  7 │           │ 10  REF1
            V⁻  8 └───────────┘ 9   CLHI
```

MSE PACKAGE
16-LEAD PLASTIC MSOP

$θ_{JA}$ = 35°C/W
EXPOSED PAD (PIN 17) MUST FLOAT OR
BE CONNECTED TO V⁺ IN ADDITION TO PIN 12

TOP VIEW

```
              −R_G,S −R_G,F +R_G,F +R_G,S
               20    19    18    17
        NIC  1 ┌───────────────┐ 16  NIC
        −IN  2 │               │ 15  REF2
        NIC  3 │               │ 14  V⁺
        NIC  4 │    21         │ 13  OUTPUT
        +IN  5 │    V⁻         │ 12  REF1
        NIC  6 └───────────────┘ 11  NIC
               7     8     9    10
               V⁻  CLLO  DNC  CLHI
```

UDC PACKAGE
20-LEAD (3mm x 4mm) PLASTIC QFN

$θ_{JA}$ = 52°C/W
EXPOSED PAD (PIN 21) IS CONNECTED
TO V⁻ (PIN 7) (PCB CONNECTION OPTIONAL)

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6372IMSE-1#PBF	LT6372IMSE-1#TRPBF	63721	16-Lead Plastic MSOP	−40°C to 85°C
LT6372HMSE-1#PBF	LT6372HMSE-1#TRPBF	63721	16-Lead Plastic MSOP	−40°C to 125°C
LT6372IUDC-1#PBF	LT6372IUDC-1#TRPBF	LHHV	20-Lead (3mm x 4mm) Plastic QFN	−40°C to 85°C
LT6372HUDC-1#PBF	LT6372HUDC-1#TRPBF	LHHV	20-Lead (3mm x 4mm) Plastic QFN	−40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V⁻, V_{CLHI} = V⁺, R_L = 2kΩ.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G	Gain Range	G = (1 + 24.2k/R_G) (Note 2)		1		1000	V/V
	Gain Error (Notes 3, 4)	G = 1			−0.004	0.01	%
		G = 1	●			0.015	%
		G = 10			−0.02	0.12	%
		G = 10	●			0.42	%
		G = 100			−0.02	0.12	%
		G = 100	●			0.42	%
		G = 1000			−0.05	0.12	%
		G = 1000	●			0.5	%
	Gain vs Temperature (Notes 3, 4)	G = 1 (Note 5)	●		0.2	0.5	ppm/°C
		G > 1 (Note 6)	●		20	35	ppm/°C
	Gain Nonlinearity (Notes 3, 7)	V_{OUT} = ±10V, G = 1			1	3	ppm
		V_{OUT} = ±10V, G = 10			3	40	ppm
		V_{OUT} = ±10V, G = 100			20	50	ppm
		V_{OUT} = ±10V, G = 1000			50		ppm
		V_{OUT} = ±10V, G = 1, R_L = 600Ω			4		ppm
		V_{OUT} = ±10V, G = 10, R_L = 600Ω			6		ppm
		V_{OUT} = ±10V, G = 100, R_L = 600Ω			70		ppm
		V_{OUT} = ±10V, G = 1000, R_L = 600Ω			250		ppm

V_{OST}, Total Input Referred Offset Voltage, V_{OST} = V_{OSI} + V_{OSO}/G

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSI}	Input Offset Voltage (Note 8)				±10	±60	μV
			●			±175	μV
V_{OSO}	Output Offset Voltage (Note 8)				±70	±275	μV
			●			±500	μV
V_{OSI}/T	Input Offset Voltage Drift (Notes 5, 8)		●			±0.6	μV/°C
	Input Offset Voltage Hysteresis (Note 9)	T_A = −40°C to 125°C	●		±3		μV
V_{OSO}/T	Output Offset Voltage Drift (Notes 5, 8)		●			±4	μV/°C
	Output Offset Voltage Hysteresis (Note 9)	T_A = −40°C to 125°C	●		±10		μV
I_B	Input Bias Current				±0.1	±0.8	nA
		T_A = −40°C to 85°C	●			±1.5	nA
		T_A = −40°C to 125°C	●			±3	nA
I_{OS}	Input Offset Current				±0.2	±1.4	nA
			●			±4	nA
	Input Noise Voltage (Note 10)	0.1Hz to 10Hz, G = 1			2		μV$_{P-P}$
		0.1Hz to 10Hz, G = 1000			0.2		μV$_{P-P}$

Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$ (Note 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
e_{ni}	Input Noise Voltage Density	f = 1kHz			7		nV/√Hz
e_{no}	Output Noise Voltage Density	f = 1kHz			65		nV/√Hz
	Input Noise Current	0.1Hz to 10Hz			10		pA$_{P-P}$
i_n	Input Noise Current Density	f = 1kHz			200		fA/√Hz
R_{IN}	Input Resistance	V_{IN} = −12.6V to 13V			225		GΩ
C_{IN}	Differential	f = 100kHz			0.9		pF
	Common Mode	f = 100kHz			15.9		pF
V_{CM}	Input Voltage Range	Guaranteed by CMRR		V⁻ + 1.8/V⁺ − 1.4			V
			●	V⁻ + 2.4		V⁺ − 2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 2kΩ.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	DC to 60Hz, 1k Source Imbalance, V_{CM} = −12.6V to 13V					
		G = 1		86	100		dB
		G = 1	●	80			dB
		G = 10		106	120		dB
		G = 10	●	100			dB
		G = 100		120	140		dB
		G = 100	●	115			dB
		G = 1000		128	150		dB
		G = 1000	●	120			dB
	AC Common Mode Rejection Ratio	f = 20kHz, QFN20 Package					
		G = 1			74		dB
		G = 10			98		dB
		G = 100			102		dB
		G = 1000			105		dB
		f = 20kHz, MS16E Package					
		G = 1			69		dB
		G = 10			92		dB
		G = 100			110		dB
		G = 1000			110		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±17.5V					
		G = 1		116	130		dB
		G = 1	●	110			dB
		G = 10		128	140		dB
		G = 10	●	120			dB
		G = 100		122	140		dB
		G = 100	●	118			dB
		G = 1000		122	140		dB
		G = 1000	●	118			dB
V_S	Supply Voltage	Guaranteed by PSRR	●	4.75		35	V
I_S	Supply Current	V_S = ±15V			2.75	2.85	mA
		T_A = −40°C to 85°C	●			3	mA
		T_A = −40°C to 125°C	●			3.1	mA
		V_S = ±2.375V			2.65	2.7	mA
		T_A = −40°C to 85°C	●			2.85	mA
		T_A = −40°C to 125°C	●			2.95	mA
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 10kΩ		−14.5	−14.9/14	13.7	V
			●	−14.3		13.6	V
		V_S = ±2.375V, R_L = 10kΩ		−2	−2.3/1.6	1.5	V
			●	−1.8		1.3	V
I_{OUT}	Output Short Circuit Current			35	55		mA
			●	30			mA
BW	−3dB Bandwidth	G = 1			3.1		MHz
		G = 10			1.15		MHz
		G = 100			184		kHz
		G = 1000			19		kHz
SR	Slew Rate	G = 1, V_{OUT} = ±10V			11		V/µs
t_S	Settling Time	20V Output Step to 0.0015%					
		G = 1			5.8		µs
		G = 10			9.8		µs
		G = 100			16		µs
		G = 1000			100		µs

Rev. 0

4

ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V^-, V_{CLHI} = V^+, R_L = 2kΩ.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{REFIN}	REF Input Resistance	REF1 or REF2, Untested REF pin floating			30		kΩ
I_{REFIN}	REF Input Current	V_{+IN} = V_{-IN} = V_{REF1} = V_{REF2}= 0V, REF1 or REF2		−20	−14	−7	µA
			●	−30		3	µA
V_{REF}	REF Voltage Range	REF1 or REF2	●	V^-		V^+	V
A_{VREF}	REF Gain to Output	V_{REF1} = 0V to 5V, V_{REF2} = 0V			0.5		V/V
	REF Gain Error	V_{REF1} = 0V to 5V, V_{REF2} = 0V		−175	±50	175	ppm
			●	−200		200	ppm
	CLLO Input Current	V_{CLLO} = 0V	●			1	µA
	CLHI Input Current	V_{CLHI} = 5V	●			1	µA
	CLLO Input Operating Voltage Range	Outside this range CLLO is disabled	●	V^- + 3		V^+ − 2	V
	CLHI Input Operating Voltage Range	Outside this range CLHI is disabled	●	V^- + 2		V^+ − 2.5	V
	CLLO Clamp Voltage (V_{OUT} − V_{CLLO})			−0.57	−0.45		V
			●	−0.74			V
	CLHI Clamp Voltage (V_{OUT} − V_{CLHI})				0.45	0.55	V
			●			0.755	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Gains higher than 1000 are possible but the resulting low R_G values can make PCB and package lead resistance a significant error source.

Note 3: Gain tests are performed with −IN at mid-supply and +IN driven.

Note 4: When the gain is greater than 1 the gain error and gain drift specifications do not include the effect of external gain set resistor R_G.

Note 5: This specification is guaranteed by design.

Note 6: This specification is guaranteed with high-speed automated testing.

Note 7: This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects are dependent on the package used, PCB layout, heat sinking and air flow conditions.

Note 8: For more information on how offsets relate to the amplifiers, see section "Input and Output Offset Voltage" in the Applications section.

Note 9: Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature), hysteresis is usually not a significant error source. Typical hysteresis is the worst case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

Note 10: Referred to the input.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V⁻, V_{CLHI} = V⁺, R_L = 2k, unless otherwise noted.
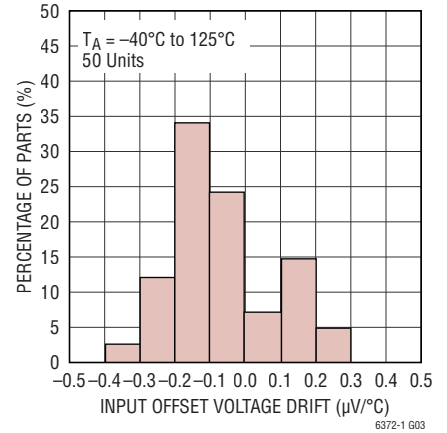
Distribution of Input Offset Voltage, MS16E Package
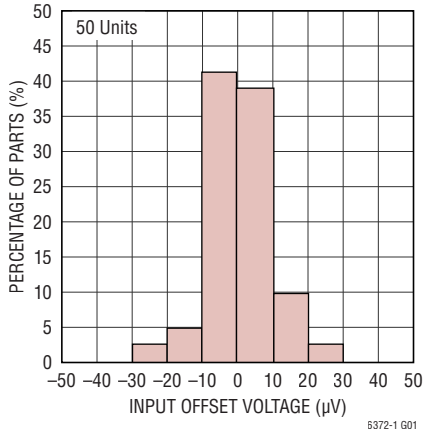
6372-1 G01

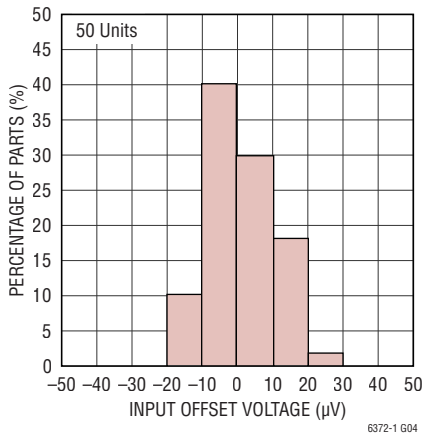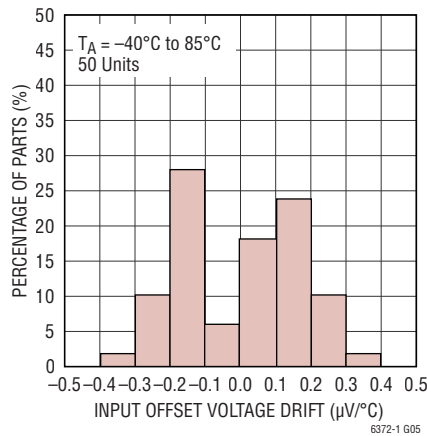**Distribution of Input Offset Voltage Drift, MS16E Package**

6372-1 G02

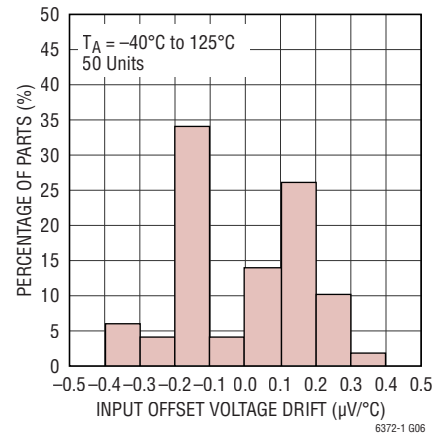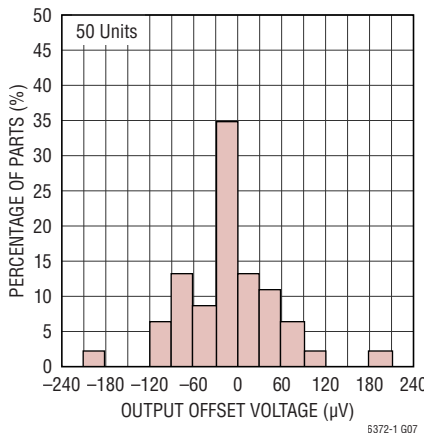**Distribution of Input Offset Voltage Drift, MS16E Package**

6372-1 G03

Distribution of Input Offset Voltage, QFN Package

6372-1 G04

Distribution of Input Offset Voltage Drift, QFN Package

6372-1 G05

Distribution of Input Offset Voltage Drift, QFN Package

6372-1 G06

Distribution of Output Offset Voltage, MS16E Package

6372-1 G07

Distribution of Output Offset Voltage Drift, MS16E Package

6372-1 G08
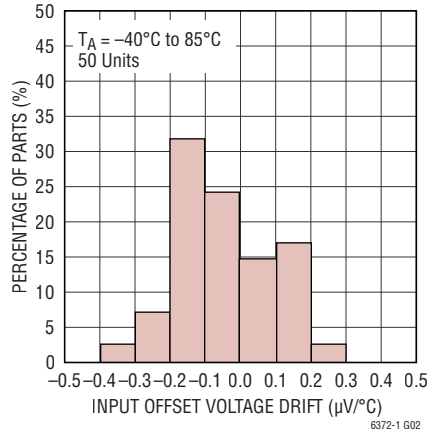
Distribution Output Offset Voltage Drift, MS16E Package
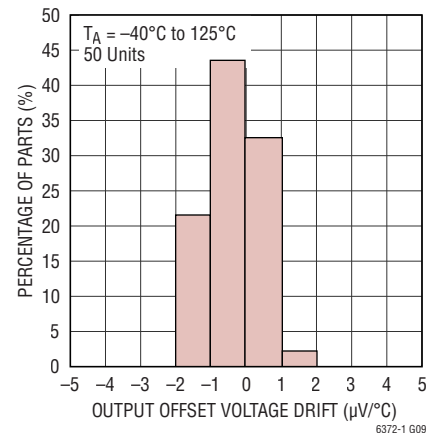
6372-1 G09

Rev. 0

6

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$, $V_{CM} = V_{REF1} = V_{REF2} = 0V$, $V_{CLLO} = V^-$, $V_{CLHI} = V^+$, $R_L = 2k$, unless otherwise noted.

Distribution of Output Offset Voltage, QFN Package
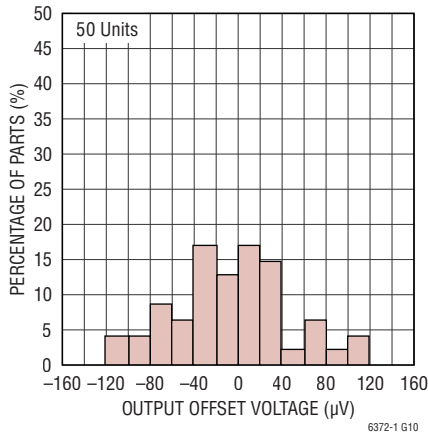
50 Units

PERCENTAGE OF PARTS (%) vs OUTPUT OFFSET VOLTAGE (µV)

6372-1 G10

Distribution of Output Offset Voltage Drift, QFN Package

$T_A = -40°C$ to $85°C$
50 Units

PERCENTAGE OF PARTS (%) vs OUTPUT OFFSET VOLTAGE DRIFT (µV/°C)

6372-1 G11

Distribution of Output Offset Voltage Drift, QFN Package

$T_A = -40°C$ to $125°C$
50 Units

PERCENTAGE OF PARTS (%) vs OUTPUT OFFSET VOLTAGE DRIFT (µV/°C)

6372-1 G12

Distribution of Gain Error

G = 1
$T_A = 25°C$
730 Units

PERCENTAGE OF PARTS (%) vs GAIN ERROR (ppm)

6372-1 G13

Distribution of Gain Error

G = 1000
$T_A = 25°C$
730 Units

PERCENTAGE OF PARTS (%) vs GAIN ERROR (ppm)

6372-1 G14
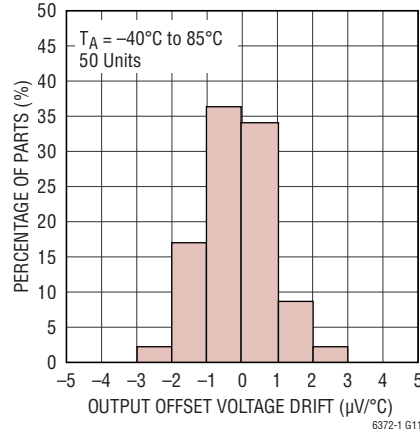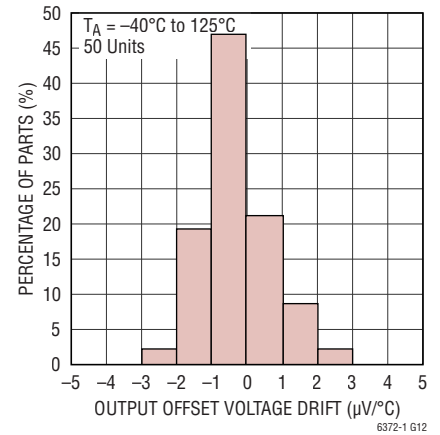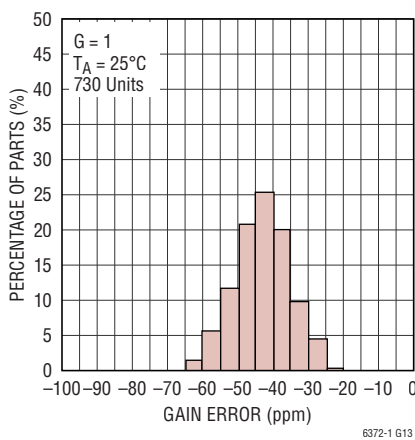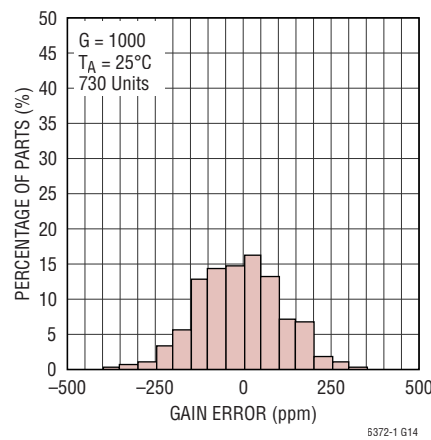
Distribution of REF Divider Gain Error

REF2 = 0V
REF1 = 0V to 5V
$T_A = 25°C$
730 Units

PERCENTAGE OF PARTS (%) vs GAIN ERROR (ppm)

6372-1 G15
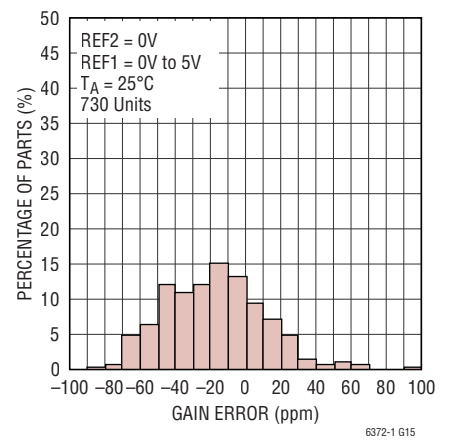
REF Divider Gain Drift

REF1 = 0V
REF2 = ±10V
10 Units
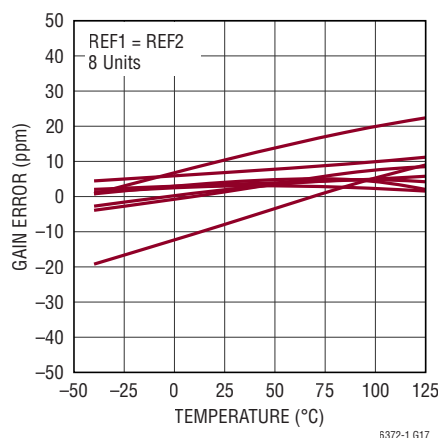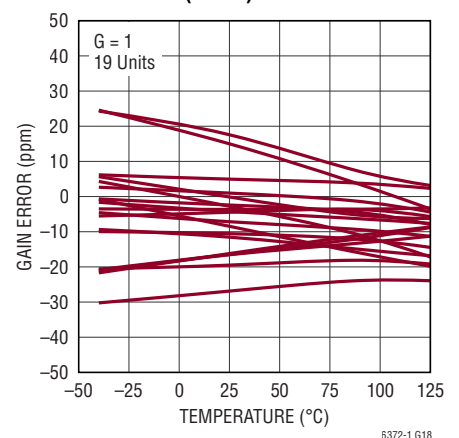
GAIN ERROR (ppm) vs TEMPERATURE (°C)

6372-1 G16

REF Gain Drift

REF1 = REF2
8 Units

GAIN ERROR (ppm) vs TEMPERATURE (°C)

6372-1 G17

Gain Drift (G = 1)

G = 1
19 Units

GAIN ERROR (ppm) vs TEMPERATURE (°C)

6372-1 G18

Rev. 0

7

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$, $V_{CM} = V_{REF1} = V_{REF2} = 0V$, $V_{CLLO} = V^-$, $V_{CLHI} = V^+$, $R_L = 2k$, unless otherwise noted.

Gain Drift (G = 1000)

6372-1 G19

Lead Free Reflow Profile Due to IR Reflow

6372-1 G20

Gain Nonlinearity (G = 1)

6372-1 G21

Gain Nonlinearity (G = 10)

6372-1 G22

Gain Nonlinearity (G = 100)

6372-1 G23

Gain Nonlinearity (G = 1000)

6372-1 G24

CMRR vs Frequency, RTI QFN Package

6372-1 G25

CMRR vs Frequency, RTI MS16E Package

6372-1 G26

Positive Power Supply Rejection Ratio vs Frequency, RTI

6372-1 G27

Rev. 0

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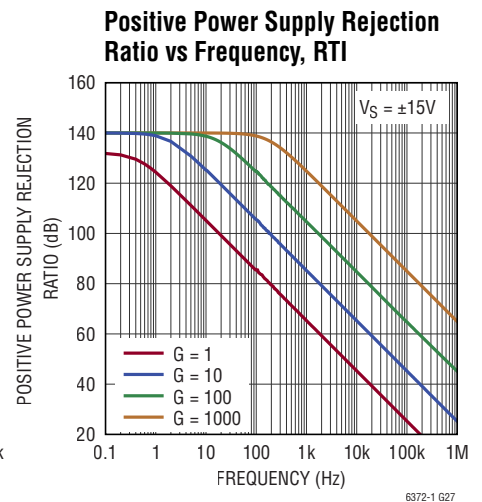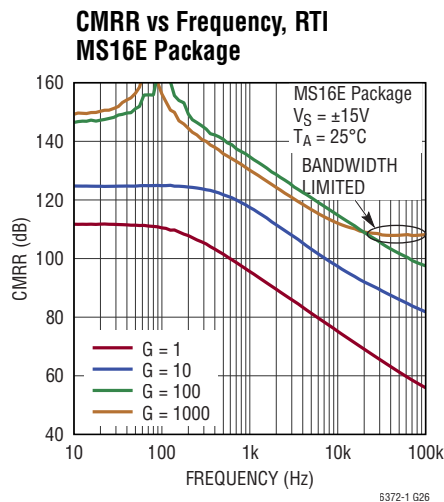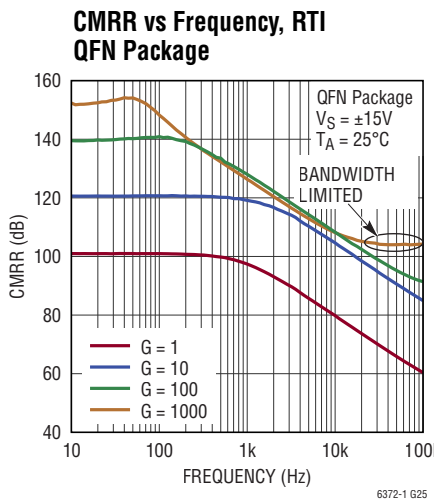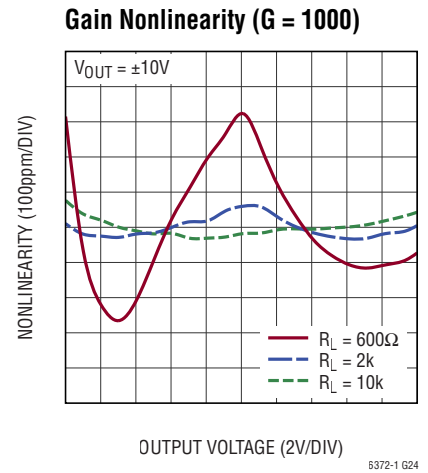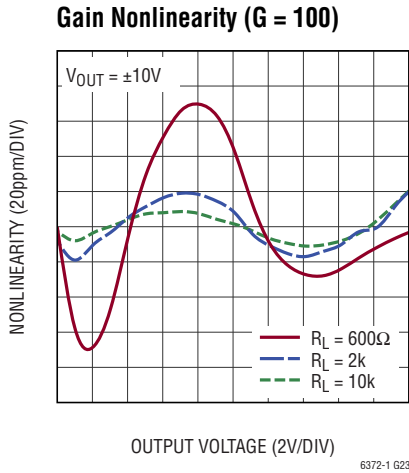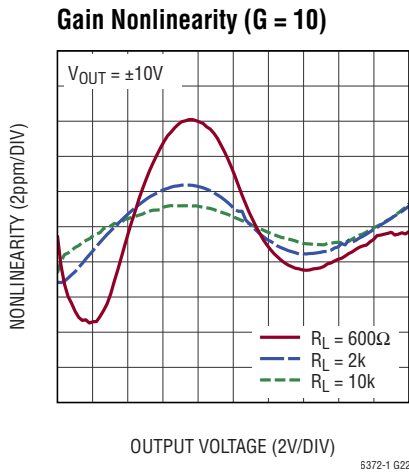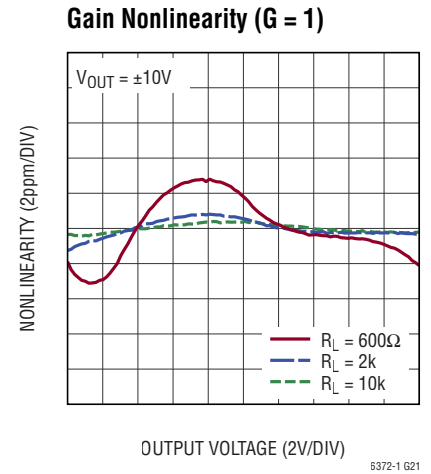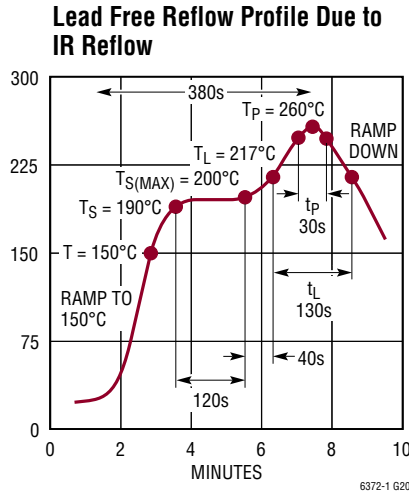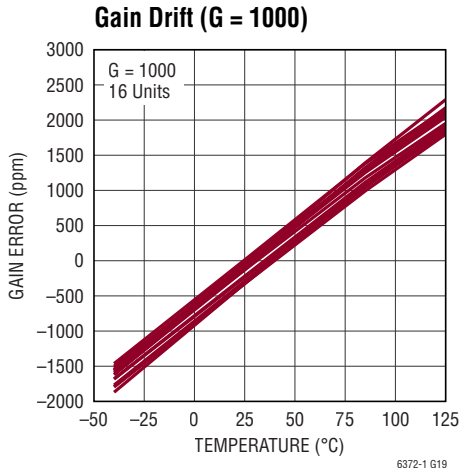
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$, $V_{CM} = V_{REF1} = V_{REF2} = 0V$, $V_{CLLO} = V^−$, $V_{CLHI} = V^+$, $R_L = 2k$, unless otherwise noted.
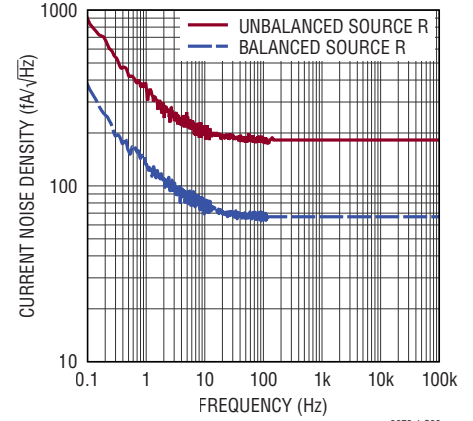
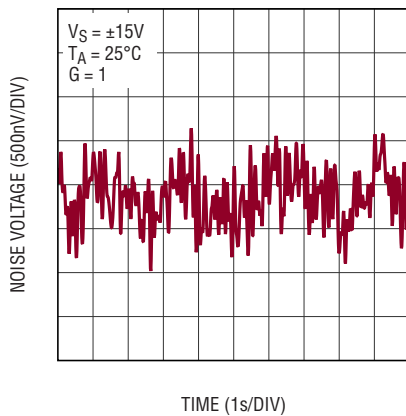**Negative Power Supply Rejection Ratio vs Frequency**
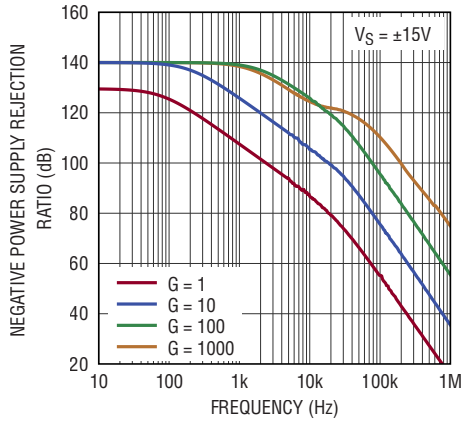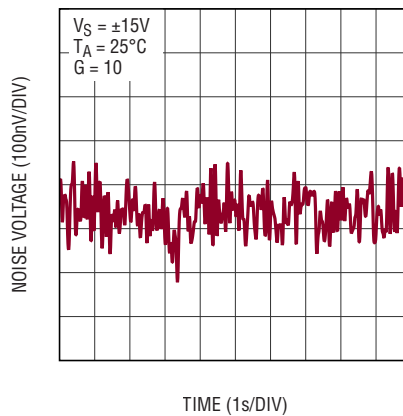
Input-Referred Voltage Noise Density vs Frequency
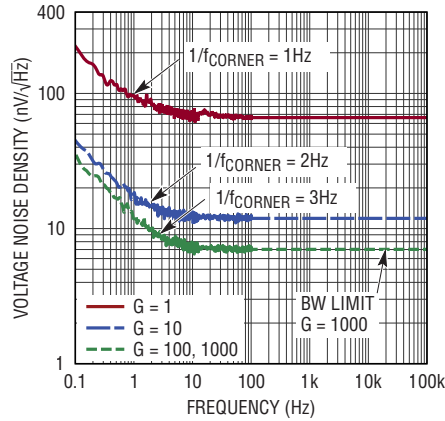
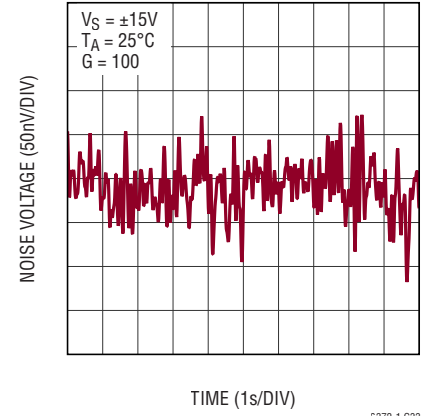**Current Noise Density vs Frequency**

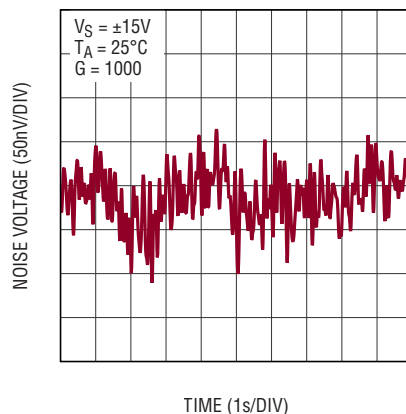**0.1Hz to 10Hz Voltage Noise, G = 1, RTI**
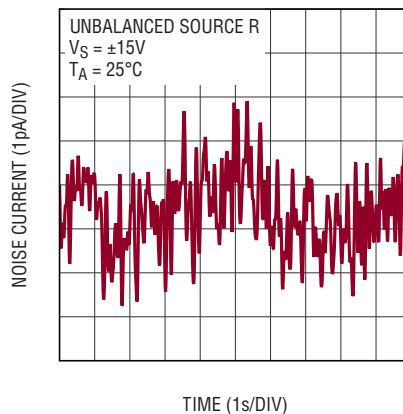
0.1Hz to 10Hz Voltage Noise, G = 10, RTI

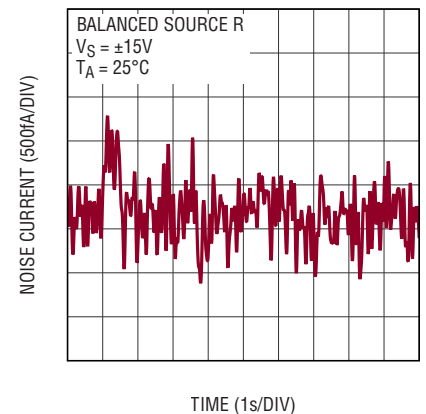**0.1Hz to 10Hz Voltage Noise, G = 100, RTI**

0.1Hz to 10Hz Voltage Noise, G = 1000, RTI

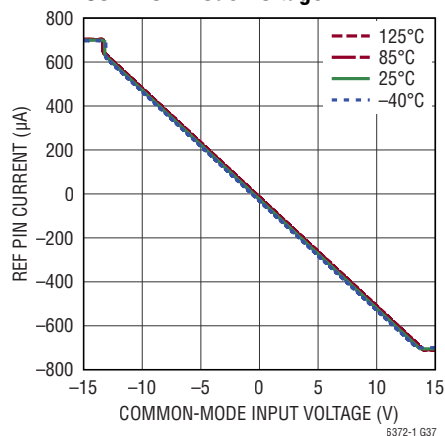**0.1Hz to 10Hz Noise Current, Unbalanced Source R**

0.1Hz to 10Hz Noise Current, Balanced Source R

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = V_{REF1} = V_{REF2} = 0V, V_{CLLO} = V⁻, V_{CLHI} = V⁺, R_L = 2k, unless otherwise noted.

REF Pin Current vs Input Common Mode Voltage

6372-1 G37

Input Bias Current vs Common Mode Voltage

6372-1 G38

Input Bias and Offset Current vs Temperature

6372-1 G39
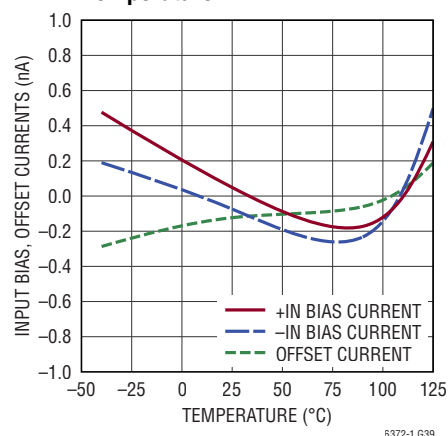
Supply Current vs Supply Voltage
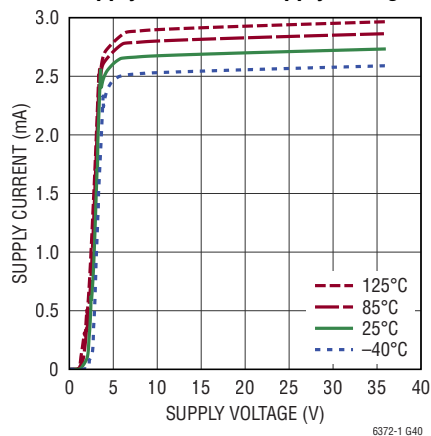
6372-1 G40

Output Voltage Swing vs Load Resistance

6372-1 G41

Output Voltage Swing vs Load Resistance

6372-1 G42
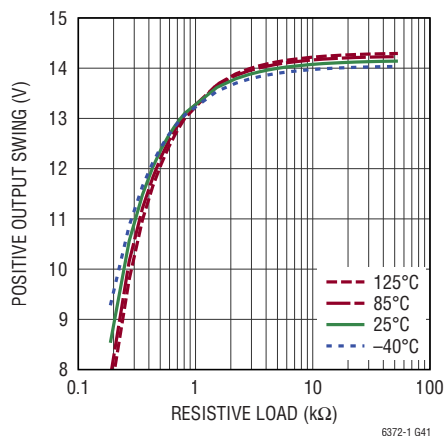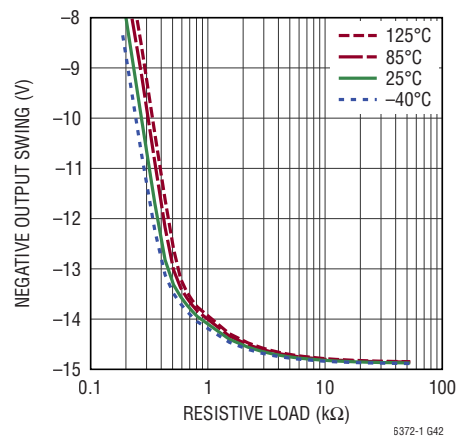
Output Short Circuit Current vs Temperature

6372-1 G43
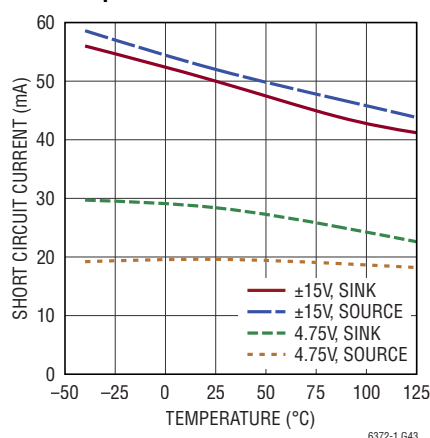
Undistorted Output Swing vs Frequency

G = 1
V_S = ±15V
T_A = 25°C
THD < −40dB

6372-1 G44
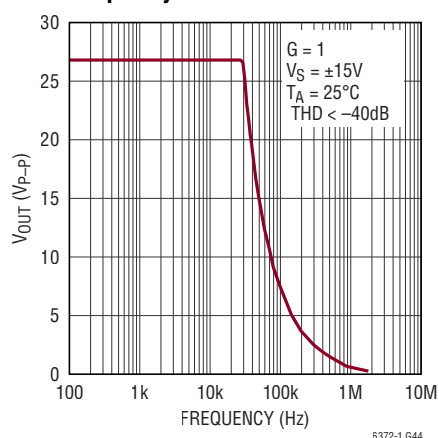
Slew Rate vs Temperature
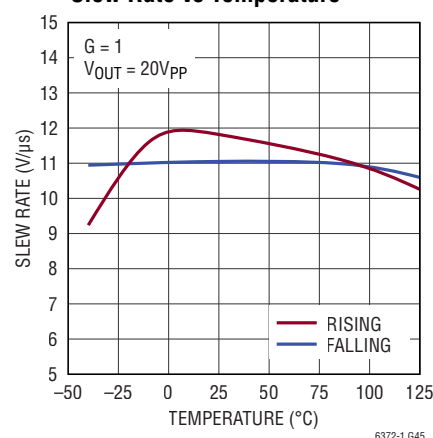
G = 1
V_{OUT} = 20V_{PP}

6372-1 G45

Rev. 0

10
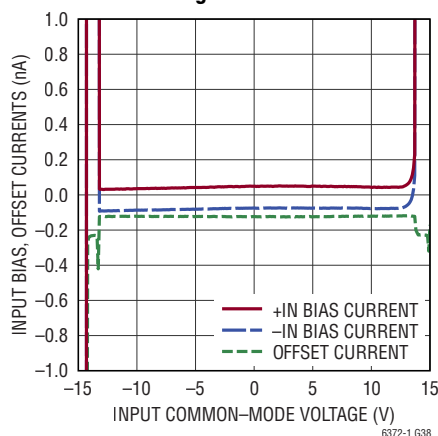
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$, $V_{CM} = V_{REF1} = V_{REF2} = 0V$, $V_{CLLO} = V^-$, $V_{CLHI} = V^+$, $R_L = 2k$, unless otherwise noted.

Large Signal Transient Response

V_OUT
2V/DIV

2µs/DIV

6372-1 G46

G = 1
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

Large Signal Transient Response

V_OUT
2V/DIV

4µs/DIV

6372-1 G47

G = 10
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

Large Signal Transient Response

V_OUT
2V/DIV

10µs/DIV

6372-1 G48

G = 100
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

Large Signal Transient Response

V_OUT
2V/DIV

100µs/DIV

6372-1 G49

G = 1000
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

Small Signal Transient Response

V_OUT
5mV/DIV

1µs/DIV

6372-1 G50

G = 1
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

Small Signal Transient Response

V_OUT
5mV/DIV

1µs/DIV

6372-1 G51

G = 10
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

Small Signal Transient Response

V_OUT
5mV/DIV

10µs/DIV

6372-1 G52

G = 100
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

Small Signal Transient Response

V_OUT
5mV/DIV

100µs/DIV

6372-1 G53

G = 1000
$V_S = ±15V$
$T_A = 25°C$
$C_L = 100pF$

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_S = ±15V$, $V_{CM} = V_{REF1} = V_{REF2} = 0V$, $V_{CLLO} = V^-$, $V_{CLHI} = V^+$, $R_L = 2k$, unless otherwise noted.

Gain vs Frequency

$V_S = ±15V$
$T_A = 25°C$

G = 1
G = 10
G = 100
G = 1000

6372-1 G54

Clamp Transient Response (Clamped Output)

V_{OUT} 2V/DIV 0V

V_{IN} 200mV/DIV 0V

$V_S = ± 15V$
$G = 20$

6372-1 G55

VCHI = 4.1V
VCLO = 0V
$V_{REF1} = 0V$
$V_{REF2} = 4.1V$

5µs/DIV

LT6372–1 Supply Current While Clamping

V_{OUT}
I^+
I^-

$V_S = ±15V$
$V_{REF2} = V_{CLHI} = 4.1V$
$V_{REF1} = V_{CLLO} = 0V$
$R_L = 10kΩ$
$G = 20$

6372-1 G56

Clamp Voltage vs Temperature

$V_S = ±15V$
$V_{CLHI} = V_{CLLO} = 0V$

CLAMPED HIGH

CLAMPED LOW

6372-1 G57

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PIN FUNCTIONS (MS16E/QFN20)

–R$_{G,F}$ (Pin 1/Pin 19): For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from –R$_{G,S}$ in order to minimize gain errors.

–R$_{G,S}$ (Pin 2/Pin 20): For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from –R$_{G,F}$ in order to minimize gain errors.

–IN (Pin 4/Pin 2): Negative Input Terminal. This input is high impedance.

+IN (Pin 5/Pin 5): Positive Input Terminal. This input is high impedance.

CLLO (Pin 7/Pin 8): Low Side Clamp Input. The voltage applied to the CLLO pin defines the lower voltage limit of the output. Typically, the output clamps 500mV below the voltage applied to the CLLO pin. Do not float CCLO.

V⁻ (Pin 8/Pin 7): Negative Power Supply. A bypass capacitor should be used between supply pins and ground.

CLHI (Pin 9/Pin 10): High Side Clamp Input. The voltage applied to the CLHI pin defines the upper voltage limit of the output. Typically, the output clamps 500mV above the voltage applied to the CLHI pin. Do not float CLHI.

REF1 (Pin 10/Pin 12): Reference for the output voltage. REF1 can be tied to REF2 and used as a reference for the output. REF1 can also be used with REF2 to form a voltage divider and level shift the output.

OUTPUT (Pin 11/Pin 13): Output voltage referenced to the REF pins.

V⁺ (Pin 12/Pin 14): Positive Power Supply. A bypass capacitor should be used between supply pins and ground.

REF2 (Pin 13/Pin 15): Reference for the output voltage. REF2 can be tied to REF1 and used as a reference for the output. REF2 can also be used with REF1 to form a voltage divider and level shift the output.

+R$_{G,S}$ (Pin 15/Pin 17): For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from +R$_{G,F}$ in order to minimize gain errors.

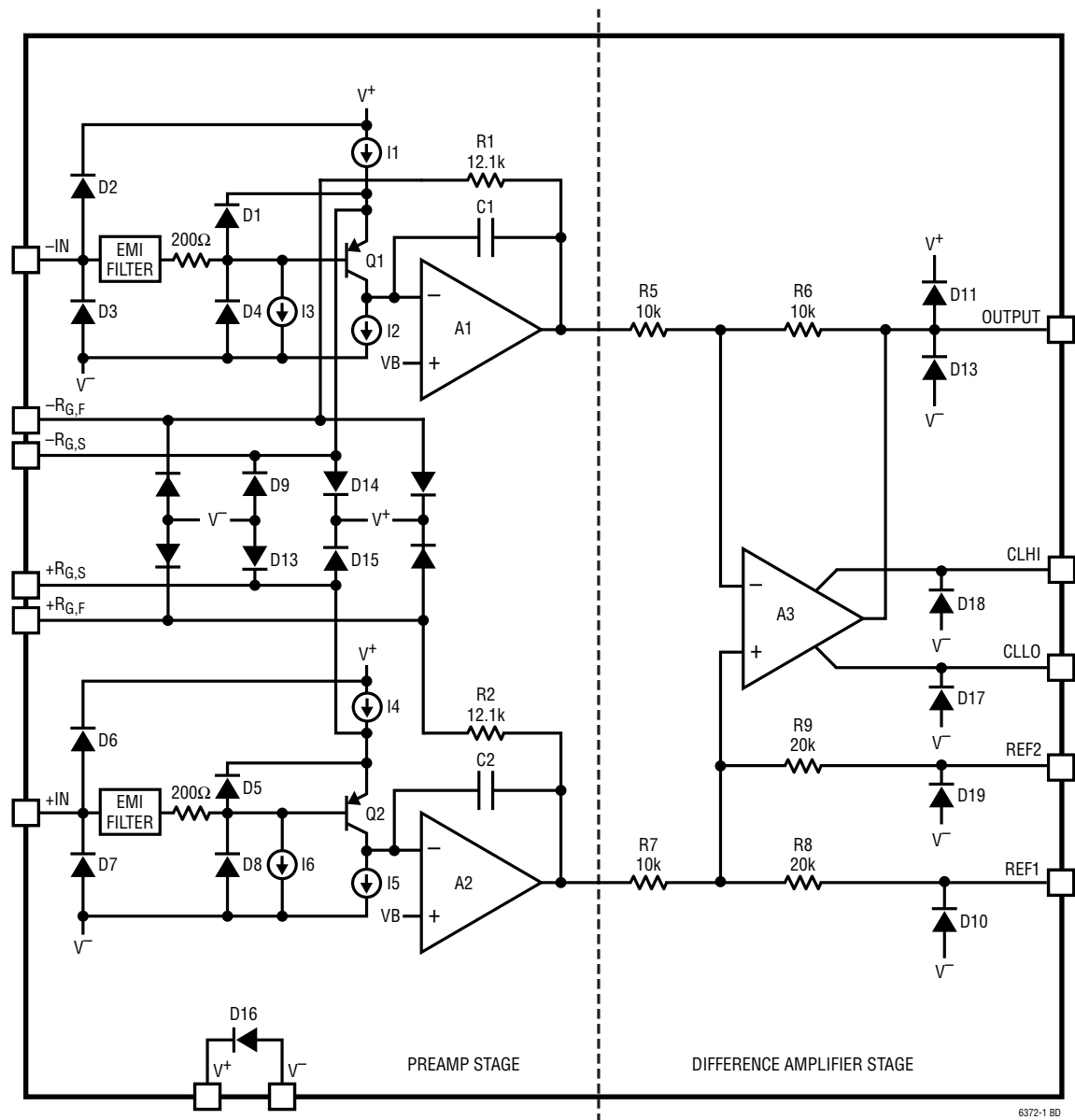**+R$_{G,F}$ (Pin 16/Pin 18):** For use with an external gain setting resistor. This connection should be routed to the gain setting resistor separately from +R$_{G,S}$ in order to minimize gain errors.

NIC (Pins 3, 6, 14/Pins 1, 3, 4, 6, 11, 16): No Internal Connection.

DNC (QFN Pin 9): Do Not Connect. This pin should float.

SIMPLIFIED BLOCK DIAGRAM

PREAMP STAGE   DIFFERENCE AMPLIFIER STAGE

6372-1 BD

THEORY OF OPERATION

The LT6372-1 is an improved version of the classic three op amp instrumentation amplifier topology that incorporates features to improve accuracy and simplify interfacing to ADCs. Laser trimming and proprietary monolithic construction allow for tight matching and extremely low drift of circuit parameters over the specified temperature range. Refer to the Simplified Block Diagram to aid in understanding the following circuit description. The collector currents in Q1 and Q2 as well as I1 and I4 are trimmed to minimize input offset voltage drift, thus assuring a high level of performance. R1 and R2 are trimmed to an absolute value of 12.1k to assure that the gain can be set accurately (0.12% at G = 100) with only one external resistor, R_G. The value of R_G determines the transconductance of the preamp stage. As R_G is reduced to increase the programmed gain, the transconductance of the input preamp stage also increases to that of the input transistors Q1 and Q2. This causes the open-loop gain to increase when the programmed gain is increased, reducing the input related errors and noise. The input voltage noise at high gains is determined only by Q1 and Q2. At lower gains the noise of the difference amplifier and preamp gain setting resistors may increase the noise. The gain bandwidth product is determined by C1, C2 and the preamp transconductance, which increases with programmed gain. Therefore, the bandwidth is self-adjusting and does not drop directly proportional to gain.

The input transistors Q1 and Q2 offer excellent matching, drift and noise performance, which is due to using a proprietary high performance process, as well as low input bias current due to the high beta of these input devices. The input bias current is further reduced by trimming I3 and I6. The collector currents in Q1 and Q2 are held constant due to the feedback through the Q1-A1-R1 loop and Q2-A2-R2 loop. The action of the amplifier loops impresses the differential input voltage across the external gain set resistor R_G. Since the current that flows through R_G also flows through R1 and R2, the ratios provide a gained-up differential voltage,

$$G = 1 + \frac{R1 + R2}{R_G}$$

to the difference amplifier A3. The difference amplifier removes the common mode voltage and provides a single-ended output voltage referenced to the average of the voltages on REF1 and REF2. This split reference resistor configuration allows the output voltage to be easily level shifted to the center of an ADCs input range without external components. The offset voltage of the difference amplifier is trimmed to minimize output offset voltage drift, thus assuring a high level of performance, even in low gains. Resistors R5 to R9 are trimmed to maximize CMRR and minimize gain error. The resulting gain equation is:

$$G = 1 + \frac{24.2k}{R_G}$$

Solving for the gain set resistor gives:

$$R_G = \frac{24.2k}{G - 1}$$

Table 1 shows appropriate 1% resistor values for a variety of gains.

Table 1. LT6372-1 Gain and R_G Lookup.

Resulting Gains for Various 1% Standard Resistor Values	
Gain	**Standard 1% Resistor Value (Ω)**
1	–
1.996	24.3k
5.007	6.04k
10.06	2.67k
20.06	1.27k
50.69	487
100.6	243
201	121
497.9	48.7
996.9	24.3
Convenient Integer Gains Using Various Standard 1% Resistor Values	
Integer Gain	**Standard 1% Resistor Value (Ω)**
1	–
3	12.1k
21	1.21k
23	1.1k
122	200
201	121
221	110
243	100
1211 (Note 2)	20

Additionally, The LT6372-1 has two integrated output voltage clamps which can be used to limit the voltage

APPLICATIONS INFORMATION

applied to an ADCs input. Typically, CLHI is tied to the ADC's reference and CLLO is tied to the ADC's ground connection.

Valid Input and Output Range

Instrumentation amplifiers traditionally specify a valid input common mode range and an output swing range.

This however often fails to identify limitations associated with internal swing limits. Referring to the Simplified Block Diagram, the output swing of pre-amplifiers A1 and A2 as well as the common-mode input range of the difference amplifier A3 impose limitations on the valid operating range. Figure 1 shows the operating region where a valid output is produced for various configurations. Further valid input and output range plots can be generated using the Diamond Plot Tool.
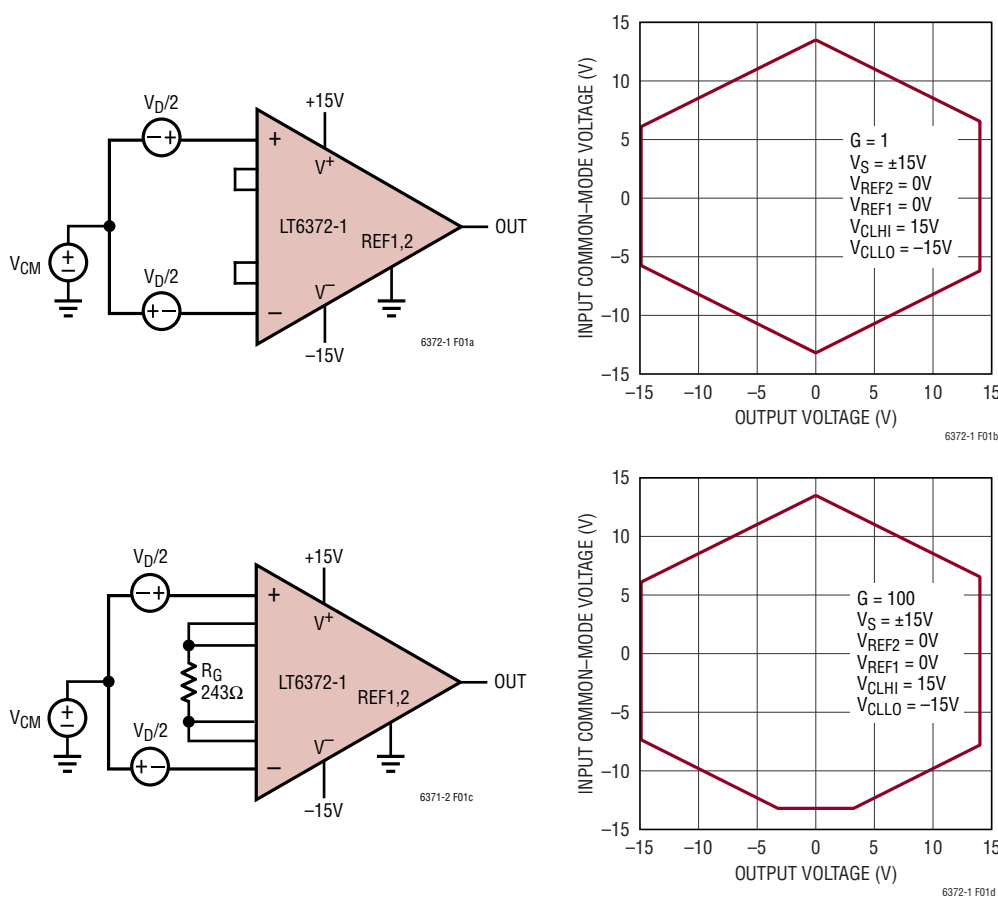
Figure 1. Input Common Mode Range vs Output Voltage
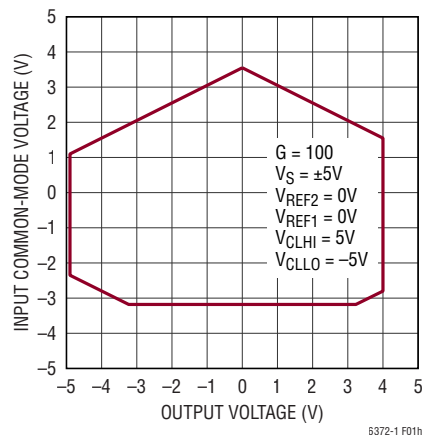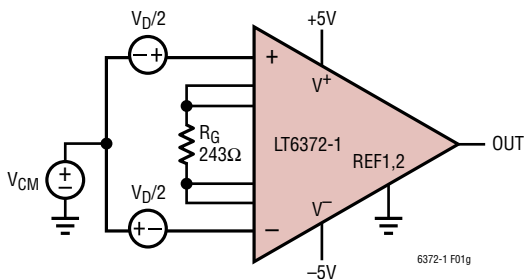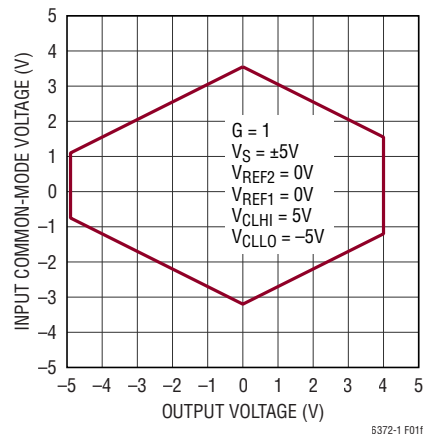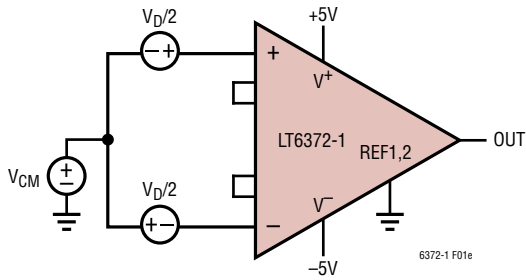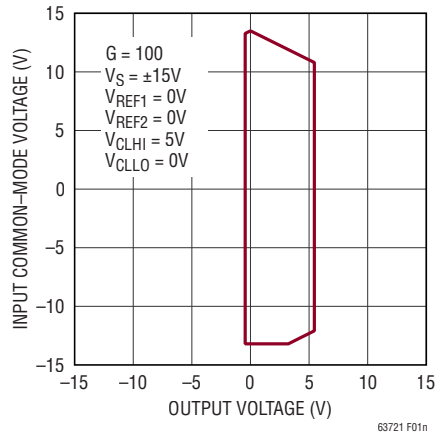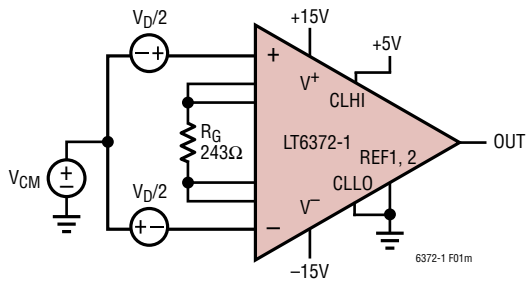
APPLICATIONS INFORMATION

Figure 1 (Continued). Input Common Mode Range vs Output Voltage
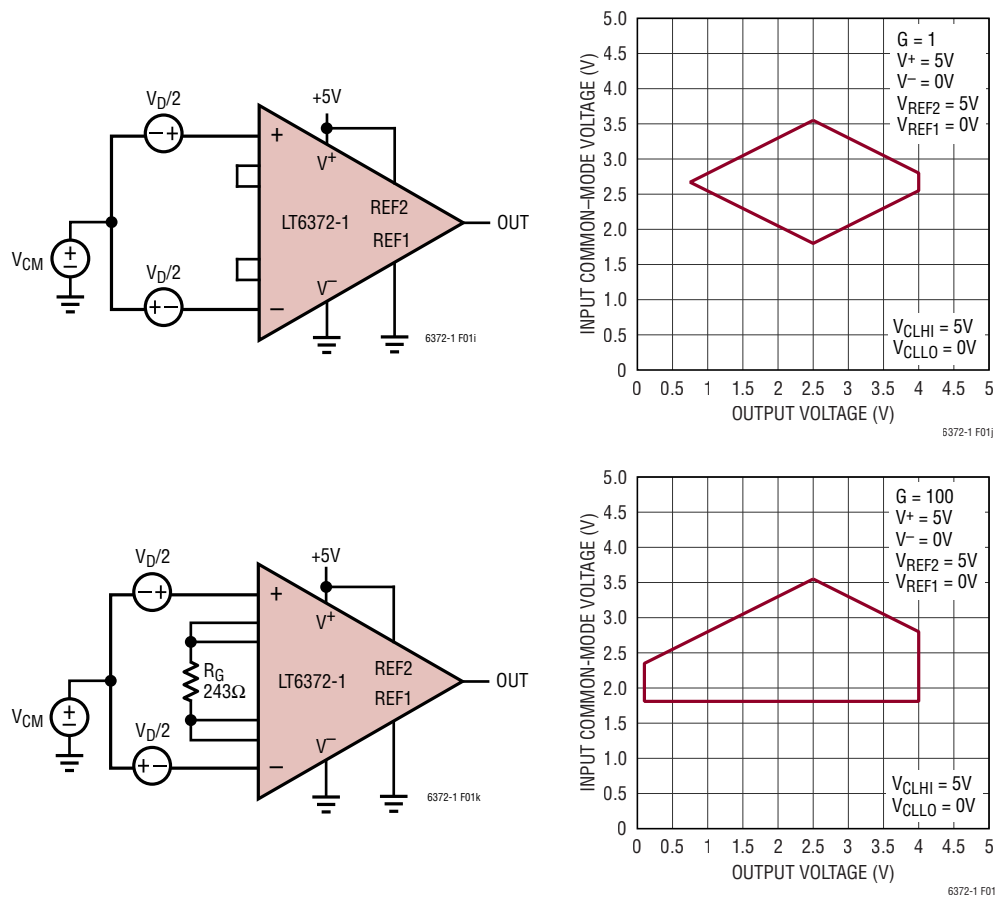
APPLICATIONS INFORMATION

Figure 1 (Continued). Input Common Mode Range vs Output Voltage

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APPLICATIONS INFORMATION

Split Reference Pins

Output Level Shifting with the LT6372-1's difference amplifier features split reference pins, REF1 and REF2, which allow the output to be easily and accurately level shifted without the use of external circuitry. REF1 and REF2 are typically tied to an ADC ground and reference respectively. In this configuration the amplifier's output is conveniently level shifted to the center of the ADC input range.

If REF1 and REF2 are shorted to each other, they can function as the reference for the output voltage like a traditional instrumentation amplifier.

Parasitic resistance in series with REF1 and REF2 should be minimized to preserve CMRR and gain performance. It is also important to note that the drift in any circuitry used to drive REF1 or REF2 can results in an additional output drift term. Therefore, it may be important to consider the temperature accuracy of the circuitry used to drive the REF pin.

Gain Setting Resistor Connections

Each pre-amplifier gives a set of RG connection terminals which should be routed separately to the gain setting resistor. Doing this minimizes the impact which parasitic trace and lead resistance has on gain accuracy. When routing to the gain setting resistors, large loops should be avoided as they can couple noise into the amplifier.

Output Clamps

The CLHI and CLLO clamp pins limit the output voltage swing of the LT6372-1. CLHI and CLLO are typically tied to the ADC supply/reference and ADC ground respectively. In this case the ADC input is protected from being overdriven by the LT6372-1 which is likely running off a higher supply voltage.

When the CLLO is tied to 0V, attempts to drive the output below 0V will be clamped at −0.45 typically. When CLHI is tied to 5V, attempts to drive the output above 5V will be clamped at 5.45V typically.

CLHI and CLLO are high impedance inputs and do not conduct significant current during clamping. Rather, internal amplifier nodes are controlled by CLHI and CLLO to limit the output voltage.

In applications where clamping is not desired, CLLO should be tied to V⁻ and CLHI to V⁺ to disable clamping.

Input and Output Offset Voltage

The offset voltage of the LT6372-1 has two main components: the input offset voltage due to the input amplifiers and the output offset due to the output amplifier. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain and adding it to the input offset voltage. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

Total input offset voltage (RTI) = $V_{OSI} + V_{OSO}/G$

Total output offset voltage (RTO) = $V_{OSI} \bullet G + V_{OSO}$

The preceding equations can also be used to calculate offset drift in a similar manner.

Output Offset Trimming

The LT6372-1 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset voltage needs to be adjusted, the circuit in Figure 2 is an example of an optional offset adjustment circuit. The op amp buffer provides a low impedance signal to the REF pin in order to achieve the best CMRR and lowest gain error.
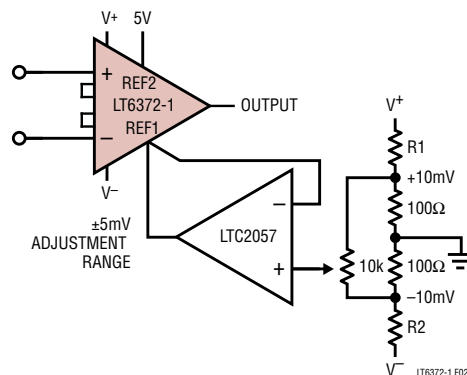
Figure 2. Optional Trimming of Output Offset Voltage

Thermocouple Effects

In order to achieve accuracy on the microvolt level, thermocouple effects must be considered. Any connection of dissimilar metals forms a thermoelectric junction and

Rev. 0

APPLICATIONS INFORMATION

generates a small temperature-dependent voltage. Also known as the Seebeck Effect, these thermal EMFs can be the dominant error source in low-drift circuits.

Connectors, switches, relay contacts, sockets, resistors, and solder are all candidates for significant thermal EMF generation. Even junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C, which is comparable to the maximum input offset voltage drift specification of the LT6372-1. Figure 3 and Figure 4 illustrate the potential magnitude of these voltages and their sensitivity to temperature.

In order to minimize thermocouple-induced errors, attention must be given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input and R_G signal paths and avoid connectors, sockets, switches, and relays whenever possible. If such components are required, they should be selected for low thermal EMF characteristics. Furthermore, the number, type, and layout of junctions should be matched for both inputs with respect to thermal gradients on the circuit board. Doing so may involve deliberately introducing dummy junctions to offset unavoidable junctions.

Air currents can also lead to thermal gradients and cause significant noise in measurement systems. It is important to prevent airflow across sensitive circuits. Doing so will often reduce thermocouple noise substantially. Placing PCB input traces close together, and on an internal PCB layer, can help minimize temperature differentials resulting from air currents reacting with the input trace thermal surface area.
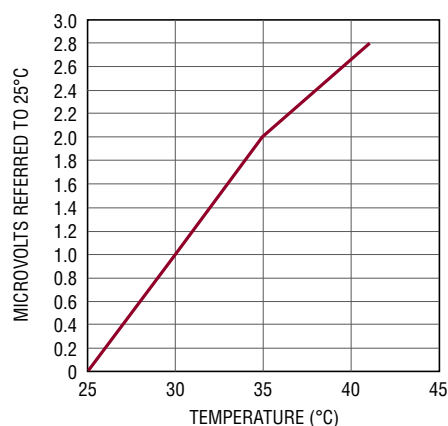
Figure 3. Thermal EMF Generated by Two Copper Wires From Different Manufacturers
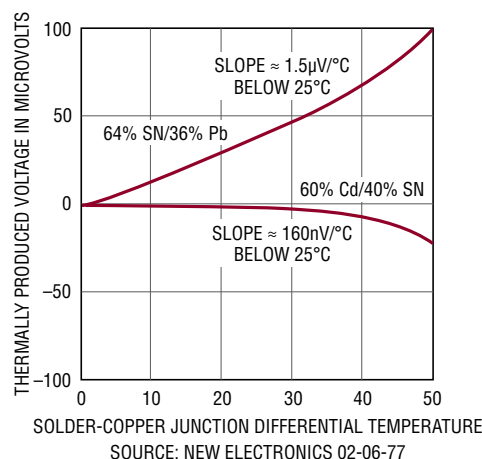
Figure 4. Solder-Copper Thermal EMFs

Reducing Board-Related Leakage Effects

Leakage currents can have a significant impact on system accuracy, particularly in high temperature and high voltage applications. Quality insulation materials should be used, and insulating surfaces should be cleaned to remove fluxes and other residues. For humid environments, surface coating may be necessary to provide a moisture barrier.

Leakage into the R_G pin conducts through the on-chip feedback resistor, creating an error at the output of the pre-amplifiers. This error is independent of gain and degrades accuracy the most at low gains. This leakage can be minimized by encircling the R_G connections with a guard-ring operated at a potential very close to that of the R_G pins. NIC pins adjacent to each R_G pin can be used to simplify the implementation of this guard-ring. These NIC pins do not provide any bias and have no internal connections. In some cases, the guard-ring can be connected to the input voltage which biases one diode drop below R_G.

Figure 5. Guard-Rings Can Be Used to Minimize Leakage into the R_G Pins

Leakage into the input pins reacts with the source resistance, creating an error directly at the input. This leakage can be minimized by encircling the input connections with a guard-rin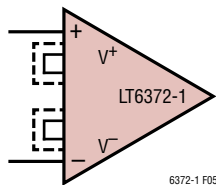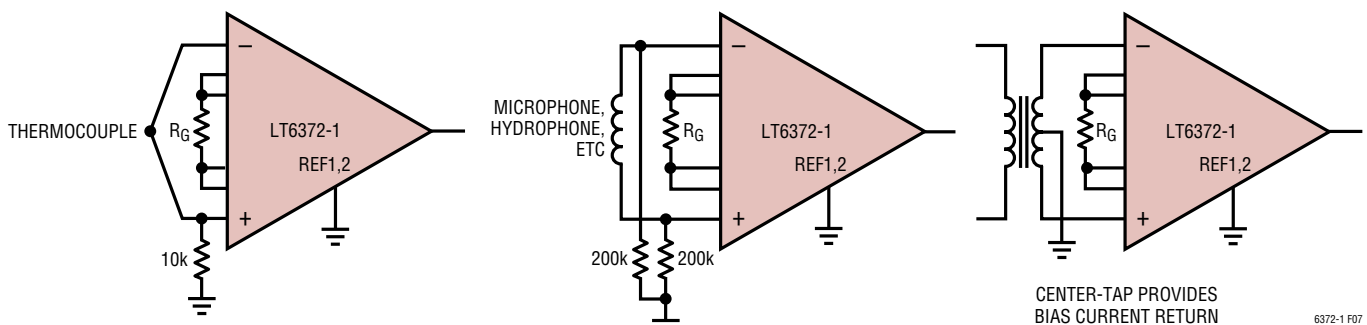gs operated at a potential very close to that of the input pins. In some cases, the guard-ring can be connected to R_G which biases one diode above the input.

For the lowest leakage, amplifiers can be used to drive the guard ring. These buffers must have very low input bias current since that will now be a leakage.
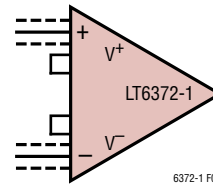
Figure 6. Guard-Rings Can Be Used to Minimize Leakage into the Input Pins

Input Bias Current Return Path

The low input bias current of the LT6372-1 (800pA max) and high input impedance (225GΩ) allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path, the inputs will float to either rail and exceed the input common mode range of the LT6372-1, resulting in a saturated input amplifier. Figure 7 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both AC and DC common mode rejection and DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

Figure 7. Providing an Input Common Mode Current Path

Rev. 0

APPLICATIONS INFORMATION

Input Protection

Additional input protection can be achieved by adding external resistors in series with each input. If low value resistors are needed, a clamp diode from the positive supply to each input will help improve robustness. A 2N4394 drain/source to gate is a good low leakage diode which can be used as shown in Figure 8. Robust input resistors should be chosen, such as carbon composite or bulk metal foil. Metal film and carbon film should not be used because of their poor performance.

Figure 8. Input Protection

Maintaining AC CMRR

To achieve optimum AC CMRR, it is important to balance the capacitance on the R_G gain setting pins. Furthermore, if the source resistance on each input is not equal, adding an additional resistance to one input to improve input source resistance matching will improve AC CMRR.
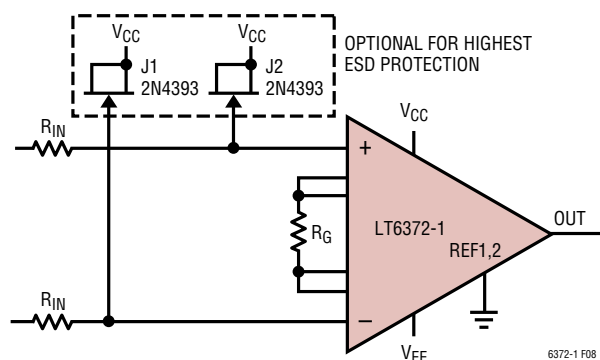
RFI Reduction/Internal RFI Filter

In many industrial and data acquisition applications, the LT6372-1 will be used to amplify small signals accurately in the presence of large common mode voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry using shielded or unshielded twisted-pair cabling, the cabling may act as an antenna, conveying very high frequency interference directly into the input stage of the LT6372-1.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing any unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

To help minimize this effect, the LT6372-1 has 50MHz on-chip RFI filters to help attenuate high frequencies before they can interact with its input transistors. These on-chip filters are well matched due to their monolithic construction, which helps minimize any degradation in AC CMRR. To reduce the effect of these out-of-band signals on the input offset voltage of the LT6372-1 further, an additional external low-pass filter can be used at the inputs. The filter should be located very close to the input pins of the circuit. An effective filter configuration is illustrated in Figure 9, where three capacitors have been added to the inputs of the LT6372-1.

The filter limits the input signal according to the following relationship:

$$\text{FilterFreq}_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$\text{FilterFreq}_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in $R \times C_C$ degrades the LT6372-1 CMRR. To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one magnitude smaller than C_D. The effect of mismatched C_Cs is reduced with a larger $C_D:C_C$ ratio.

Rev. 0

APPLICATIONS INFORMATION
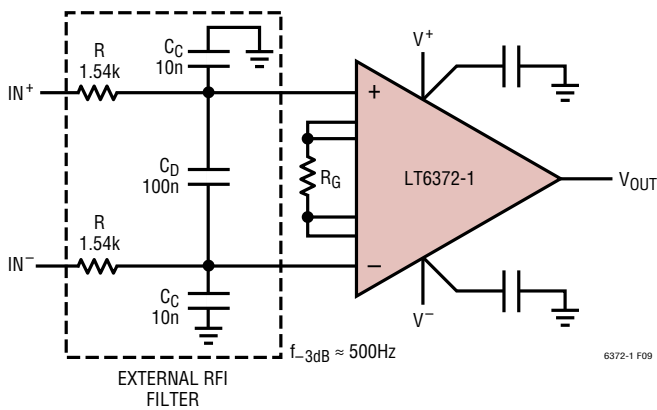
Figure 9. Adding a Simple External RC Filter at the Inputs to an Instrumentation Amplifier Is Effective in Further Reducing Rectification of High Frequency Out-Of-Band Signals

To avoid any possibility of common mode to differential mode signal conversion, match the common mode low-pass filter on each input to 1% or better. Here are the steps to help determine appropriate values for the filter:

1. Pick R and C_D to have a low pass pole at least 10x higher than the highest signal of interest (e.g. 500Hz for a 50Hz signal) using:

$$\text{FilterFreq}_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$= \frac{1}{2\pi R(2C_D + 0.1C_D)}$$

$$= \frac{1}{4.2\pi RC_D}$$

2. Select $C_C = C_D/10$.

If implemented this way, the common-mode pole frequency is placed about 20x higher than the differential pole frequency. Here are the differential and common-mode low pass pole frequencies for the values shown in Figure 9:

FilterFreq_{DIFF} = 500Hz

FilterFreq_{CM} = 10kHz

APPLICATIONS INFORMATION

Error Budget Analysis

The LT6372-1 features a split reference configuration providing a convenient and effective way to interface a bipolar swing to an ADC input without additional precision components. Performing the same level shift with traditional intsrumentation amplifiers as shown in Figure 11 requires external precison components which decrease accuracy, increase cost and occupy valuable PCB space. The error budget in Table 2 shows the total system error of a LT6372-1 used as a bridge amplifier.

PRECISION BRIDGE TRANSDUCER

LT6370A MONOLITHIC
INSTRUMENTATION AMPLIFIER
G = 100, R_G = ±0.1%, ±10ppm TC
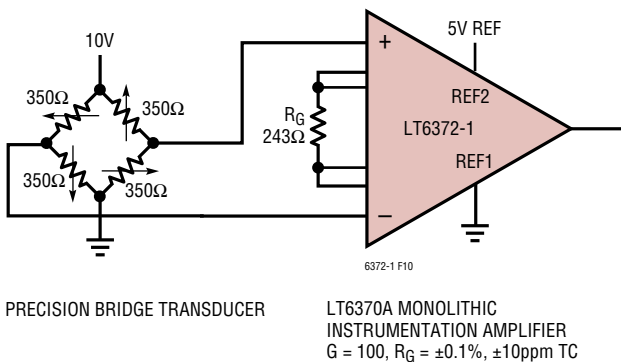
Figure 10. Precision Bridge Amplifier Using LT6372-1

PRECISION BRIDGE TRANSDUCER

LT6370A MONOLITHIC
INSTRUMENTATION AMPLIFIER
G = 100, R_G = ±0.1%, ±10ppm TC
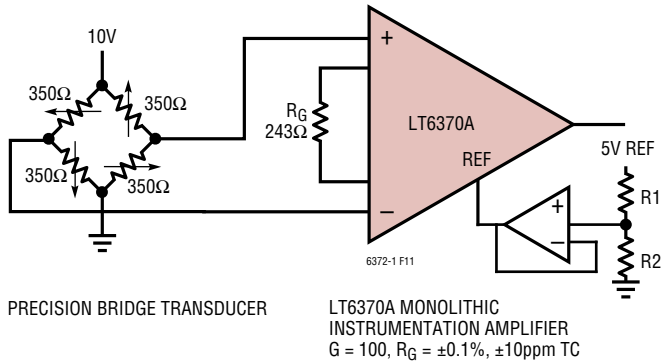
Figure 11. Precision Bridge Amplifier with External Level Shift

Table 2. Error Budget

ERROR SOURCE	CALCULATION	ERROR, ppm OF FULL SCALE
		LT6372-1
Absolute Accuracy at T_A = 25°C		
Gain Error, %	Gain Error in % • 10k + 1000	2200
Input Offset Voltage, µV	V_{OSI}/20mV	3000
Output Offset Voltage, µV	[V_{OSO}/100]/20mV	137.5
Input Offset Current, nA	[(I_{OS})(350)/2]/20mV	12.25
CMRR, dB	[(CMRR in ppm)(5V)/20mV	250
	Total Accuracy Error	**5599.75**
Drift to 85°C		
Gain Drift, ppm/°C	(Gain Drift + 10ppm/°C)(60°C)	2700
Input Offset Voltage Drift, µV/°C	[(V_{OSI} Drift)(60°C)]/20mV	1800
Output Offset Voltage Drift, µV/°C	[(V_{OSO} Drift)(60°C)]/100/20mV	120
	Total Drift Error	**4620**
Resolution		
Gain Nonlinearity, ppm of Full Scale		50
Typ 0.1Hz to 10Hz Voltage Noise, µV$_{P-P}$	(0.1Hz to 10Hz Noise)/20mV	10
	Total Resolution Error	**60**
	Grand Total Error	**10279.75**

G = 100

All errors are min/max and referred to input.

TYPICAL APPLICATIONS

Differential Output Instrumentation Amplifier

+V_S
+IN +
R_G
LT6372-1
REF1,2
−IN −
−V_S
10k
+OUT
12pF
10k
V_BIAS
− +
LTC2057
−OUT
6372-1 TA02
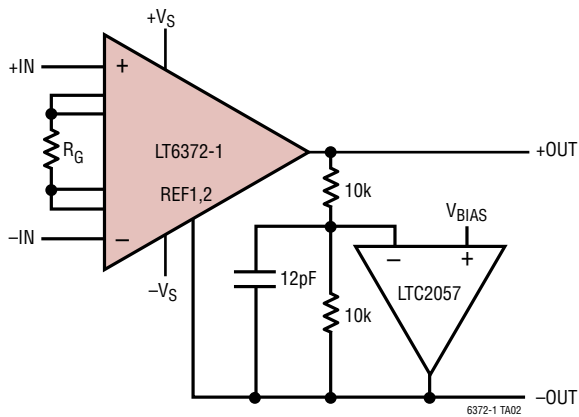
AC Coupled Instrumentation Amplifier

+V_S
+IN +
R_G
LT6372-1
REF1,2
−IN −
−V_S
C1 0.3µF
R1 500k
OUTPUT
−
LTC2057
+
$f_{-3dB} = \dfrac{1}{(2\pi)(R1)(C1)}$
$= 1.06Hz$
6372-1 TA03
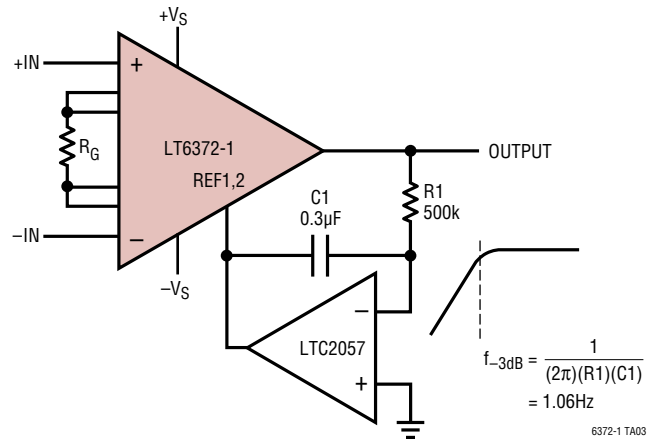
Precision Voltage-to-Current Converter

V_S
+IN +
R_G
LT6372-1
REF1,2
−IN −
−V_S
R_X
V_X
I_L
−
LTC2057
+
LOAD

$I_L = \dfrac{V_X}{R_X} = \dfrac{[(+IN) - (-IN)]G}{R_X}$

$G = \dfrac{24.2k\Omega}{R_G} + 1$

6372-1 TA04
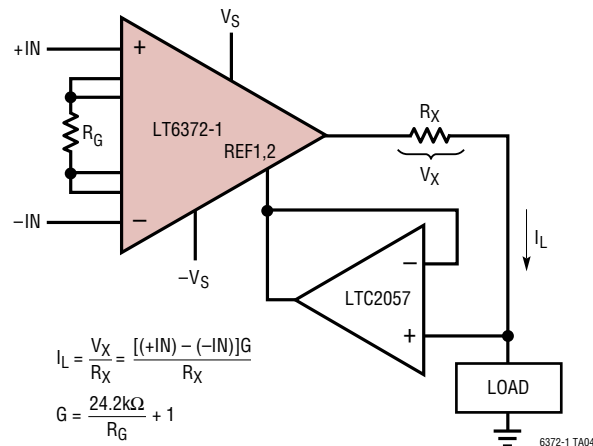
High Side, Bidirectional Current Sense

$I_L = \pm2A$
R_SENSE 0.05Ω
V_BUS
V_BUS > −12V
V_BUS < 11V
+V_S
LOAD
+
R_G 499Ω
LT6372-1
REF1,2
−
−V_S

$V_{OUT} = I_L \bullet R_{SENSE} \bullet \left(1 + \dfrac{24.2k}{R_G}\right)$

$= 2.5V / A$

6372-1 TA05

PACKAGE DESCRIPTION

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)

3.50 ±0.05
2.10 ±0.05
1.50 REF
2.65 ±0.05
1.65 ±0.05

0.70 ±0.05

PACKAGE OUTLINE

0.25 ±0.05
0.50 BSC
2.50 REF
3.10 ±0.05
4.50 ±0.05

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

3.00 ±0.10
0.75 ±0.05
PIN 1
TOP MARK
(NOTE 6)
4.00 ±0.10

0.200 REF
0.00 – 0.05

PIN 1 NOTCH
R = 0.20 OR 0.25
× 45° CHAMFER
R = 0.05 TYP
1.50 REF
19 20
0.40 ±0.10
1
2
2.65 ±0.10
2.50 REF
1.65 ±0.10
R = 0.115
TYP
0.25 ±0.05
0.50 BSC

(UDC20) QFN 1106 REV Ø

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

Rev. 0

For more information www.analog.com

PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)

BOTTOM VIEW OF
EXPOSED PAD OPTION

2.845 ±0.102
(.112 ±.004)

0.889 ±0.127
(.035 ±.005)

5.10
(.201)
MIN

1.651 ±0.102   3.20 – 3.45
(.065 ±.004)   (.126 – .136)

0.305 ±0.038
(.0120 ±.0015)
TYP

0.50
(.0197)
BSC

RECOMMENDED SOLDER PAD LAYOUT

2.845 ±0.102
(.112 ±.004)

1   8

1.651 ±0.102
(.065 ±.004)

16   9

DETAIL "B"

0.35
REF

0.12 REF

DETAIL "B"
CORNER TAIL IS PART OF
THE LEADFRAME FEATURE.
FOR REFERENCE ONLY
NO MEASUREMENT PURPOSE

DETAIL "A"

0.254
(.010)

0° – 6° TYP

GAUGE PLANE

0.53 ±0.152
(.021 ±.006)

DETAIL "A"

0.18
(.007)

4.039 ±0.102
(.159 ±.004)
(NOTE 3)

16 15 14 13 12 11 10 9

0.280 ±0.076
(.011 ±.003)
REF

4.90 ±0.152
(.193 ±.006)

3.00 ±0.102
(.118 ±.004)
(NOTE 4)

1 2 3 4 5 6 7 8

1.10
(.043)
MAX

0.86
(.034)
REF

SEATING
PLANE

0.17 – 0.27
(.007 – .011)
TYP

0.50
(.0197)
BSC

0.1016 ±0.0508
(.004 ±.002)

MSOP (MSE16) 0213 REV F

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

Programmable Gain Amplifier

6372-1 TA06

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Instrumentation Amplifiers		
AD8429	Low Noise Instrumentation Amplifier	$V_S = 36V$, $I_S = 6.7mA$, $V_{OS} = 50\mu V$, BW = 15MHz, eni = $1nV/\sqrt{Hz}$, eno = $45nV/\sqrt{Hz}$
LT6372-0.2	Low Drift Instrumentation Amplifier	LT6372-1 with Min Gain = 0.2V/V
LT6370	Low Drift Instrumentation Amplifier	$V_S = 30V$, $I_S = 2.65mA$, $V_{OS} = 25\mu V$, BW = 3.1MHz, eni = $7nV/\sqrt{Hz}$, eno = $65nV/\sqrt{Hz}$
LTC1100	Zero-Drift Instrumentation Amplifier	$V_S = 18V$, $I_S = 2.4mA$, $V_{OS} = 10\mu V$, BW = 19kHz, $1.9\mu V_{P-P}$ DC to 10Hz
AD8421	Low Noise Instrumentation Amplifier	$V_S = 36V$, $I_S = 2mA$, $V_{OS} = 25\mu V$, BW = 10MHz, eni = $3nV/\sqrt{Hz}$, eno = $60nV/\sqrt{Hz}$
AD8221	Low Power Instrumentation Amplifier	$V_S = 36V$, $I_S = 900\mu A$, $V_{OS} = 25\mu V$, BW = 825kHz, eni = $8nV/\sqrt{Hz}$, eno = $75nV/\sqrt{Hz}$
LT1167	Instrumentation Amplifier	$V_S = 36V$, $I_S = 900\mu A$, $V_{OS} = 40\mu V$, BW = 1MHz, eni = $7.5nV/\sqrt{Hz}$, eno = $67nV/\sqrt{Hz}$
AD620	Low Power Instrumentation Amplifier	$V_S = 36V$, $I_S = 900\mu A$, $V_{OS} = 50\mu V$, BW = 1MHz, eni = $9nV/\sqrt{Hz}$, eno = $72nV/\sqrt{Hz}$
LTC6800	RRIO Instrumentation Amplifier	$V_S = 5.5V$, $I_S = 800\mu A$, $V_{OS} = 100\mu V$, BW = 200kHz, $2.5\mu V_{P-P}$ DC to 10Hz
LTC2053	Zero-Drift Instrumentation Amplifier	$V_S = 11V$, $I_S = 750\mu A$, $V_{OS} = 10\mu V$, BW = 200kHz, $2.5\mu V_{P-P}$ DC to 10Hz
LT1168	Low Power Instrumentation Amplifier	$V_S = 36V$, $I_S = 350\mu A$, $V_{OS} = 40\mu V$, BW = 400kHz, eni = $10nV/\sqrt{Hz}$, eno = $165nV/\sqrt{Hz}$
Operational Amplifiers		
LTC2057	40V Zero Drift Op Amp	$V_{OS} = 4\mu V$, Drift = 15nV/°C, $I_B = 200pA$, $I_S = 900\mu A$
Analog to Digital Converters		
LTC2389-16	16-Bit SAR ADC	2.5Msps, 96dB SNR, 162.5mW
LTC2367-16	16-Bit SAR ADC	500Ksps, 94.7dB SNR, 6.8mW

ANALOG DEVICES