

- Member of the Texas Instruments Widebus™ Family
- Low-Power Advanced CMOS Technology
- Operates From 3-V to 3.6-V V_{CC}
- Load Clock and Unload Clock Can Be Asynchronous or Coincident
- Full, Empty, and Half-Full Flags
- Programmable Almost-Full/Almost-Empty Flag
- Fast Access Times of 18 ns With a 50-pF Load and All Data Outputs Switching Simultaneously
- Data Rates up to 40 MHz
- 3-State Outputs
- Pin-to-Pin Compatible With SN74ACT7804, SN74ACT7806, and SN74ACT7814
- Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Spacing

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALVC7814 is an 18-bit FIFO with high speed and fast access times. Data is processed at rates up to 40 MHz with access times of 18 ns in a bit-parallel format. These memories are designed for 3-V to 3.6-V V_{CC} operation.

Data is written into memory on a low-to-high transition of the load clock (LDCK) and is read out on a low-to-high transition of the unload clock (UNCK). The memory is full when the number of words clocked in exceeds the number of words clocked out by 64. When the memory is full, LDCK has no effect on the data residing in memory. When the memory is empty, UNCK has no effect.

Status of the FIFO memory is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full and high when the memory is not full. The $\overline{EMPTY}$ output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 32 or more words and low when it contains 31 or fewer words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{PEN}$) is low. The AF/AE flag is high when the FIFO contains X or fewer words or $(64 - Y)$ or more words. The AF/AE flag is low when the FIFO contains between $(X + 1)$ and $(63 - Y)$ words.

DL PACKAGE
(TOP VIEW)

RESET	1	56	OE
D17	2	55	Q17
D16	3	54	Q16
D15	4	53	Q15
D14	5	52	GND
D13	6	51	Q14
D12	7	50	V_{CC}
D11	8	49	Q13
D10	9	48	Q12
V_{CC}	10	47	Q11
D9	11	46	Q10
D8	12	45	Q9
GND	13	44	GND
D7	14	43	Q8
D6	15	42	Q7
D5	16	41	Q6
D4	17	40	Q5
D3	18	39	V_{CC}
D2	19	38	Q4
D1	20	37	Q3
D0	21	36	Q2
HF	22	35	GND
$\overline{PEN}$	23	34	Q1
AF/AE	24	33	Q0
LDCK	25	32	UNCK
NC	26	31	NC
NC	27	30	NC
FULL	28	29	EMPTY

NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

SN74ALVC7814

64 × 18

LOW-POWER FIRST-IN, FIRST-OUT MEMORY

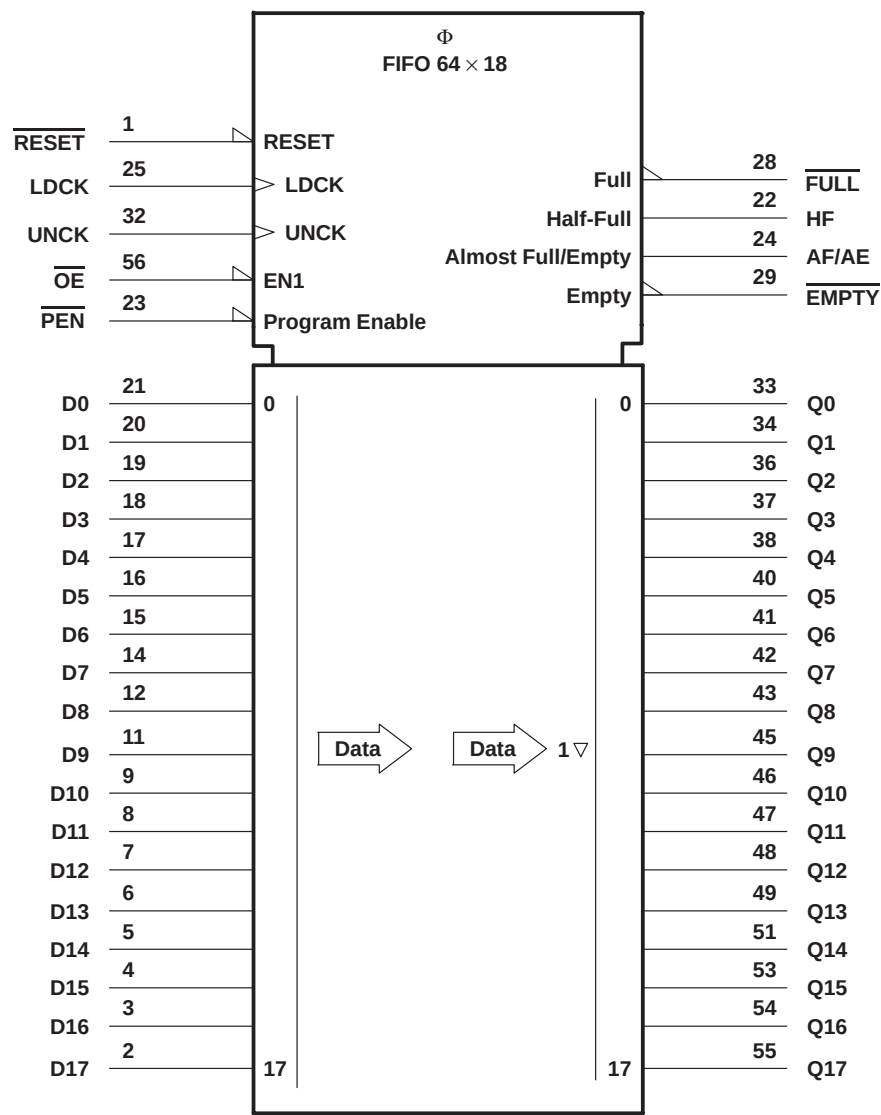
SCAS592A – OCTOBER 1997 – REVISED APRIL 1998

description (continued)

A low level on the reset ($\overline{\text{RESET}}$) resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset on power up. The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The data outputs are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) is high.

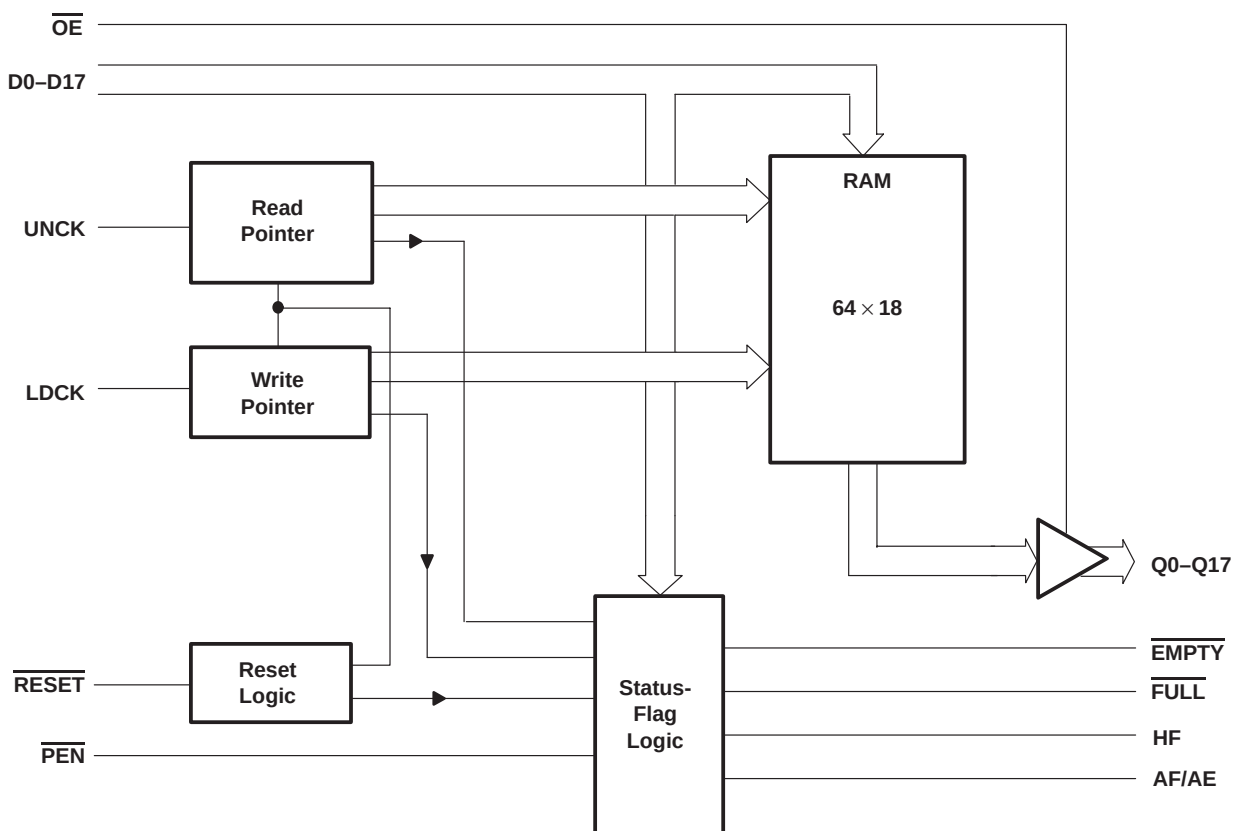
The SN74ALVC7814 is characterized for operation from 0°C to 70°C.

logic symbol†



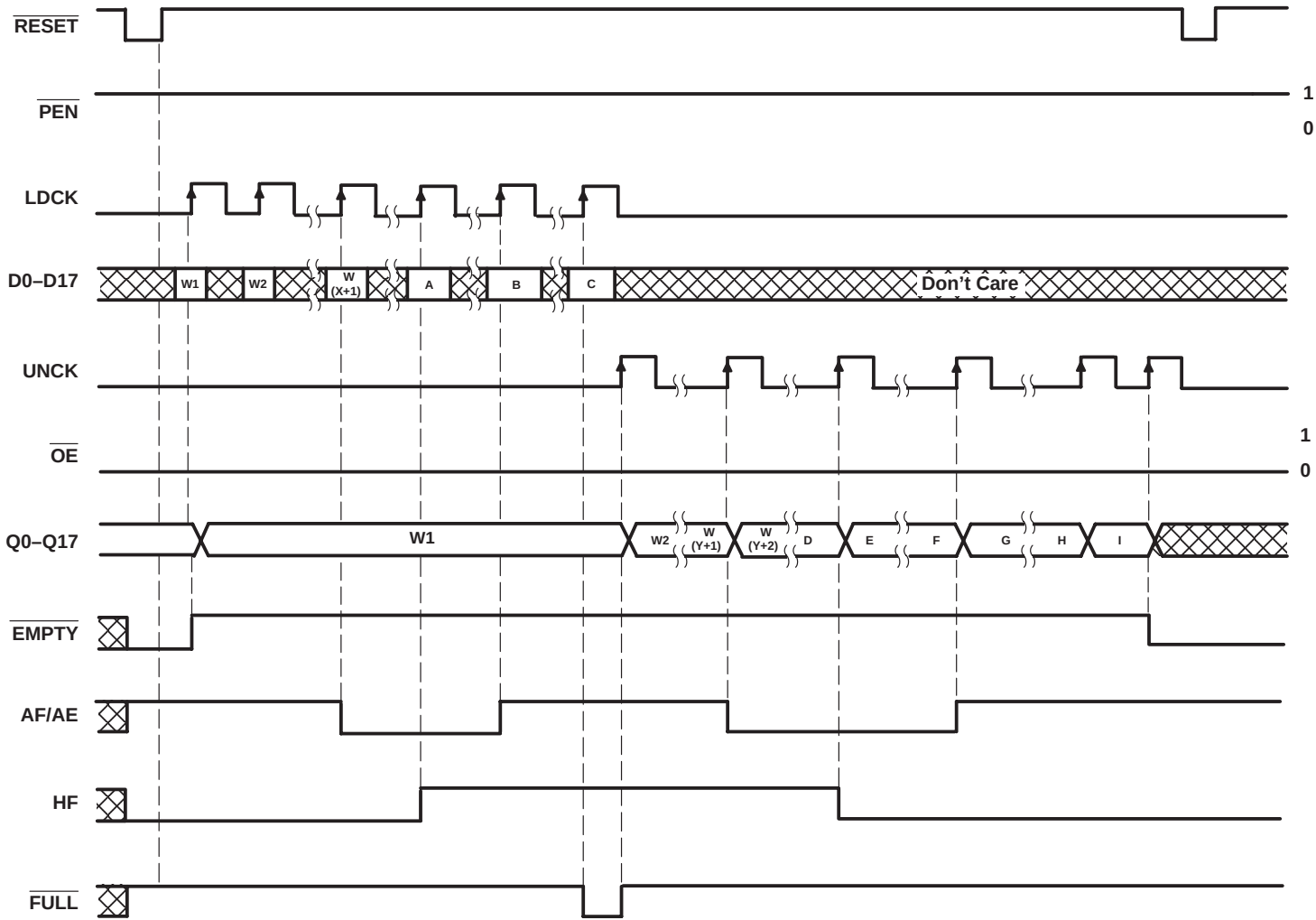
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost full/almost empty flag. Depth-offset values can be programmed for this flag or the default value of 64 can be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or fewer words or (64 – Y) or more words. AF/AE is high after reset.
D0–D17	2–9, 11–12, 14–21	I	18-bit data input port
EMPTY	29	O	Empty flag. <u>EMPTY</u> is low when the FIFO is empty. A FIFO reset also causes <u>EMPTY</u> to go low.
FULL	28	O	Full flag. <u>FULL</u> is low when the FIFO is full. A FIFO reset causes <u>FULL</u> to go high.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when <u>FULL</u> is high.
<u>OE</u>	56	I	Output enable. When <u>OE</u> is high, the data outputs are in the high-impedance state.
<u>PEN</u>	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when <u>PEN</u> is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
<u>RESET</u>	1	I	Reset. A low level on <u>RESET</u> resets the FIFO and drives AF/AE and <u>FULL</u> high and HF and <u>EMPTY</u> low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when <u>EMPTY</u> is high.



Define the AF/AE Flag Using the Default Value of X and Y

Figure 1. Write, Read, and Flag Timing Reference

DATA-WORD NUMBERS FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD								
	A	B	C	D	E	F	G	H	I
SN74ALVC7814	W32	W(64 – Y)	W64	W33	W34	W(64 – X)	W(65 – X)	W64	W64

Figure 1. Write, Read, and Flag Timing Reference (Continued)

offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or fewer words or (512 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset. On the following low-to-high transition of LDCK, the binary value on D0–D7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 32 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 8, $\overline{\text{PEN}}$ must be held high.

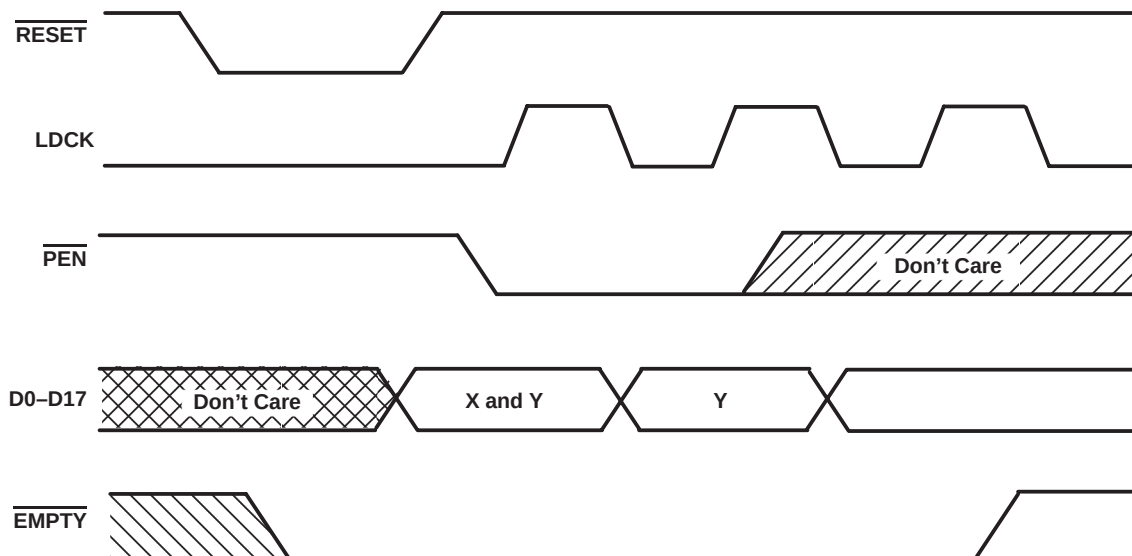


Figure 2. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Voltage applied to a disabled 3-state output	–0.5 V to 3.6 V
Package thermal impedance, θ_{JA} (see Note 3)	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		'ALVC7814-25		'ALVC7814-40		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	3	3.6	3	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current, Q outputs, flags	$V_{CC} = 3$ V		–8		mA
I_{OL}	Low-level output current, Q outputs, flags	$V_{CC} = 3$ V		16		mA
T_A	Operating free-air temperature	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
V _{OH}	Flags, Q outputs	V _{CC} = 3 V to 3.6 V,	I _{OH} = −100 μA	V _{CC} −0.2		2.4	V
		V _{CC} = 3 V,	I _{OH} = −8 mA				
V _{OL}	Flags, Q outputs	V _{CC} = 3 V to 3.6 V,	I _{OL} = 100 μA			0.2	V
	Flags	V _{CC} = 3 V,	I _{OL} = 8 mA			0.4	
	Q outputs	V _{CC} = 3 V,	I _{OL} = 16 mA			0.55	
I _I		V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±5	μA
I _{OZ}		V _{CC} = 3.6 V,	V _O = V _{CC} or GND			±10	μA
I _{CC}		V _{CC} = 3.6 V,	V _I = V _{CC} or GND, I _O = 0			40	μA
ΔI _{CC} [§]		V _{CC} = 3.6 V, One input at V _{CC} −0.6 V, Other inputs at V _{CC} or GND				500	μA
C _i		V _{CC} = 3.3 V,	V _I = V _{CC} or GND	3			pF
C _O		V _{CC} = 3.3 V,	V _O = V _{CC} or GND	6			pF

[‡] All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

^{\S} This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

timing requirements over recommended operating conditions (see Figures 1 through 3)

			'ALVC7814-25		'ALVC7814-40		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		40		25		MHz
t _w	Pulse duration	D0–D17 high or low	8		12		ns
		LDCK high or low	8		12		
		UNCK high or low	8		12		
		PEN low	8		12		
		RESET low	10		12		
t _{su}	Setup time	D0–D17 before LDCK↑	5		5		ns
		LDCK inactive before RESET high	6		6		
		PEN before LDCK↑	8		8		
t _h	Hold time	D0–D17 after LDCK↑	0		0		ns
		PEN high after LDCK low	0		0		
		PEN low after LDCK↑	3		3		
		LDCK inactive after RESET high	6		6		

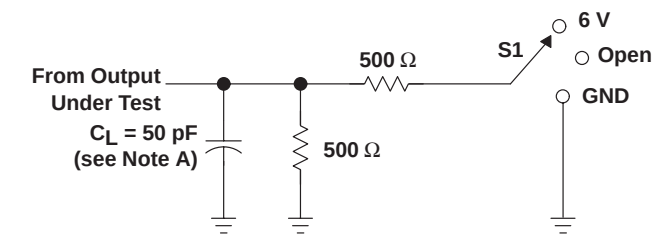
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ALVC7814-25		'ALVC7814-40		UNIT
			MIN	MAX	MIN	MAX	
f _{max}	LDCK or UNCK		40		25		MHz
t _{pd}	LDCK↑	Any Q	9	22	9	24	ns
	UNCK↑		6	18	6	20	
t _{PLH}	LDCK↑	EMPTY	6	17	6	19	ns
t _{PHL}	UNCK↑	EMPTY	6	17	6	19	ns
	RESET low		4	18	4	20	
t _{PLH}	UNCK↑	FULL	6	17	6	19	ns
	RESET low		4	20	4	22	
t _{PHL}	LDCK↑	FULL	6	17	6	19	ns
t _{pd}	LDCK↑	AF/AE	7	20	7	22	ns
	UNCK↑		7	20	7	22	
t _{PLH}	RESET low	AF/AE	2	12	2	14	ns
	LDCK↑	HF	5	20	5	22	
t _{PHL}	UNCK↑	HF	7	20	7	22	ns
	RESET low		3	14	3	16	
t _{en}	OE	Any Q	2	10	2	11	ns
t _{dis}	OE	Any Q	2	11	2	12	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

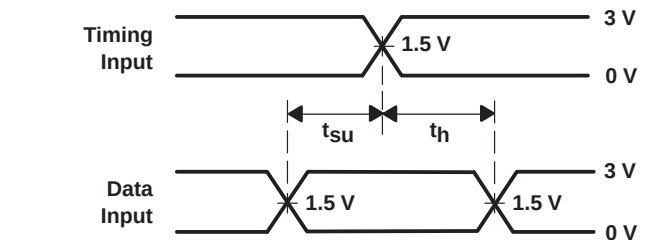
PARAMETER			TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C _L = 50 pF, f = 5 MHz		53	pF

PARAMETER MEASUREMENT INFORMATION

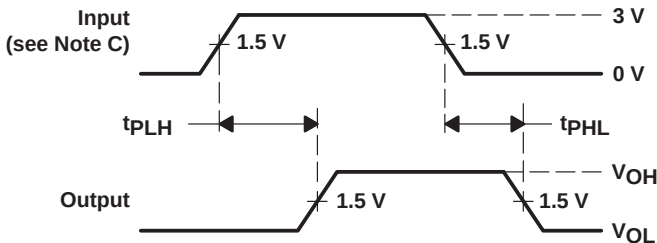


LOAD CIRCUIT FOR OUTPUTS

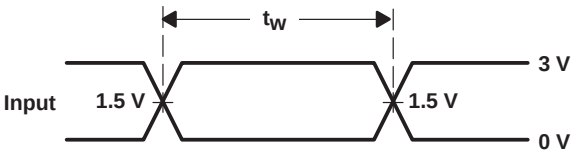
PARAMETER		S1
ten	tpZH	GND
	tpZL	6 V
tdis	tpHZ	GND
	tpLZ	6 V
tpd	tpLH/tpHL	Open



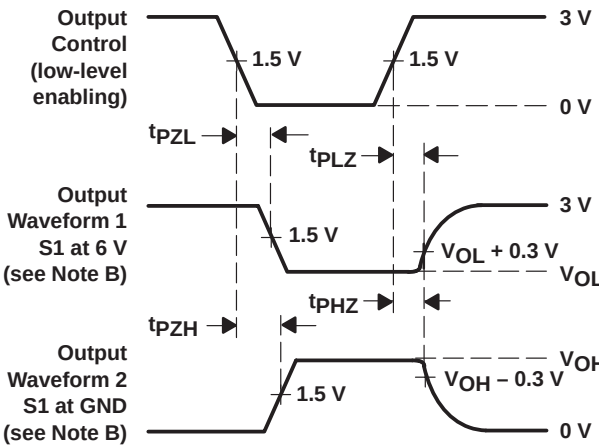
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. CL includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.

Figure 3. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)

TYPICAL CHARACTERISTICS

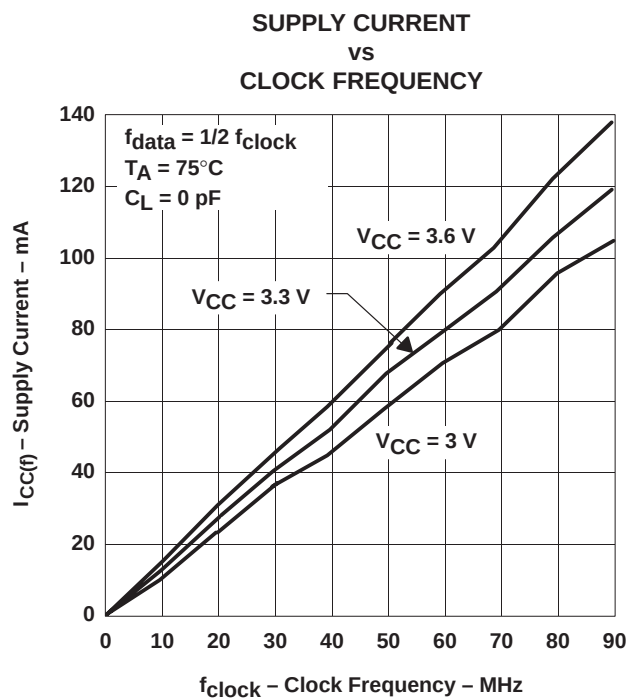


Figure 4

APPLICATION INFORMATION

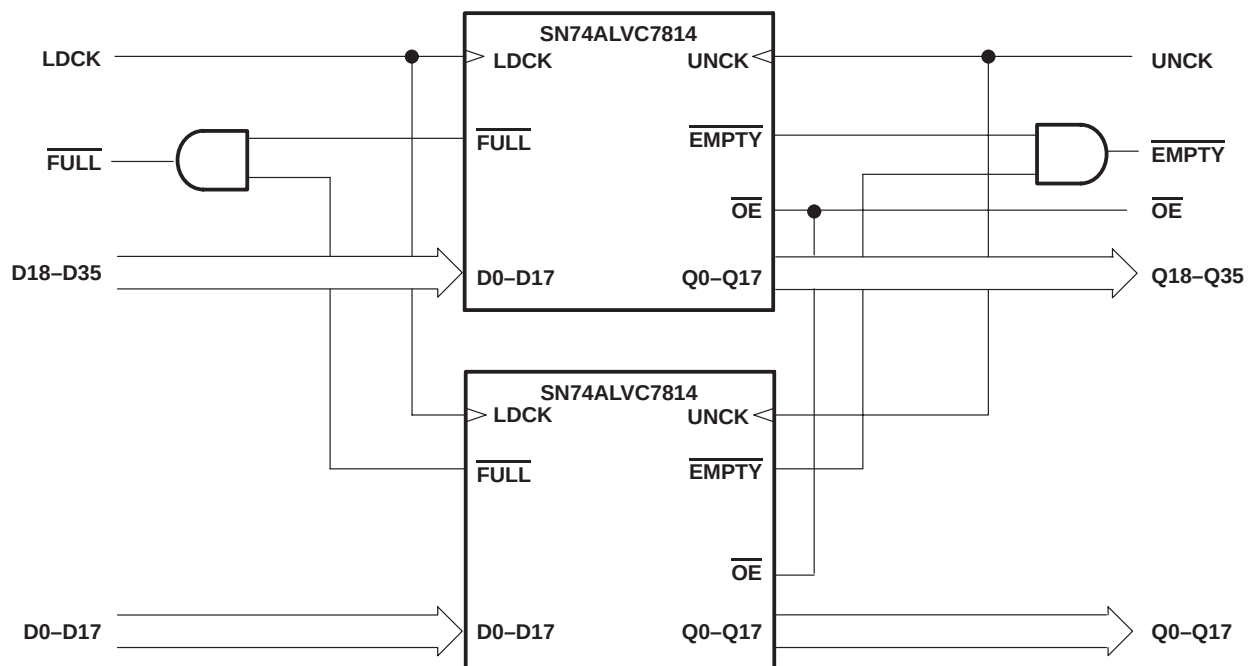


Figure 5. Word-Width Expansion: 64 × 36 Bits

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVC7814-40DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALVC7814-40

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE

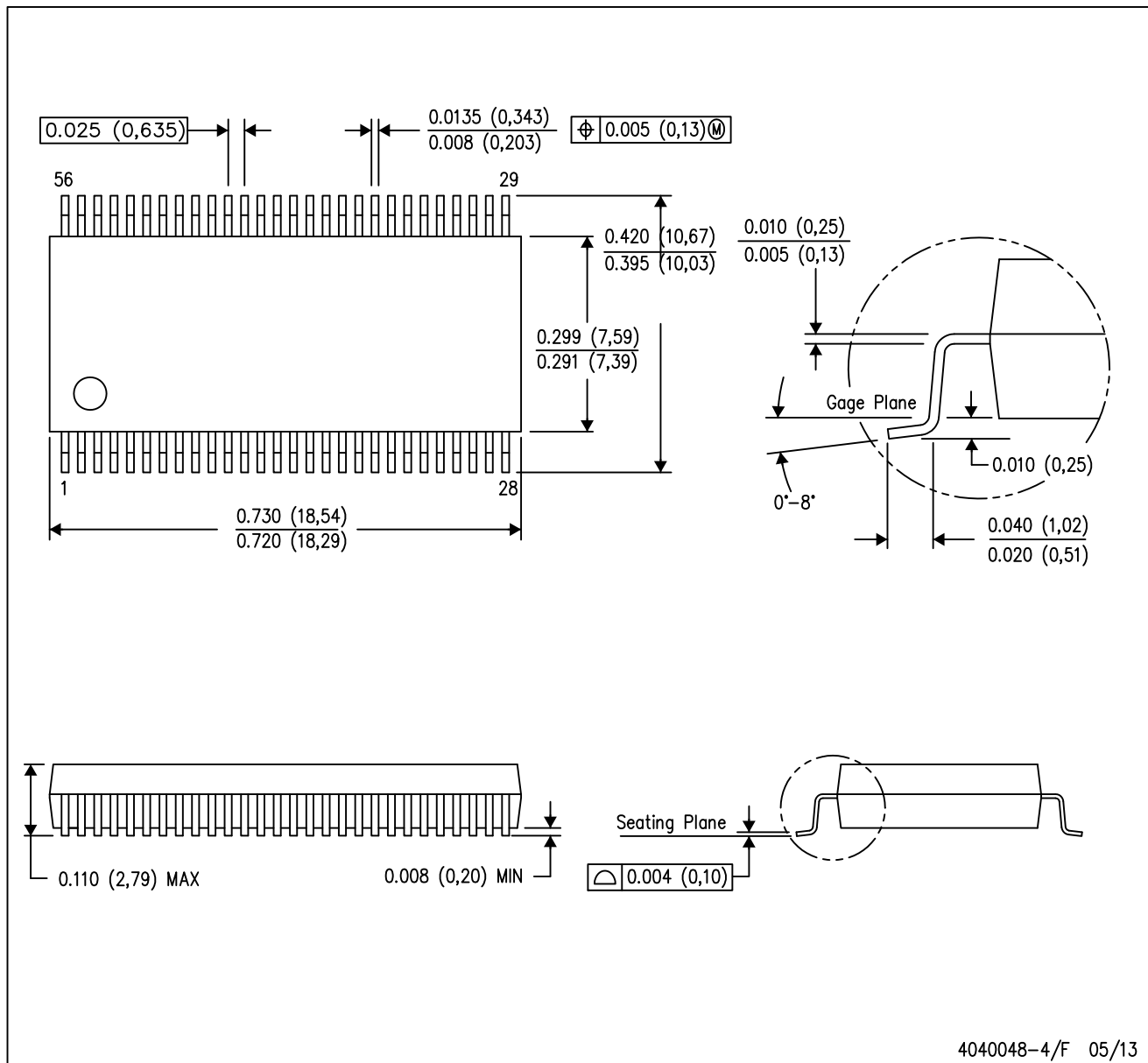


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALVC7814-40DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated