1/3-Inch 1.2Mp CMOS Digital Image Sensor with Global Shutter

AR0134 Data Sheet, Rev. D

Features

- Aptina's 3rd Generation Global Shutter Technology
- Superior low-light performance
- HD video (720p60)
- Video/Single Frame mode
- Flexible row-skip modes
- On-chip AE and statistics engine
- Parallel and serial output
- Support for external LED or flash
- Auto black level calibration
- Context switching

Applications

- Scene processing
- Scanning and machine vision
- 720p60 video applications

General Description

Aptina's AR0134 is a 1/3-inch 1.2Mp CMOS digital image sensor with an active-pixel array of 1280H x 960V. It is designed for low light performance and features a global shutter for accurate capture of moving scenes. It includes sophisticated camera functions such as auto exposure control, windowing, scaling, row skip mode, and both video and single frame modes. It is programmable through a simple two-wire serial interface. The AR0134 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and industrial inspection.

Table 1: Key Parameters

Parameter		Typical Value
Optical format		1/3-inch (6 mm)
Active pixels		1280H x 960V = 1.2 Mp
Pixel size		3.75µm
Color filter array		RGB Bayer or Monochrome
Shutter type		Global shutter
Input clock range		6 – 50 MHz
Output pixel clock (maximum)		74.25 MHz
Output	Serial	HiSPi
	Parallel	12-bit

Table 1: Key Parameters (continued)

Parameter		Typical Value
Frame rate	Full resolution	54 fps
	720p	60 fps
Responsivity	Monochrome	6.1 V/lux-sec
	Color	5.3 V/lux-sec
SNR_{MAX}		38.6 dB
Dynamic range		64 dB
Supply voltage	I/O	1.8 or 2.8 V
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.4 V
Power consumption		<400 mW
Operating temperature		–30°C to +70°C (ambient) –30°C to +80°C (junction)
Package options		9 x 9 mm 64-pin iBGA
		10x10 mm 48-pin iLCC
		Bare die

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
AR0134CSSM25SUEA0	Mono, iBGA, 25deg shift
AR0134CSSM00SUEA0	Mono, iBGA
AR0134CSSM00SUEAH	Mono, iBGA, Head Board
AR0134CSSM00SUEAD	Mono, iBGA, Demo Kit
AR0134CSSC00SUEA0	Color, iBGA
AR0134CSSC00SUEAH	Color, iBGA, Head Board
AR0134CSSC00SUEAD	Color, iBGA, Demo Kit
AR0134CSSM00SPCA0	Mono, iLCC (Parallel)
AR0134CSSM25SPCA0	Mono, iLCC (Parallel), 25deg shift
AR0134CSSC00SPCA0	Color, iLCC (Parallel)
AR0134CSSC00SPD20	Color, Bare die
AR0134CSSM00SPD20	Mono, Bare die
AR0134CSSM25SPD20	Mono, Bare die, 25deg shift

Table of Contents

List of Figures

List of Tables

General Description

The Aptina™ AR0134 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 54 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (HiSPi) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock. A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

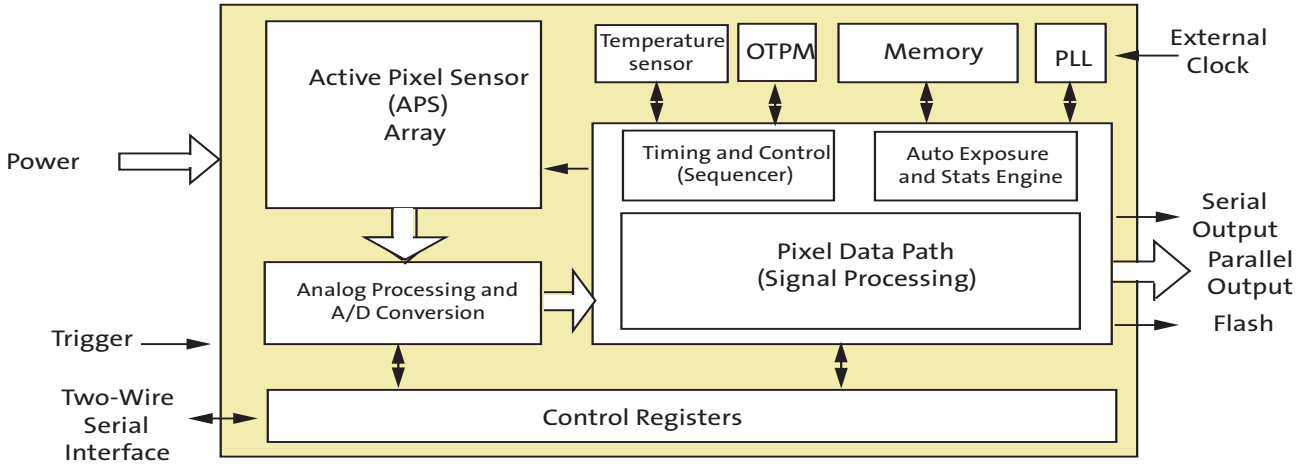
The AR0134 includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, on-board temperature sensor, and row skip and digital binning modes.

The sensor is designed to operate in a wide temperature range (–30°C to +70°C).

Functional Overview

The AR0134 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

Figure 1: Block Diagram



User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.2 Mp Active- Pixel Sensor array. The AR0134 features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All rows simultaneously integrate light prior to readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to- digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital

processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

Features Overview

The AR0134 Global Sensor shutter has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0134 Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

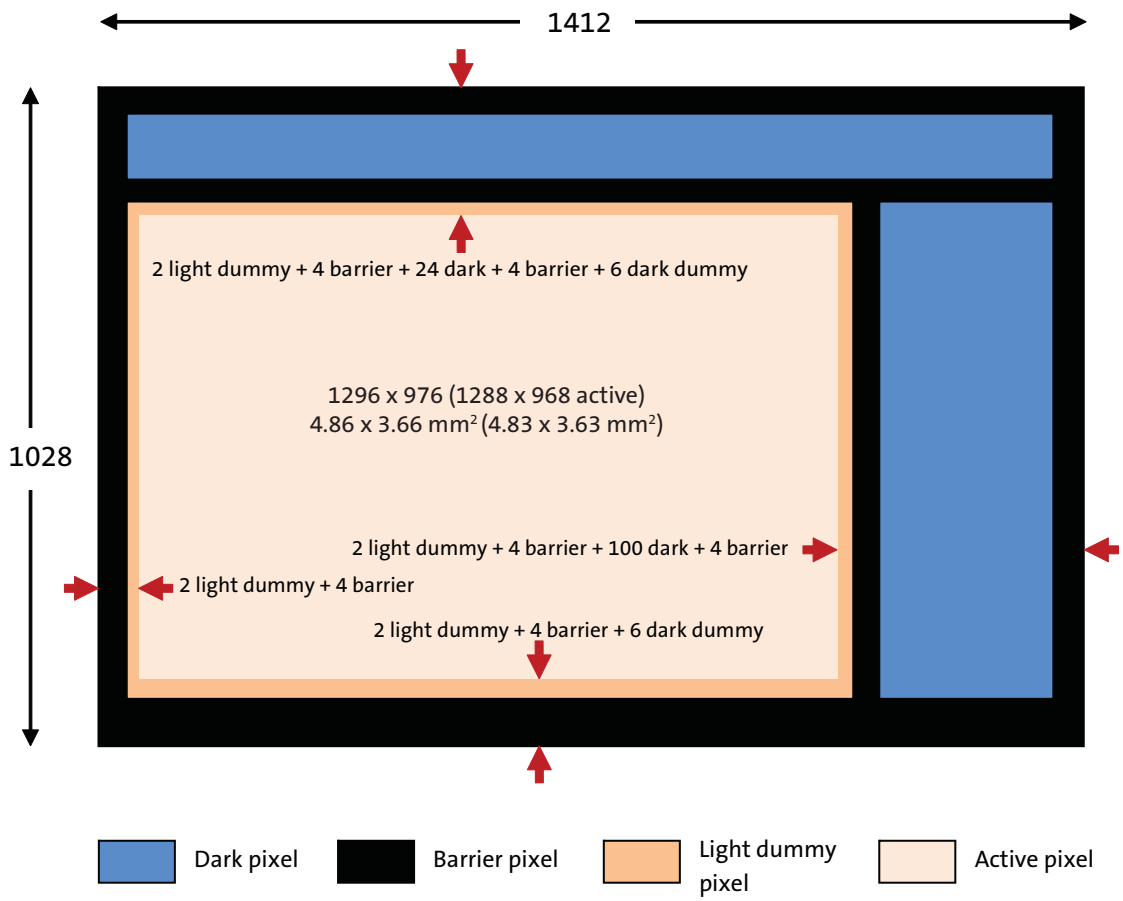
- Operating Modes
  The AR0134 works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes. Trigger mode is not compatible with the HiSPi interface.
- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.
- Context Switching
  Context switching may be used to rapidly switch between two sets of register values. Refer to the AR0134 Developer Guide for a complete set of context switchable registers.
- Gain
  The AR0134 Global Shutter sensor can be configured for analog gain of up to 8x, and digital gain of up to 8x.
- Automatic Exposure Control
  The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame. Refer to the AR0134 Developer Guide for more details.
- HiSPi
  The AR0134 Global Shutter image sensor supports two or three lanes of Streaming-SP or Packetized-SP protocols of Aptina's High-Speed Serial Pixel Interface.
- PLL
  An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.
- Reset
  The AR0134 may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The AR0134 output pins may be tri-stated using a dedicated output enable pin.
- Temperature Sensor
  The temperature sensor is only guaranteed to be functional when the AR0134 is initially powered-up or is reset at temperatures at or above 0°C.
- Black Level Correction
- Row Noise Correction
- Column Correction
- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to grey, and a walking 1s test pattern.

Pixel Data Format

Pixel Array Structure

The AR0134 pixel array is configured as 1412 columns by 1028 rows, (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. Of the right 108 columns, 64 are dark pixels used for row noise correction. Of the top 24 rows of pixels, 12 of the dark rows are used for black level correction. There are 1296 columns by 976 rows of optically active pixels. While the sensor's format is 1280 x 960, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

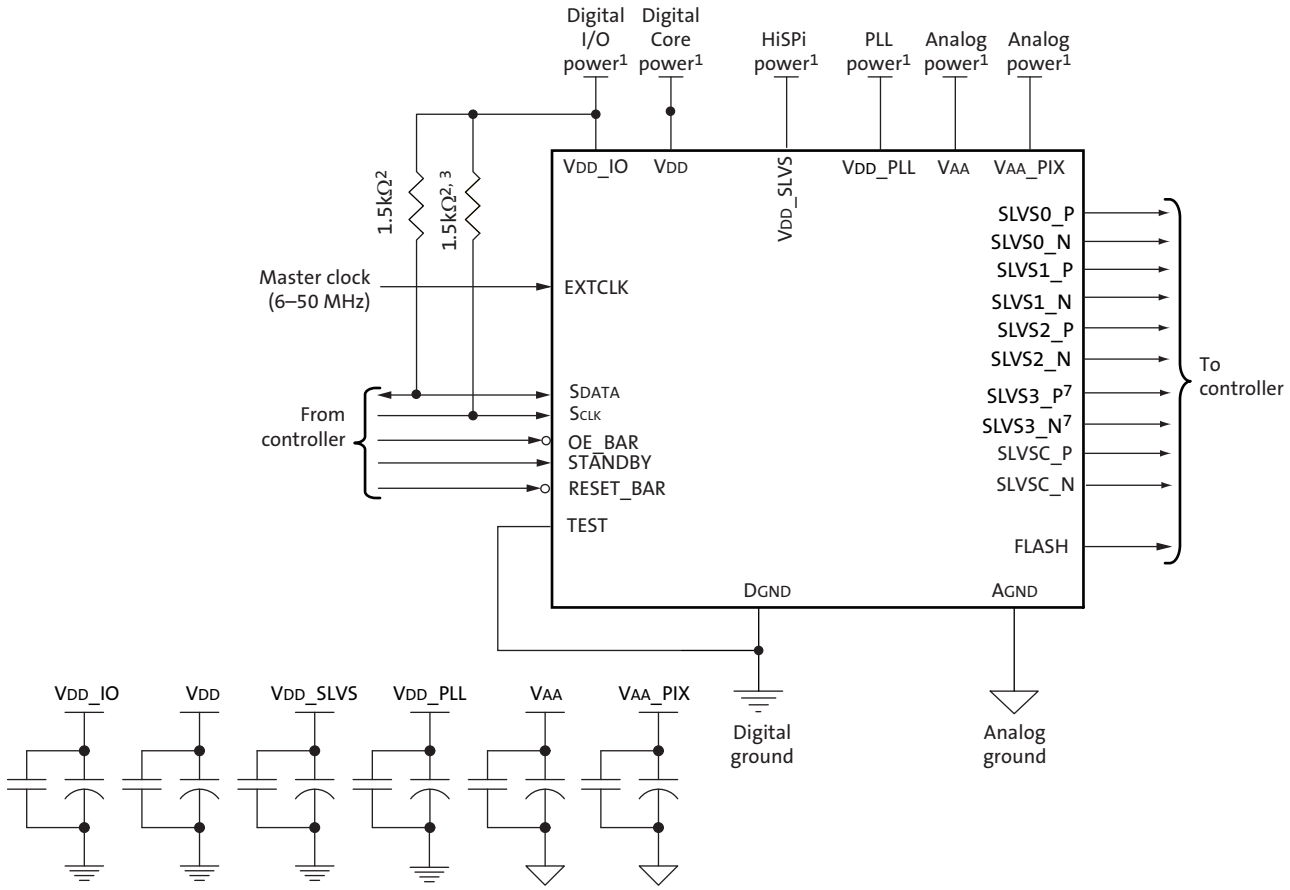
Figure 2: Pixel Array Description



Configuration and Pinout

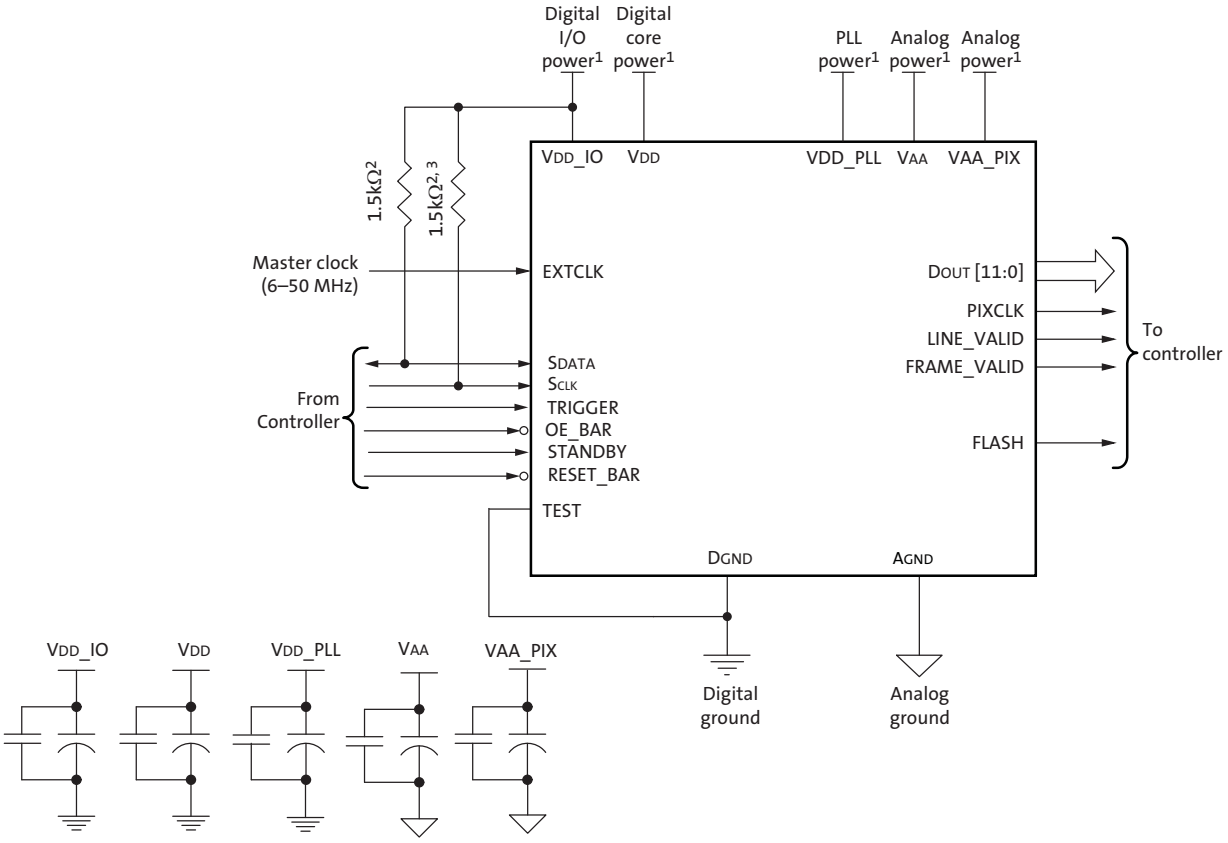
The figures and tables below show a typical configuration for the AR0134 image sensor and show the package pinouts.

Figure 4: Typical Configuration: Serial Four-Lane HiSPi Interface



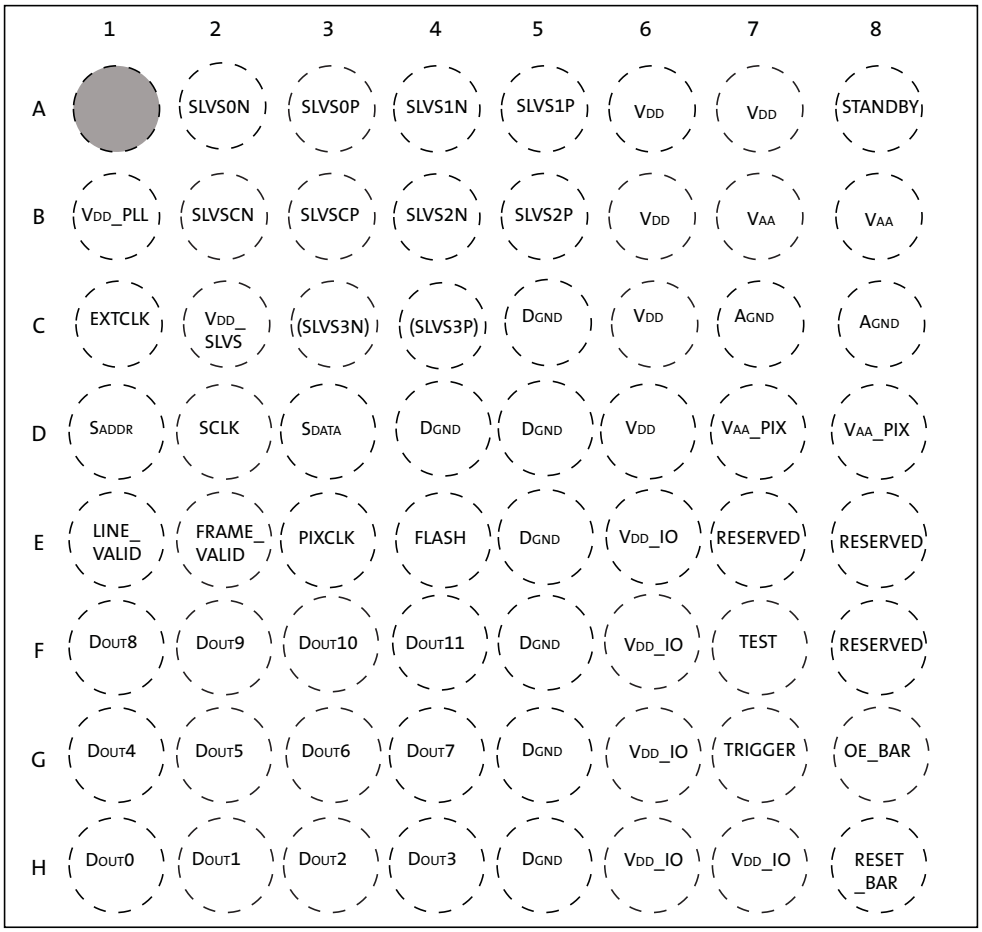
Notes:
1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. Aptina recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0134 demo headboard schematics for circuit recommendations.
6. Aptina recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
7. Although 4 serial lanes are shown, the AR0134 supports only 2 or 3 lane HiSPi.

Figure 5: Typical Configuration: Parallel Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. Aptina recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0134 demo headboard schematics for circuit recommendations.
6. Aptina recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.

Figure 6: 9x9mm 63-Ball iBGA Package



Top View
(Ball Down)

Table 3: Pin Descriptions - 63-Ball iBGA Package

Name	iBGA Pin	Type	Description
SLVS0_N	A2	Output	HiSPi serial data, lane 0, differential N.
SLVS0_P	A3	Output	HiSPi serial data, lane 0, differential P.
SLVS1_N	A4	Output	HiSPi serial data, lane 1, differential N.
SLVS1_P	A5	Output	HiSPi serial data, lane 1, differential P.
STANDBY	A8	Input	Standby-mode enable pin (active HIGH).
VDD_PLL	B1	Power	PLL power.
SLVSC_N	B2	Output	HiSPi serial DDR clock differential N.
SLVSC_P	B3	Output	HiSPi serial DDR clock differential P.
SLVS2_N	B4	Output	HiSPi serial data, lane 2, differential N.
SLVS2_P	B5	Output	HiSPi serial data, lane 2, differential P.
VAA	B7, B8	Power	Analog power.
EXTCLK	C1	Input	External input clock.
VDD_SLVS	C2	Power	HiSPi power. (May leave unconnected if parallel interface is used)
SLVS3_N	C3	Output	(Unsupported) HiSPi serial data, lane 3, differential N.
SLVS3_P	C4	Output	(Unsupported) HiSPi serial data, lane 3, differential P.
DGND	C5, D4, D5, E5, F5, G5, H5	Power	Digital GND.
VDD	A6, A7, B6, C6, D6	Power	Digital power.
AGND	C7, C8	Power	Analog GND.
SADDR	D1	Input	Two-Wire Serial address select.
SCLK	D2	Input	Two-Wire Serial clock input.
SDATA	D3	I/O	Two-Wire Serial data I/O.
VAA_PIX	D7, D8	Power	Pixel power.
LINE_VALID	E1	Output	Asserted when DOUT line data is valid.
FRAME_VALID	E2	Output	Asserted when DOUT frame data is valid.
PIXCLK	E3	Output	Pixel clock out. DOUT is valid on rising edge of this clock.
FLASH	E4	Output	Control signal to drive external light sources.
VDD_IO	E6, F6, G6, H6, H7	Power	I/O supply power.
DOUT8	F1	Output	Parallel pixel data output.
DOUT9	F2	Output	Parallel pixel data output.
DOUT10	F3	Output	Parallel pixel data output.
DOUT11	F4	Output	Parallel pixel data output (MSB)
TEST	F7	Input	Manufacturing test enable pin (connect to DGND).
DOUT4	G1	Output	Parallel pixel data output.
DOUT5	G2	Output	Parallel pixel data output.
DOUT6	G3	Output	Parallel pixel data output.
DOUT7	G4	Output	Parallel pixel data output.
TRIGGER	G7	Input	Exposure synchronization input. (Connect to DGND if HiSPi interface is used)
OE_BAR	G8	Input	Output enable (active LOW).
DOUT0	H1	Output	Parallel pixel data output (LSB)
DOUT1	H2	Output	Parallel pixel data output.
DOUT2	H3	Output	Parallel pixel data output.
DOUT3	H4	Output	Parallel pixel data output.
RESET_BAR	H8	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
Reserved	E7, E8, F8	n/a	Reserved (do not connect).

Figure 7: 48 iLCC Package, Parallel Output

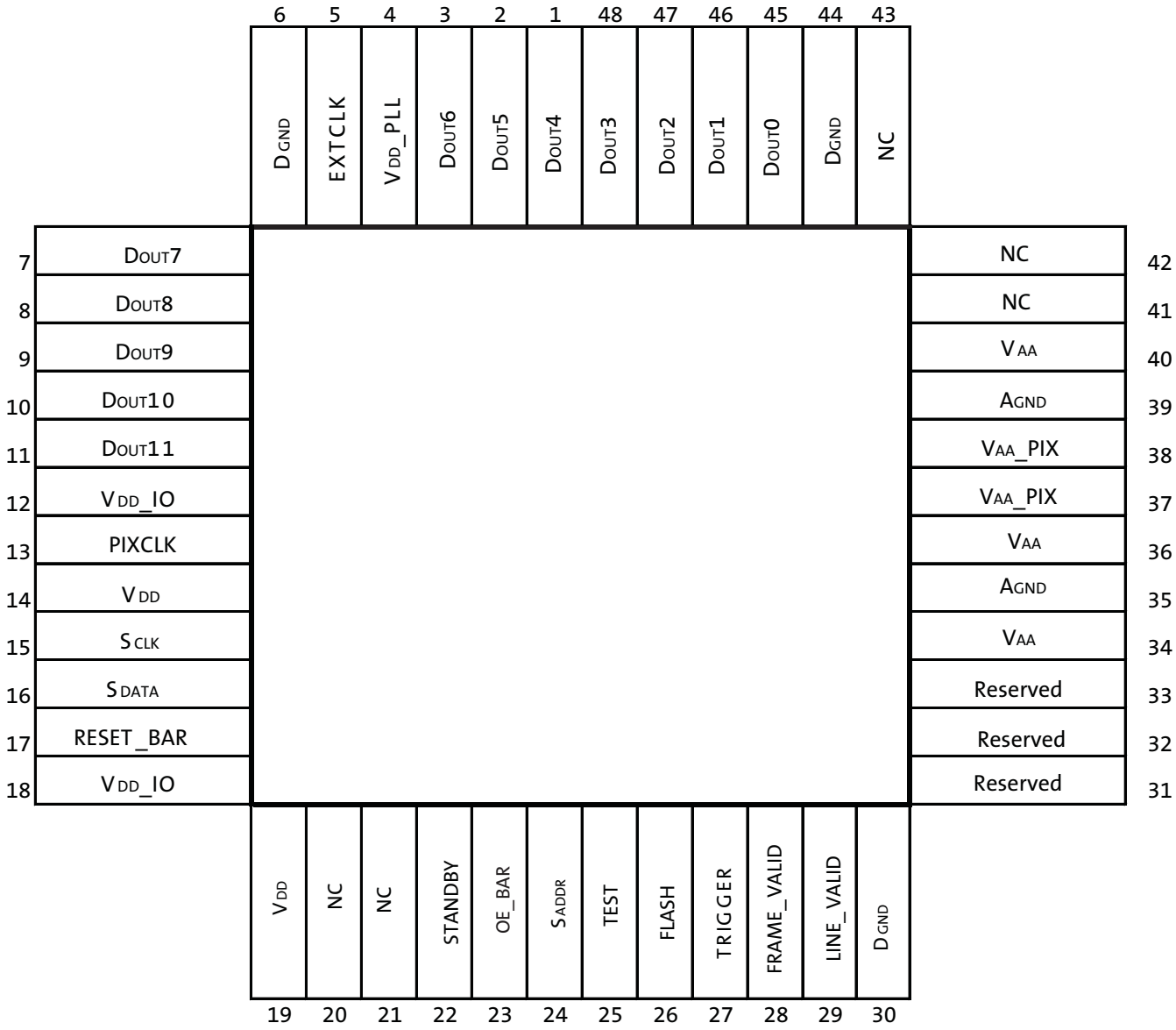


Table 4: Pin Descriptions - 48 iLCC Package, Parallel

Pin Number	Name	Type	Description
1	DOUT4	Output	Parallel pixel data output.
2	DOUT5	Output	Parallel pixel data output.
3	DOUT6	Output	Parallel pixel data output.
4	VDD_PLL	Power	PLL power.
5	EXTCLK	Input	External input clock.
6	DGND	Power	Digital ground.
7	DOUT7	Output	Parallel pixel data output.
8	DOUT8	Output	Parallel pixel data output.
9	DOUT9	Output	Parallel pixel data output.
10	DOUT10	Output	Parallel pixel data output.
11	DOUT11	Output	Parallel pixel data output (MSB).
12	VDD_IO	Power	I/O supply power.
13	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.
14	VDD	Power	Digital power.
15	SCLK	Input	Two-Wire Serial clock input.
16	SDATA	I/O	Two-Wire Serial data I/O.
17	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
18	VDD_IO	Power	I/O supply power.
19	VDD	Power	Digital power.
20	NC		No connection.
21	NC		No connection.
22	STANDBY	Input	Standby-mode enable pin (active HIGH).
23	OE_BAR	Input	Output enable (active LOW).
24	SADDR	Input	Two-Wire Serial address select.
25	TEST	Input	Manufacturing test enable pin (connect to DGND).
26	FLASH	Output	Flash output control.
27	TRIGGER	Input	Exposure synchronization input.
28	FRAME_VALID	Output	Asserted when DOUT frame data is valid.
29	LINE_VALID	Output	Asserted when DOUT line data is valid.
30	DGND	Power	Digital ground
31	Reserved	n/a	Reserved (do not connect).
32	Reserved	n/a	Reserved (do not connect).
33	Reserved	n/a	Reserved (do not connect).
34	VAA	Power	Analog power.
35	AGND	Power	Analog ground.
36	VAA	Power	Analog power.
37	VAA_PIX	Power	Pixel power.
38	VAA_PIX	Power	Pixel power.
39	AGND	Power	Analog ground.
40	VAA	Power	Analog power.
41	NC		No connection.
42	NC		No connection.
43	NC		No connection.
44	DGND	Power	Digital ground.
45	DOUT0	Output	Parallel pixel data output (LSB)
46	DOUT1	Output	Parallel pixel data output.

Table 4: Pin Descriptions (continued)- 48 iLCC Package, Parallel

Pin Number	Name	Type	Description
47	DOUT2	Output	Parallel pixel data output.
48	DOUT3	Output	Parallel pixel data output.

Two-Wire Serial Register Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0134.The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR0134 uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0134 are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the SADDR input.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

This sequence (Figure 8 on page 18) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 8 shows how the internal register address maintained by the AR0134 is loaded and incremented as the sequence proceeds.

Figure 8: Single READ from Random Location

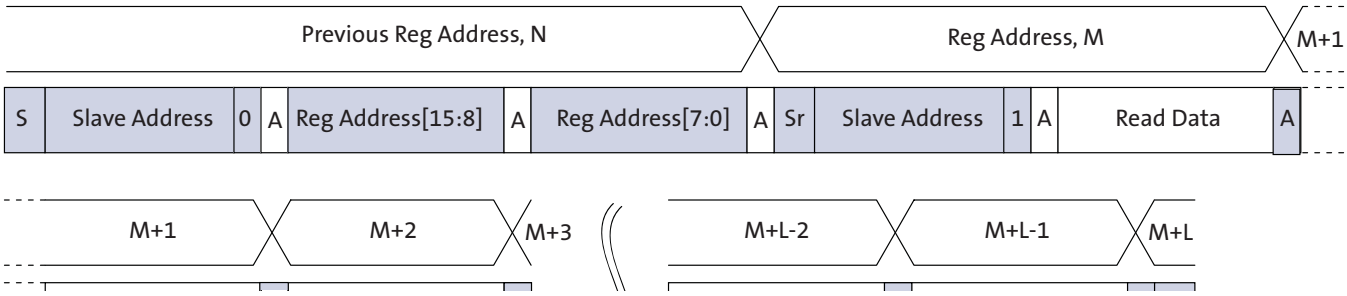
Single READ from Current Location

This sequence (Figure 9) performs a read using the current value of the AR0134 internal

Sequential READ, Start from Random Location

This sequence (Figure 10) starts in the same way as the single READ from random location (Figure 8). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

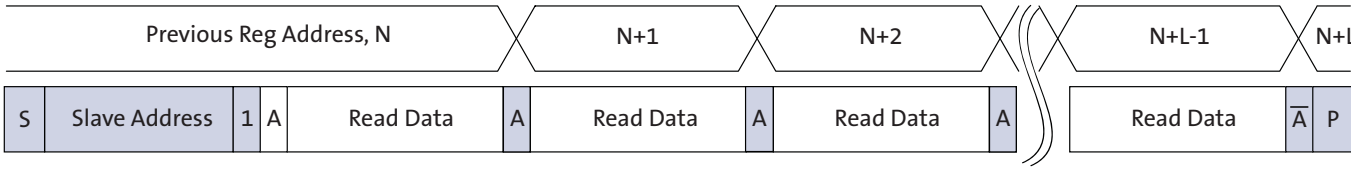
Figure 10: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 11) starts in the same way as the single READ from current location (Figure 9 on page 18). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

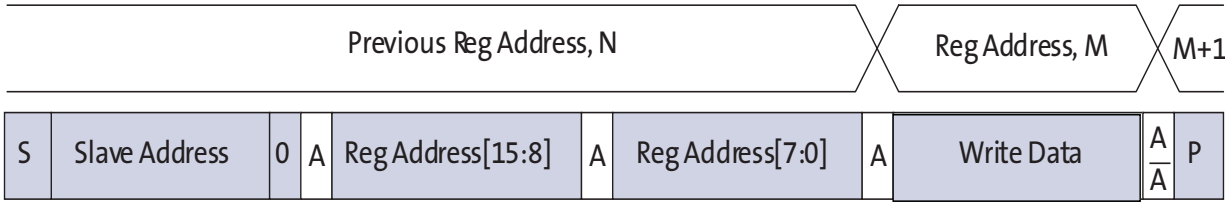
Figure 11: Sequential READ, Start from Current Location



Single WRITE to Random Location

This sequence (Figure 12) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

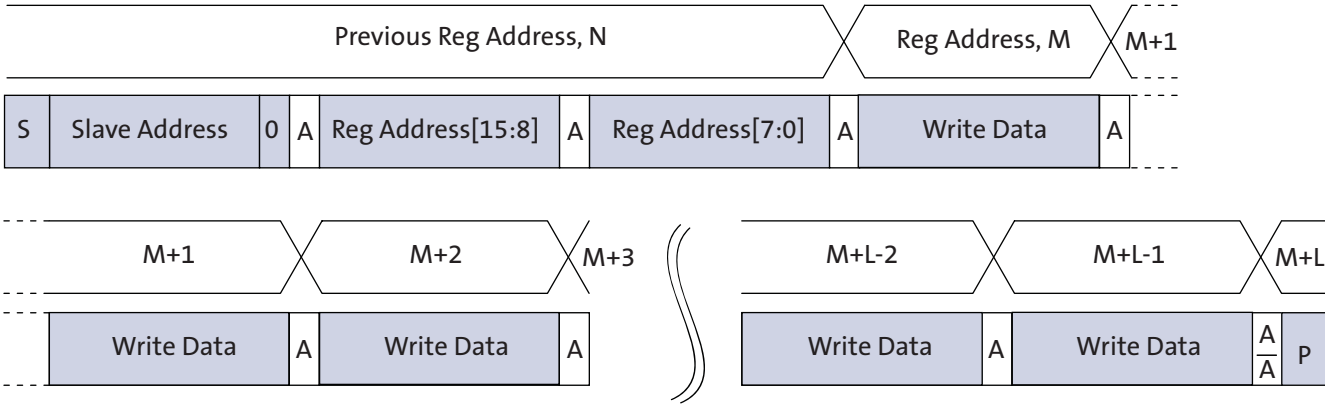
Figure 12: Single WRITE to Random Location



Sequential WRITE, Start at Random Location

This sequence (Figure 13) starts in the same way as the single WRITE to random location (Figure 12). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 13: Sequential WRITE, Start at Random Location



Electrical Specifications

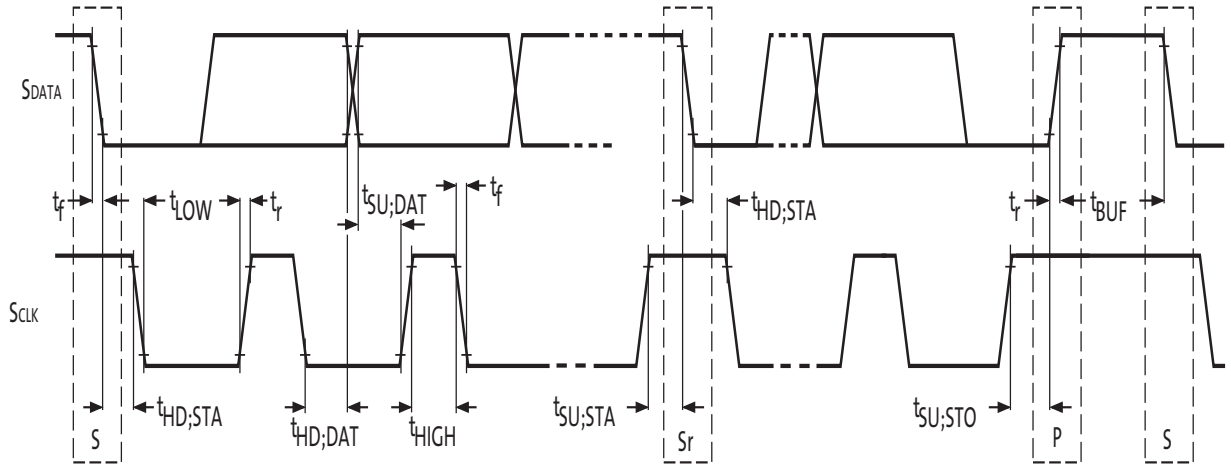
Unless otherwise stated, the following specifications apply to the following conditions:

VDD = 1.8V – 0.10/+0.15; VDD_IO = VDD_PLL = VAA = VAA_PIX = 2.8V ± 0.3V; VDD_SLVS = 0.4V – 0.1/+0.2; T_A = -30°C to +70°C; output load = 10pF; PIXCLK frequency = 74.25 MHz; HiSPi off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 14 and Table 5.

Figure 14: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 5: Two-Wire Serial Bus Characteristics

fEXTCLK = 27 MHz; VDD = 1.8V; VDD_IO = 2.8V; VAA = 2.8V; VAA_PIX = 2.8V; VDD_PLL = 2.8V; VDD_DAC = 2.8V; T_A = 25°C

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	fSCL	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	tHD;STA	4.0	-	0.6	-	µS
LOW period of the SCLK clock	tLOW	4.7	-	1.3	-	µS
HIGH period of the SCLK clock	tHIGH	4.0	-	0.6	-	µS
Set-up time for a repeated START condition	tSU;STA	4.7	-	0.6	-	µS
Data hold time:	tHD;DAT	0[4]	3.45[5]	0[6]	0.9[5]	µS
Data set-up time	tSU;DAT	250	-	100[6]	-	nS
Rise time of both SDATA and SCLK signals	tr	-	1000	20 + 0.1Cb[7]	300	nS
Fall time of both SDATA and SCLK signals	tf	-	300	20 + 0.1Cb[7]	300	nS
Set-up time for STOP condition	tSU;STO	4.0	-	0.6	-	µS

Table 5: Two-Wire Serial Bus Characteristics

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8V; V_{DD}_IO = 2.8V; V_{AA} = 2.8V; V_{AA}_PIX = 2.8V; V_{DD}_PLL = 2.8V; V_{DD}_DAC = 2.8V; T_A = 25°C

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
Bus free time between a STOP and START condition	^{t}BUF	4.7	-	1.3	-	µS
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	CIN_SI	-	3.3	-	3.3	pF
SDATA max load capacitance	CLOAD_SD	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

Notes:
1. This table is based on I^{2}C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I^{2}C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
6. A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0134 launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV and LV using the rising edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028. See Figure 15 and Table 6 for I/O timing (AC) characteristics.

Figure 15: I/O Timing Diagram

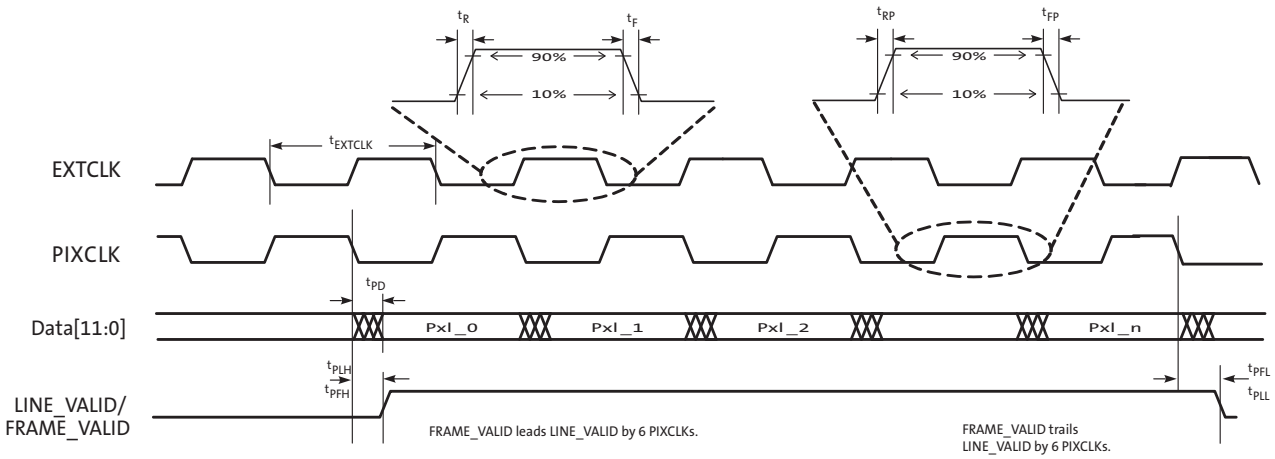


Table 6: I/O Timing Characteristics, Parallel Output (1.8V VDD_IO)[1]

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input clock frequency		6		50	MHz
t_{EXTCLK}	Input clock period		20		166	ns
t_R	Input clock rise time	PLL enabled		3		ns
t_F	Input clock fall time	PLL enabled		3		ns
t_{JITTER}	Input clock jitter				600	ns
t_{CP}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL disabled, PIXCLK slew rate = 4	5.7		14.3	ns
t_{RP}	PIXCLK rise time	PCLK slew rate = 6	1.3		4.0	ns
t_{FP}	PIXCLK fall time	PCLK slew rate = 6	1.3		3.9	ns
	PIXCLK duty cycle		40	50	60	%
f_{PIXCLK}	PIXCLK frequency	PIXCLK slew rate = 6, Data slew rate = 7	6		74.25	MHz
t_{PD}	PIXCLK to data valid	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-3		1.5	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-3		1.5	ns
CIN	Input pin capacitance			2.5		pf

Notes: 1. Minimum and maximum values are taken at 70°C, 1.7V and -30°C, 1.95V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 7: I/O Timing Characteristics, Parallel Output (2.8V V_{DD}_IO)[1]

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input clock frequency		6		50	MHz
t_{EXTCLK}	Input clock period		20		166	ns
t_R	Input clock rise time	PLL enabled		3		ns
t_F	Input clock fall time	PLL enabled		3		ns
$t_{jJITTER}$	Input clock jitter				600	ns
t_{cp}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL disabled, PIXCLK slew rate = 4	5.3		13.4	ns
t_{RP}	PIXCLK rise time	PCLK slew rate = 6	1.3		4.0	ns
t_{FP}	PIXCLK fall time	PCLK slew rate = 6	1.3		3.9	ns
	PIXCLK duty cycle		40	50	60	%
f_{PIXCLK}	PIXCLK frequency	PIXCLK slew rate = 6, Data slew rate = 7	6		74.25	MHz
t_{PD}	PIXCLK to data valid	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
C_{IN}	Input pin capacitance			2.5		pf

Notes: 1. Minimum and maximum values are taken at 70°C, 1.7V and -30°C, 1.95V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 8: I/O Rise Slew Rate (2.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.50	2.50	3.90	V/ns
6	Default	0.98	1.62	2.52	V/ns
5	Default	0.71	1.12	1.79	V/ns
4	Default	0.52	0.82	1.26	V/ns
3	Default	0.37	0.58	0.88	V/ns
2	Default	0.26	0.40	0.61	V/ns
1	Default	0.17	0.27	0.40	V/ns
0	Default	0.10	0.16	0.23	V/ns

Note: 1. Minimum and maximum values are taken at 70°C, 2.5V and -30°C, 3.1V. The loading used is 10 pF.

Table 9: I/O Fall Slew Rate (2.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.40	2.30	3.50	V/ns
6	Default	0.97	1.61	2.48	V/ns
5	Default	0.73	1.21	1.86	V/ns
4	Default	0.54	0.88	1.36	V/ns
3	Default	0.39	0.63	0.88	V/ns
2	Default	0.27	0.43	0.66	V/ns
1	Default	0.18	0.29	0.44	V/ns
0	Default	0.11	0.17	0.25	V/ns

Note: 1. Minimum and maximum values are taken at 70°C, 2.5V and -30°C, 3.1V. The loading used is 10 pF.

Table 10: I/O Rise Slew Rate (1.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.57	0.91	1.55	V/ns
6	Default	0.39	0.61	1.02	V/ns
5	Default	0.29	0.46	0.75	V/ns
4	Default	0.22	0.34	0.54	V/ns
3	Default	0.16	0.24	0.39	V/ns
2	Default	0.12	0.17	0.27	V/ns
1	Default	0.08	0.11	0.18	V/ns
0	Default	0.05	0.07	0.10	V/ns

Note: 1. Minimum and maximum values are taken at 70°C, 1,7V and -30°C, 1.95V. The loading used is 10 pF.

Table 11: I/O Fall Slew Rate (1.8V V_{DD}_IO)[1]

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.57	0.92	1.55	V/ns
6	Default	0.40	0.64	1.08	V/ns
5	Default	0.31	0.50	0.82	V/ns
4	Default	0.24	0.38	0.61	V/ns
3	Default	0.18	0.27	0.44	V/ns
2	Default	0.13	0.19	0.31	V/ns
1	Default	0.09	0.13	0.20	V/ns
0	Default	0.05	0.08	0.12	V/ns

Notes: 1. Minimum and maximum values are taken at 70°C, 1.7V and -30°C, 1.95V. The loading used is 10 pF.

DC Electrical Characteristics

The DC electrical characteristics are shown in Table 12, Table 13, Table 14, and Table 15.

Table 12: DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.95	V
V_{DD_IO}	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.5	2.8	3.1	V
V_{DD_SLVS}	HiSPi supply voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH voltage		V_{DD_IO} * 0.7	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{DD_IO} * 0.3	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	20	–	–	µA
V_{OH}	Output HIGH voltage		V_{DD_IO} – 0.3	–	–	V
V_{OL}	Output LOW voltage	V_{DD_IO} = 2.8V	–	–	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	–22	–	–	mA
I_{OL}	Output LOW current	At specified V_{OL}	–	–	22	mA

Caution **Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
V_{SUPPLY}	Power supply voltage (all supplies)	–0.3	4.5	V	V_{SUPPLY}
I_{SUPPLY}	Total power supply current	–	200	mA	I_{SUPPLY}
I_{GND}	Total ground current	–	200	mA	I_{GND}
V_{IN}	DC input voltage	–0.3	V_{DD_IO} + 0.3	V	V_{IN}
V_{OUT}	DC output voltage	–0.3	V_{DD_IO} + 0.3	V	V_{OUT}
T_{STG}[1]	Storage temperature	–40	+85	°C	T_{STG}[1]

Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 14: Operating Current Consumption for Parallel Output

V_{AA} = V_{AA_PIX} = V_{DD_IO} = V_{DD_PLL} = 2.8V; V_{DD}= 1.8V; PLL Enabled and PIXCLK = 74.25 MHz; T_A = 25°C; C_{LOAD} = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	Parallel, Streaming, Full resolution 54 fps	I_{DD1}		46	60	mA
I/O digital operating current	Parallel, Streaming, Full resolution 54 fps	I_{DD_IO}		52	–	mA
Analog operating current	Parallel, Streaming, Full resolution 54 fps	I_{AA}		46	55	mA
Pixel supply current	Parallel, Streaming, Full resolution 54 fps	I_{AA_PIX}		7	9	mA
PLL supply current	Parallel, Streaming, Full resolution 54 fps	I_{DD_PLL}		8	10	mA

Table 15: Standby Current Consumption
Analog - V_{AA} + V_{AA_PIX} + V_{DD_PLL}; Digital - V_{DD} + V_{DD_IO}; T_A = 25°C

Definition	Condition	Min	Typ	Max	Unit
Hard standby (clock off, driven low)	Analog, 2.8V	–	3	15	µA
	Digital, 1.8V	–	25	80	µA
Hard standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V	–	12	25	µA
	Digital, 1.8V	–	1.1	1.7	mA
Soft standby (clock off, driven low)	Analog, 2.8V	–	3	15	µA
	Digital, 1.8V	–	25	80	µA
Soft standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V	–	12	25	µA
	Digital, 1.8V	–	1.1	1.7	mA

HiSPi Electrical Specifications

The Aptina AR0134 sensor supports SLVS mode only, and does not have a DLL for timing adjustments. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The V_{DD_SLVS} supply in this data sheet corresponds to V_{DD_TX} in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD_HiSPi} as referenced in the specification. The HiSPi transmitter electrical specifications are listed at 700 MHz.

Table 16: Input Voltage and Current (HiSPi Power Supply 0.4 V)
Measurement Conditions: Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Supply current (P_{WR}HiSPi) (driving 100Ω load)	I_{DD_SLVS}	–	10	15	mA
HiSPi common mode voltage (driving 100Ω load)	V_{CMD}	V_{DD_SLVS} x 0.45	V_{DD_SLVS}/2	V_{DD_SLVS} x 0.55	V
HiSPi differential output voltage (driving 100Ω load)	$\|V_{OD}\|$	V_{DD_SLVS} x 0.36	V_{DD_SLVS}/2	V_{DD_SLVS} x 0.64	V
Change in V_{CM} between logic 1 and 0	ΔV_{CM}			25	mV
Change in $\|V_{OD}\|$ between logic 1 and 0	$\|V_{OD}\|$			25	mV
Vod noise margin	NM	–		30	%
Difference in V_{CM} between any two channels	$\|\Delta V_{CM}\|$			50	mV
Difference in V_{OD} between any two channels	$\|\Delta V_{OD}\|$			100	mV
Common-mode AC voltage (pk) without V_{CM} cap termination	ΔV_{CM_ac}			50	mV
Common-mode AC voltage (pk) with V_{CM} cap termination	ΔV_{CM_ac}			30	mV
Max overshoot peak $\|V_{OD}\|$	V_{OD_ac}			1.3 x $\|V_{OD}\|$	V
Max overshoot Vdiff pk-pk	V_{diff_pkpk}			2.6 x $\|V_{OD}\|$	V
Eye Height	V_{eye}	1.4 x V_{OD}			
Single-ended output impedance	Ro	35	50	70	Ω
Output impedance mismatch	ΔRo			20	%

Figure 16: Differential Output Voltage for Clock or Data Pairs

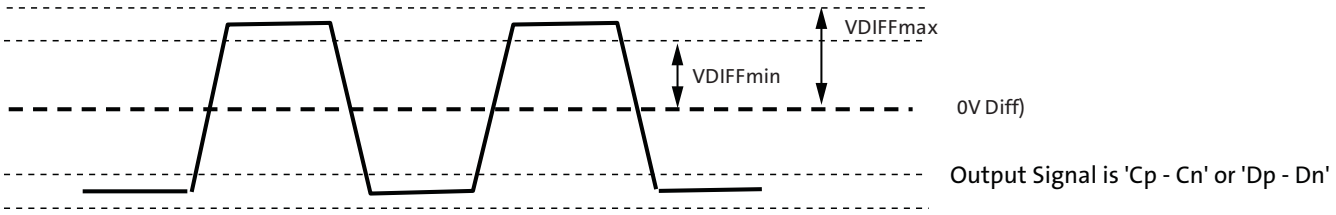


Table 17: Rise and Fall Times
Measurement Conditions: HiSPi Power Supply 0.4V, Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	1/UI	280	–	700	Mb/s
Max setup time from transmitter	TxPRE	0.3	–	–	UI[1]
Max hold time from transmitter	TxPost	0.3	–	–	UI
Rise time (20% - 80%)	RISE	–	0.25UI	–	
Fall time (20% - 80%)	FALL	150ps	0.25 UI	–	
Clock duty	PLL_DUTY	45	50	55	%
Bitrate Period	t_{pw}	1.43		3.57	ns[1]
Eye Width	t_{eye}	0.3			UI[1, 2]
Data Total jitter (pk pk)@1e-9	$t_{totaljit}$			0.2	UI[1, 2]
Clock Period Jitter (RMS)	t_{ckjit}			50	ps[2]
Clock cycle to cycle jitter (RMS)	t_{cyjit}			100	ps[2]
Clock to Data Skew	t_{chskew}	-0.1		0.1	UI[1, 2]
PHY-to-PHY Skew	$t_{\|PHYskew\|}$			2.1	UI[1, 5]
Mean differential skew	$t_{DIFFSKEW}$	–100		100	ps[6]

Notes:
1. One UI is defined as the normalized mean time between one edge and the following edge of the clock.
2. Taken from 0V crossing point.
3. Also defined with a maximum loading capacitance of 10pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3UI.
4. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.
5. The absolute mean skew between any Clock in one PHY and any Data lane in any other PHY between any edges.
6. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean VCM point.

Figure 17: Eye Diagram for Clock and Data Signals

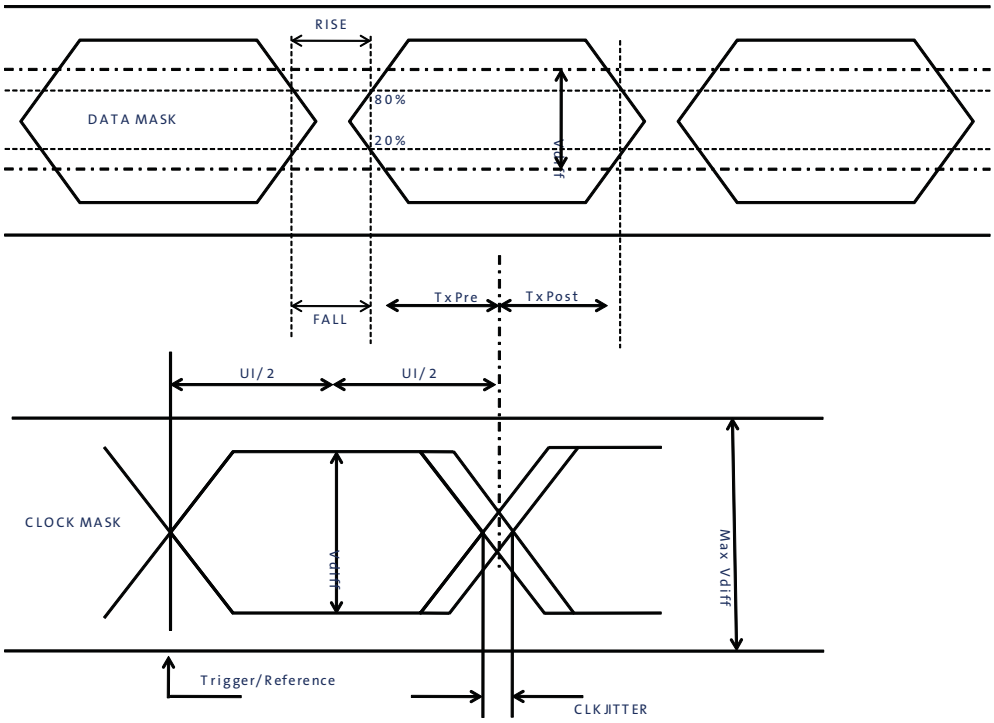
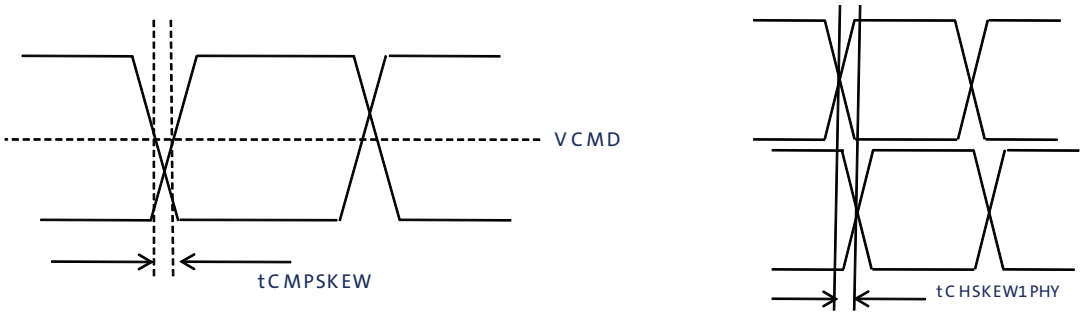


Figure 18: Skew Within the PHY and Output Channels



Power-On Reset and Standby Timing

Power-Up Sequence

The recommended power-up sequence for the AR0134 is shown in Figure 19. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply.
2. After 0–10µs, turn on VAA and VAA_PIX power supply.
3. After 0–10µs, turn on VDD_IO power supply.
4. After the last power supply is stable, enable EXTCLK.
5. If RESET_BAR is in a LOW state, hold RESET_BAR LOW for at least 1ms.
   If RESET_BAR is in a HIGH state, assert RESET_BAR for at least 1ms.
6. Wait 160000 EXTCLKs (for internal initialization into software standby).
7. Configure PLL, output, and image settings to desired values.
8. Wait 1ms for the PLL to lock.
9. Set streaming mode (R0x301a[2] = 1).

Figure 19: Power Up

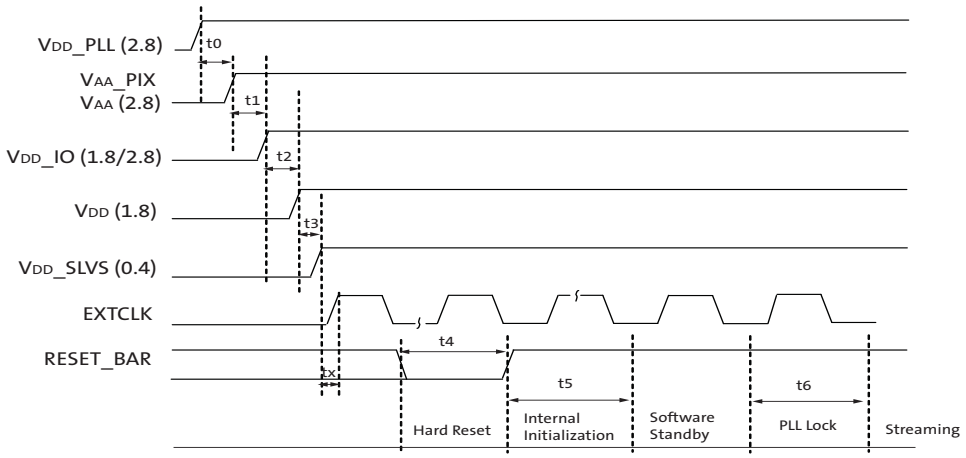


Table 18: Power-Up Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX	t0	0	10	–	µs
VAA/VAA_PIX to VDD_IO	t1	0	10	–	µs
VDD_IO to VDD	t2	0	10	–	µs
VDD to VDD_SLVS	t3	0	10	–	µs
Xtal settle time	tx	–	30[1]	–	ms
Hard Reset	t4	1[2]	–	–	ms
Internal Initialization	t5	160000	–	–	EXTCLKs
PLL Lock Time	t6	1	–	–	ms

Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after

other supplies then the sensor may have functionality issues and will experience high current draw on this supply.

Power-Down Sequence

The recommended power-down sequence for the AR0134 is shown in Figure 20. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off VDD_SLVS.
4. Turn off VDD.
5. Turn off VDD_IO
6. Turn off VAA/VAA_PIX.
7. Turn off VDD_PLL.

Figure 20: Power Down

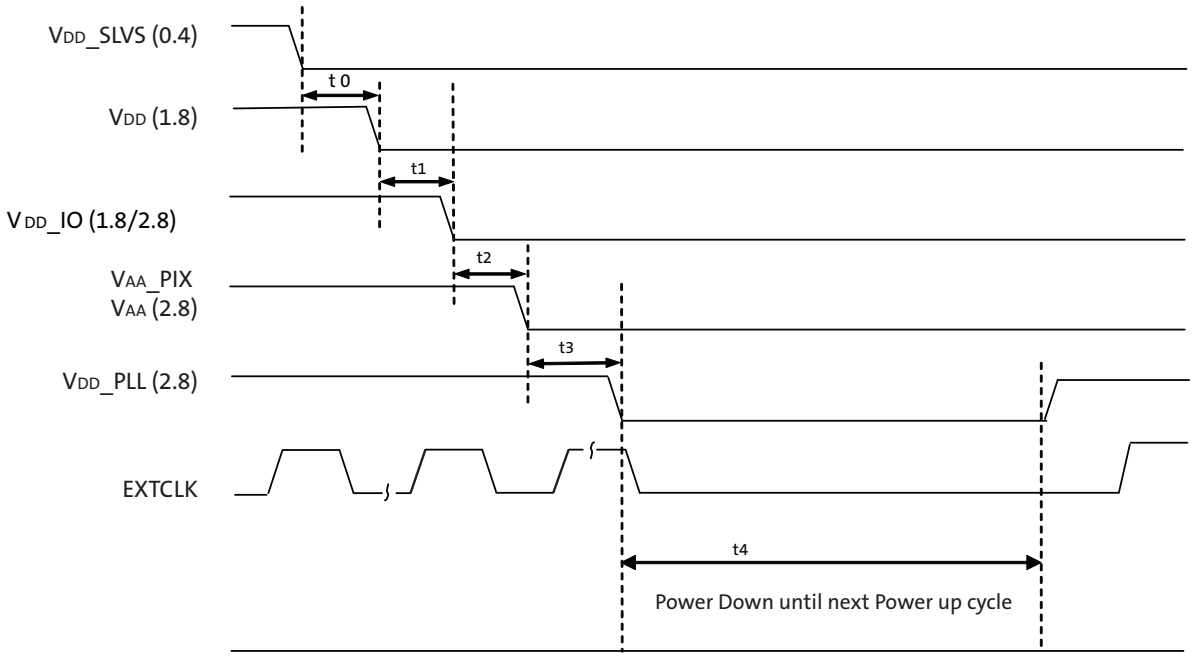


Table 19: Power-Down Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_SLVS to VDD	t0	0	–	–	µS
VDD to VDD_IO	t1	0	–	–	µS
VDD_IO to VAA/VAA_PIX	t2	0	–	–	µS
VAA/VAA_PIX to VDD_PLL	t3	0	–	–	µS
PwrDn until Next PwrUp Time	t4	100	–	–	mS

Note: t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

Standby Sequence

Figures 21 and 22 show timing diagrams for entering and exiting standby. Delays are shown indicating the last valid register write prior to entering standby as well as the first valid write upon exiting standby. Also shown is timing if the EXTCLK is to be disabled during standby.

Figure 21: Enter Standby Timing

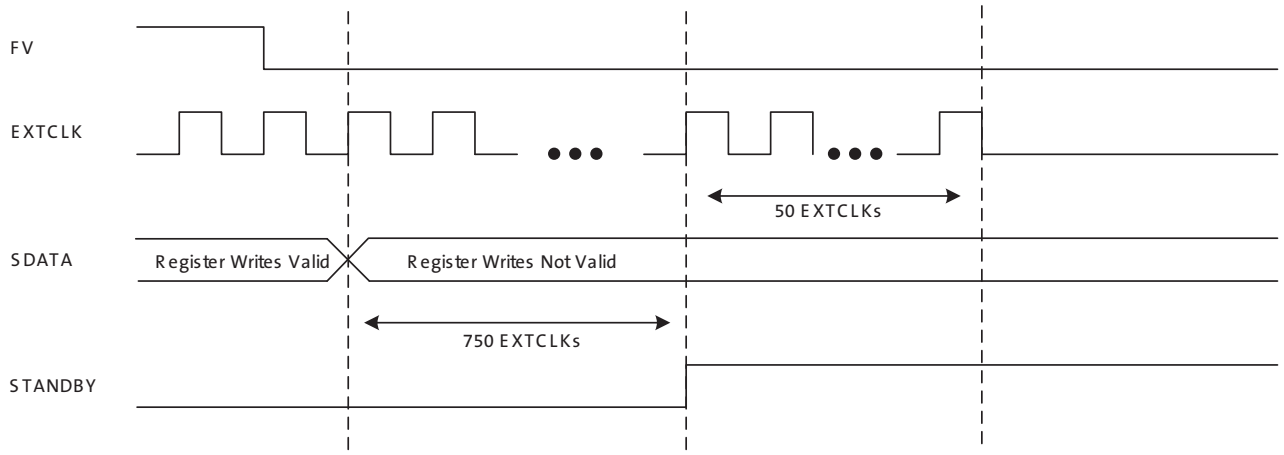


Figure 22: Exit Standby Timing

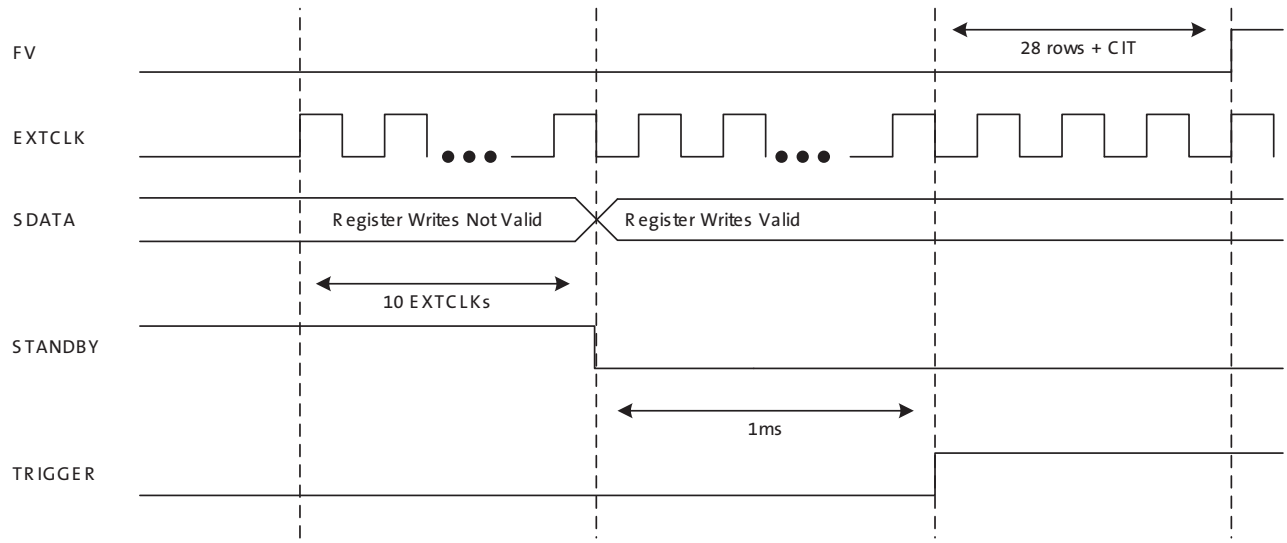


Figure 23: Quantum Efficiency – Monochrome Sensor (Typical)

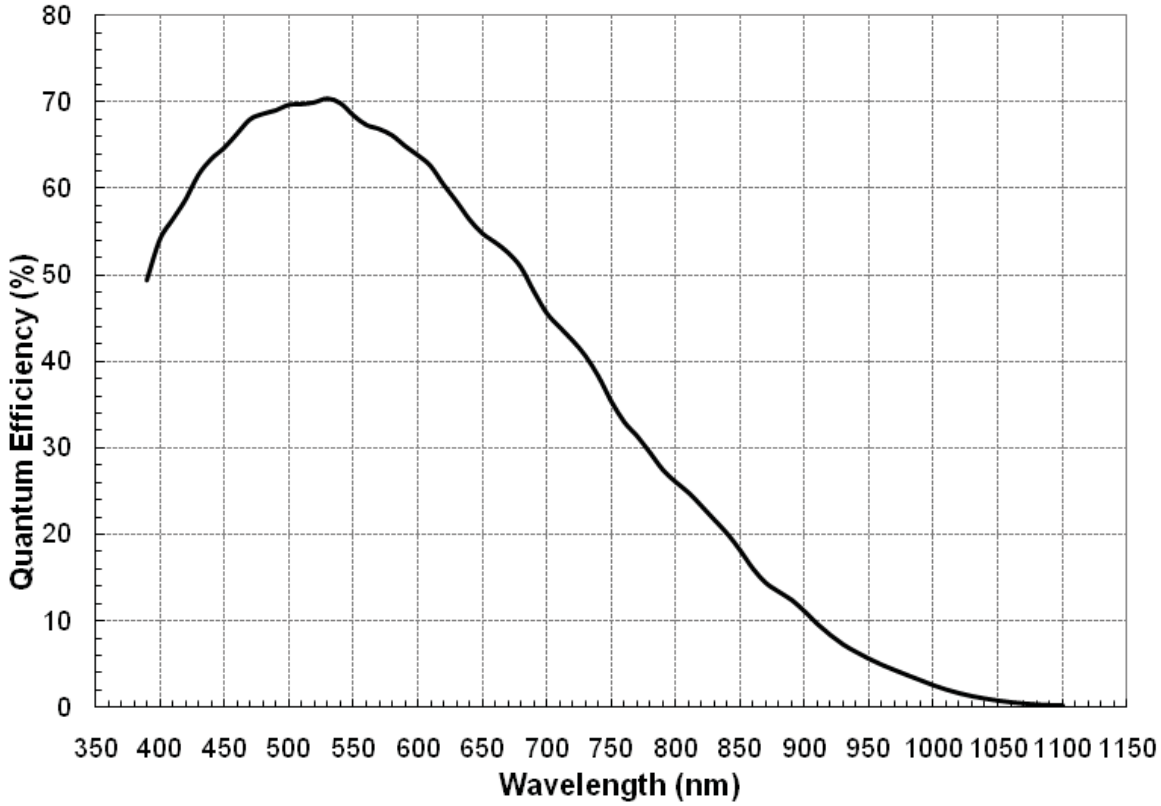


Figure 24: Quantum Efficiency – Color Sensor (Typical)

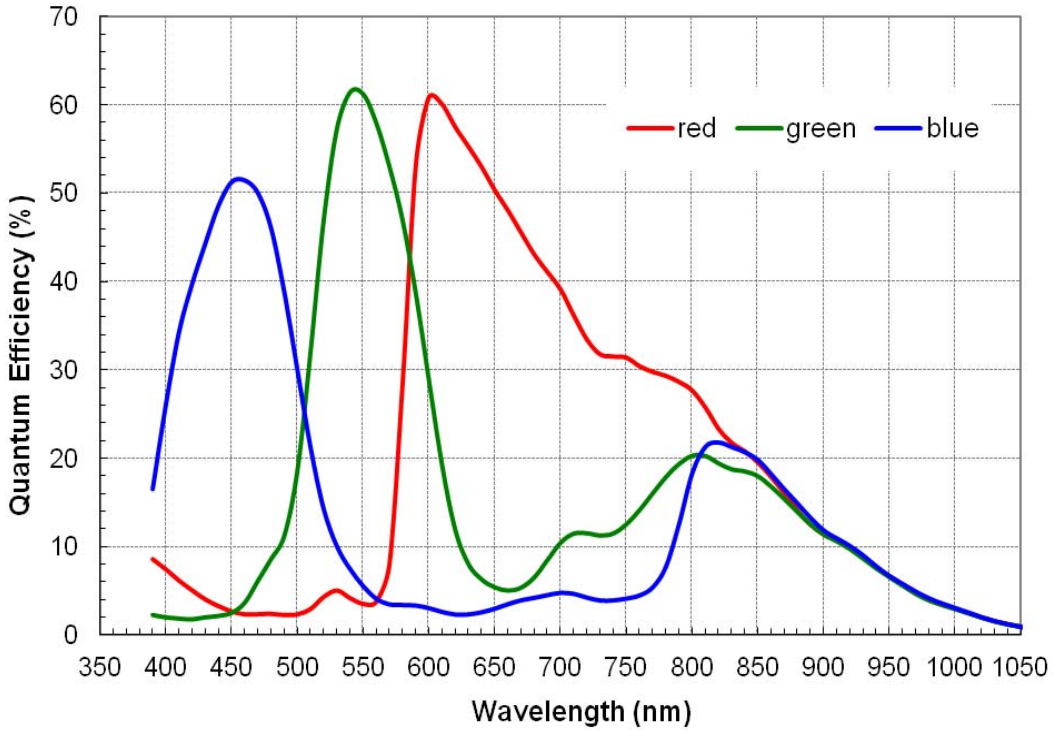


Table 20: Chief Ray Angle - 25deg Mono

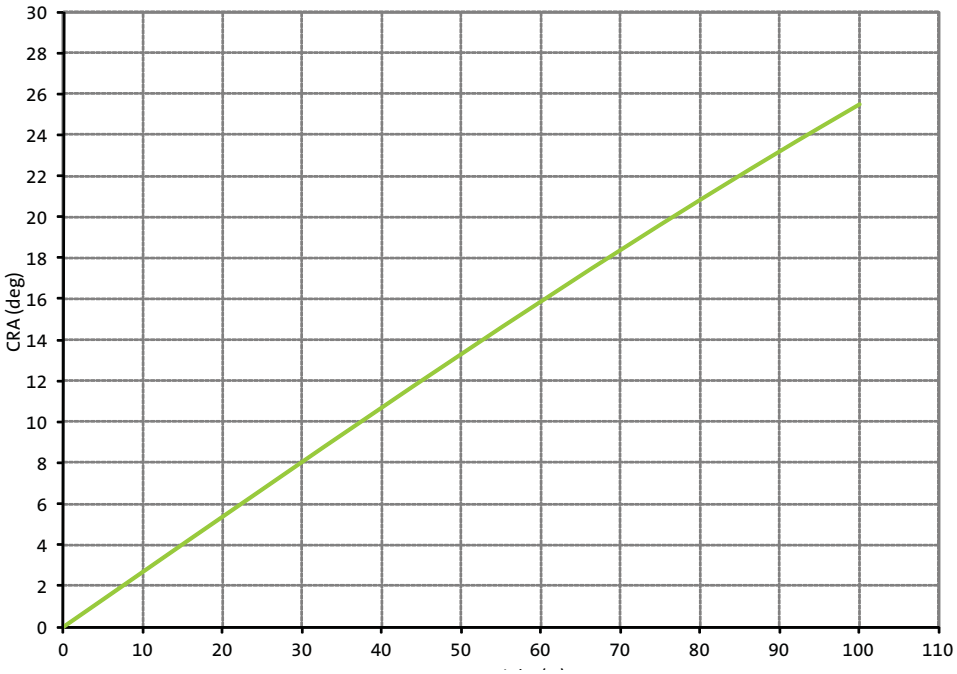
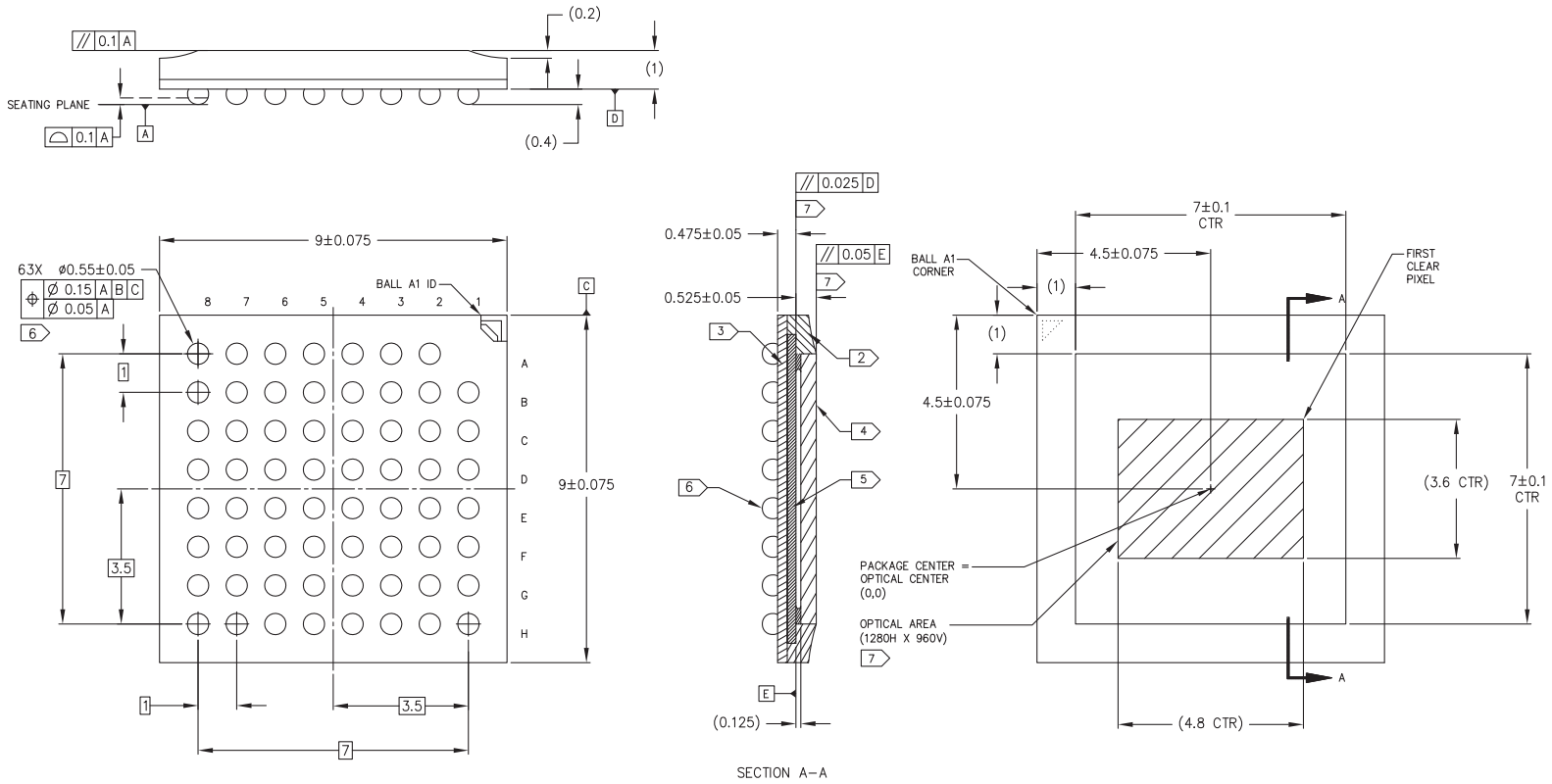


Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.150	1.35
10	0.300	2.70
15	0.450	4.04
20	0.600	5.39
25	0.750	6.73
30	0.900	8.06
35	1.050	9.39
40	1.200	10.71
45	1.350	12.02
50	1.500	13.33
55	1.650	14.62
60	1.800	15.90
65	1.950	17.16
70	2.100	18.41
75	2.250	19.64
80	2.400	20.85
85	2.550	22.05
90	2.700	23.22
95	2.850	24.38
100	3000	25.51

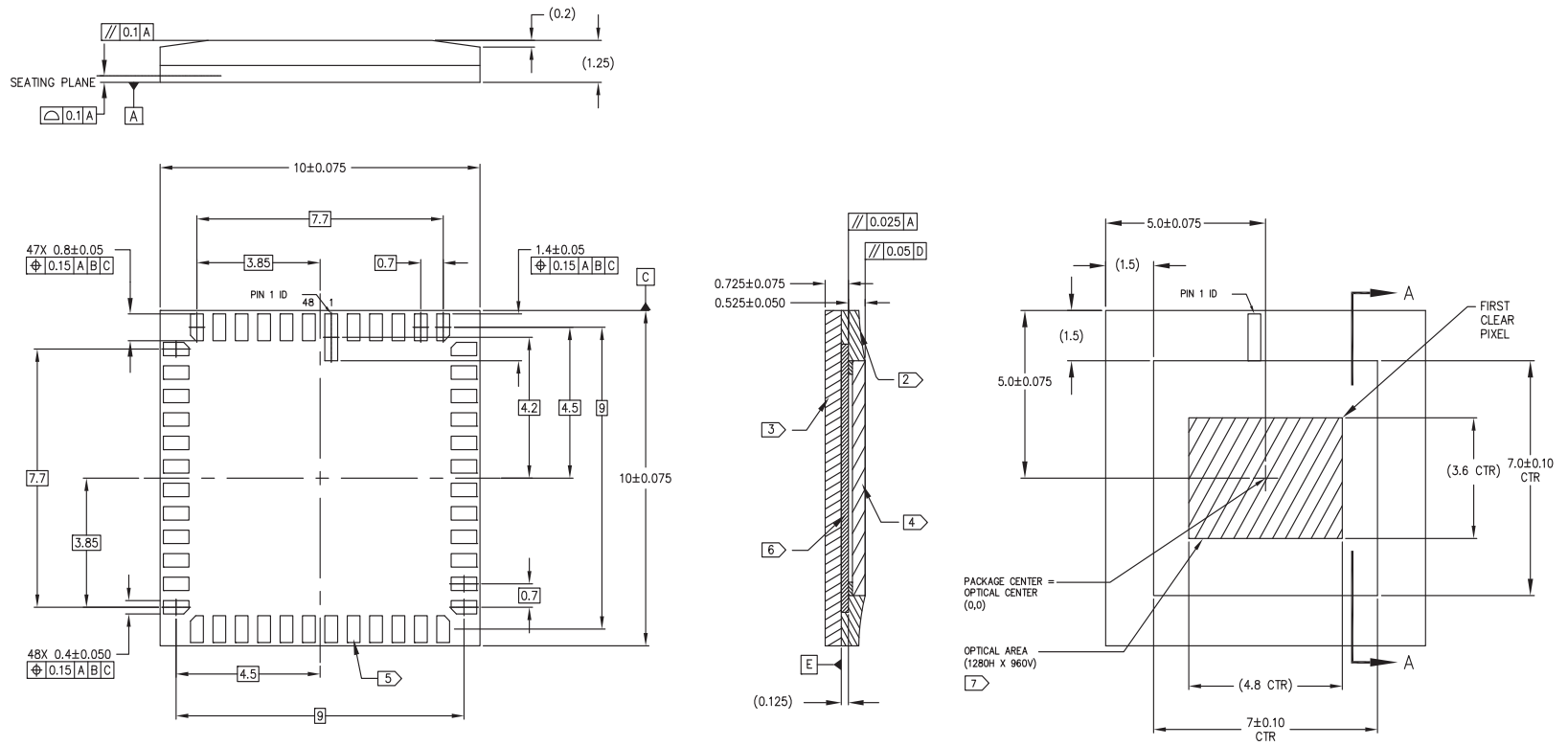
Package Dimensions

Figure 25: 63-Ball iBGA Package Outline Drawing



Notes:
1. Dimensions in mm. Dimensions in () are for reference only.
2. Encapsulant: Epoxy.
3. Substrate material: Plastic laminate 0.25 thickness.
4. Lid material: Borosilicate glass 0.4 ± 0.04 thickness.
   Refractive index at 20C = 1.5255 @ 546nm and 1.5231 @ 588nm.
   Double side AR Coating: 530-570nm R< 1%; 420-700nm R < 2%.
5. Image sensor die: 0.2mm thickness.
6. Solder ball material: SAC305 (95% Sn, 3% Ag, 0.5% Cu).
   Dimensions apply to solder balls post reflow.
   Pre-flow ball is0.5 on a Ø0.4 SMD ball pad.
7. Maximum rotation of optical area relative to package edges: 1°.
   Maximum tilt of optical area relative to substrate plane D : 25 µm.
   Maximum tilt of cover glass relative to optical area plane E : 50 µm.

Figure 26: 48-pin iLCC Package Drawing



Notes:
1. Dimensions in mm. Dimensions in () are for reference only.
2. Encapsulant: Epoxy.
3. Substrate material: Plastic laminate 0.5 thickness.
4. Lid material: Borosilicate glass 0.4 ± 0.04 thickness.
   Refractive index at 20C = 1.5255 @ 546nm and 1.5231 @ 588nm.
   Double side AR Coating: 530-570nm R< 1%; 420-700nm R < 2%.
5. Lead finish: Gold plating, 0.5 microns minimum thickness.
6. Image sensor die: 0.2mm thickness.
7. Maximum rotation of optical area relative to package edges: 1°.
   Maximum tilt of optical area relative to substrate plane D : 25 µm.
   Maximum tilt of cover glass relative to optical area plane E : 50 µm.

Revision History

Rev. D 6/13/14

- Updated Table 1, “Key Parameters,” on page 1
- Updated Figure 4: “Typical Configuration: Serial Four-Lane HiSPi Interface,” on page 9
- Updated Figure 6: “9x9mm 63-Ball iBGA Package,” on page 11
- Updated Table 5, “Two-Wire Serial Bus Characteristics,” on page 21
- Updated Table 6, “I/O Timing Characteristics, Parallel Output (1.8V VDD_IO)[1],” on page 23
- Updated Table 7, “I/O Timing Characteristics, Parallel Output (2.8V VDD_IO)[1],” on page 24
- Updated “Two-Wire Serial Register Interface” on page 16
- Split Table 6 and updated values in Table 8, “I/O Rise Slew Rate (2.8V VDD_IO)[1],” on page 25 and Table 9, “I/O Fall Slew Rate (2.8V VDD_IO)[1],” on page 25
- Updated “Power-Up Sequence” on page 31
- Updated Figure 19: “Power Up,” on page 31
- Updated Figure 25: “63-Ball iBGA Package Outline Drawing,” on page 37
- Updated Figure 26: “48-pin iLCC Package Drawing,” on page 38

Rev. C 6/13/13

- Updated to Production
- Applied updated Aptina template
- Updated “General Description” on page 1
- Updated Table 1, “Key Parameters,” on page 1
- Updated Table 2, “Available Part Numbers,” on page 1
- Updated “Features Overview” on page 6
- Added “Pixel Data Format” on page 7
- Updated Table 6, “I/O Timing Characteristics, Parallel Output (1.8V VDD_IO)[1],” on page 23
- Updated Table 7, “I/O Rise Slew Rate (2.8V Vdd_IO)1,” on page 23
- Updated Table 8, “I/O Fall Slew Rate (2.8V Vdd_IO)1,” on page 23
- Updated Table 9, “I/O Rise Slew Rate (1.8V Vdd_IO)1,” on page 23
- Added “Two-Wire Serial Register Interface” on page 16
- Added “Standby Sequence” on page 33
- Added Table 20, “Chief Ray Angle - 25deg Mono,” on page 36

Rev. B 1/23/13

- Updated to Preliminary
- Updated “Features” on page 1
- Updated third paragraph of “General Description” on page 5
- Updated Figure 15: “I/O Timing Diagram,” on page 23
- Updated Table 6, “I/O Timing Characteristics, Parallel Output (1.8V VDD_IO)[1],” on page 23
- Added Figure 21: “Enter Standby Timing,” on page 33
- Added Figure 22: “Exit Standby Timing,” on page 33
- Added Table 7, “I/O Rise Slew Rate (2.8V Vdd_IO)1,” on page 23
- Added Table 8, “I/O Fall Slew Rate (2.8V Vdd_IO)1,” on page 23
- Added Table 9, “I/O Rise Slew Rate (1.8V Vdd_IO)1,” on page 23

- Added Table 10, “I/O Fall Slew Rate (1.8V Vdd_IO)1,” on page 24
- Updated “Power-Up Sequence” on page 31
- Updated Table 18, “Power-Up Sequence,” on page 31
- Added Figure 21: “Enter Standby Timing,” on page 33
- Added Figure 22: “Exit Standby Timing,” on page 33
- Added Figure 23: “Quantum Efficiency – Monochrome Sensor (Typical),” on page 34

Rev. A 9/19/12

- Initial release

180 Clemenceau Avenue, #05-02/04 Haw Par Centre, Singapore 239922 prodmktg@aptina.com www.aptina.com

AR0134 Register Reference, Rev. D

For more information, refer to the data sheet on Aptina's Web site: www.aptina.com

AR0134 Register Reference

Table of Contents

List of Tables

Introduction

This register reference is provided for engineers who are designing cameras that use the AR0134.

Conventions and Notations

This document follows the conventions and notations described below.

- Hexadecimal numbers have a 0x prefix
- Binary numbers have 0b prefix
  Example: 0b1010 = 0xA

Register Address Space

The AR0134 provides a 16-bit register address space accessed through a serial interface. Each register location is 8 or 16 bits in size.

The address space is divided into the five major regions shown in Table 1.

Table 1: Address Space Regions

Address Range	Description
0x0000–0x0FFF	Reserved
0x1000–0x1FFF	Reserved
0x2000–0x2FFF	Reserved
0x3000–0x3FFF	Manufacturer-specific registers (read-only and read-write dynamic registers)
0x4000–0xFFFF	Reserved (undefined)

Register Notation

The underlying mechanism for reading and writing registers provides byte write capability. However, it is convenient to consider some registers as multiple adjacent bytes. The AR0134uses 8-bit, 16-bit, and 32-bit registers, all implemented as 1 or more bytes at naturally aligned, contiguous locations in the address space.

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x3024 is an 8-bit register at address 0x3024, and R0x3000–1 is a 16-bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

Register Aliases

A consequence of the internal architecture of the AR0134 is that some registers are decoded at multiple addresses. Some registers in “configuration space” are also decoded in “manufacturer-specific space.” To provide unique names for all registers, the name of the register within manufacturer-specific register space has a trailing underscore. For example, R0x0000–1 is model_id, and R0x3000–1 is model_id_. The effect of reading or writing a register through any of its aliases is identical.

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the model_id register are referred to as model_id[3:0] or R0x0000–1[3:0].

Bit Field Aliases

In addition to the register aliases described above, some register fields are aliased in multiple places. For example, R0x0100 (mode_select) only has one operational bit, R0x0100[0]. This bit is aliased to R0x301A–B[2]. The effect of reading or writing a bit field through any of its aliases is identical.

Byte Ordering

Registers that occupy more than 1 byte of address space are shown with the lowest address in the highest-order byte lane to match the byte-ordering on the bus. For example, the model_id register is R0x0000–1. In the register table the default value is shown as 0x2600. This means that a READ from address 0x0000 would return 0x26, and a READ from address 0x0001 would return 0x00. When reading this register as two 8-bit transfers on the serial interface, the 0x26 will appear on the serial interface first, followed by the 0x00.

Address Alignment

All register addresses are aligned naturally. Registers that occupy two bytes of address space are aligned to even 16-bit addresses, and registers that occupy four bytes of address space are aligned to 16-bit addresses that are an integer multiple of 4.

Bit Representation

For clarity, 32-bit hex numbers are shown with an underscore between the upper and lower 16 bits. For example: 0x3000_01AB.

Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 2.

Table 2: Data Formats

Name	Description
FIX16	Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = –128, 0xFFFF = –0.0039065
UFIX16	Unsigned fixed-point, 16-bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5
FLP32	Signed floating-point, 32-bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0

Register Behavior

Registers vary from “read-only,” “read/write,” and “read, write-1-to-clear.”

Double-Buffered Registers

Some sensor settings cannot be changed during frame readout. For example, changing x_addr_start partway through frame readout would result in inconsistent row lengths within a frame. To avoid this, the AR0134 double-buffers many registers by implementing a “pending” and a “live” version. READs and WRITEs access the pending register; the live register controls the sensor operation.

The value in the pending register is transferred to a live register at a fixed point in the frame timing, called frame start. Frame start is defined as the point at which the first dark row is read out internally to the sensor. In the register tables the “Buffering” column shows which registers or register fields are single- or double-buffered

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.
Y—Yes. Changing the register value might produce a bad frame.
YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x301A[9]) is set to “1.”

Register Summary Tables

Note: Green1 corresponds to greenR; green2 corresponds to greenB.

Caution **Writing and changing the value of a reserved register (word or bit) puts the device in an unknown state and may damage the device.**

Manufacturer-Specific Registers

Table 3: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288 (R0x3000)	chip_version_reg	dddd dddd dddd dddd	9222 (0x2406)
R12290 (R0x3002)	y_addr_start	0000 00dd dddd dddd	0 (0x0000)
R12292 (R0x3004)	x_addr_start	0000 0ddd dddd dddd	0 (0x0000)
R12294 (R0x3006)	y_addr_end	0000 00dd dddd dddd	959 (0x03BF)
R12296 (R0x3008)	x_addr_end	0000 0ddd dddd dddd	1279 (0x04FF)
R12298 (R0x300A)	frame_length_lines	dddd dddd dddd dddd	990 (0x03DE)
R12300 (R0x300C)	line_length_pck	dddd dddd dddd ddd0	1388 (0x056C)
R12302 (R0x300E)	revision_number	dddd dddd	19 (0x13)
R12306 (R0x3012)	coarse_integration_time	dddd dddd dddd dddd	100 (0x0064)
R12308 (R0x3014)	fine_integration_time	dddd dddd dddd dddd	0 (0x0000)
R12310 (R0x3016)	coarse_integration_time_cb	dddd dddd dddd dddd	16 (0x0010)
R12312 (R0x3018)	fine_integration_time_cb	dddd dddd dddd dddd	0 (0x0000)
R12314 (R0x301A)	reset_register	d00d dddd dddd dddd	4312 (0x10D8)
R12318 (R0x301E)	data_pedestal	0000 dddd dddd dddd	300 (0x012C)
R12326 (R0x3026)	gpi_status	0000 0000 0000 ????	0 (0x0000)
R12328 (R0x3028)	row_speed	0000 0000 0ddd 0000	16 (0x0010)
R12330 (R0x302A)	vt_pix_clk_div	0000 0000 dddd dddd	8 (0x0008)
R12332 (R0x302C)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12334 (R0x302E)	pre_pll_clk_div	0000 0000 00dd dddd	2 (0x0002)
R12336 (R0x3030)	pll_multiplier	0000 0000 dddd dddd	44 (0x002C)
R12338 (R0x3032)	digital_binning	0000 0000 00dd 00dd	0 (0x0000)
R12346 (R0x303A)	frame_count	dddd dddd dddd dddd	0 (0x0000)
R12348 (R0x303C)	frame_status	0000 0000 0000 00??	0 (0x0000)
R12352 (R0x3040)	read_mode	dd00 0000 0000 0000	0 (0x0000)
R12356 (R0x3044)	dark_control	000d ddd0 d000 dd00	1028 (0x0404)
R12358 (R0x3046)	flash	??00 000d d000 0000	0 (0x0000)
R12374 (R0x3056)	green1_gain	0000 0000 dddd dddd	32 (0x0020)
R12376 (R0x3058)	blue_gain	0000 0000 dddd dddd	32 (0x0020)
R12378 (R0x305A)	red_gain	0000 0000 dddd dddd	32 (0x0020)
R12380 (R0x305C)	green2_gain	0000 0000 dddd dddd	32 (0x0020)
R12382 (R0x305E)	global_gain	0000 0000 dddd dddd	32 (0x0020)
R12388 (R0x3064)	embedded_data_ctrl	000d dddd d0d0 dddd	6530 (0x1982)
R12398 (R0x306E)	datapath_select	dddd dd0d 000d 00dd	36864 (0x9000)
R12400 (R0x3070)	test_pattern_mode	0000 000d 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red	0000 dddd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr	0000 dddd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue	0000 dddd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb	0000 dddd dddd dddd	0 (0x0000)
R12410 (R0x307A)	test_raw_mode	0000 0000 0000 00dd	0 (0x0000)
R12422 (R0x3086)	seq_data_port	dddd dddd dddd dddd	0 (0x0000)
R12424 (R0x3088)	seq_ctrl_port	?d00 000d dddd dddd	49152 (0xC000)
R12426 (R0x308A)	x_addr_start_cb	0000 0ddd dddd dddd	2 (0x0002)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12428 (R0x308C)	y_addr_start_cb	0000 00dd dddd dddd	4 (0x0004)
R12430 (R0x308E)	x_addr_end_cb	0000 0ddd dddd dddd	1281 (0x0501)
R12432 (R0x3090)	y_addr_end_cb	0000 00dd dddd dddd	963 (0x03C3)
R12448 (R0x30A0)	x_even_inc	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc	0000 0000 0000 000d	1 (0x0001)
R12452 (R0x30A4)	y_even_inc	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc	0000 0000 0ddd dddd	1 (0x0001)
R12456 (R0x30A8)	y_odd_inc_cb	0000 0000 0ddd dddd	63 (0x003F)
R12458 (R0x30AA)	frame_length_lines_cb	dddd dddd dddd dddd	90 (0x005A)
R12460 (R0x30AC)	frame_exposure	???? ???? ???? ????	16 (0x0010)
R12464 (R0x30B0)	digital_test	dddd dddd dddd 0000	128 (0x0080)
R12466 (R0x30B2)	tempsens_data	0000 00dd dddd dddd	0 (0x0000)
R12468 (R0x30B4)	tempsens_ctrl	0000 0000 00dd dddd	0 (0x0000)
R12476 (R0x30BC)	green1_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12478 (R0x30BE)	blue_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12480 (R0x30C0)	red_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12482 (R0x30C2)	green2_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12484 (R0x30C4)	global_gain_cb	0000 0000 dddd dddd	32 (0x0020)
R12486 (R0x30C6)	tempsens_calib1	dddd dddd dddd dddd	0 (0x0000)
R12488 (R0x30C8)	tempsens_calib2	dddd dddd dddd dddd	0 (0x0000)
R12490 (R0x30CA)	tempsens_calib3	dddd dddd dddd dddd	0 (0x0000)
R12492 (R0x30CC)	tempsens_calib4	dddd dddd dddd dddd	0 (0x0000)
R12500 (R0x30D4)	column_correction	ddd0 0000 0000 dddd	57351 (0xE007)
R12544 (R0x3100)	ae_ctrl_reg	0000 0000 0ddd dddd	0 (0x0000)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12546 (R0x3102)	ae_luma_target_reg	dddd dddd dddd dddd	1280 (0x0500)
R12552 (R0x3108)	ae_min_ev_step_reg	dddd dddd dddd dddd	112 (0x0070)
R12554 (R0x310A)	ae_max_ev_step_reg	dddd dddd dddd dddd	8 (0x0008)
R12556 (R0x310C)	ae_damp_offset_reg	dddd dddd dddd dddd	512 (0x0200)
R12558 (R0x310E)	ae_damp_gain_reg	dddd dddd dddd dddd	8192 (0x2000)
R12560 (R0x3110)	ae_damp_max_reg	dddd dddd dddd dddd	320 (0x0140)
R12572 (R0x311C)	ae_max_exposure_reg	dddd dddd dddd dddd	672 (0x02A0)
R12574 (R0x311E)	ae_min_exposure_reg	dddd dddd dddd dddd	1 (0x0001)
R12580 (R0x3124)	ae_dark_cur_thresh_reg	dddd dddd dddd dddd	32767 (0x7FFF)
R12586 (R0x312A)	ae_current_gains	0000 00?? ???? ????	32 (0x0020)
R12608 (R0x3140)	ae_roi_x_start_offset	0000 0ddd dddd ddd0	0 (0x0000)
R12610 (R0x3142)	ae_roi_y_start_offset	0000 00dd dddd ddd0	0 (0x0000)
R12612 (R0x3144)	ae_roi_x_size	0000 0ddd dddd ddd0	1280 (0x0500)
R12614 (R0x3146)	ae_roi_y_size	0000 00dd dddd ddd0	960 (0x03C0)
R12626 (R0x3152)	ae_mean_l	???? ???? ???? ????	0 (0x0000)
R12644 (R0x3164)	ae_coarse_integration_time	???? ???? ???? ????	0 (0x0000)
R12646 (R0x3166)	ae_ag_exposure_hi	dddd dddd dddd dddd	986 (0x03DA)
R12648 (R0x3168)	ae_ag_exposure_lo	dddd dddd dddd dddd	419 (0x01A3)
R12680 (R0x3188)	delta_dk_level	???? ???? ???? ????	0 (0x0000)
R12736 (R0x31C0)	hispi_timing	0ddd dddd dddd dddd	0 (0x0000)
R12742 (R0x31C6)	hispi_control_status	??00 00dd dddd dd00	32768 (0x8000)
R12744 (R0x31C8)	hispi_crc_0	???? ???? ???? ????	65535 (0xFFFF)
R12746 (R0x31CA)	hispi_crc_1	???? ???? ???? ????	65535 (0xFFFF)
R12748 (R0x31CC)	hispi_crc_2	???? ???? ???? ????	65535 (0xFFFF)

Table 3: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12750 (R0x31CE)	hispi_crc_3	???? ???? ???? ????	65535 (0xFFFF)
R12754 (R0x31D2)	stat_frame_id	dddd dddd dddd dddd	0 (0x0000)
R12758 (R0x31D6)	i2c_wrt_checksum	dddd dddd dddd dddd	65535 (0xFFFF)
R12776 (R0x31E8)	horizontal_cursor_position	0000 00dd dddd dddd	0 (0x0000)
R12778 (R0x31EA)	vertical_cursor_position	0000 0ddd dddd dddd	0 (0x0000)
R12780 (R0x31EC)	horizontal_cursor_width	0000 00dd dddd dddd	0 (0x0000)
R12782 (R0x31EE)	vertical_cursor_width	0000 0ddd dddd dddd	0 (0x0000)
R12796 (R0x31FC)	i2c_ids	dddd dddd dddd dddd	12320 (0x3020)

Detailed Register Descriptions

Manufacturer-Specific Registers

Table 4: Manufacturer-Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12288 R0x3000	15:0	0x2406	chip_version_reg (R/W)	N	N	
	Model ID. Read-only. Can be made read/write by clearing R0x301A[3].					
12290 R0x3002	15:0	0x0000	y_addr_start (R/W)	Y	YM	D
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.					
12292 R0x3004	15:0	0x0000	x_addr_start (R/W)	Y	N	D
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value.					
12294 R0x3006	15:0	0x03BF	y_addr_end (R/W)	Y	YM	D
	The last row of visible pixels to be read out.					
12296 R0x3008	15:0	0x04FF	x_addr_end (R/W)	Y	N	D
	The last column of visible pixels to be read out.					
12298 R0x300A	15:0	0x03DE	frame_length_lines (R/W)	Y	YM	D
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines.					
12300 R0x300C	15:0	0x056C	line_length_pck (R/W)	Y	YM	S
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. The minimum supported value is 0x056C.					
12302 R0x300E	7:0	0x13	revision_number (R/W) The upper four bits represent silicon revision, the lower four bits indicate OTPM version.	N	N	
12306 R0x3012	15:0	0x0064	coarse_integration_time (R/W)	Y	N	S
	Integration time specified in multiples of line_length_pck_.					
12308 R0x3014	15:0	0x0000	fine_integration_time (R/W)	Y	N	D
	The fine integration time increases the integration time. The resolution is 1 pixel clock time.					
12310 R0x3016	15:0	0x0010	coarse_integration_time_cb (R/W)	N	N	S
	Coarse integration time in context B.					
12312 R0x3018	15:0	0x0000	fine_integration_time_cb (R/W)	N	N	D
	Fine integration time in context B.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12314 R0x301A	15:0	0x10D8	reset_register (R/W)	N	Y	
	15	0x0000	grouped_parameter_hold 0: Register updates are synchronized to next frame start. 1: Register changes will remain pending until this bit is returned to 0, after which the register updates will take effect at the next frame start.	N	N	
	14:13	X	Reserved			
	12	0x0001	smia_serialiser_dis This bit disables the serial (HiSPi) interface	N	N	
	11	0x0000	forced_pll_on When set, forces the PLL on, no matter sensor state.	N	N	
	10	0x0000	restart_bad 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N	
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N	
	8	0x0000	gpi_en 0: The primary input buffers associated with the OUTPUT_ENABLE_N, TRIGGER and STANDBY inputs are powered down and cannot be used. 1: The input buffers are enabled and can be read through R0x3026.	N	N	
	7	0x0001	parallel_en 0: The parallel data interface (DOUT[9:0], LINE_VALID, FRAME_VALID, and PIXCLK) is disabled and the outputs are placed in a high-impedance state. 1: The parallel data interface is enabled. The output signals can be switched between a driven and a high-impedance state using output-enable control.	N	N	
	6	0x0001	drive_pins 0: The parallel data interface (DOUT[9:0], LINE_VALID, FRAME_VALID, and PIXCLK) may enter a high-impedance state (depending upon the configuration of R0x3026). 1: The parallel data interface is driven. This bit is “do not care” unless bit[7]=1.	N	N	
	5	X	Reserved			
	4	0x0001	stdby_eof 0: Transition to standby is synchronized to the end of a sensor row readout (held-off until LINE_VALID has fallen). 1: Transition to standby is synchronized to the end of a frame.	N	Y	
	3	0x0001	lock_reg Many parameter limitation registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N	

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
	2	0x0000	stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N	
	1	0x0000	restart This bit always reads as 0. Setting this bit has two effects: first, the current frame is read out and the sensor enters standby. Second, any writes to frame-synchronized registers and the shutter width registers take effect immediately, and a new frame starts. The current frame completes before the new frame is started, so the time between issuing the Restart and the beginning of the next frame is a maximum of t_{FRAME}	N	Y	
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	Y	
	Controls the operation of the sensor. For details see the bit field descriptions.					
12318 R0x301E	15:0	0x012C	data_pedestal (R/W)	N	Y	
	Constant offset that is added to pixel values at the end of datapath (after all corrections).					
12326 R0x3026	15:0	0x0000	gpi_status (RO)	N	N	
	15:4	X	Reserved			
	3	RO	standby Read-only. Return the current state of the STANDBY input pin. Invalid if R0x301A[8]=0.	N	N	
	2	RO	trigger Read-only. Return the current state of the TRIGGER input pin. Invalid if R0x301A[8]=0.	N	N	
	1	RO	oe_n Read-only. Return the current state of the OUTPUT_ENABLE_N input pin. Invalid if R0x301A[8]=0.	N	N	
	0	RO	saddr Read-only. Return the current state of the pin SADDR input pin. Invalid if R0x301A[8]=0.	N	N	
	Reflects the status of the input pins: STANDBY(3), TRIGGER(2), OUTPUT_ENABLE_N(1). Bit 0 is not used.					
12328 R0x3028	15:0	0x0010	row_speed (R/W)	N	N	
	Bits [6:4] of this register define the phase of the output pixclk. 2 sets of values are valid: a) 000, 010, 100, 110 => 0 delay (rising edge of PIXCLK coincides DOUT change). b) 001, 011, 101, 111 => 1/2 clk delay (falling edge of pixclk coincides DOUT change).					
12330 R0x302A	15:0	0x0008	vt_pix_clk_div (R/W)	N	N	
	Sets the ratio of the serial output clock and sensor operation clock (P2 clock divider in PLL).					
12332 R0x302C	15:0	0x0001	vt_sys_clk_div (R/W)	N	N	
	Sets the ratio of the VCO clk and the serial output clock (P1 divider in PLL).					
12334 R0x302E	15:0	0x0002	pre_pll_clk_div (R/W)	N	N	
	Referring to the PLL documentation: shows the n value.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12336 R0x3030	15:0	0x002C	pll_multiplier (R/W)	N	N	
	PLL_MULTIPLIER: shows m value.					
12338 R0x3032	15:0	0x0000	digital_binning (R/W)	N	N	
	15:6	X	Reserved			
	5:4	0x0000	digital_binning_cb DIGITAL_BINNING for context B 00: No binning 01: Horizontal only binning 10: Horizontal and Vertical binning	N	N	
	3:2	X	Reserved			
	1:0	0x0000	digital_binning_ca DIGITAL_BINNING for context A 00: No binning 01: Horizontal only binning 10: Horizontal and Vertical binning	N	N	
12346 R0x303A	15:0	0x0000	frame_count (R/W)	N	N	
	Counts the number of output frames. At the startup is initialized to 0xffff.					
12348 R0x303C	15:0	0x0000	frame_status (RO)	N	N	
	15:2	X	Reserved			
	1	RO	standby_status This bit indicates whether the sensor is in standby state. Can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit R0x301A[4].	N	N	
	0	RO	framesync Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.	N	N	
12352 R0x3040	15:0	0x0000	read_mode (R/W)	Y	YM	
	15	0x0000	vert_flip 0: Normal readout 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first. Setting this bit will change the Bayer pixel order.	Y	YM	D
	14	0x0000	horiz_mirror 0: Normal readout 1: Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first. Setting this bit will change the Bayer pixel order.	Y	YM	D
	13:0	X	Reserved			

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12356 R0x3044	15:0	0x0404	dark_control (R/W)	N	N	
	15:13	X	Reserved			
	12	0x0000	show_colcorr_rows When set, the column correction and delta dark rows are included in the frame valid and are output from the chip. The order of lines in frame valid will be: col_corr, delta dark, embedded data, image data,.. No correction will be applied to the data.	N	N	
	11	0x0000	show_dark_extra_rows When set, the delta dark rows (including the guard/extra rows) will be included in frame valid and output. The order of rows will be: delta dark rows, embedded data, image data, .. No correction will be applied to the dark row data.	N	N	
	10	0x0001	row_noise_correction_en 0: Row-noise cancellation algorithm is disabled 1: Row-noise cancellation algorithm is enabled.	N	N	
	9	0x0000	show_dark_cols When set, the row noise correction columns (tied pixels) will be added to line valid and output. No correction will be applied to the dark row data.	N	N	
	8:0	X	Reserved			
12358 R0x3046	15:0	0x0000	flash (R/W)	Y	Y	
	15	RO	strobe Reflects the current state of the FLASH output signal. Read-only.	N	N	
	14	RO	triggered Indicates that the FLASH output signal was asserted for the current frame. Read-only.	N	N	
	13:9	X	Reserved			
	8	0x0000	en_flash Enables LED flash. The flash is asserted with the start integration. The flash is de-asserted when the integration is complete.	Y	Y	S
	7	0x0000	invert_flash Invert flash output signal. When set, the FLASH output signal will be active low.	N	N	
	6:0	X	Reserved			
12374 R0x3056	15:0	0x0020	green1_gain (R/W)	Y	N	D
	Digital gain for green1 (Gr) pixels, in format of xxx.yyyyy.					
12376 R0x3058	15:0	0x0020	blue_gain (R/W)	Y	N	D
	Digital gain for Blue pixels,, in format of xxx.yyyyy.					
12378 R0x305A	15:0	0x0020	red_gain (R/W)	Y	N	D
	Digital gain for Red pixels, in format of xxx.yyyyy.					
12380 R0x305C	15:0	0x0020	green2_gain (R/W)	Y	N	D
	Digital gain for green2 (Gb) pixels in format of xxx.yyyyy.					
12382 R0x305E	15:0	0x0020	global_gain (R/W)	Y	N	D
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers. Reading from this register returns the value most recently written to the green1_gain register.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12388 R0x3064	15:0	0x1982	embedded_data_ctrl (R/W)	N	N	
	15:13	X	Reserved			
	12	X	Reserved			
	11:10	X	Reserved			
	9	X	Reserved			
	8	0x0001	embedded_data 0: Frames out of the sensor exclude the embedded data. 1: Frames out of the sensor include 2 rows of embedded data. This register field should only be changed while the sensor is in software standby.	N	N	
	7	0x0001	embedded_stats_en Enables two rows of statistical data (used by external auto-exposure), after the transmission image data. Cannot be enabled unless EMBEDDED_DATA_EN is enabled.	N	Y	
	6:4	X	Reserved			
	3:0	X	Reserved			
12398 R0x306E	15:0	0x9000	datapath_select (R/W)	N	N	
	15:13	0x0004	slew_rate_ctrl_parallel Selects the slew (edge) rate for the DOUT[9:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects FLASH outputs when parallel data output is disabled. The value 7 results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N	
	12:10	0x0004	slew_rate_ctrl_pixclk Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value 7 results in the fastest edge rates on this signal. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N	
	9	X	Reserved			
	8	0x0000	postscaler_data_sel 0: Statistics data are generated from pixel data before scaler. 1: Statistics data are generated from pixel data after scaler.	N	N	
	7:5	X	Reserved			
	4	0x0000	true_bayer Enables true Bayer scaling mode.	N	N	
	3:2	X	Reserved			
	1:0	0x0000	special_line_valid 00: Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID	N	N	
12400 R0x3070	15:0	0x0000	test_pattern_mode (R/W)	N	Y	
	0: Normal operation: Generate output data from pixel array 1: Solid color test pattern. 2: 100% color bar test pattern 3: Fade to gray color bar test pattern 256 : Walking 1s test pattern (12 bit) Other: Reserved.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12402 R0x3072	15:0	0x0000	test_data_red (R/W)	N	Y	
	The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors.					
12404 R0x3074	15:0	0x0000	test_data_greenr (R/W)	N	Y	
	The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors.					
12406 R0x3076	15:0	0x0000	test_data_blue (R/W)	N	Y	
	The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors.					
12408 R0x3078	15:0	0x0000	test_data_greenb (R/W)	N	Y	
	The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors.					
12422 R0x3086	15:0	0x0000	seq_data_port (R/W)	N	N	
	Register used to write to or read from the sequencer RAM.					
12424 R0x3088	15:0	0xC000	seq_ctrl_port (R/W)	N	N	
	15	RO	sequencer_stopped Showing that sequencer is stopped (STANDBY mode) and the RAM is available for read or write.	N	N	
	14	0x0001	auto_inc_on_read 1: The access_address is incremented (by 1) after each read operation from seq_data_port (which returns only1 byte)	N	N	
	13:9	X	Reserved			
	8:0	0x0000	access_address When in STANDBY (not streaming) mode: address pointer to the sequencer RAM.	N	N	
	Register controlling the read and write to sequencer RAM.					
12426 R0x308A	15:0	0x0002	x_addr_start_cb (R/W)	N	N	D
	x_address_start context B					
12428 R0x308C	15:0	0x0004	y_addr_start_cb (R/W)	N	N	D
	y_addr_start for context B					
12430 R0x308E	15:0	0x0501	x_addr_end_cb (R/W)	N	N	D
	x_addr_end for context B					
12432 R0x3090	15:0	0x03C3	y_addr_end_cb (R/W)	N	N	D
	Y_ADDR_END for context B					
12448 R0x30A0	15:0	0x0001	x_even_inc (RO)	N	N	
	Read-only.					
12450 R0x30A2	15:0	0x0001	x_odd_inc (R/W)	Y	YM	
	Not supported.					
12452 R0x30A4	15:0	0x0001	y_even_inc (RO)	N	N	
	Read-only.					
12454 R0x30A6	15:0	0x0001	y_odd_inc (R/W)	Y	YM	D
	Row skip factor: 1: No Skip 3: Skip Factor 2 7: Skip Factor 4 15: Skip Factor 8 31: Skip Factor 16 63: Skip Factor 32 127: Skip Factor 64					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12456 R0x30A8	15:0	0x003F	y_odd_inc_cb (R/W)	N	N	D
	y_odd_inc for context B					
12458 R0x30AA	15:0	0x005A	frame_length_lines_cb (R/W)	N	N	D
	frame_length_lines for context B.					
12460 R0x30AC	15:0	0x0010	frame_exposure (LK)	N	N	
	Shows the current frame exposure time in rows.					
12464 R0x30B0	15:0	0x0080	digital_test (R/W)	N	Y	
	15	X	Reserved			
	14	0x0000	pll_complete_bypass When set, the EXTCLK will be used and PLL will be completely bypassed. Note that the serial interface would not function.	N	N	
	13	0x0000	context_b 0: Use context A 1: Use Context B	N	N	
	12:11	X	Reserved			
	10	0x0000	enable_short_llpck This bit allows the line length to be reduced to 1388 and must be set to 1 for correct line timing for non-skipping modes. It must be set to 0 for skip modes. Triggered mode does not support short line lengths - so it must be set to 0 for trigger mode.	N	N	
	9:8	0x0000	col_gain_cb Column gain for Context B 00: 1 01: 2 10: 4 11: 8	N	N	D
	7	0x0001	mono_chrome When set the CFA is monochrome and not color. Some features like skipping and corrections are affected.	N	N	
	6	X	Reserved			
	5:4	0x0000	col_gain Column gain: 00: 1 01: 2 10: 4 11: 8	N	N	D
	3:0	X	Reserved			
12466 R0x30B2	15:0	0x0000	tempsens_data (R/W)	N	N	
	Data from temperature sensor					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12468 R0x30B4	15:0	0x0000	tempsens_ctrl (R/W)	N	N	
	15:6	X	Reserved			
	5	0x0000	temp_clear_value	N	N	
	4	0x0000	temp_start_conversion	N	N	
	3:1	0x0000	tempsens_test_ctrl	N	N	
	0	0x0000	tempsens_power_on	N	N	
	Control register for temp sensor: Bit[0]: Tempsens power on when set. Bits [3:1]: Tempsens test ctrl Bit [4]: Tempsens starts conversion when set Bit [5]: Tempsens clears value when set.					
12476 R0x30BC	15:0	0x0020	green1_gain_cb (R/W)	N	N	D
	Digital gain green1 context B					
12478 R0x30BE	15:0	0x0020	blue_gain_cb (R/W)	N	N	D
	digital gain blue context B					
12480 R0x30C0	15:0	0x0020	red_gain_cb (R/W)	N	N	D
	digital gain red context B					
12482 R0x30C2	15:0	0x0020	green2_gain_cb (R/W)	N	N	D
	digital gain green 2 context B					
12484 R0x30C4	15:0	0x0020	global_gain_cb (R/W)	N	N	D
	global digital gain context B					
12486 R0x30C6	15:0	0x0000	tempsens_calib1 (R/W) This register will read out sensor-specific calibration data.	N	N	
12488 R0x30C8	15:0	0x0000	tempsens_calib2 (R/W) This register will read out sensor-specific calibration data.	N	N	
12490 R0x30CA	15:0	0x0000	tempsens_calib3 (R/W) This register is not used.	N	N	
12492 R0x30CC	15:0	0x0000	tempsens_calib4 (R/W) This register is not used.			
12500 R0x30D4	15:0	0xE007	column_correction (R/W)	N	N	
	15	0x0001	enable Enable column correction.	N	N	
	14	0x0001	double_range Doubles the range of the correction value but halves the precision.	N	N	
	13	0x0001	double_samples Makes the column correction use 128 rows instead of 64. Adds 64 to the minimum frame blanking.	N	N	
	12:4	X	Reserved			
	3:0	0x0007	colcorr_rows Value showing the number of column correction rows - 1.	N	N	

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12544 R0x3100	15:0	0x0000	ae_ctrl_reg (R/W)			
	15:7	X	Reserved			
	6:5	0x0000	min_ana_gain Minimum analog gain to be used by AE. 00:1x (default) 01: 2x 10: 4x 11: 8x	N	N	
	4	0x0000	auto_dg_en Automatic control of digital gain by AE is enabled.	N	N	
	3:2	X	Reserved			
	1	0x0000	auto_ag_en When set, enables the automatic AE control of analog gain.	N	N	
	0	0x0000	ae_enable 1: Enables the on-chip AE algorithm. Auto Exposure also requires embedded_data_en R0x3064[8] and embedded_stats_en R0x3064[7] to be set to 1 for proper operation.	N	N	
12546 R0x3102	15:0	0x0500	ae_luma_target_reg (R/W)	N	N	
	Average luma target value to be reached by the auto exposure					
12552 R0x3108	15:0	0x0070	ae_min_ev_step_reg (R/W)	N	N	
	Minimum exposure value step size [15:8]: Reserved [7:0] : Min_EV_stepsize = (min step size)*256. Since Min_EV_step sizes are small and they are typically less than 1 e.g. 1/16, 7/16 etc... these are multiplied by 256 and then the value is written to this register.					
12554 R0x310A	15:0	0x0008	ae_max_ev_step_reg (R/W)	N	N	
	Maximum exposure value step size. Note that since this value is always greater than 1 there is no need to multiply by 256 as in the case of min_EV_stepsize.					
12556 R0x310C	15:0	0x0200	ae_damp_offset_reg (R/W)	N	N	
	Adjusts step size and settling speed.					
12558 R0x310E	15:0	0x2000	ae_damp_gain_reg (R/W)	N	N	
	Adjusts step size and settling speed.					
12560 R0x3110	15:0	0x0140	ae_damp_max_reg (R/W)			
	Max value allowed for recursiveDamp (multiplied by 256 since internal value is typical <1). For most applications, the value of recursiveDamp should be <1, otherwise AE will overshoot the target. For applications with fast settling required, it may be desirable to allow recursiveDamp >1. Default value: 0.875 * 256 = 0x00E0					
12572 R0x311C	15:0	0x02A0	ae_max_exposure_reg (R/W)	N	N	
	Maximum integration (exposure) time in rows to be used by AE.					
12574 R0x311E	15:0	0x0001	ae_min_exposure_reg (R/W)			
	Minimum integration (exposure) time in rows to be used by AE.					
12580 R0x3124	15:0	0x7FFF	ae_dark_cur_thresh_reg (R/W)			
	The dark current level that stops AE from increasing integration time. Note that increased integration time would increase dark current as well and signal level (SNR) would drop because photo diode well capacity is limited.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12586 R0x312A	15:0	0x0020	ae_current_gains (RO)			
	15:10	X	Reserved			
	9:8	RO	ae_ana_gain The gain decided by AE, when it is enabled and can control the analog gain.	N	N	
	7:0	RO	ae_dig_gain The gain decided by AE, when it is enabled and can control the digital gain.	N	N	
	Shows the gain settings decided by AE.					
12608 R0x3140	15:0	0x0000	ae_roi_x_start_offset (R/W)			
	Number of pixels into each row before the ROI starts NOTE: if statistics are being gathered from a scaled image then the 'number of pixels' value must be the number of scaled pixels					
12610 R0x3142	15:0	0x0000	ae_roi_y_start_offset (R/W)			
	Number of rows into each frame before the ROI starts					
12612 R0x3144	15:0	0x0500	ae_roi_x_size (R/W)			
	Number of columns in the ROI					
12614 R0x3146	15:0	0x03C0	ae_roi_y_size (R/W)			
	Number of rows in the ROI					
12626 R0x3152	15:0	0x0000	ae_mean_l (RO)			
	The true mean of all Gr pixels in the ROI (16 least significant bits)					
12644 R0x3164	15:0	0x0000	ae_coarse_integration_time (RO)			
	The integration time decided by AE.					
12646 R0x3166	15:0	0x03DA	ae_ag_exposure_hi (R/W)			
	At this integration time, the analog gain is increased (when AE is enabled to control also the analog gain).					
12648 R0x3168	15:0	0x01A3	ae_ag_exposure_lo (R/W)	N	N	
	At this integration time, the AE is reduced (when AE is enabled to control the analog gain also),					
12680 R0x3188	15:0	0x0000	delta_dk_level (RO)	N	N	
	Measured dark current.					
12736 R0x31C0	15:0	0x0000	hispi_timing (R/W)	N	N	
	Bits [2:0]: DLL delay setting for data lane 0 Bits [5:3]: DLL delay setting for data lane 1 Bits [8:6]: DLL delay setting for data lane 2 Bits [11:9]: DLL delay setting for data lane 3 Bits [14:12]: DLL delay setting for clock lane The delay setting selects a tap along a delay element. Each stage is 1/8 of a symbol period. When the delay is set to zero, the delay element is powered down.					

Table 4: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit; Y (Yes); N (No); YM (Yes, Masked); S (Single Buffered); D (Double Buffered)

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame	Buffering
12742 R0x31C6	15:0	0x8000	hispi_control_status (R/W)	N	N	
	15:14	RO	hispi_status	N	N	
	13:10	X	Reserved			
	9:2	0x0000	hispi_control Bit[2]: Stream mode enable. Bit[3]: Enable 3 lanes for compressed data Bit[6:4]: Test mode: //////////////////////////////// 000: Transmit constant 0 on all enabled data lanes. 001: Transmit constant 1 on all enabled data lanes. 010: Transmit square wave at the half the potential serial data rate on all the enabled lanes. 011: Transmit square wave at the pixel data rate on all the enabled lanes. 100: Transmit a continuous, repeated, sequence of pseudo random data, with no SAV code, copied on all enabled data lanes. 101: Replace pixel data with a known sequence (PN9), copied on all the enabled data lanes. // Bit[7]: Test mode enable Bit[8]: IO test enable Bit[9]: Frame wide checksum test enable	N	N	
	1:0	X	Reserved			
12744 R0x31C8	15:0	0xFFFF	hispi_crc_0 (RO)	N	N	
12746 R0x31CA	15:0	0xFFFF	hispi_crc_1 (RO)			
12748 R0x31CC	15:0	0xFFFF	hispi_crc_2 (RO)	N	N	
12750 R0x31CE	15:0	0xFFFF	hispi_crc_3 (RO)			
12754 R0x31D2	15:0	0x0000	stat_frame_id (R/W)	N	N	
12758 R0x31D6	15:0	0xFFFF	i2c_wrt_checksum (R/W)	N	N	
	Checksum of I^2C write operations.					
12776 R0x31E8	15:0	0x0000	horizontal_cursor_position (R/W)	N	N	
	Specifies the start row for the test cursor.					
12778 R0x31EA	15:0	0x0000	vertical_cursor_position (R/W)	N	N	
	Specifies the start column for the test cursor.					
12780 R0x31EC	15:0	0x0000	horizontal_cursor_width (R/W)	N	N	
	Specifies the width, in rows, of the horizontal test cursor. A width of 0 disables the cursor.					
12782 R0x31EE	15:0	0x0000	vertical_cursor_width (R/W)			
	Specifies the width, in columns, of the vertical test cursor. A width of 0 disables the cursor.					
12796 R0x31FC	15:0	0x3020	i2c_ids (R/W)	N	N	
	I^2C addresses.					

Revision History

Rev. D 6/12/14

- Updated corporate address on last page
- Deleted lock_control from Table 3, “Manufacturer-Specific Register List,” on page 7 and Table 4, “Manufacturer-Specific Register Descriptions,” on page 12
- Updated descriptions of register field “restart” and “enable_short_llpck” in Table 3, “Manufacturer-Specific Register List,” on page 7 and Table 4, “Manufacturer-Specific Register Descriptions,” on page 12
- Updated description of register field “col_gain_cb” in Table 4.

Rev. C 4/25/13

- Updated to Production
- Updated default values of:
  - frame_length_lines
  - digital_test
  - enable_short_llpck
  - revision_number
- Updated description of ae_enable

Rev. B 1/23/13

- Updated to Preliminary
- Updated the default values for:
  - revision_number
  - reset_register
  - digital_test
  - tempsens_calib1
  - tempsens_calib2
  - tempsens_calib3
  - tempsens_calib4
- Updated the descriptions for:
  - frame_length_lines
  - line_length_pck
  - show_dark_extra_rows
  - show_dark_cols
  - enable_short_llpck
  - tempsens_calib1
  - tempsens_calib2
  - tempsens_calib3
  - tempsens_calib4
  - grouped_parameter_hold
- Added description for bit 10 of R0x30B0
- Updated “Bad Frames” on page 6

Revision A **11/2/12**

- Initial release

180 Clemenceau Avenue, #05-02/04 Haw Par Centre, Singapore 239922 prodmktg@aptina.com www.aptina.com

1/3-Inch CMOS Digital Image Sensor

AR0134 Developer Guide, Rev. C

For the latest data sheet, refer to Aptina's Web site: www.aptina.com

AR0134 Developer Guide

Table of Contents

List of Figures

List of Tables

Introduction

This Developer Guide provides detailed descriptions and usage guidelines for various features of the AR0134 Global Shutter Sensor. Also provided are guidelines for optimal settings for various use cases. For detailed electrical and timing specifications or register descriptions, refer to the AR0134 Data Sheet and the AR0134 Register Reference documents, respectively.

Optimal Setting Guidelines

The AR0134 Global Shutter Sensor has many built-in features and is capable of many resolutions and frame rates. Guidelines for setting resolution and frame rate are provided in this section. Detailed settings for the many features are provided throughout the remainder of this Developer Guide. Window registers are also provided to enable context switching. See the section on Real-Time Context Switching and the register reference guide for more details.

Resolution

Aptina's AR0134 sensor is capable of a maximum resolution of 1280 x 960 at up to 54 fps, or it may be configured to run 720p at 60fps. Registers y_addr_start, x_addr_start, y_addr_end, and x_addr_end are used to specify the image window. The minimum value for x_addr_start is 0 and the maximum value for x_addr_end is 1279. The minimum y_addr_start and maximum y_addr_end are 0 and 975, respectively.

Frame Rate

Achieving the desired frame rate at the proper resolution is a balancing act between row timing and the number of rows in the image. Integration time and the pixel clock frequency are additional factors. The minimum line length is 1388 pixel clocks which enables a frame rate of 54 fps. When using trigger mode, the minimum line length is 1650 pixel clocks.

Blanking Control

Horizontal blanking and vertical blanking times are controlled by the Line_length_Pck and Frame_Length_Lines registers, respectively.

- Horizontal blanking is specified in terms of pixel clocks. It is calculated by subtracting the X window size from the Line_Length_Pck register. The minimum horizontal blanking time is 108 pixel clocks when the X window is set to 1280. If the X window size is configured to less than 1280, the sum of the X window size and the horizontal blanking must be equal to or greater than 1388.
- Vertical blanking is specified in terms of numbers of lines. It is calculated by subtracting the Y window size from the Frame_Length_Lines register. The minimum value for vertical blanking is 23 lines.

The actual imager timing is described in the Frame Time section of this Developer Guide.

Pixel Data Format

Pixel Array Structure

The AR0134 pixel array is configured as 1412 columns by 1028 rows, (see Figure 1). The dark pixels are optically black and are used internally to monitor black level. Of the right 108 columns, 64 are dark pixels used for row noise correction. Of the top 24 rows of pixels, 12 of the dark rows are used for black level correction. There are 1296 columns by 976 rows of optically active pixels. While the sensor's format is 1280 x 960, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

Figure 1: Pixel Array Description

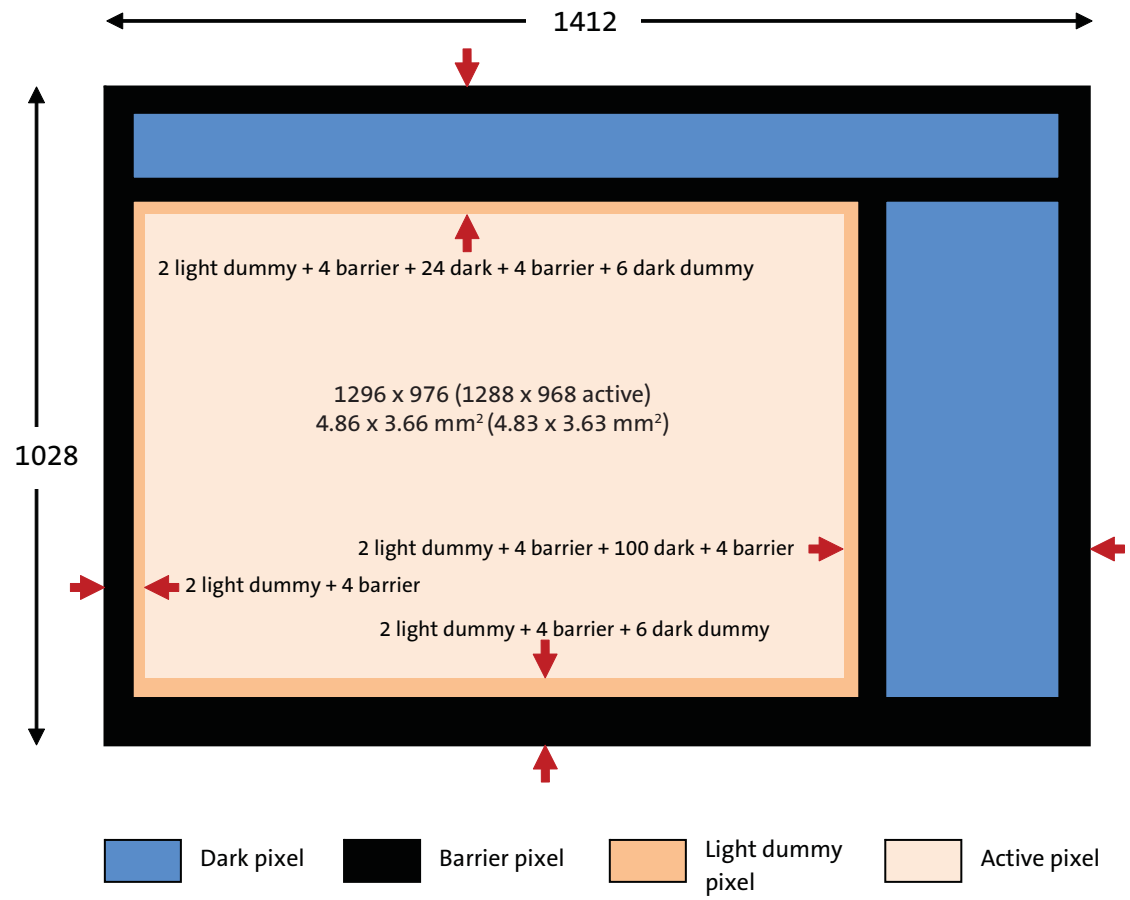
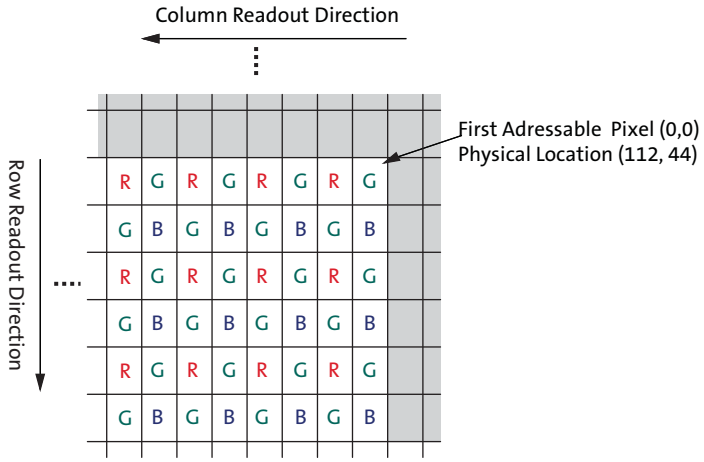


Figure 2: Pixel Color Pattern Detail (Top Right Corner)

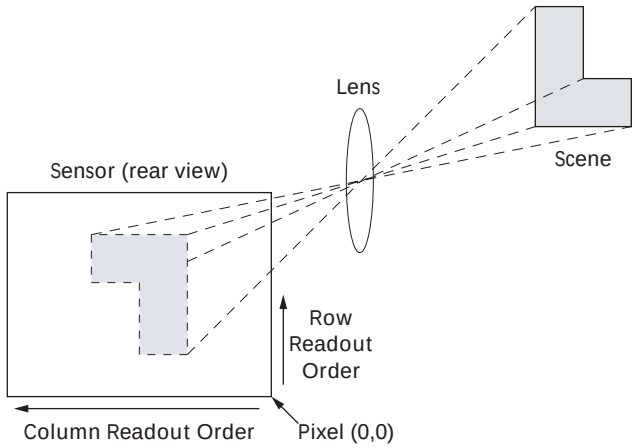


Default Readout Order

By convention, the sensor core pixel array is shown with the first addressable (logical) pixel (0,0) in the top right corner (see Figure 2). This reflects the actual layout of the array on the die. Also, the physical location of the first pixel data read out of the sensor in default condition is that of pixel (112, 44).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 3. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 3 on page 8.

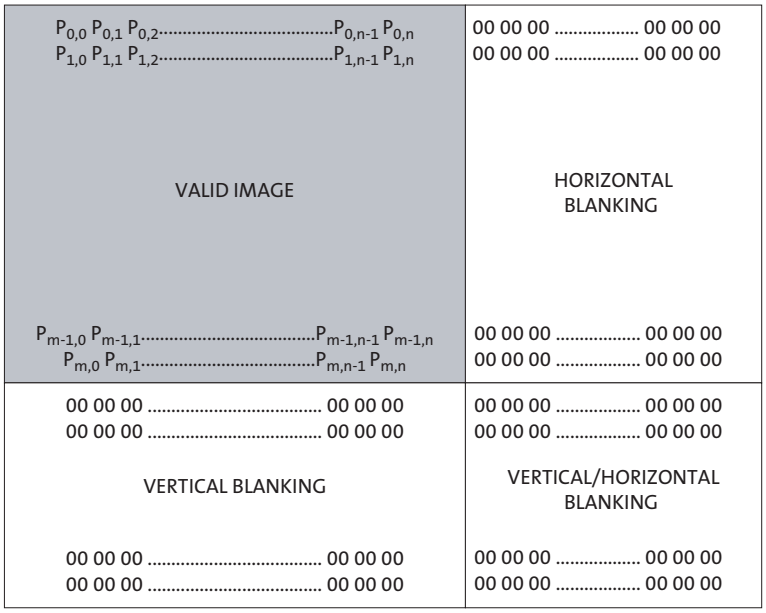
Figure 3: Imaging a Scene



Output Data Format

The AR0134 image data is read out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking (see Figure 4). The amount of horizontal row time (in clocks) is programmable through R0x300C. The amount of vertical frame time (in rows) is programmable through R0x300A. Line_Valid (LV) is HIGH during the shaded region of Figure 4. Optional embedded register setup information and histogram statistic information are available in the first two and the last two rows of image data.

Figure 4: Spatial Illustration of Image Readout



Readout Sequence

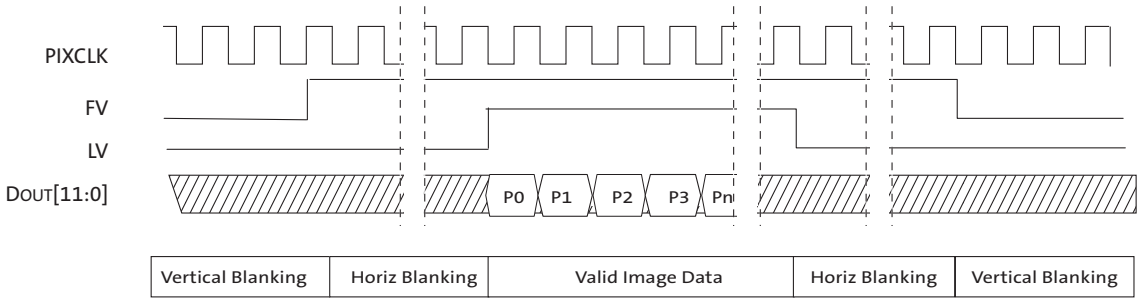
Typically, the readout window is set to a region including only active pixels. The user has the option of reading out dark regions of the array, but if this is done, consideration must be given to how the sensor reads the dark regions for its own purposes.

Parallel Output Data Timing

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 964 rows of 1280 columns each. The FV and LV signals indicate the boundaries between frames and lines, respectively. PIXCLK can be used as a clock to latch the data. One 12-bit pixel datum is launched on the DOUT pins for each falling edge of PIXCLK. The launch edge of PIXCLK may be set in register R0x3028. When both FV and LV are asserted, the pixel is valid. PIXCLK cycles that occur when FV is de-asserted are called vertical blanking. PIXCLK cycles that occur when only LV is de-asserted are called horizontal blanking.

To enable the parallel output pins, set R0x301A[7] = 1, and set R0x301A[12] = 1 to disable the HiSPi serializer. The parallel input pins (i.e. TRIGGER, STANDBY, etc) may be enabled by setting R0x301A[8] = 1. Only one output interface should be enabled at a time.

Figure 5: Default Pixel Output Timing



LV and FV

The timing of the FV and LV outputs is closely related to the row time and the frame time.

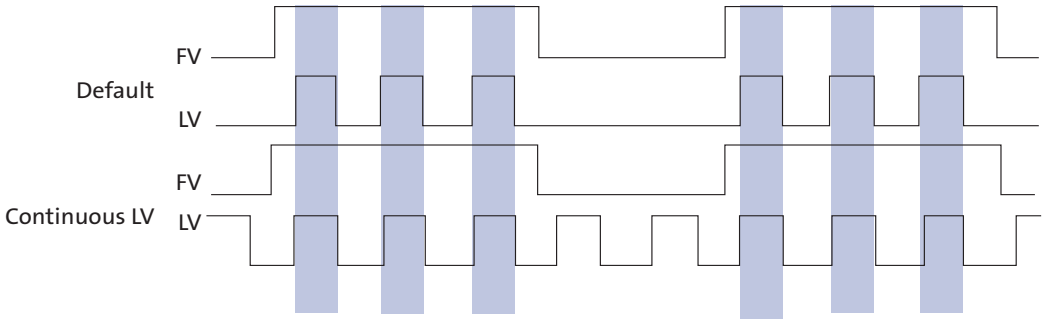
FV will be asserted for an integral number of row times, which will normally be equal to the height of the output image.

LV will be asserted during the valid pixels of each row. The leading edge of LV will be offset from the leading edge of FV by 6 PIXCLKs. Normally, LV will only be asserted if FV is asserted; this is configurable as described below.

LV Format Options

The default situation (R0x306E[1:0] = 0x0) is for LV to be de-asserted when FV is de-asserted. By setting R0x306E[1:0]= 0x1, a continuous LV signal will be output. The formats for reading out four lines and two vertical blanking lines are shown in Figure 6.

Figure 6: LV Format Options



The timing of an entire frame is shown in Figure 12: “Line Timing and FRAME_VALID/LINE_VALID Signals,” on page 14. For detailed timing diagrams and switching parameters, refer to the AR0134 data sheet.

High Speed Serial Pixel Interface

The AR0134 also uses Aptina's High-Speed Serial Pixel Interface (HiSPi™). The AR0134 HiSPi interface supports two protocols, Streaming-SP, and Packetized SP. The streaming protocol conforms to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data. Refer to Table 1 for HiSPi protocol and lane settings.

Table 1: AR0134 HiSPi Protocol Configuration Settings

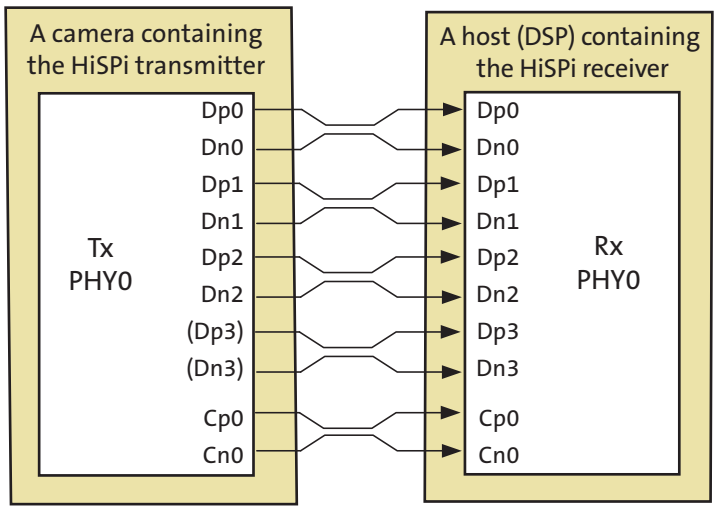
Protocol	R0x31C6
Streaming-SP 2 Lane	0x0004
Streaming-SP 3 Lane	0x000C
Packetized-SP 2 Lane	0x0000
Packetized-SP 3 Lane	0x0008

These protocols are further described in the High-Speed Serial Pixel (HiSPi™) Interface Protocol Specification V1.50.00.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. Figure 7 shows the configuration between the HiSPi transmitter and the receiver.

To enable the serial interface, set R0x301A[7] = 0, and set R0x301A[12] = 0 to enable the HiSPi serializer. Refer to “Clocks” on page 26 for PLL configuration when using the HiSPi interface.

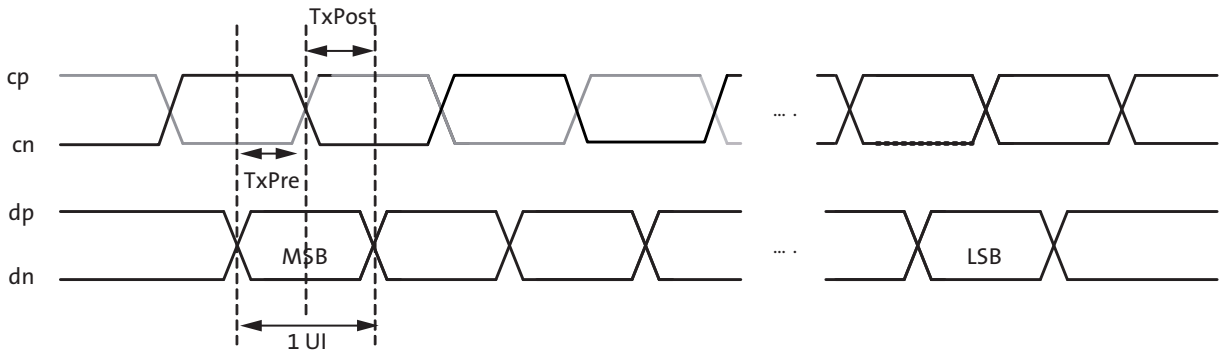
Figure 7: HiSPi Transmitter and Receiver Interface Block Diagram



HiSPi Physical Layer

The HiSPi physical layer is partitioned into blocks of four data lanes and an associated clock lane. Depending on the operating mode and data rate, it can be configured from two to three lanes. Dp3 and Dn3 are not supported by the AR0134 but pins are connected on the package. The PHY will serialize a 12-bit data word and transmit on both edges of the clock. Figure 8 shows bit transmission. In this example, the word is transmitted in order of MSB to LSB. The receiver latches data at the rising and falling edge of the clock. The AR0134 supports only the SLVS mode of the HiSPi electrical specification. For detailed timing and electrical specifications for the HiSPi interface, refer to the AR0134 Datasheet.

Figure 8: Timing Diagram



DLL Timing Adjustment

The AR0134 includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design.

Delay compensation may be set for clock and/or data lines in the hispi_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.

Figure 9: Block Diagram of DLL Timing Adjustment

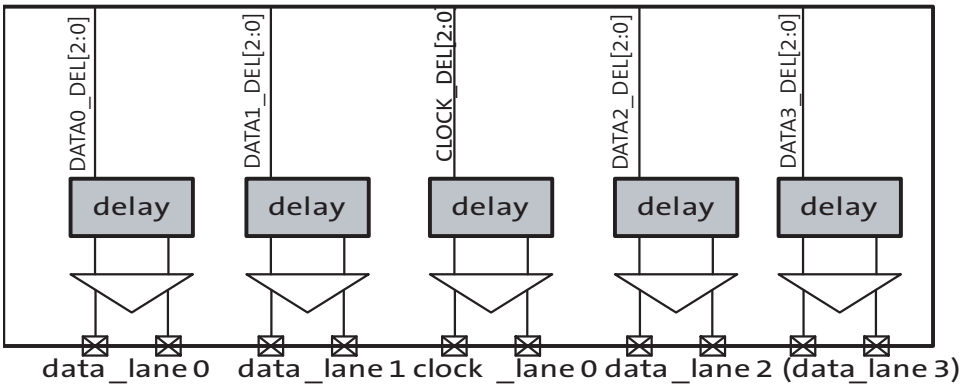


Figure 10: Delaying the Clock with Respect to Data

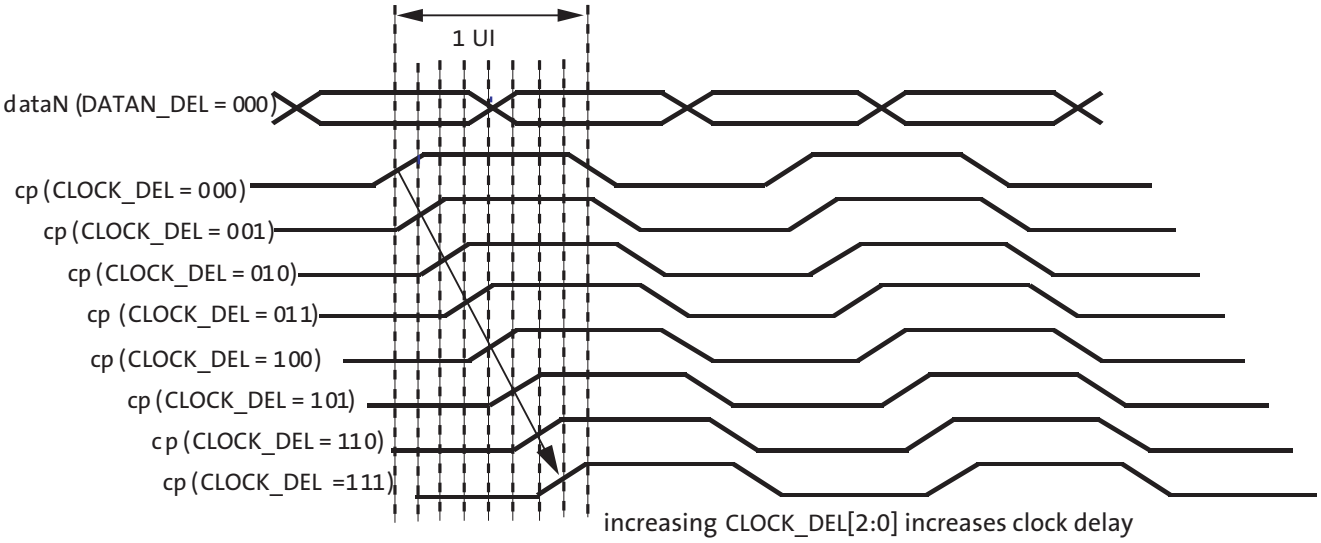
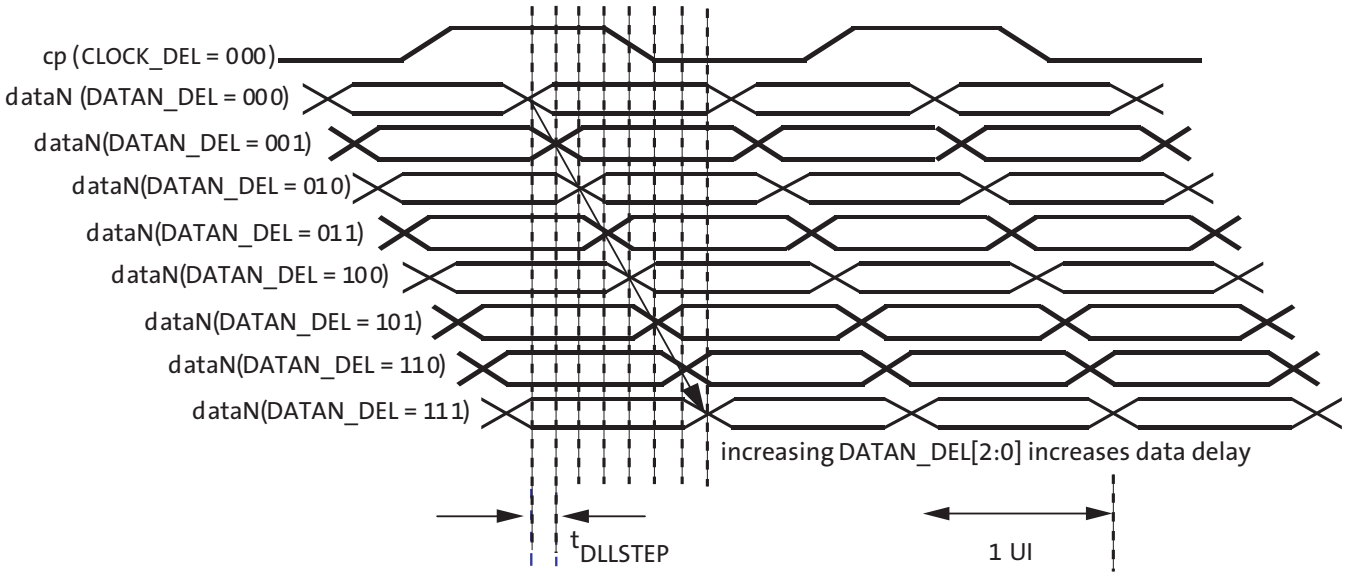


Figure 11: Delaying Data with Respect to the Clock



Frame Time

The pixel clock (PIXCLK) represents the time needed to sample one pixel from the array. The sensor outputs data at the maximum rate of one pixel per PIXCLK. One row time (t_{ROW}) is the period from the first pixel output in a row to the first pixel output in the next row. The row time and frame time are defined by equations in Table 2.

Figure 12: Line Timing and FRAME_VALID/LINE_VALID Signals

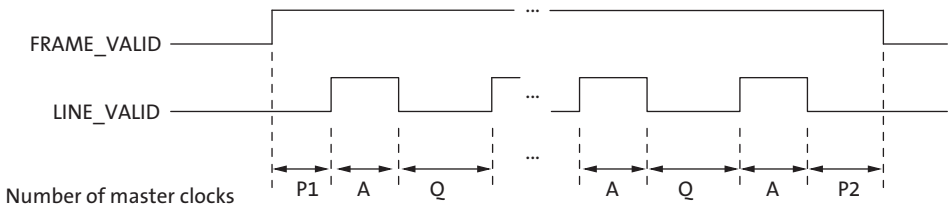


Table 2: Frame Time (Example Based on 1280 x 960, 54 Frames Per Second)

Parameter	Name	Equation	Default Timing at 74.25 MHz
A	Active data time	Context A: R0x3008 - R0x3004 + 1 Context B: R0x308E - R0x308A + 1	1280 pixel clocks = 17.23µs
P1	Frame start blanking	6 (fixed)	6 pixel clocks = 0.08µs
P2	Frame end blanking	6 (fixed)	6 pixel clocks = 0.08µs
Q	Horizontal blanking	R0x300C - A	108 pixel clocks = 1.45µs

Table 2: Frame Time (Example Based on 1280 x 960, 54 Frames Per Second)

Parameter	Name	Equation	Default Timing at 74.25 MHz
A+Q	Row Time (t_{ROW})	R0x300C	1388 pixel clocks = 18.69µs
V	Vertical blanking	Context A: [(R0x300A - (R0x3006 - R0x3002 + 1)) * (A + Q)] Context B: [(R0x300A - (R0x3090 R0x308C + 1)) * (A + Q)]	51,356 pixel clocks = 691.7µs
Nrows * (A + Q)	Frame valid time	Context A: ((R0x3006-R0x3002+1)*(A+Q))-Q+P1+P2 Context B: ((R0x3090-R0x308C+1)*(A+Q))-Q+P1+P2	1,332,384 pixel clocks = 17.94ms
F	Total frame time	V + (Nrows * (A + Q))	1,383,836 pixel clocks = 18.6ms

Sensor timing is shown in terms of pixel clock cycles (see Figure 5: "Default Pixel Output Timing," on page 10). The recommended pixel clock frequency is 74.25 MHz. The vertical blanking and the total frame time equations assume that the integration time (coarse integration time plus fine integration time) is less than the number of active lines plus the blanking lines:

Coarse Integration Time < Window Height + Vertical Blanking *(EQ 1)*

If this is not the case, the number of integration lines must be used instead to determine the frame time, (see Table 3). In this example, it is assumed that the coarse integration time control is programmed with 2000 rows and the fine shutter width total is zero.

For Master mode, if the integration time registers exceed the total readout time, then the vertical blanking time is internally extended automatically to adjust for the additional integration time required. This extended value is **not** written back to the frame_length_lines register. The frame_length_lines register can be used to adjust frame-to-frame readout time. This register does not affect the exposure time but it may extend the readout time.

Table 3: Frame Time: Long Integration Time

Parameter	Name	Equation (Number of Pixel Clock Cycles)	Default Timing at 74.25 MHz
F'	Total frame time (long integration time)	Context A: (R0x3012 * (A + Q)) - R0x3014 + P1 + P2 Context B: (R0x3016 * (A + Q)) - R0x3018 + P1 + P2	2,776,012 pixel clocks = 37.4ms

Exposure

Total integration time is the result of coarse_integration_time and fine_integration_time registers, and depends also on whether manual or automatic exposure is selected.

The actual total integration time, t_{INT} is defined as:

$$t_{INT} = t_{INTCoarse} + t_{INTFine} \quad \text{(EQ 2)}$$

= (number of lines of integration * line time) + (number of pixels of integration * pixel time)

where:

- Number of Lines of Integration (Auto Exposure Control: Enabled)
  When automatic exposure control (AEC) is enabled, the number of lines of integration may vary from frame to frame, with the limits controlled by R0x311E (minimum auto exposure time) and R0x311C (maximum auto exposure time). For a specific frame output, the exposure time (in rows) can be read in R0x30AC. Fine integration time is not used by the auto exposure function.

- Number of Lines of Integration (Auto Exposure Control: Disabled)
  Context A: the number of lines of integration equals the value in R0x3012.
  Context B: the number of lines of integration equals the value in R0x3016.

- Number of Pixels of Integration (Auto Exposure Control: Disabled.)
  Context A: the number of pixels of integration equals the value in R0x3014.
  Context B: the number of pixels of integration equals the value in R0x3018.
  Maximum value for $t_{INTFine}$ is line_length_pck - 742.

If the exposure time is to be set to approximately 2.22ms and default settings are being used (where one row-time equals 22.22µs), a value of "100" is entered in R0x3012 (2.22ms / 22.22µs = 100). In this mode, only whole number row-time increments are allowed—no fractional time increments can be achieved. It may be possible to adjust the number of horizontal active or blanking pixels to bring the desired exposure time to a whole number row-time increment.

The exposure time using the default power up settings of the sensor can be determined as follows:

$$exposure\_time = coarse\_integration\_time \times row\_time \quad \text{(EQ 3)}$$

$$exposure\_time = (100\ rows) \times (22.22\ \mu s) = 2.22ms \quad \text{(EQ 4)}$$

–

Typically, the value of the coarse_integration_time register is limited to the number of lines per frame (which includes vertical blanking lines), such that the frame rate is not affected by the integration time.

Row-Time Definition

One row-time is equal to the sum of the number of active pixels (columns) and the number of horizontal blanking pixels divided by the pixel readout rate:

$$row\_time = \frac{active\_pixels + horizontal\_blank\_pixels}{PIXCLK\_frequency} \quad \text{(EQ 5)}$$

$$row\_time_{default\_settings} = \frac{line\_length\_pck(R0x300C)}{PIXCLK\_frequency} = \frac{1388}{74.25MHz} = 18.69\mu s \quad \text{(EQ 6)}$$

Exposure Indicator

The AR0134 provides an output pin, FLASH, to indicate when the exposure takes place. When R0x3046[8]is set, FLASH is HIGH during exposure. By using R0x3046[7], the polarity of the FLASH pin can be inverted.

Real-Time Context Switching

In the AR0134, the user may switch between two full register sets (listed in Table 4) by writing to a context switch change bit in R0x30B0[13]. This context switch will change all registers (no shadowing) at the frame start time and have the new values apply to the immediate next exposure and readout time.

Table 4: Real-Time Context-Switchable Registers

Register Description	Register Number	
	Context A	Context B
y_addr_start	R0x3002	R0x308C
x_addr_start	R0x3004	R0x308A
y_addr_end	R0x3006	R0x3090
x_addr_end	R0x3008	R0x308E
coarse_integration_time	R0x3012	R0x3016
fine_integration_time	R0x3014	R0x3018
y_odd_Inc	R0x30A6	R0x30A8
green1_gain (GreenR)	R0x3056	R0x30BC
blue_gain	R0x3058	R0x30BE
red_gain	R0x305A	R0x30C0
green2_gain (GreenB)	R0x305C	R0x30C2
global_gain	R0x305E	R0x30C4
frame_length_lines	R0x300A	R0x30AA
digital_binning	R0x3032[1:0]	R0x3032[5:4]
column_gain	R0x30B0[5:4]	R0x30B0[9:8]

Features

Note: See the AR0134 Register Reference for additional details.

Operational Modes

The AR0134 works in master (video) or trigger (single frame) modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes.

Note: Trigger mode is not compatible with the HiSPi interface.

Master Mode

In master mode, the exposure period occurs simultaneously with the frame readout (see Figures 13 and 14). This makes master mode the fastest mode of operation. When exposure time is greater than the frame length, the number of vertical blanking rows is increased automatically to accommodate the exposure time.

Figure 13: Master Mode Synchronization Waveform #1

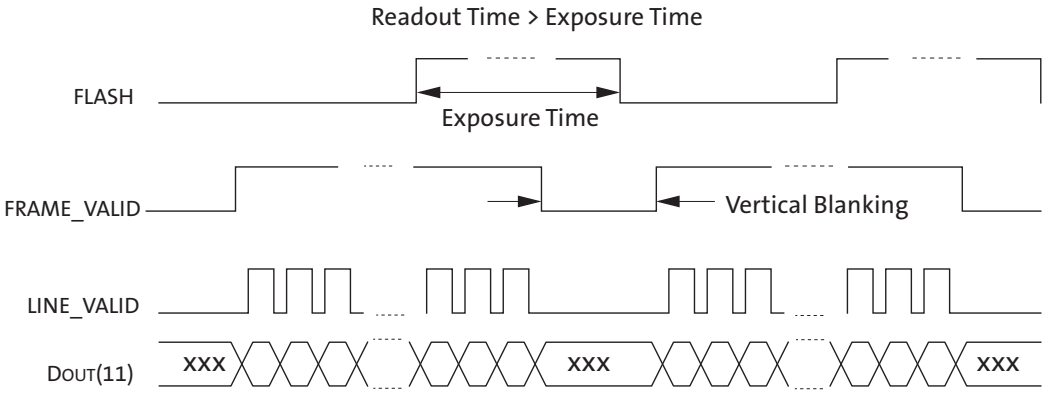
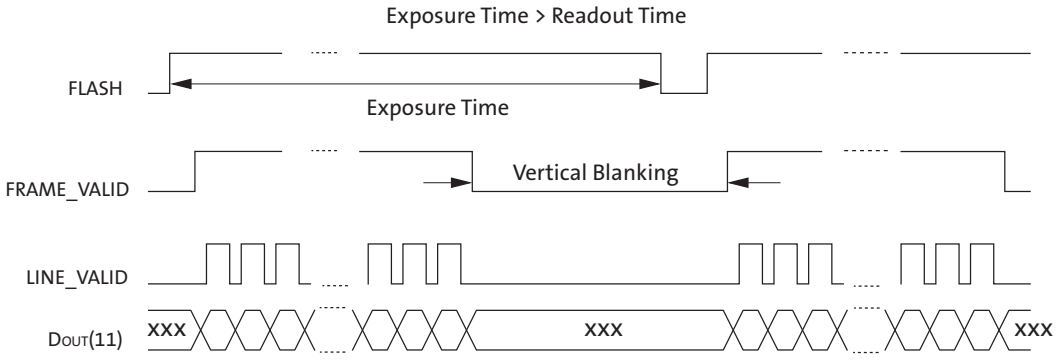


Figure 14: Master Mode Synchronization Waveform #2



Trigger Mode

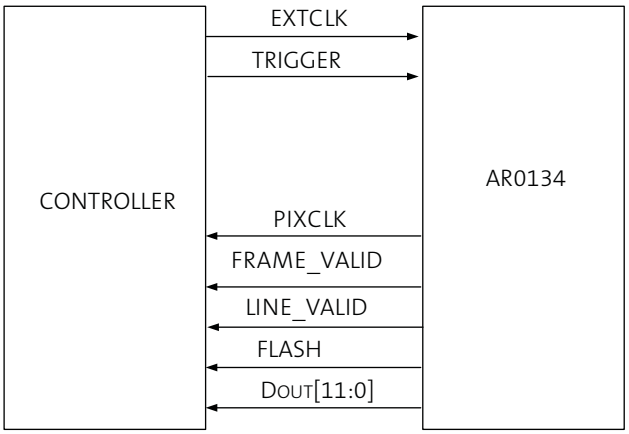
In trigger mode, the exposure period and the frame readout occur sequentially (see Figure 16 and Figure 17 on page 20). This makes trigger mode slower than master mode. Two options of triggering are made available. A Pulsed Trigger mode where only a single frame is output, and an Automatic Trigger mode where a series of frames are output.

Triggered System Details

Many imaging applications commonly require the image sensor to capture an image only after a triggering action has taken place. This triggering action can be the passing of an object on a conveyor belt, the flash of a strobe light, or the press of a button.

The AR0134 offers the ability to synchronize the start of the image sensor's exposure with this triggering action. This synchronization is controlled on the image sensor through the use of the TRIGGER input signal. Additionally, the image sensor offers the flexibility to program the exposure time remotely. This Developer Guide only addresses the single image sensor (non-stereoscopic) mode of operation.

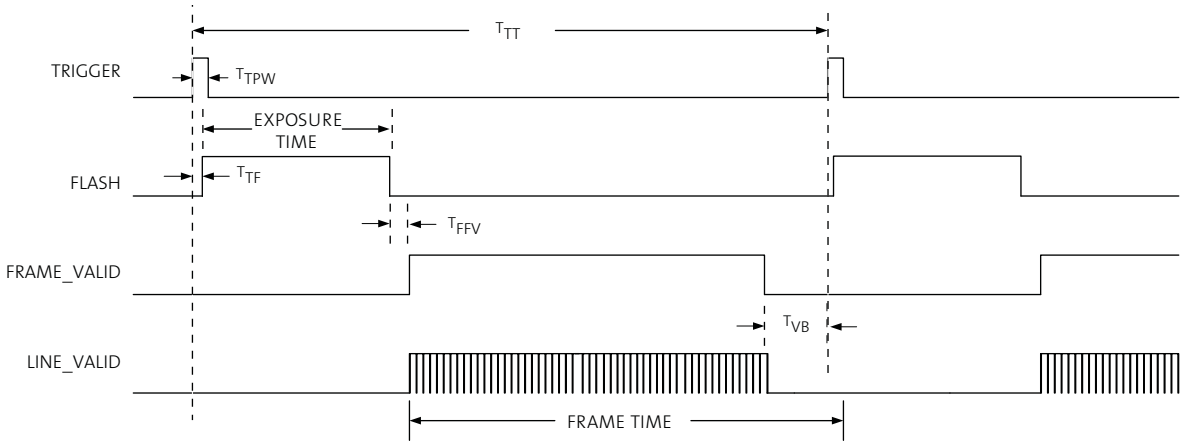
Figure 15: Block Diagram



Trigger Mode Overview

When the image sensor is set to trigger mode, the beginning and duration of the exposure time are controlled. The global shutter feature of the image sensor allows all pixels to be exposed in parallel—all pixels start exposing (integrating charge) simultaneously and stop exposing simultaneously. When exposure stops, the per-pixel integrated charges are digitized and read out of the chip. A new exposure begins only after the readout of all pixels is complete. If the TRIGGER input is left in the asserted state, the sensor will automatically initiate a new frame acquisition sequence upon completion of the current frame.

Figure 16: Pulsed Trigger Mode



Notes:
1. Not drawn to scale.
2. Frame readout shortened for clarity.
3. Progressive scan readout mode shown.

Figure 17: Automatic Trigger Mode

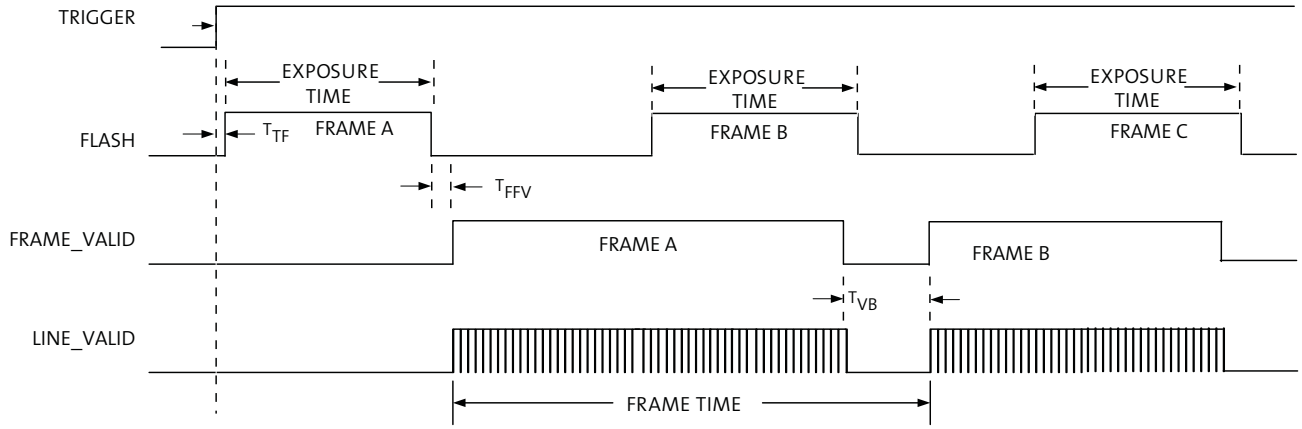


Table 5: Exposure Timing

Symbol	Description	Value
T_{TT}	TRIGGER signal period	T_{TF} + EXPOSURE TIME + T_{FFV} + FRAME TIME
T_{TPW}	TRIGGER signal pulse width	10 row times (MIN)
T_{TF}	TRIGGER to FLASH	8.21 row-times
T_{FFV}	FLASH to FRAME_VALID	18.21 row times
T_{VB}	Vertical blanking time	R0x300A - (R0X3006 - R0x3002 + 1)) * (Active Data Time + Horizontal Blanking Time) (MIN 23Lines)

Notes:
1. EXTCLK-cycle unit is defined as the reciprocal of the EXTCLK input frequency.
2. See "Exposure and Data Synchronization Outputs" on page 22 for the row-time unit definition.
3. To change exposure time, change the coarse integration time registers R0x3012 for Context A or R0x3016 for Context B.
4. To change frame rate, change the T_{TT} value.

Register Settings

The TRIGGER mode of operation requires that register R0x301A (Reset Register) bit 2 be set to "0". Setting this register to "1" will switch the sensor back to the master mode of operation. The general purpose I/O (GPI) pins must also be enabled as shown in Table 6.

Table 6: Snapshot Mode Register Settings

Register	Register Name	Bit	Bit Name	Bit Description	Value in Dec (Hex)
R0x301A	Reset Register	2	Stream	0 = Trigger mode 1 = master mode	0
R0x301A	Reset Register	8	GPI_EN	0 = GPI input buffers disabled 1 =GPI input buffers enabled	1
R0x301A	Reset Register	11	forced_pll_on	0 = PLL powered down in standby 1 =PLL always powered	1

Start of Exposure

The start of exposure is controlled by the TRIGGER input on the image sensor. Normally, TRIGGER is held in a LOW state. To start exposing, this signal is changed to a HIGH state. This HIGH state is then sampled on the rising edge of the master clock (EXTCLK) of the image sensor. TRIGGER must be held HIGH for greater than 10 row times.

Duration of Exposure

The duration of the exposure is set by the value stored in R0x3012, which represents an equivalent number of row-times (see "Exposure and Data Synchronization Outputs" on page 22) to the actual exposure time.

The minimum exposure time supported by the AR0134 image sensor in trigger mode is 3 row-times.

A restriction exists on coarse integration time when using trigger mode to ensure correct output of the FLASH signal. The following values for coarse integration time should be avoided:

$$coarse\_integration\_time = frame\_length\_lines - (active\_rows + col\_correction\_rows\ (8) + delta\_dark\_rows\ (6) + embedded\_stats\ (2) + 7) \quad (EQ\ 7)$$

As an example, if frame_length_lines is 990 and the number of active rows is 960 (964 minus 4 embedded stats and data rows), then an integration time of:

$$(CIT = 990 - (960 + 8 + 6 + 2 + 7)) = 7 \quad (EQ\ 8)$$

should be avoided to ensure proper exposure in trigger mode. This restriction does not apply to master mode operation. If column correction is disabled, the 8 rows in EQ5 should be replaced with zero.

Exposure and Data Synchronization Outputs

The AR0134 image sensor offers an output synchronization signal (FLASH) that can be used to control the flash of a light source. The timing of this signal in trigger mode is similar to the other exposure modes. The signal is normally held in a LOW state. FLASH changes to a HIGH state when the image sensor is exposing (integrating charge). FLASH returns to the normal LOW state once the exposure (set by register R0x3012 (Context A), or register R0x3016 (Context B)) has timed out.

To indicate a valid frame of video data is being output from the image sensor, FRAME_VALID switches to a HIGH state. The change of state occurs slightly over 18 row-times after the exposure time ends. FRAME_VALID returns to a LOW state after the active rows have been read out. The number of active rows plus vertical blanking is stored in the FRAME_LENGTH_LINES register (R0x300A) (default value is 990).

During the valid video frame state, LINE_VALID switches to a HIGH state to indicate a valid row of video data is being presented. LINE_VALID returns to a LOW state after a set number of PIXCLK cycles corresponding to the number of active pixels per line. The number of active pixels plus horizontal blanking is stored in the LINE_LENGTH_PCK register (R0x300C) (required value for trigger mode is 1650).

TRIGGER Input Restrictions

The minimum time between two successive TRIGGER input pulses (shown as T_{TT} in Figure 16 on page 20) is calculated from the exposure time and the frame time. The exposure time is described in "Exposure and Data Synchronization Outputs" on page 22. The frame time may be calculated from two variables: the row-time, and the number of rows-per-frame. The number of rows-per-frame is equal to the sum (R0x300A) of the number of active rows and the number of vertical blanking rows:

$$rows\_per\_frame = active\ rows + vertical\ blanking\ rows \quad \text{(EQ 9)}$$

$$rows\_per\_frame_{default\_settings} = frame\_length\_lines\ (R0x300A) = 990\ rows \quad \text{(EQ 10)}$$

The frame time is equal to the product of the number of rows-per-frame and the row-time.

$$frame\_time = rows\_per\_frame\ x\ (row\_time) \quad \text{(EQ 11)}$$

$$frame\_time_{default\_settings} = (990\ rows) x \left(\frac{22.22\,\mu s}{row}\right) = 22.0ms \quad \text{(EQ 12)}$$

The minimum time between two successive TRIGGER pulses equals the sum of the frame time, the exposure time, T_{TF} and T_{FFV}:

$$T_{TT} = (frame\_time) + (exposure\_time) + (T_{TF} + T_{FFV}) \quad \text{(EQ 13)}$$

Further, the maximum allowable frame rate may be calculated from these same three variables. The maximum frame rate is the reciprocal of the sum of the frame time, the exposure time, trigger to flash, and flash to frame valid times:.

$$frame\_rate = \frac{1}{frame\_time + exposure\_time + T_{TF} + T_{FFV}} \quad \text{(EQ 14)}$$

The TRIGGER pulse period should correspond to the desired frame rate. For individual (asynchronous) trigger pulses, the TRIGGER signal should be asserted no sooner than FRAME_VALID is deasserted, and the minimum of 23 rows of vertical blanking has elapsed.

Example Frame Rate Calculations

Two examples follow on performing frame rate calculations for the AR0134 image sensors, shown in Table 7 below and Table 8 on page 24.

Example 1 shows maximum allowable frame rate or case where trigger pin is only asserted once per frame:

Table 7: Example 1 (With Default Setting for Full Resolution)

Image Sensor Condition	Setting Description	Register [Bits] = Value
Exposure mode	Trigger	R0x301A[2] = 0 R0x301A[8] = 1 R0x301A[11] = 1
PIXCLK frequency	74.25 MHz	N/A
Window height	964[1]	R0x3006 = 959 R0x3002 = 0
Window width	1280	R0x3008 = 1279 R0x3004 = 0
line_length_pck	1650	R0x300C = 1650
frame_length_lines	990	R0x300A = 990
Integration time	100	R0x3012 = 100

Notes: 1. Window height is 964 rows with embedded stats and data enabled.

Step 1: Calculate the row-time.

$$row\_time = \frac{line\_length\_pck}{PIXCLK\_frequency} \quad \text{(EQ 15)}$$

$$row\_time = \frac{1650}{74.25\ MHz} = 22.22\,\mu s \quad \text{(EQ 16)}$$

Step 2: Calculate the rows-per-frame read out.

$$rows\_per\_frame = frame\_length\_lines \quad \text{(EQ 17)}$$

$$rows\_per\_frame = 990\ \ rows \quad \text{(EQ 18)}$$

Step 3: Calculate the frame time.

$$frame\_time = (rows\_per\_frame)x(row\_time) \quad \text{(EQ 19)}$$

$$frame\_time = (990\ rows)x\left(\frac{22.22\mu s}{row}\right) = 22.0ms \quad \text{(EQ 20)}$$

Step 4: Calculate the actual exposure time.

$$exposure\_time = (integration\_time) \times (row\_time)$$
$$exposure\_time = (100\ rows) \times 22.22\mu s = 2.22\dot{m}s \quad \text{(EQ 21)}$$

Step 5: Calculate $T_{TF} + T_{FFV}$.

$$T_{TF} + T_{FFV} = (8.21\ rows + 18.21\ rows) \times row\_time \quad \text{(EQ 22)}$$
$$= 26.42\ rows \times 22.22\mu s$$
$$= 587\mu s$$

(EQ 23)

Step 6: Calculate the maximum allowable frame rate.

$$frame\_rate = \frac{1}{frame\_time + exposure\_time + T_{TF} + T_{FFV}}$$
$$frame\_rate = \frac{1}{22.0ms + 2.22ms + 587\mu s} \quad \text{(EQ 24)}$$
$$frame\_rate = = \frac{1}{24.81ms}$$
$$frame\_rate = = 40.3Hz$$

Table 8: Example 2 (With Default Settings for 720p)

Image Sensor Condition	Setting Description	Register[Bits] = Value
Exposure mode	Trigger	R0x301A[2] = 0 R0x301A[8] = 1 R0x301A[11] = 1
PIXCLK frequency	74.25 MHz	N/A
Window height	720	R0x3006 = 839 R0x3002 = 120
Window width	1280	R0x3008 = 1279 R0x3004 = 0
line_length_pck	1650	R0x300C = 1650
frame_length_lines	747	R0x300A = 747
Integration time	100	R0x3012 = 100

Step 1: Calculate the row-time.

$$row\_time = \frac{line\_length\_pck}{PIXCLK\_frequency} \quad \text{(EQ 25)}$$

$$row\_time = \frac{1650}{74.25\ MHz} = 22.22\,\mu s \quad \text{(EQ 26)}$$

Step 2: Calculate the rows-per-frame read out.

$$rows\_per\_frame = frame\_length\_lines \quad \text{(EQ 27)}$$

$$row\_per\_frame = 747\ rows \quad \text{(EQ 28)}$$

Step 3: Calculate the frame time.

$$frame\_time = (rows\_per\_frame)x(row\_time) \quad \text{(EQ 29)}$$

$$frame\_time = (747\ rows)x\left(\frac{22.22\,\mu s}{row}\right) = 16.6ms \quad \text{(EQ 30)}$$

Step 4: Calculate the actual exposure time.

$$exposure\_time = (integration\_time)x(row\_time) \quad \text{(EQ 31)}$$

$$exposure\_time = (100\ rows \times 22.22\,\mu s) = 2.22ms \quad \text{(EQ 32)}$$

Step 5: Calculate $T_{TF} + T_{FFV}$.

$$\begin{aligned} T_{TF} + T_{FFV} &= (8.21\ rows + 18.21\ rows) \times row\_time \\ &= 26.42\ rows \times 22.22\,\mu s \\ &= 587\,\mu s \end{aligned} \quad \text{(EQ 33)}$$

(EQ 34)

Step 6: Calculate the maximum allowable frame rate.

$$frame\_rate = \frac{1}{frame\_time + exposure\_time + T_{TF} + T_{FFV}}$$

$$frame\_rate = \frac{1}{16.6ms + 2.22ms + 587\,\mu s} \quad \text{(EQ 35)}$$

$$frame\_rate = = \frac{1}{19.4\ ms}$$

$$frame\_rate = = 51.5Hz$$

Reset

The AR0134 may be reset by using RESET_BAR or the reset register.

Hard Reset of Logic

The host system can reset the image sensor by bringing the RESET_BAR pin to a LOW state. Alternatively, the RESET_BAR pin can be connected to an external RC circuit for simplicity. Registers written via the two-wire interface will not be preserved following a hard reset.

Soft Reset of Logic

Soft reset of logic is controlled by bit 0 of the R0x301A Reset register. This bit is a self-resetting bit and also returns to “0” during two-wire serial interface reads. Registers written via the two wire interface will not be preserved following a soft reset.

Output Enable

The AR0134’s outputs can be tri-stated with the OE_BAR pin. Before the external pin can be used to control output enable, set register R0x301A[6] = 0 to disable the output drivers. Then set R0x301A[8] = 1 to enable the input pins (OE_BAR, TRIGGER, and STANDBY). Driving OE_BAR low will enable the output drivers, while driving it high will tri-state the parallel output pins. The parallel outputs can also be tri-stated by setting R0x301A[7] = 0.

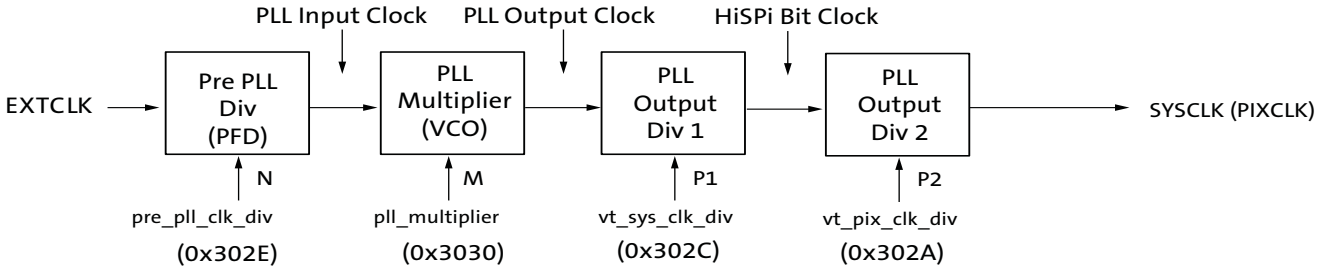
Clocks

PLL-Generated Master Clock

The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and two divider stages to generate the output clock. The clocking structure is shown in Figure 18. The AR0134 default power up state for the PLL dividers is for a pixel clock of 74.25 MHz that is generated from a 27 MHz EXTCLK. PLL control registers can be programmed to generate frequencies other than the default power up state. Refer to Table 9 on page 27 for PLL parameters for the parallel interface, and Table 11 on page 27 for the HISPi interface. Example PLL configurations are also provided using an EXTCLK of 27MHz.

Note: The PLL control registers must be programmed while the sensor is in the software Standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is undefined.

Figure 18: PLL Block Diagram



The PLL is enabled by default on the AR0134. To configure and use the PLL:

1. Bring the AR0134 up as normal; make sure that fEXTCLK is between 6 and 50 MHz and ensure the sensor is in software standby (R0x301A[2]= 0). PLL control registers must be set in software standby.
2. Set pll_multiplier, pre_pll_clk_div, vt_sys_clk_div, and vt_pix_clk_div based on the desired input (f_{EXTCLK}) and output (f_{PIXCLK}) frequencies. Determine the M, N, P1, and P2 values to achieve the desired f_{PIXCLK} using the formula:

$$f_{PIXCLK} = (f_{EXTCLK} \times M) / (N \times P1 \times P2) \quad \text{(EQ 36)}$$

where

M = pll_multiplier
N = pre_pll_clk_div
P1 = vt_sys_clk_div
P2 = vt_pix_clk_div

3. Wait 1ms to ensure that the VCO has locked.
4. Set R0x301A[2]=1 to enable streaming and to switch from EXTCLK to the PLL-generated clock.

Table 9: PLL Parameters for the Parallel Interface

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	50	MHz
VCO Clock	FVCO	384	768	MHz
Output Clock	PIXCLK		74.25	Mpixel/s

Table 10: Example PLL Configuration for the Parallel Interface

Parameter	Register Value	Output
FVCO		594 MHz
pre_pll_clk_div (N)	2	
pll_multiplier (M)	44	
vt_sys_clk_div	1	
vt_pix_clk_div	8	
PIXCLK		74.25 MPixel/s
Output pixel rate		74.25 MPixel/s

Table 11: PLL Parameters for the Serial Interface

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	50	MHz
VCO Clock	FVCO	384	768	MHz
Readout Clock	PIXCLK	74.25		Mpixel/s
Output Serial Data Rate Per Lane	FSERIAL	280 (HiSPi)	700 (HiSPi)	Mbps
Output Serial Clock Speed Per Lane	FSERIAL_CLK	140 (HiSPi)	350(HiSPi)	MHz

Table 12: Example PLL Configurations for the Serial Interface

Parameter	Register Value		Units
	3-lane	2-lane	
FVCO	742.5	445.5	MHz
pre_pll_clk_div	2	2	
pll_multiplier	55	33	
vt_sys_clk_div	2	1	
vt_pix_clk_div	5	6	
HiSPi Bit Clock	371.25	445.5	MHz
HiSPi Differential Clock	185.63	222.75	MHz
PIXCLK	74.25	74.25	Mpixel/s

Notes:
1. The PLL can be bypassed at any time (sensor will run directly off EXTCLK) by setting R0x30B0[14]=1. However, only the parallel data interface is supported with the PLL bypassed. The PLL is always bypassed in software standby mode. PLL bypass should only be enabled or disabled while the sensor is in standby.
2. The following restrictions apply to the PLL tuning parameters:
   $32 \le M \le 255$
   $1 \le N \le 63$
   $1 \le P1 \le 16$
   $4 \le P2 \le 16$
3. The VCO frequency, defined as $f_{VCO} = f_{EXTCLK} \times M/N$ must be within 384–768 MHz.
4. If using HiSPi output mode, use the following settings for P2 (vt_pix_clk_div).
   4a. If 12-bit mode (3 lanes): set P2 (R0x302A) = 5
   4b. If 12-bit mode (2 lanes): set P2 (R0x302A) = 6

The user can utilize the Register Wizard tool accompanying DevWare to generate PLL settings given a supplied input clock and desired output frequency.

Spread-Spectrum Clocking

To facilitate improved EMI performance, the external clock input allows for spread spectrum sources, with no impact on image quality. Limits of the spread spectrum input clock are:

- 5% maximum clock modulation
- 35 kHz maximum modulation frequency
- Accepts triangle wave modulation, as well as sine or modified triangle modulations.

Stream/Standby Control

The sensor supports two standby modes: Hard Standby and Soft Standby. In both modes, external clock can be optionally disabled to further minimize power consumption. If this is done, then the power-up sequence described in the AR0134 data sheet must be followed.

Soft Standby

Soft Standby is a low power state that is controlled through register R0x301A[2]. Depending on the value of R0x301A[4], the sensor will go to standby after completion of the current frame readout (default behavior) or after the completion of the current row readout. When the sensor comes back from Soft Standby, previously written register settings are still maintained. Soft standby will not occur if the TRIGGER pin is held high. A specific sequence needs to be followed to enter and exit from Soft Standby.

Entering Soft Standby:
1. Set R0x301A[12] = 1 if serial mode was used
2. Set R0x301A[2] = 0 and drive the TRIGGER pin LOW.
3. External clock can be turned off to further minimize power consumption (Optional)

Exiting Soft Standby:
1. Enable external clock if it was turned off
2. R0x301A[2] = 1 or drive the TRIGGER pin HIGH.
3. R0x301A[12] = 0 if serial mode is used

Hard Standby

Hard Standby puts the sensor in a lower power state. Register settings will be preserved.

A specific sequence needs to be followed to enter and exit from Hard Standby.

Entering Hard Standby:
1. R0x301A[8] = 1
2. R0x301A[12] = 1 if serial mode was used
3. Assert STANDBY pin
4. External clock can be turned off to further minimize power consumption (optional)

Exiting Hard Standby:
1. Enable external clock if it was turned off
2. De-assert STANDBY pin
3. Set R0x301A[8] = 0 (unless other inputs are used such as trigger, output_en, etc.)

Window Control

Registers x_addr_start, x_addr_end, y_addr_start, and y_addr_end control the size and starting coordinates of the image window.

The exact window height and width out of the sensor is determined by the difference between the Y address start and end registers or the X address start and end registers, respectively.

The AR0134 allows different window sizes for context A and context B.

Blanking Control

Horizontal blank and vertical blank times are controlled by the line_length_pck and frame_length_lines registers, respectively.

- Horizontal blanking is specified in terms of pixel clocks. It is calculated by subtracting the X window size from the line_length_pck register. The minimum horizontal blanking is 108 pixel clocks.
- Vertical blanking is specified in terms of numbers of lines. It is calculated by subtracting the Y window size from the frame_length_lines register. The minimum vertical blanking is 23 lines.

The actual imager timing can be calculated using Table 2 on page 14 and Table 3 on page 15, which describe the Line Timing and FV/LV signals.

Readout Modes

By default, the resolution of the output image is the full width and height of the FOV as defined above. The output resolution can be reduced by digital binning.

Digital Binning

All of the pixels in the FOV contribute to the output image in digital binning mode. This can result in a more pleasing output image with reduced artifacts. It also improves low-light performance. For RGB and monochrome mode, the digital binning factor is set by the register DIGITAL_BINNING (R0x3032). For Context A, use bits [1:0], for Context B, use bits [5:4]. Available settings are: 00 = No binning; 01 = Horizontal binning; 10 = Horizontal and vertical binning. For RGB mode, resampling must be enabled by setting bit 4 of register 0x306E. For monochrome operation, R0x30B0[7] must be set to 1. Enabling horizontal or vertical binning mode does not affect the sensor frame rate.

Skipping

Skipping reduces resolution by using only selected rows from the FOV in the output image. In skip mode, entire rows of pixels are not sampled, resulting in a lower resolution output image. A skip 2X mode skips one Bayer pair of pixels for every pair output. Skipping is set by R0x30A6 (context A) and R0x30A8 (context B). The maximum supported skip is 64 rows. Both Bayer and monochrome skip modes are supported. Refer to Table 13 on page 30 for supported skip factors.

When enabling a skip mode, register R0x30B0[10] should be set low. It should be returned to the default state (R0x30B0[10]=1) when exiting skip modes. If this is not done, a noticeable change in intensity may be observed when entering and exiting skip mode.

Table 13: Skip Mode Settings

Skip Factor	R0x30A6 (R0x30A8)
No Skip	0x0001
2	0x0003
4	0x0007
8	0x000F
16	0x001F
32	0x003F
64	0x007F

Figure 19: Pixel Readout (no skipping)

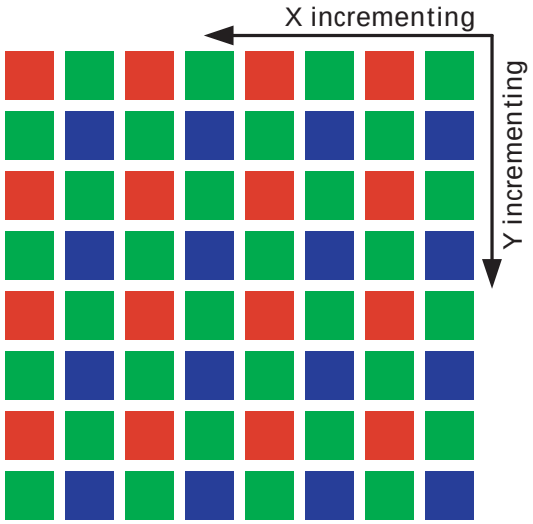


Figure 20: Pixel Readout (Row Skip 2X Bayer)

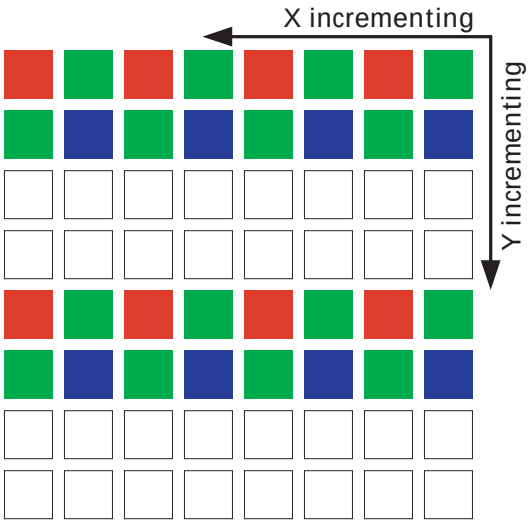
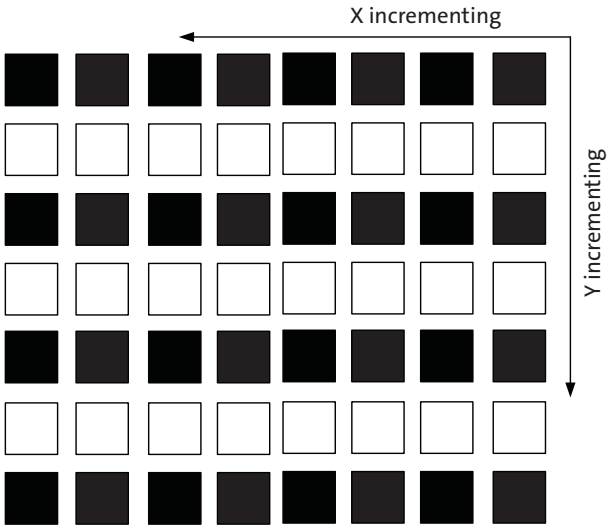


Figure 21: Pixel Readout (Row Skip 2X Monochrome)



Mirror

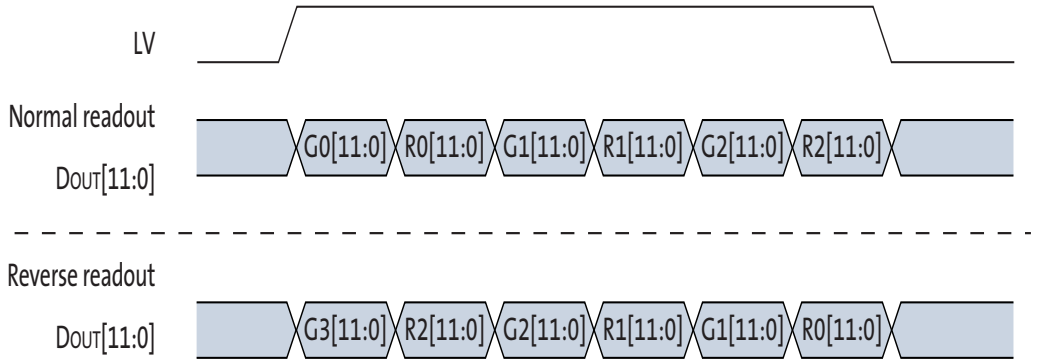
Column Mirror Image

By setting R0x3040[14] = 1, the readout order of the columns is reversed, as shown in Figure . The starting color, and therefore the Bayer pattern, is preserved when mirroring the columns.

When using horizontal mirror mode, the user must retrigger column correction. Refer to the column correction section to see the procedure for column correction retriggering.

Bayer resampling must be enabled, by setting bit 4 of register 0 x 306E[4] = 1.

Table 14: Six Pixels in Normal and Column Mirror Readout Modes

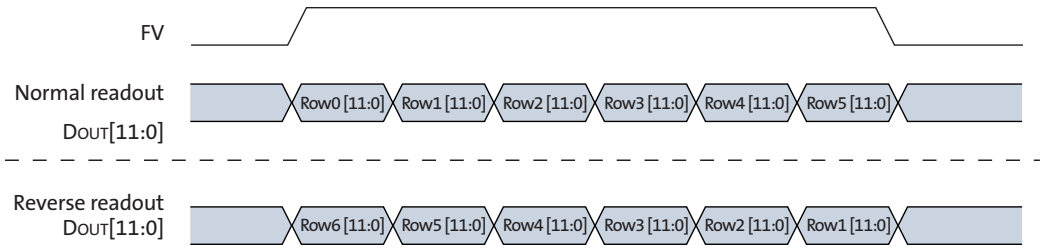


Row Mirror Image

By setting R0x3040[15] = 1, the readout order of the rows is reversed as shown in Figure 22. The starting Bayer color pixel is maintained in this mode by a 1-pixel shift in the imaging array. When using horizontal mirror mode, the user must retrigger column correction. Refer to the column correction section to see the procedure for column correction retriggering.

Bayer resampling must be enabled, by setting bit 4 of register 0 x 306E[4] = 1.

Figure 22: Six Rows in Normal and Row Mirror Readout Modes



Maintaining a Constant Frame Rate

Maintaining a constant frame rate while continuing to have the ability to adjust certain parameters is the desired scenario. This is not always possible, however, because register updates are synchronized to the read pointer, and the shutter pointer for a frame is usually active during the readout of the previous frame. Therefore, any register changes that could affect the row time or the set of rows sampled causes the shutter pointer to start over at the beginning of the next frame.

By default, the following register fields cause a "bubble" in the output rate (that is, the vertical blank increases for one frame) if they are written in video mode, even if the new value would not change the resulting frame rate. The following list shows only a few examples of such registers; a full listing can be seen in the AR0134 Register Reference.

- X_Addr_Start
- X_Addr_End
- Y_Addr_Start
- Y_Addr_End
- Frame_Length_Lines
- Line_Length_Pclk
- Coarse_Integration_Time
- Fine_Integration_Time
- Read_Mode

The size of this bubble is (Integration_Time × ^{t}ROW), calculating the row time according to the new settings.

The Coarse_Integration_Time and Fine_Integration_Time fields may be written to without causing a bubble in the output rate under certain circumstances. Because the shutter sequence for the next frame often is active during the output of the current frame, this would not be possible without special provisions in the hardware. Writes to these registers take effect two frames after the frame they are written, which allows the integration time to increase without interrupting the output or producing a corrupt frame (as long as the change in integration time does not affect the frame time).

Synchronizing Register Writes to Frame Boundaries

Changes to most register fields that affect the size or brightness of an image take effect on the frame after the one during which they are written. These fields are noted as "synchronized to frame boundaries" in the AR0134 Register Reference. To ensure that a register update takes effect on the next frame, the write operation must be completed after the leading edge of FV and before the trailing edge of FV.

As a special case, in trigger mode, register writes that occur after FV but before the next trigger will take effect immediately on the next frame, as if there had been a Restart. However, if the trigger for the next frame occurs during FV, register writes take effect as with video mode.

Fields not identified as being frame-synchronized are updated immediately after the register write is completed. The effect of these registers on the next frame can be difficult to predict if they affect the shutter pointer.

Figure 23: Latency For Single Buffered Registers - Coarse Integration Time Example

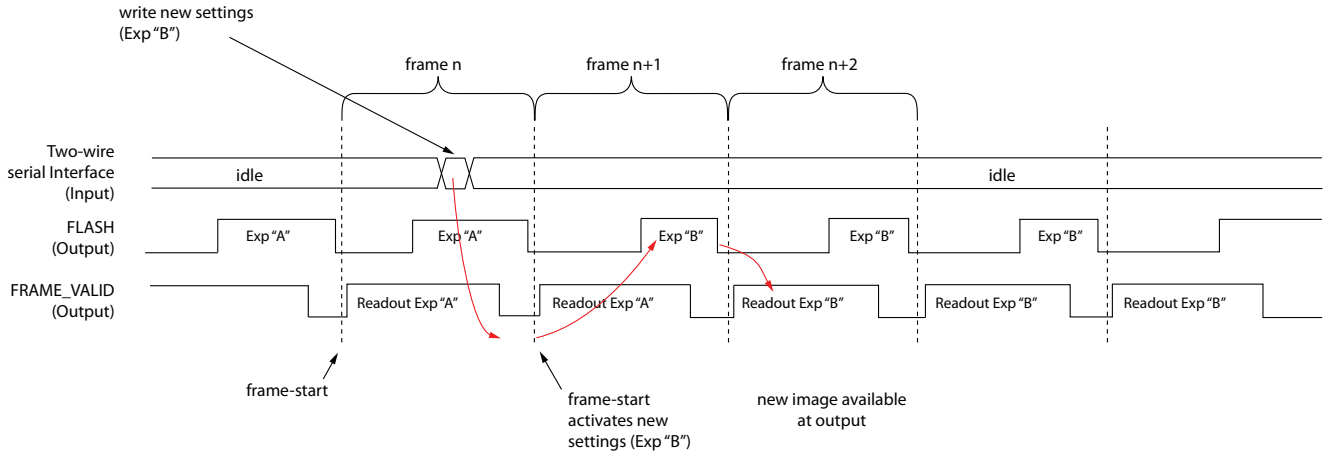


Figure 24: Latency For Double Buffered Registers - Column Gain Example

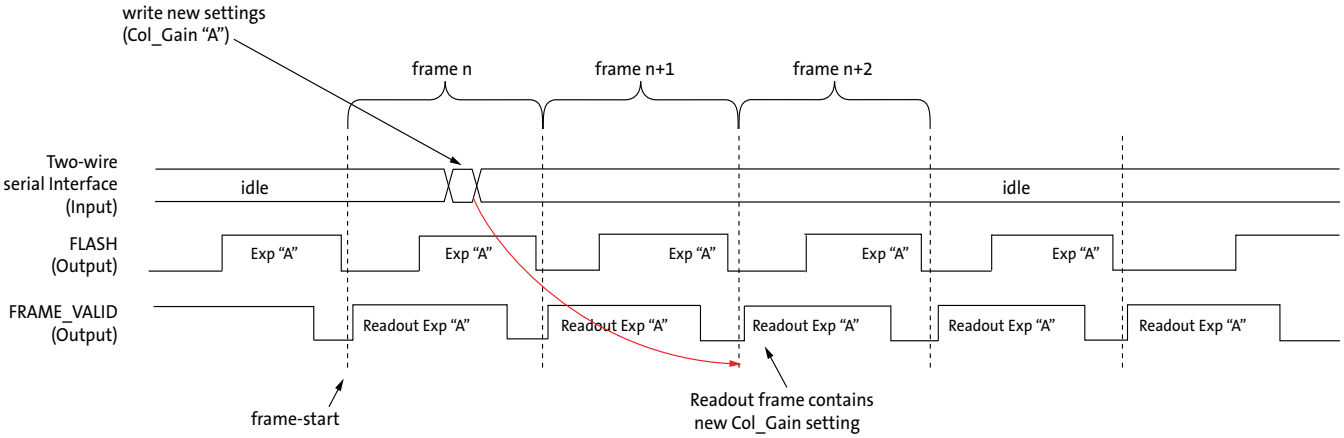
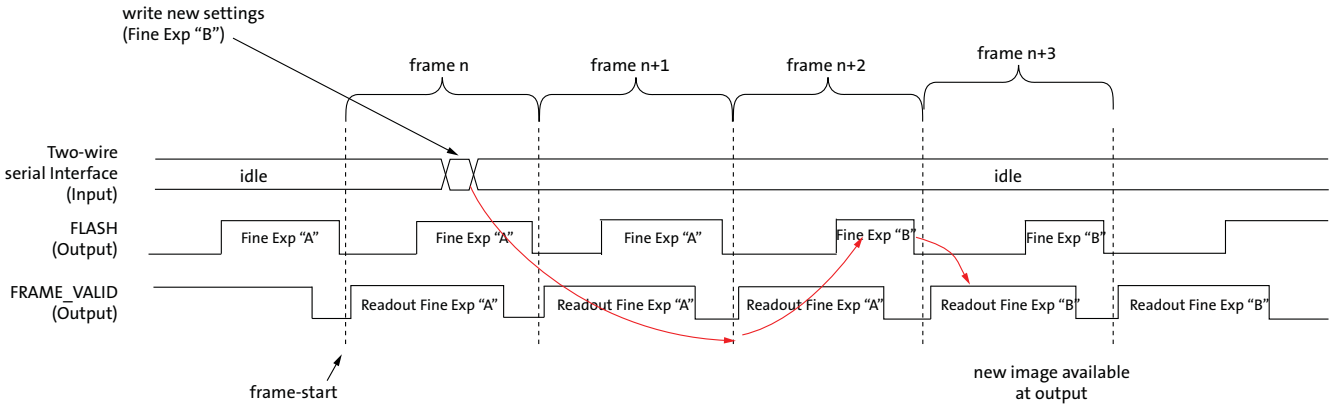


Figure 25: Latency For Double Buffered Registers - Fine Integration Time Example



Restart

To restart the AR0134 at any time during the operation of the sensor, write a "1" to the Restart register (R0x301A[1] = 1). This has two effects: first, the current frame is read out and the sensor enters standby. Second, any writes to frame-synchronized registers and the shutter width registers take effect immediately, and a new frame starts. The current frame completes before the new frame is started, so the time between issuing the Restart and the beginning of the next frame is a maximum of t_{FRAME}.

Temperature Sensor

The AR0134 sensor has a built-in PTAT-based (Proportional To Absolute Temperature) temperature sensor, accessible through registers, that is capable of measuring die junction temperature. The temperature sensor can be enabled by writing R0x30B4[0]=1 and R0x30B4[4]=1. After this, the temperature sensor output value can be read from R0x30B2[10:0].

The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function as in Equation 37 can be used to convert the ADC output value to the final temperature in degrees Celsius.

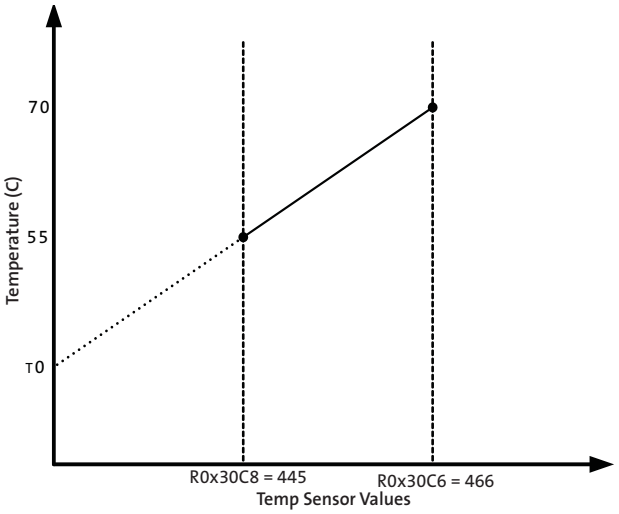
$$\text{Temperature} = \text{slope} \times \text{R0x30B2[10:0]} + \text{T0} \quad \text{(EQ 37)}$$

For this conversion, a minimum of 2 known points are needed to construct the line formula by identifying the slope and y-intercept "T0". These calibration values can be read from registers R0x30C6 and R0x30C8 which correspond to values read at 70°C and 55°C respectively. Once read, the slope and y-intercept values can be calculated and used in the above equation.

Example: What is the temperature in degrees Celsius when R0x30B2 = 0x1A2 (418)?

For this particular sensor, the 70°C calibration data reads R0x30C6 = 0x01D2 (466), and the 50°C calibration data reads R0x30C8 = 0x01BD (445). From these values, the correct temperature reading can be found as follows:

Figure 26: Calculating Temperature Sensor Value



slope = (70 - 55) / (466 - 445) = (15/21) = 0.714

From here, the intercept T0 can be found:

55 = (0.714) x (445) + T0
T0 = -262.73

Now, the temperature corresponding to a register reading of 0x1A2 can be determined:

Temperature = (0.714) x (418) - 262.73
Temperature = 35.7°C

For more information on the temperature sensor registers, refer to the AR0134 Register Reference.

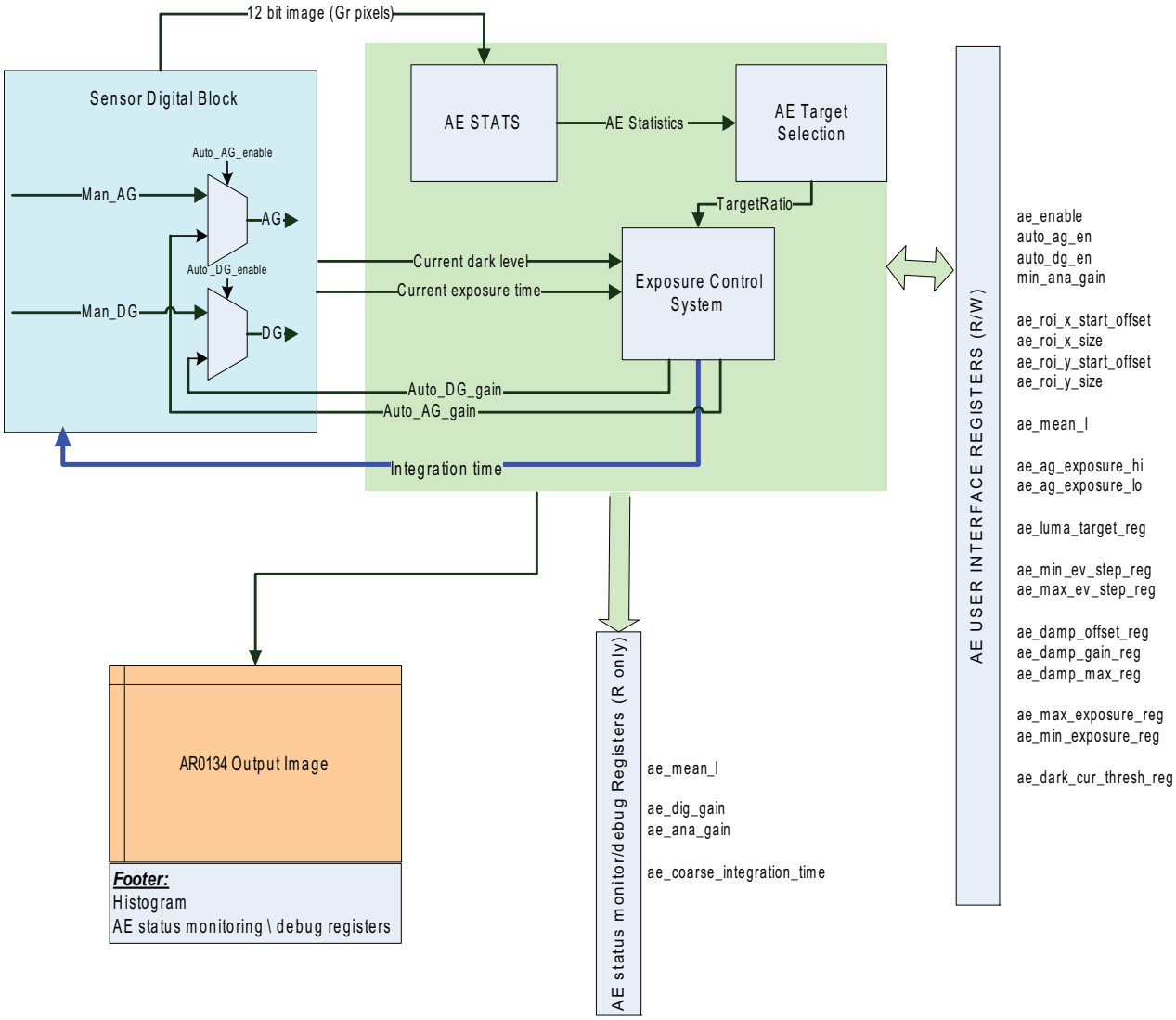
Auto Exposure

The integrated automatic exposure control (AEC) is responsible for ensuring that optimal settings of exposure and gain are computed and updated every other frame. AEC can be enabled or disabled by R0x3100[0]. When AEC is disabled (R0x3100[0] = 0), the sensor uses the manual exposure value in the coarse and fine integration time registers and the manual gain value in the gain registers. When AEC is enabled (R0x3100[0]=1), the target luma value is set by AE_LUMA_TARGET_REG (R0x3102). For AR0134, this target luma has a default value of 0x0500. The luma target maximum auto exposure value is limited by R0x311C; the minimum auto exposure is limited by R0x311E. These values are in units of line-times. The minimum value for register 0x311E is 1 line. The exposure control measures current scene luminosity by accumulating a histogram of Gr pixel values while reading out a frame. It then compares the current luminosity to the desired output luminosity. Finally, the appropriate adjustments are made to the exposure time and gain.

Auto Exposure Implementation

The AR0134 Auto Exposure control is implemented as three main blocks - AE Stats Calculation, AE Target Selection, and an Exposure Control System. See Figure 27 for details.

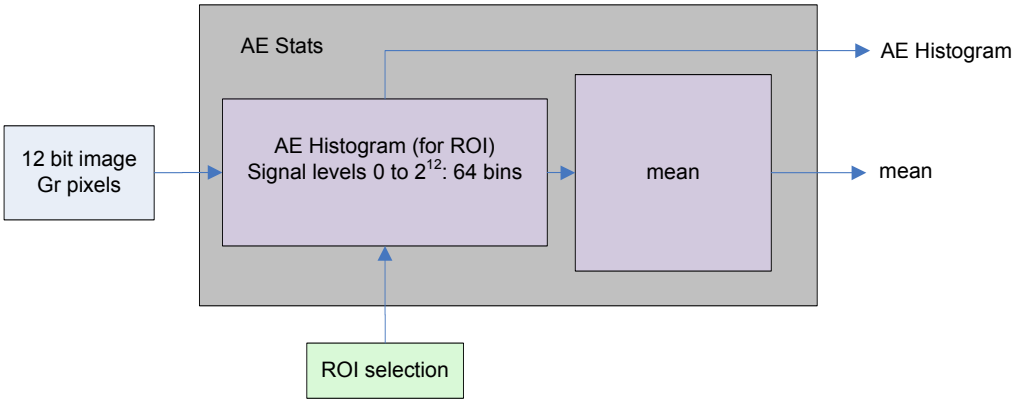
Figure 27: AE Block Diagram



AE Embedded Statistics and Data

The AE Stats Calculation block (Figure 28) takes the user specified Region of Interest (ROI) and creates a histogram of 64 evenly distributed bins from 0 to the maximum code value of 4095 based on Gr pixels. If no ROI is specified, statistics are gathered from the full output frame. From this histogram, all relevant auto exposure statistics are generated:

Figure 28: AE Stats Calculation Block



1.AE Histogram: 64 evenly spaced bins for digital code values 0 to 4095, If a ROI is specified, the histogram is populated only with Gr pixels which lie in the ROI.

2.mean: Mean code value of AE Histogram

The generation of statistics for use by off-chip AE algorithms must be enabled by setting register R0x3064[7] = 1. Embedded statistics will not be output if this register is not set. Embedded data may also be enabled by setting register R0x3064[8] = 1, but is not necessary for statistics generation. To enable on-chip auto exposure, however, both embedded stats and data must be enabled.

All the statistics data (including histogram data) is embedded in the two rows immediately following the image. The embedded statistics are output as shown in Figure 30. The first line contains histogram data. Only histogram data for bins 0 to 63 are relevant - higher bins will output all zeros. The second line contains statistics based on the histogram for the current frame. The only relevant statistic for AR0134 auto exposure is the mean. If the on-chip auto exposure is not used, it is recommended that auto exposure algorithms be developed based on the histogram data found in line 1.

Figure 29: Frame Format with Embedded Data Lines Enabled

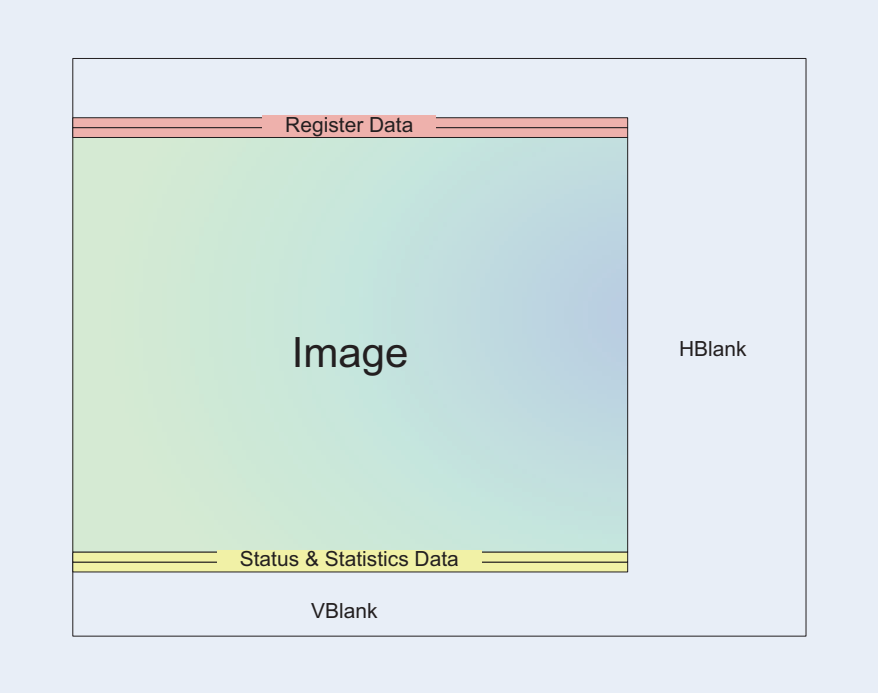
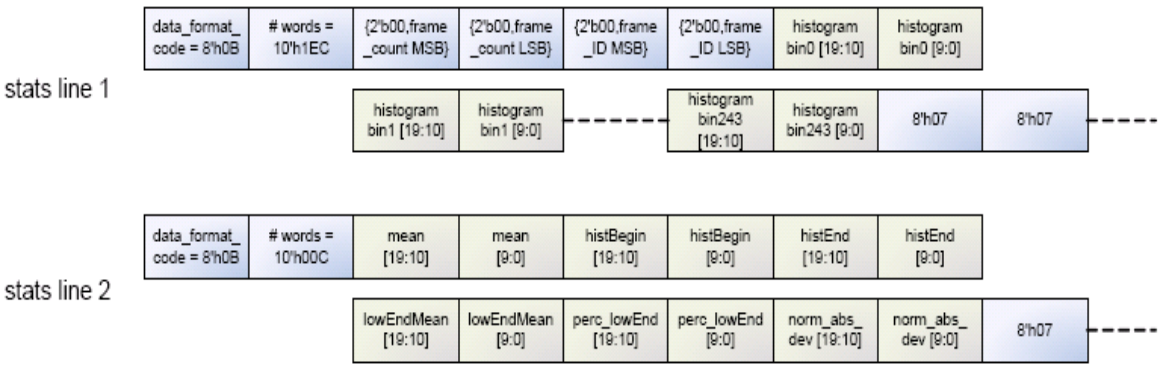


Figure 30: Embedded Statistics Format



The embedded data contains the configuration of the image being displayed, and is found in the first two rows of the image. This includes all register settings used to capture the current frame. The registers embedded in these rows are as follows:

Line 1: Registers R0x3000 to R0x312F

Line 2: Registers R0x3136 to R0x31BF, R0x31D0 to R0x31FF

Only values for registers found in the Register Reference document are relevant. The format of the embedded register data transmission is as follows. In parallel mode, since the pixel word depth is 12 bits/pixel, the sensor's 16-bit register data will be transferred

over 2 pixels where the register data will be broken up into 8msb and 8 LSB. The alignment of the 8-bit data will be on the 8 MSB bits of the 12-bit pixel word. For example, if a register value of 0x1234 is to be transmitted, it will be transmitted over two 12-bit pixels as follows: 0x120, 0x340. The 10-bit histogram data is not broken up and is output msb aligned over the 12 bit parallel interface and padded with zeros.

AE Target Selection

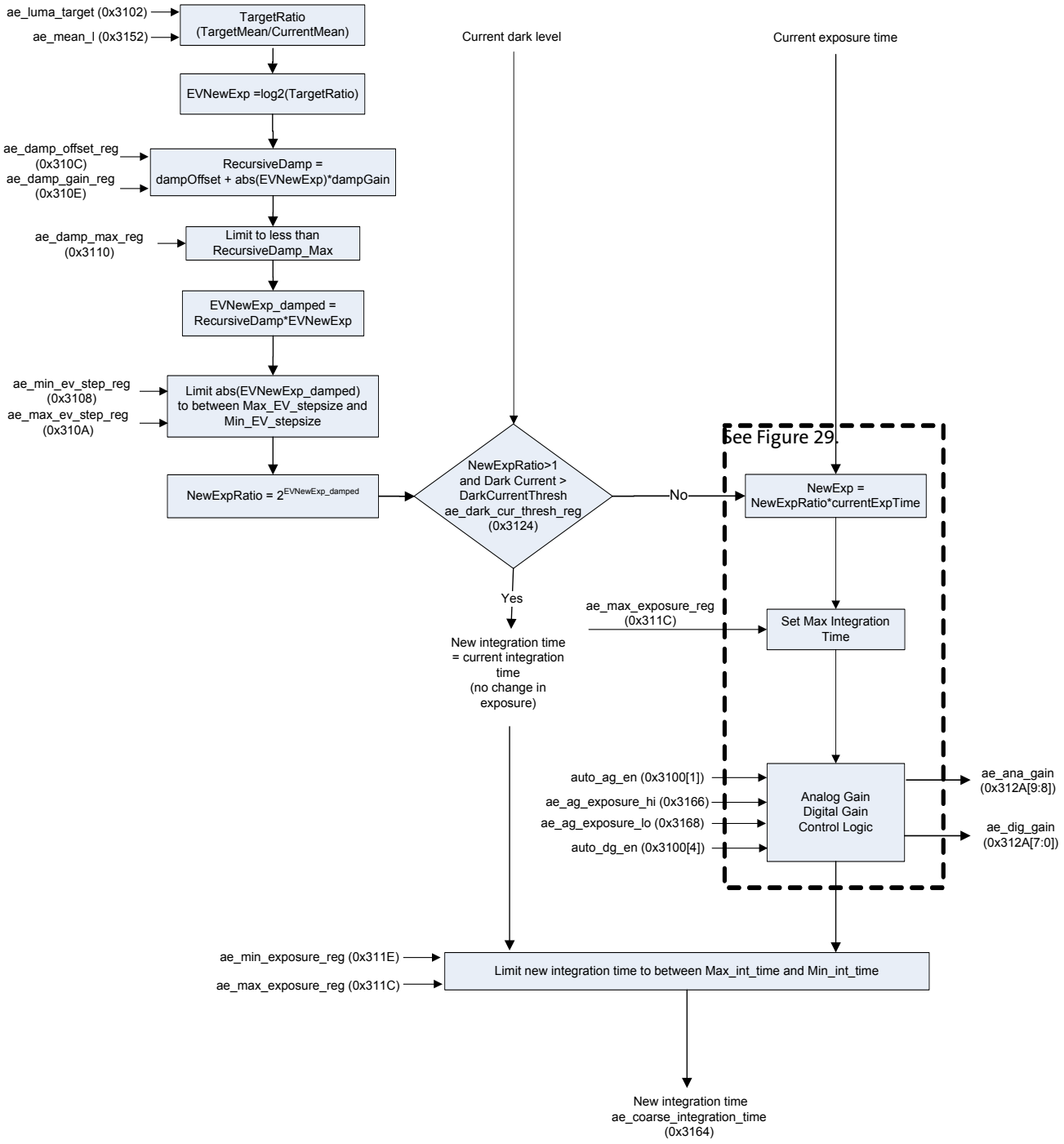
The Exposure Target Selection block determines a ratio based on the mean value of the generated histogram of the current frame, and the target mean value as specified by the user (R0x3102). This ratio allows the Control System to determine how much and in what direction to adjust the exposure relative to the current exposure value.

The mean target ratio (TargetRatio) is the exposure change, expressed as a ratio, to move the current image mean (CurrentMean) to a user-specified mean target (TargetMean). See the “Exposure Control System” section and Figure 31 for more information.

Exposure Control System

The Exposure Control System outputs the new integration time along with a damping factor to prevent too rapid of a response. If enabled, analog and digital gains will be selected as well. The Control System will also monitor the dark current. If the Exposure Target Selection block indicates that the exposure should be increased, but the dark current exceeds a user specified threshold, the Control System will maintain the current integration time. The automatic digital and analog gains and exposure limits enclosed by the dashed line in Figure 31 is illustrated in more detail in Figure 33 on page 45 and described in “Controlling Auto Exposure” on page 43.

Figure 31: Exposure Control System



Values found here are described in Table 15 on page 43.

Table 15: Exposure Control Variables

Internal Value	Description
EVNewExp	Target ratio translated into EV units (stops). Can be positive or negative. In EV units, >0 means exposure is increasing, <0 means exposure is decreasing.
RecursiveDamp	Damping factor. Should be >0 and <1 for desirable AE operation. If less than 0, AE will step further from the target; if greater than 1, AE will overstep the target.
EVNewExp_damped	New exposure step in EV units. Can be positive or negative.
NewExpRatio	New exposure step as ratio. Should be positive. As ratio, >1 means exposure is increasing, <1 means exposure is decreasing.
NewExp	New exposure expressed as rows of integration or possibly msec (depends on rest of system).

Auto Exposure Control

Enabling Auto Exposure

Several registers are used to enable various features of the automatic exposure control. The auto exposure block is enabled or disabled by register R0x3100[0]. By default, the AEC will only modify the coarse integration time to reach the target exposure. If enabled, analog and digital gains may be adjusted as well. Analog gain adjustment is enabled by setting auto_ag_en (R0x3100[1] = 1), and digital gain adjustment is enabled by setting auto_dg_en (R0x3100[4] = 1). A minimum column gain (1x, 2x, 4x, 8x), min_ana_gain, may be defined in register R0x3100[6:5]. Digital gain may be adjusted from 1x to 7.97x. A summary of AEC enable registers is listed in Table 16.

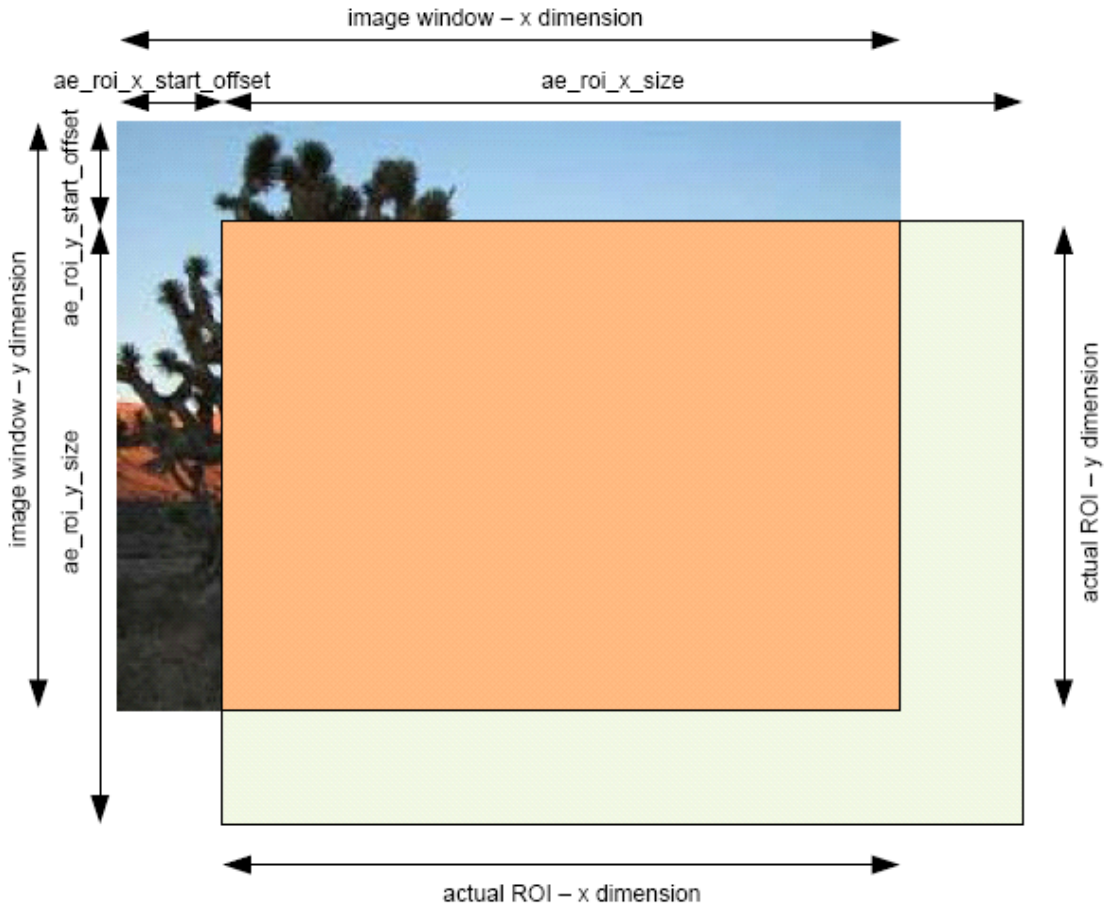
Table 16: AE Enable Registers

Register	Name	Function
0x3100[0]	ae_enable	0: On-chip AE disabled 1: On-chip AE enabled
0x3100[1]	auto_ag_en	0: AE will not control analog gain 1: AE will control analog gain
0x3100[4]	auto_dg_en	0: AE will not control digital gain 1: AE will control digital gain
0x3100[6:5]	min_ana_gain	Minimum analog gain to be used by AE 00: 1x (default) 01: 2x 10: 4x 11: 8x

Controlling Auto Exposure

The histogram is generated and statistics calculated based on the Gr pixels within a user specified region of interest. The ROI is specified by four programmable register values - ae_roi_x_start_offset, ae_roi_y_start_offset, ae_roi_x_size and ae_roi_y_size. The ae_roi_x_start_offset and ae_roi_y_start_offset values define the starting coordinate of the ROI with respect to the image window that is output and the ae_roi_x_size and ae_roi_y_size values define the dimensions of the ROI. Each value must be an even number. If the requested ROI extends 'beyond' the image window then it will be restricted in size such that the final pixel of the ROI will be the final pixel of the image window, as illustrated in Figure 32

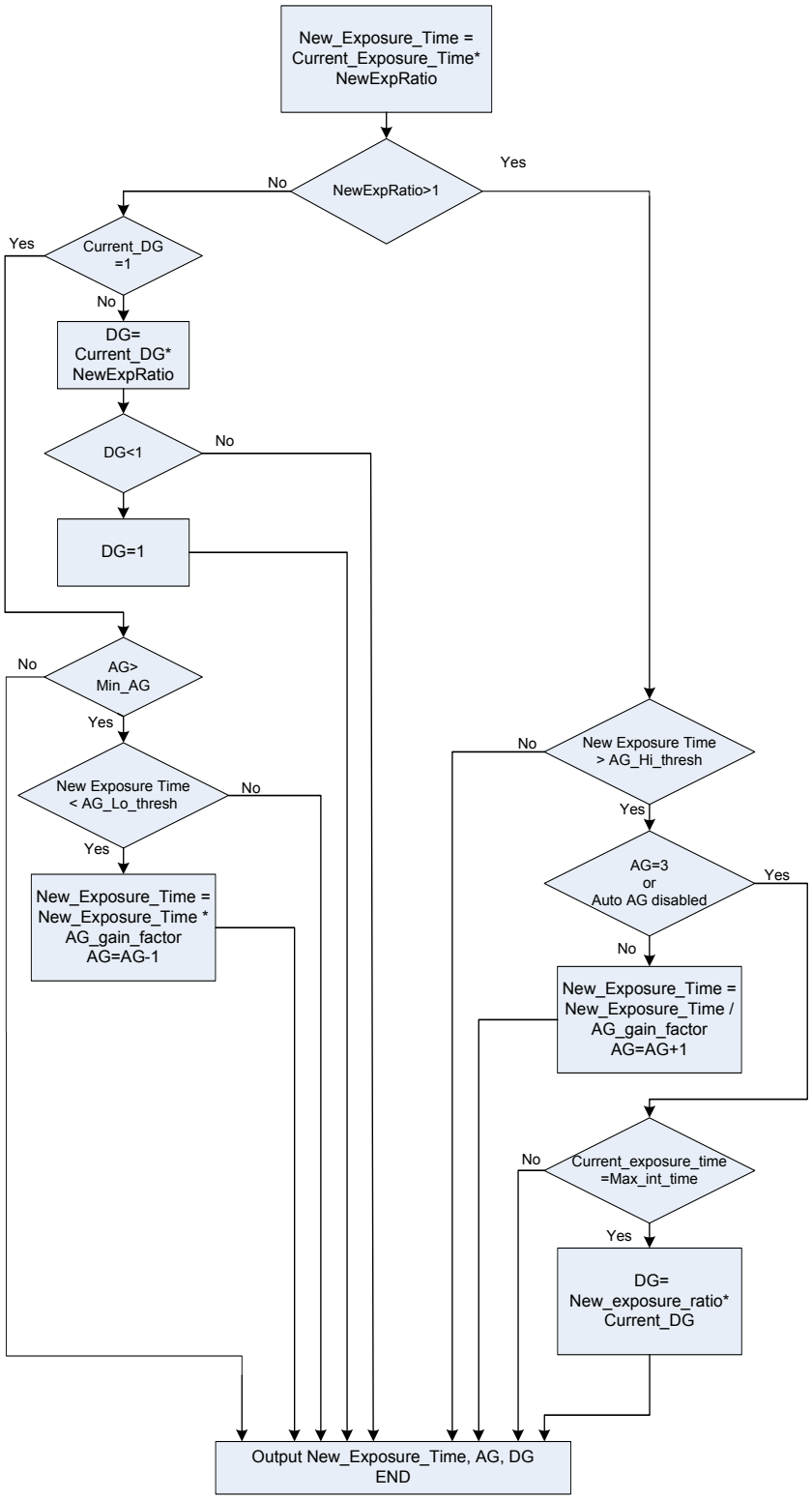
Figure 32: Selecting the ROI



The target luma value may be set in the ae_luma_target_reg register. The AE Target Selection block will use this value to determine the target ratio provided to the Exposure Control System as illustrated in Figure 31 on page 42. The exposure range can be limited by setting values for ae_max_exposure_reg and ae_min_exposure_reg. The integration time fed back to the Sensor Digital Block (see Figure 27 on page 38) will not fall outside of this specified range.

To extend the exposure range, the AE logic can also automatically adjust analog gain and digital gain. The controls for enabling automatic analog and digital gain selection may be found in Table 16 on page 43. The control flow chart is shown in Figure 33 and is an expanded view of the portion of Figure 31 on page 42 that is enclosed by the dashed line.

Figure 33: Automatic Gain Control



If auto_ag_en is set, the automatic adjustment of analog gains may be restricted based on integration time. By setting a value for ae_ag_exposure_hi, the analog gain will not be increased until the integration time set by this register is reached. Similarly, the analog gain will not be decreased unless the integration time is reduced below the value set in ae_ag_exposure_lo. To avoid oscillation, the ae_ag_exposure_lo setting should be lower than the ae_ag_exposure_hi setting. Refer to Table 17 on page 47 for auto exposure control registers.

The integration time and analog gain selected by the exposure control system may be found in the ae_coarse_integration_time (R0x3164) and ae_ana_gain(R0x312A[9:8]) registers, respectively. The minimum analog gain to be selected may be set in the min_ana_gain (R0x3100[6:5]) register, and can be 1x, 2x, 4x, or 8x. If auto_dg_en (R0x3100[4]) is set, the digital gain selected by the exposure control system can be read from register ae_dig_gain (R0x312A[7:0]). The digital gain can vary from 1 to 7.97. The minimum step is 1/32.

The step size of the AE control may be configured. Both a minimum and maximum step size may be set in units of EV (exposure value) steps in registers 0x3108 and 0x310A, respectively. The step size represents the minimum or maximum value that the AE Target Selection will use for the next exposure value. It does not represent the incremental change from frame to frame. The selected new exposure value will be clipped to the minimum EV step if it is less than the value specified in R0x3108. Because the minimum step size in EV units is typically a small number less than one, it should be scaled by 256 before setting the register value.

Changes in exposure are smoothed based on damping parameters. A maximum damping value may be specified in R0x3110. Additional damping controls include ae_damp_gain_reg and ae_damp_offset_reg. These can be thought of as a coarse and fine damping control, respectively.

At high temperature, the sensor may have high dark current which will increase with longer exposures. To avoid increasing the exposure when there is excessive dark current, AE has a dark current check. The sensor supplies the current dark current level to AE and if the dark current is greater than the user-specified (R0x3124) darkCurrentThresh, AE does not increase exposure.

```
If (NewExpRatio > 1) & (DarkCurrent > DarkCurrentThresh)
NewExpRatio = 1;  //Do not increase exposure
End
```

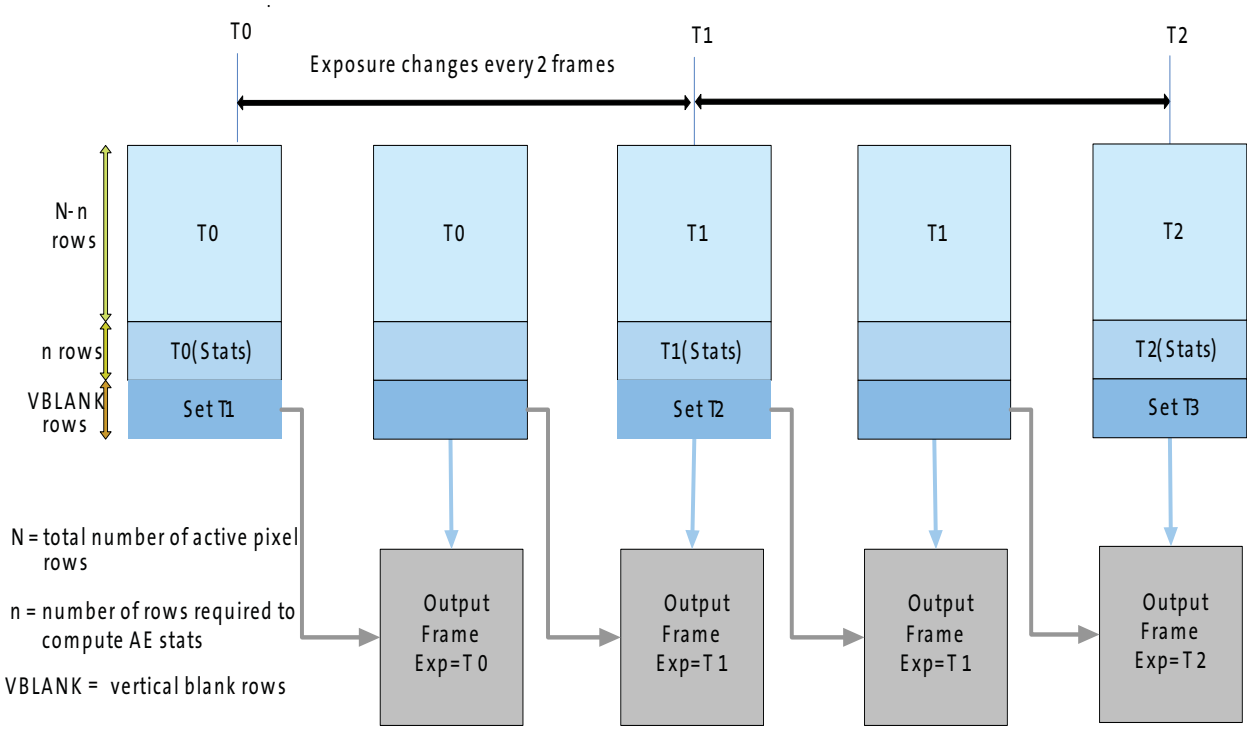
Table 17: Auto Exposure Control Registers

Register	Name	Function
0x3140	ae_roi_x_start_offset	Number of pixels into each row before the ROI starts
0x3142	ae_roi_y_start_offset	Number of rows into each frame before the ROI starts
0x3144	ae_roi_x_size	Number of columns in the ROI
0x3146	ae_roi_y_size	Number of rows in the ROI
0x3102	ae_luma_target_reg	Average luma target value to be reached by the auto exposure
0x3108	ae_min_ev_step_reg	Minimum exposure value step size. Since min_ev_step sizes are small (typically less than 1), they are multiplied by 256 and then the value is written to this register.
0x310A	ae_max_ev_step_reg	Maximum exposure value step size. Since this value is always greater than 1 there is no need to multiply by 256 as in the case of min_EV_stepsize.
0x310C	ae_damp_offset_reg	Adjusts step size and settling speed.
0x310E	ae_damp_gain_reg	Adjusts step size and settling speed.
0x3110	ae_damp_max_reg	Max value allowed for damping (multiplied by 256 since internal value is typically <1). For most applications, the value of damping should be <1, otherwise AE will overshoot the target. For applications with fast settling required, it may be desirable to allow damping >1. Default value: 0.875 * 256 = 0x00E0
0x311C	ae_max_exposure_reg	Maximum integration (exposure) time in rows to be used by AE.
0x311E	ae_min_exposure_reg	Minimum integration (exposure) time in rows to be used by AE.
0x3166	ae_ag_exposure_hi	At this integration time, the analog gain is increased (when AE is enabled to control analog gain).
0x3168	ae_ag_exposure_lo	At this integration time, the analog gain is reduced (when AE is enabled to control analog gain).
0x3124	ae_dark_cur_thresh_reg	The dark current level that stops AE from increasing integration time. Note that increased integration time would increase dark current as well and signal level (SNR) would drop because photo diode well capacity is limited.

AE Frame Synchronization

A delay is incurred between the time when a frame with the newly updated AE value applied is seen by the AE module and when it reaches the sensor core logic (which sets the exposure times for the sensor). This delay is associated with the Delay Buffers and Sensor Data Path delays. The AE module will perform its calculations during the vertical blanking time and the new exposure value will be seen by the sensor core logic after the next frame has started. Therefore the result is that the third frame after the current frame will reflect the new exposure time. Figure 34 illustrates how the exposure changes every two frames.

Figure 34: AE Frame Synchronization



Gain

Digital Gain

Digital gain can be controlled globally by R0x305E (Context A) or R0x30C4 (Context B). There are also registers that allow individual control over each Bayer color channel:

GreenR	R0x3056
GreenB	R0x305C
Red	R0x305A
Blue	R0x3058

The format for digital gain setting is xxx.yyyyy where 0b00100000 represents a 1x gain setting and 0b00110000 represents a 1.5x gain setting. The step size for yyyyy is 0.03125 while the step size for xxx is 1. Therefore to set a gain of 2.09375 one would set digital gain to 01000011. The maximum digital gain is 7.97x.

Column Gain

The AR0134 has a column parallel architecture and therefore has an analog gain stage per column. The column (analog) gain can be set to 1x, 2x, 4x or 8x. This can be set in R0x30B0[5:4](Context A) or R0x30B0[9:8] (Context B).

Black Level Correction

Black level correction is handled automatically by the image sensor. No adjustments are provided except to enable or disable this feature. Setting R0x30EA[15] disables the automatic black level correction. Default setting is for automatic black level calibration to be enabled.

The automatic black level correction measures the average value of pixels from a set of optically black lines in the image sensor. The pixels are averaged as if they were light-sensitive and passed through the appropriate gain. This line average is then digitally low-pass filtered over many frames to remove temporal noise and random instabilities associated with this measurement. The new filtered average is then compared to a minimum acceptable level, low threshold, and a maximum acceptable level, high threshold. If the average is lower than the minimum acceptable level, the offset correction value is increased by a predetermined amount. If it is above the maximum level, the offset correction value is decreased by a predetermined amount. The high and low thresholds have been calculated to avoid oscillation of the black level from below to above the targeted black level.

Row-wise Noise Correction

Row (Line)-wise Noise Correction is handled automatically by the image sensor. No adjustments are provided except to enable or disable this feature. Clearing R0x3044[10] disables the row noise correction. Default setting is for row noise correction to be enabled.

Row-wise noise correction is performed by calculating an average from a set of optically black pixels at the start of each line and then applying each average to all the active pixels of the line.

Column Correction

The AR0134 uses a column parallel readout architecture to achieve fast frame rates. Without any corrections, the consequence of this architecture is that different column signal paths have slightly different offsets that might show up on the final image as structured fixed pattern noise.

The AR0134 has column correction circuitry that measures this offset and removes it from the image before output. This is done by sampling dark rows containing tied pixels and measuring an offset coefficient per column to be corrected later in the signal path.

Column correction can be enabled/disabled via R0x30D4[15]. Additionally, the number of rows used for this offset coefficient measurement is set in R0x30D4[3:0]. By default this register is set to 0x7, which means that 8 rows are used. This is the recommended value. Other control features regarding column correction can be viewed in the AR0134 Register reference. Any changes to column correction settings need to be done when the sensor streaming is disabled and the appropriate triggering sequence must be followed as described below.

Column Correction Triggering

Column correction requires a special procedure to trigger depending on which state the sensor is in.

Column Triggering on Startup

When streaming the sensor for the first time after powerup, a special sequence needs to be followed to make sure that the column correction coefficients are internally calculated properly.

1. Follow proper power up sequence for power supplies and clocks.
2. Apply sequencer settings.
3. Apply frame timing and PLL settings as required by application.
4. Set analog and digital gains to 1x.
5. Enable column correction and settings (R0x30D4 = 0xE007).
6. Enable streaming (R0x301A[2]=1)or drive the TRIGGER pin HIGH.
7. Wait 8 frames to settle.
8. Disable streaming (R0x301A[2]=0) or drive the TRIGGER pin LOW.

After this, the sensor has calculated the proper column correction coefficients and the sensor is ready for streaming. Any other settings (including gain, integration time, etc.) can be done afterwards without affecting column correction.

Column Correction Retriggering Due to Mode Change

Since column offsets are sensitive to changes in the analog signal path, such changes require column correction circuitry to be retriggered for the new path. Examples of such mode changes include: horizontal mirror, vertical flip, changes to column correction settings.

When such changes take place, the following sequence needs to take place:

1. Disable streaming (R0x301A[2]=0) or drive the TRIGGER pin LOW.
2. Enable streaming (R0x301A[2]=1) or drive the TRIGGER pin HIGH.
3. Wait 9 frames to settle.

Note: The above steps are not needed if the sensor is being reset (soft or hard reset) upon the mode change.

Test Patterns

The AR0134 has the capability of injecting a number of test patterns into the top of the datapath to debug the digital logic. With one of the test patterns activated, any of the datapath functions can be enabled to exercise it in a deterministic fashion. Test patterns are selected by test_pattern_mode register (R0x3070). Only one of the test patterns can be enabled at a given point in time by setting the test_pattern_mode register according to Table 18. When test patterns are enabled the active area will receive the value specified by the selected test pattern and the dark pixels will receive the value in test_pattern_green (R0x3074 and R0x3078) for green pixels, test_pattern_blue (R0x3076) for blue pixels, and test_pattern_red (R0x3072) for red pixels.

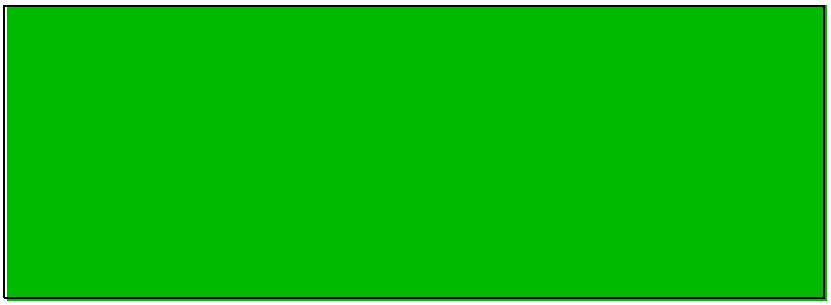
Table 18: Test Pattern Modes

Test_Pattern_Mode	Test Pattern Output
0	No test pattern (normal operation)
1	Solid color test pattern
2	100% color bar test pattern
3	Fade-to-grey color bar test pattern
256	Walking 1s test pattern (12-bit)

Color Field

When the color field mode is selected, the value for each pixel is determined by its color. Green pixels will receive the value in test_pattern_green, red pixels will receive the value in test_pattern_red, and blue pixels will receive the value in test_pattern_blue. See Figure 35 for a solid green pattern with Gr = Gb = 3072.

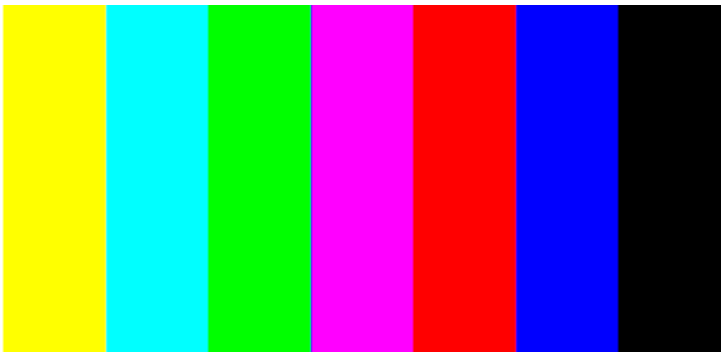
Figure 35: Solid Color



Vertical Color Bars

When the vertical color bars mode is selected, a typical color bar pattern will be sent through the digital pipeline. See Figure 36:

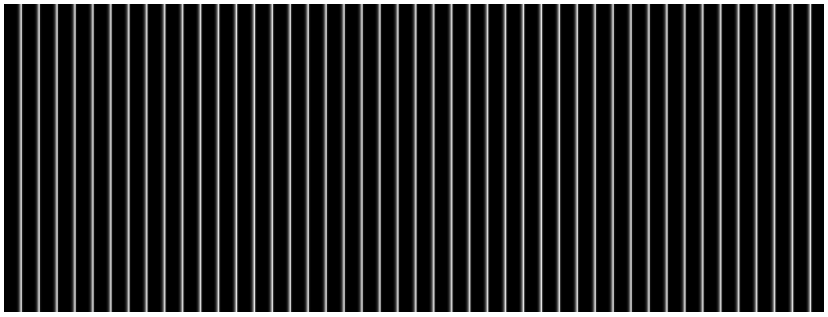
Figure 36: Vertical Color Bars



Walking 1s

When the walking 1s mode is selected, a walking 1s pattern will be sent through the digital pipeline. The first value in each row is 1. See Figure 37:

Figure 37: Walking 1s



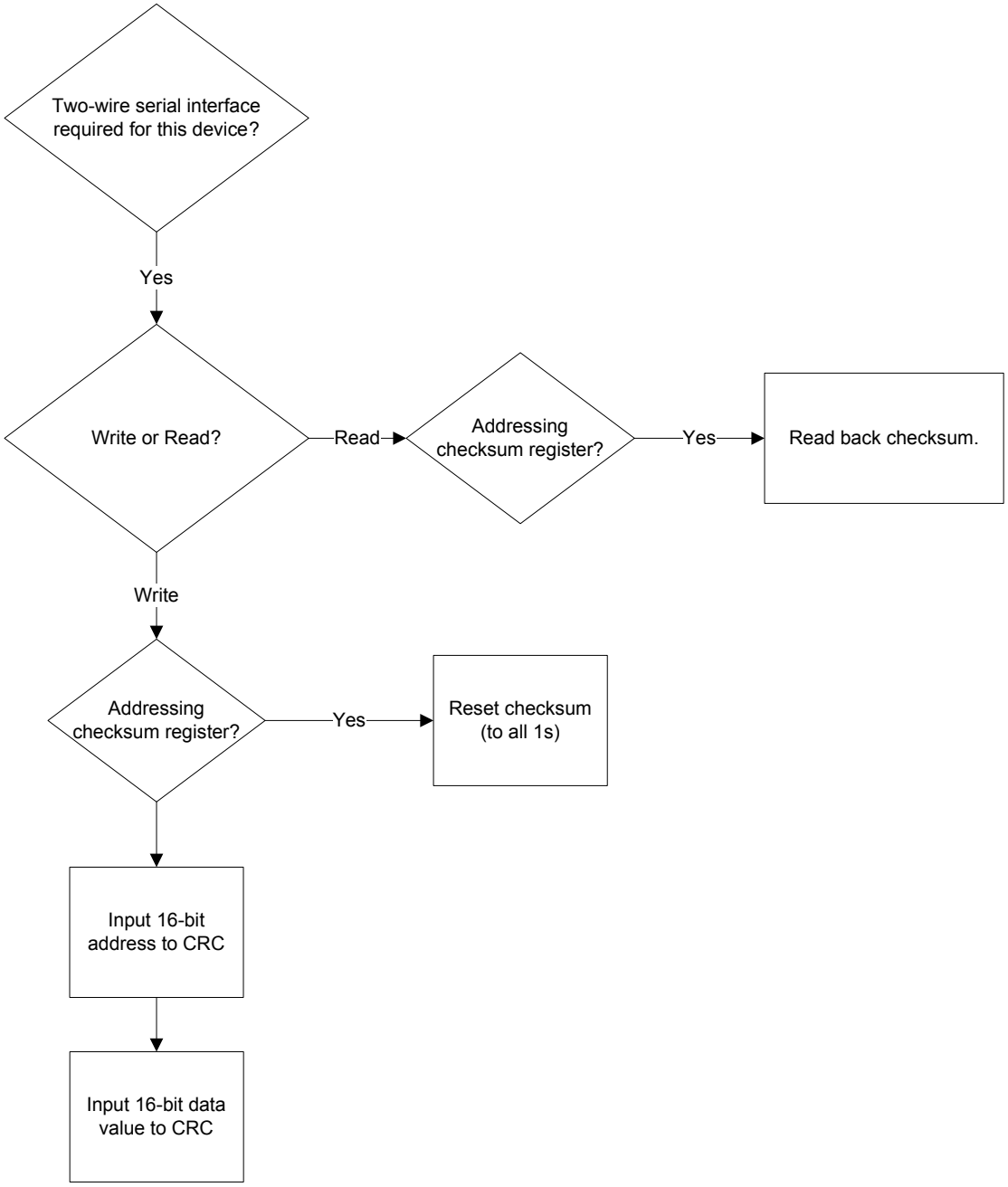
Two-Wire Serial Interface CRC

AR0134 includes a means of validating two-wire serial interface communications. The AR0134 confirms that all two-wire serial interface write requests to the device are successful by means of a checksum, generated from all address and data values associated with such transactions.

These requirements are interpreted as follows:

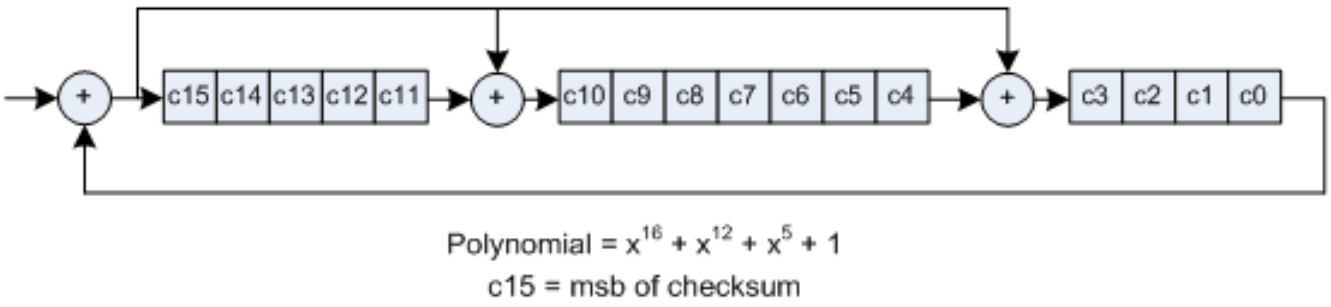
- For all two-wire serial interface writes to the camera the 16-bit register address and 2 bytes of data are fed into a 16-bit CRC to generate a checksum.
- That checksum is stored in a two-wire serial interface accessible register at address 0x31D6.
- The checksum can be read via two-wire serial interface and will also be output in the embedded registers (if enabled).
- A write via two-wire serial interface to the checksum register will reset the checksum to the start value of 0xFFFF.

Figure 38: Checksum Generation Flow Within the Sensor



The 16-bit value will be input to the CRC MSB first, i.e., b15 through b0. The CRC used will implement the polynomial $x^{16} + x^{12} + x^5 + 1$, as illustrated inFigure 39 on page 55.

Figure 39: Definition of 16-bit CRC Shift Register



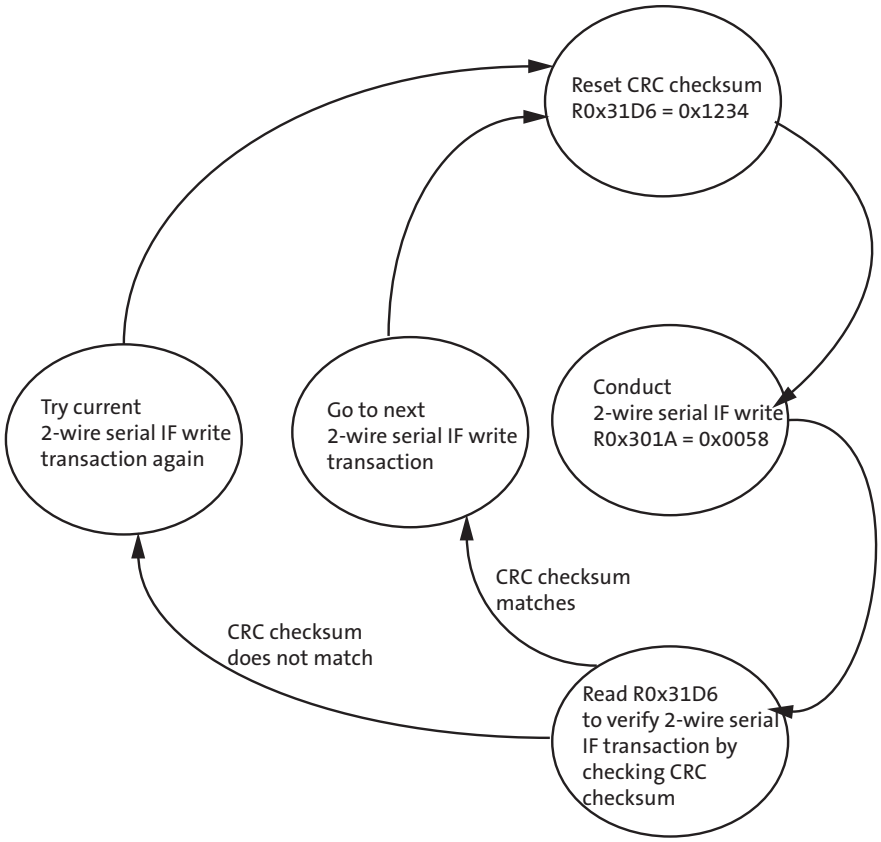
The recommended procedure to use CRC checksum as follows:

Step 1: Reset CRC checksum register(R0x31D6) by writing R0x31D6 with any value to reset CRC checksum register before write two-wire serial interface write command.

Step 2: Conduct two-wire serial interface write command to a desired register

Step3: Read CRC checksum register (R0x31D6) to verify that two-wire serial interface write command was done successfully by comparing the read CRC checksum register(R0x31D6) with a expected CRC checksum value.

Step4: Go back to step 1.



Two-Wire Serial Interface Sequential Writes

The input to the 16-bit CRC logic is either a 16-bit address or a 16-bit write data value. If the 16-bit address matches the CRC register, the CRC register is initialized to all ones. Otherwise, the 16-bit write data value is input (serially) into the CRC generator, and a 16-bit CRC value results unique to that 16-bit write data value. Sequentially, either CRC address or other addressed data values are presented to the CRC generator and resulting CRC register. At the end of a sequential write of addresses with 16-bit address data values, the CRC register contains the CRC value of sequentially processed write data values that were sequentially addressed.

Note, if the two-wire serial interface write is only 8-bits to a single register address, that write is serviced by reading the pair of 8-bit addresses addressed by the 15 MSBs of the 8-bit address, and the 8-bit write data value that is being modified is combined with the 8-bit data address value NOT being modified, and the resulting 16-bits is input into the CRC for that 8-bit address.

In summary, the CRC checksum(R0x31D6) continues to update, as all non-CRC registers are written. At any time, if CRC register is read, the current CRC register value is read back. At any time, if CRC register is written (with any value), the CRC register is initialized to all ones.

Reading the Sensor CRA and Chromaticity

Follow the steps below to obtain the CRA value of the Image Sensor:

1. Set the register bit field R0x301A[5] = 1.
2. Read the register bit fields R0x31FA[11:8].
3. Determine the CRA value according to Table 19.

Table 19: CRA Value

Hex Value of R0x31FA[11:8]	CRA Value	Chromaticity
0x01	0	Mono
0x1	0	Mono
0x2	25	Mono
0x3	25	Mono
0x4	0	Color
0x5	0	Color

Revision History

Rev. C 6/13/14

- Updated corporate address on last page
- Updated “Blanking Control” on page 6
- Updated Figure 7: “HiSPi Transmitter and Receiver Interface Block Diagram,” on page 12
- Updated Figure 9: “Block Diagram of DLL Timing Adjustment,” on page 13
- Updated Table 5, “Exposure Timing,” on page 20
- Updated“Exposure and Data Synchronization Outputs” on page 22
- Updated“TRIGGER Input Restrictions” on page 22
- Updated“Blanking Control” on page 29
- Updated Figure 23: “Latency For Single Buffered Registers - Coarse Integration Time Example,” on page 35
- Added Figure 24: “Latency For Double Buffered Registers - Column Gain Example,” on page 35
- Updated Figure 25: “Latency For Double Buffered Registers - Fine Integration Time Example,” on page 36
- Added “Two-Wire Serial Interface CRC” on page 53
- Updated Figure 38: “Checksum Generation Flow Within the Sensor,” on page 54
- Added “Reading the Sensor CRA and Chromaticity” on page 56

Rev. B 6/11/13

- Updated to Production
- Updated Table 4, “Real-Time Context-Switchable Registers,” on page 17
- Updated “Frame Rate” on page 6
- Added Figure 9: “Block Diagram of DLL Timing Adjustment,” on page 13
- Updated “Exposure” on page 16
- Updated Table 4, “Real-Time Context-Switchable Registers,” on page 17
- Updated “Operation Details” and changed title to “Triggered System Details” on page 19
- Updated “Trigger Mode” on page 19
- Updated last paragraph of “Duration of Exposure” on page 21 (including Equation 8 on page 21
- Updated “Exposure and Data Synchronization Outputs” on page 22
- Updated “TRIGGER Input Restrictions” on page 22
- Updated Table 7, “Example 1 (With Default Setting for Full Resolution),” on page 23
- Updated Equation 16 on page 23, Equation 21, Equation 22, Equation 23, and Equation 24 on page 24
- Updated “Reset” on page 26
- Updated “Hard Reset of Logic” on page 26
- Updated “Blanking Control” on page 29
- Moved Figure 23, Latency For Single Buffered Registers - Coarse Integration Time Example and Figure 24, Latency For Double Buffered Registers - Column Gain Example to page 35
- Updated “Restart” on page 36
- Moved Figure 29, Frame Format with Embedded Data Lines Enabled to page 40
- Moved section on Two-wire Serial Register Interface to the data sheet.

Rev. A 1/23/13

- Initial release

180 Clemenceau Avenue, #05-02/04 Haw Par Centre, Singapore 239922 prodmktg@aptina.com www.aptina.com