TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

# TCKE8xx Series

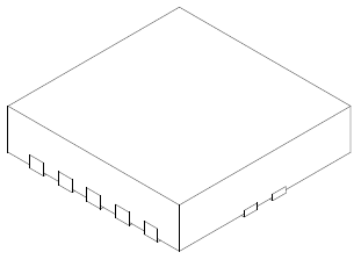
## 18 V, 5A eFuse IC with Adjustable Overcurrent Protection and Reverse Current Blocking FET Control

## 1. Description

The TCKE8xx series is 18 V high input voltage Single Input-Single Output eFuse ICs. It can be used as a reusable fuse, and includes protection features like adjustable over current limit by an external resistor, short circuit protection, over voltage clamp, adjustable slew rete control by an external capacitance, under voltage protection, thermal shutdown and reverse current blocking by external MOSFET control circuit.

Switch ON resistance is only 28 mΩ (typ.), high output current is up to 5.0 A, and wide input voltage operation characteristics makes this series ideal for power management applications such as in the power supply circuit of hard disk drive and battery charging applications.

This series is available in 0.5 mm pitch small package WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.)). Thus this series is ideal for various applications such as portable electronics that require high-density soldering



WSON10B

Weight : 19.3mg ( typ.)

## 2. Feature

- High input voltage: $V_{IN\ max}$ = 18.0 V
- High output current: $I_{OUT\ (DC)}$ = 5.0 A
- Low ON resistance : $R_{ON}$ = 28 mΩ (typ.)
- Adjustable overcurrent limit : up to 5.0 A (Max)
- Fixed over voltage clamp
  5 V power rail TCKE805 : $V_{OVC}$ = 6.04 V (typ.)
  12 V power rail TCKE812 : $V_{OVC}$ = 15.1 V (typ.)
  TCKE800 : No over voltage clamp
- Programmable slew rate control by external capacitance for inrush current reduction
- Programmable under voltage lockout by external resistor
- Reverse current blocking support by built in MOSFET driver
- Thermal shutdown
- Auto-discharge
- Small package:
  WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.))
- IEC62368-1 Certified

## Notice

This series is sensitive to electrostatic discharge.

Please ensure equipment and tools are adequately earthed when handling.

Start of commercial production
2019-09

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## 3. Absolute Maximum Ratings (Note) (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Input voltage | $V_{IN}$ | -0.3 to 18.0 | V |
| ILIM voltage | $V_{ILIM}$ | -0.3 to 6.0 | V |
| dV/dT voltage | $V_{dV/dT}$ | -0.3 to 6.0 | V |
| Control voltage | $V_{EN/UVLO}$ | -0.3 to 18.0 | V |
| Output voltage | $V_{OUT}$ | -0.3 to $V_{IN}$ + 0.3 or 18.0 V which is smaller | V |
| External MOSFET voltage | $V_{EFET}$ | -0.3 to 30.0 | V |
| Power dissipation | $P_D$ | 2.4 (Note 1) | W |
| Junction temperature | Tj | 150 | °C |
| Storage temperature | $T_{stg}$ | –55 to 150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Rating at mounting on a board: FR4 board. (76.2mm * 114.3mm * 1.6mm, 4 layer )

## 4. Operating Ranges

| Characteristics | Symbol | Ranges | | Unit |
|---|---|---|---|---|
| Input voltage | $V_{IN}$ | 4.4 to 18.0 | | V |
| Output current | $I_{OUT}$ | DC | 0 to 5.0 | A |
| ILIM External resistance | $R_{ILIM}$ | 20 to 300 | | kΩ |
| Control voltage | $V_{EN/UVLO}$ | 0 to 18 | | V |
| External MOSFET voltage | $V_{EFET}$ | 0 to $V_{IN}$ + 4.9 | | V |
| Operating Ambient temperature range | $Ta_{_opr}$ | –40 to 85 | | °C |
| External capacitance | $C_{dV/dT}$ | 1 (typ.), 100 (max) | | nF |


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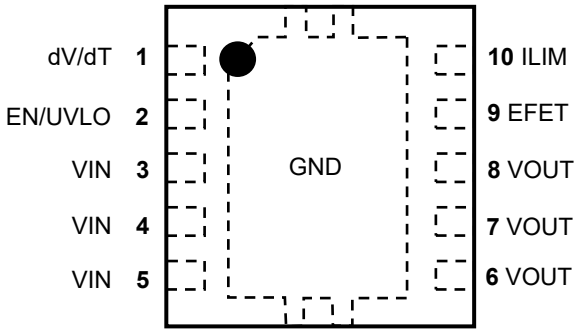
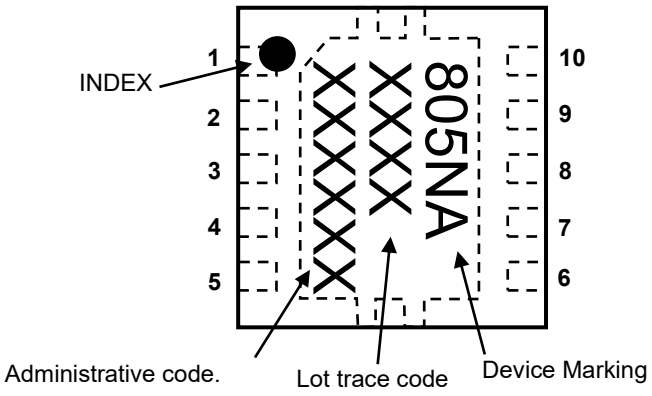
## 5. Pin Assignment (Top view)

WSON10B




## 6. Top Marking (Top view)

Example: TCKE805NA





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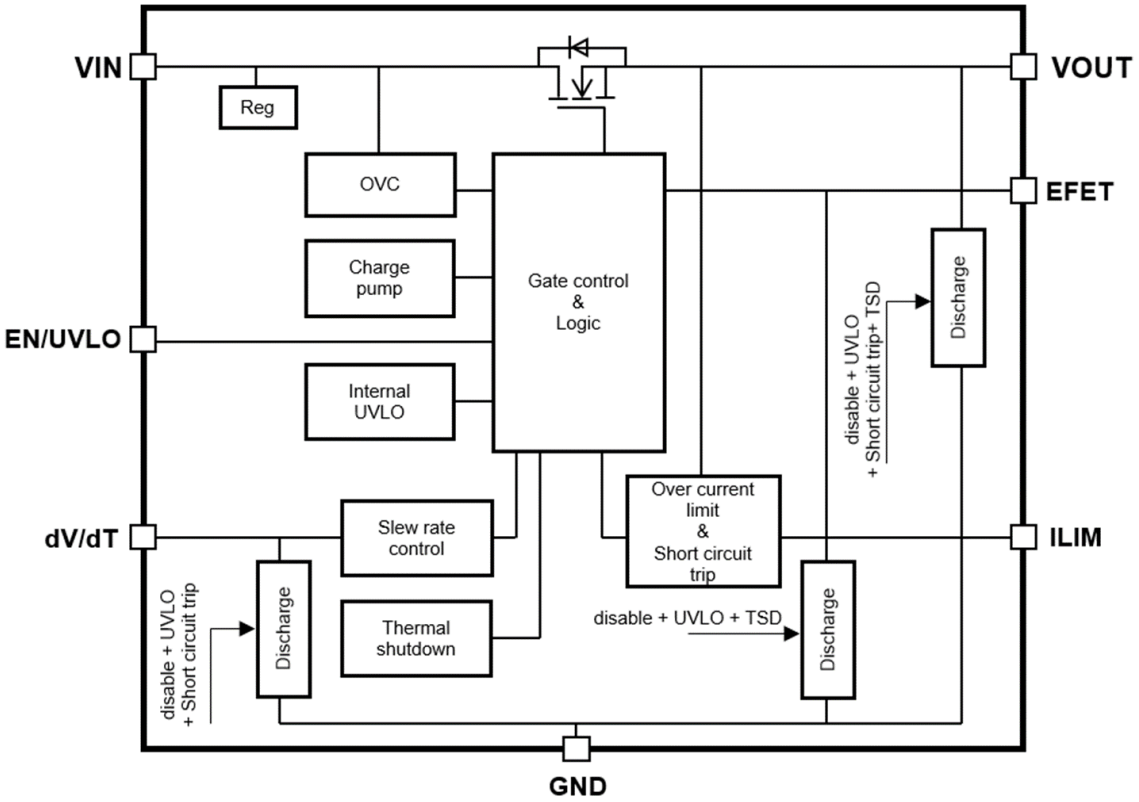
## 7. Product list

| Part number | Over voltage Clamp | CE function | Fault Response | Top Marking | Package |
|---|---|---|---|---|---|
| TCKE800NA | N/A | Active High | Auto-retry | 800NA | WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.)) |
| TCKE800NL | N/A | Active High | Latched | 800NL | WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.)) |
| TCKE805NA | 6.04V (typ.) | Active High | Auto-retry | 805NA | WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.)) |
| TCKE805NL | 6.04V (typ.) | Active High | Latched | 805NL | WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.)) |
| TCKE812NA | 15.1V (typ.) | Active High | Auto-retry | 812NA | WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.)) |
| TCKE812NL | 15.1V (typ.) | Active High | Latched | 812NL | WSON10B (3.0 mm x 3.0 mm, t: 0.7 mm (typ.)) |

## 8. Block Diagram





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## 9. PIN Description

| PIN Name | Description |
|---|---|
| EN/UVLO | This pin has two functions. One function turns on the output voltage of the internal MOSFET and EFET terminal as an enable signal. Another function can be used as a UVLO trip point with external resistors. |
| ILIM | Current limit set input. A resistor between ILIM terminal and GND sets the current limit. |
| dV/dT | Rise time set input. A capacitor between dV/dT terminal and GND sets the slew rate of VOUT when the device turns on. |
| EFET | Connect this pin to the gate of a blocking Nch MOSFET. This pin can be left floating if it is not used |
| VIN | Supply Input. Input to the power switch and the supply voltage for the device. |
| GND | Ground. |
| VOUT | Output. Output of the power switch. |

## 10. Operation Logic Table

| | EN/UVLO “Low” | EN/UVLO “ High” |
|---|---|---|
| **Output** | **OFF** | **ON** |


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# 11. Electrical Characteristics

## 11.1 TCKE805 DC Characteristics (Unless otherwise specified, $V_{IN}$ = 5 V, $R_{ILIM}$ = 20 kΩ)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40 to 85°C (Note 2) | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ. | Max | Min | Max | |
| **Basic operation** | | | | | | | | |
| VIN under voltage lockout (UVLO) threshold, rising | $V_{IN_UVLO}$ | — | — | 4.15 | — | 4.00 | 4.40 | V |
| VIN under voltage lockout (UVLO) hysteresis | $V_{IN_UVhyst}$ | — | — | 5 | — | — | — | % |
| EN/UVLO threshold voltage, rising | $V_{ENR}$ | — | — | 1.1 | — | 1.0 | 1.2 | V |
| EN/UVLO threshold voltage, falling | $V_{ENF}$ | — | — | 0.96 | — | 0.89 | 1.01 | V |
| On resistance | $R_{ON}$ | $I_{OUT}$ = 1.5 A | — | 28 | — | — | 38 | mΩ |
| Quiescent current (ON state) | $I_{Q(ON)}$ | $V_{EN}$ = 3 V, $R_{ILIM}$ = 120 kΩ, $I_{OUT}$ = 0 A | — | 0.46 | — | — | 0.61 | mA |
| Quiescent current (OFF state) | $I_{Q(OFF)}$ | $V_{EN}$ = 0V | — | 33 | — | — | 48 | μA |
| **dV/dT control** | | | | | | | | |
| CdV/dT Voltage | $V_{dV/dT}$ | — | — | 3 | — | — | — | V |
| Charging Current | $I_{dV/dT}$ | $V_{dV/dT}$ = 0 V | — | 250 | — | — | — | nA |
| Discharge resistance | $R_{dV/dT}$ | $V_{EN}$ = 0 V, $I_{dV/dT}$ = 10 mA | — | 5 | — | 3 | 9 | Ω |
| dV/dT to OUT gain | $GAIN_{dV/dT}$ | (Note 2) $V_{dV/dT}$ = 0.3 V | — | 10.5 | — | — | — | — |
| **External FET Gate driver** | | | | | | | | |
| Charging Current | $I_{EFET}$ | $V_{EFET}$ = 5 V (Note 2) | — | 2 | — | — | — | μA |
| Output voltage | $V_{EFET}$ | (Note 2) | — | $V_{IN}$+4.9 | — | $V_{IN}$+4.4 | $V_{IN}$+5.3 | V |
| Discharge resistance | $R_{EFET}$ | $V_{EN}$ = 0 V, $I_{EFET}$ = 20 mA | — | 24 | — | 12 | 40 | Ω |
| **Over-voltage Protection** | | | | | | | | |
| Over voltage clamp (OVC) | $V_{OVC}$ | $V_{IN}$ = 7 V, $I_{OUT}$ = 1 A | — | 6.04 | — | 5.62 | 6.45 | V |
| **Overcurrent Protection** | | | | | | | | |
| Overcurrent limit (Note3) | $I_{LIM}$ ($I_{OUT_CL}$) | $R_{ILIM}$ = 20 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 5.15 | — | 4.44 | 5.87 | A |
| | | $R_{ILIM}$ = 24 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 4.38 | — | 3.88 | 4.88 | |
| | | $R_{ILIM}$ = 35.1 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 3.06 | — | 2.70 | 3.41 | |
| | | $R_{ILIM}$ = 62 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 1.78 | — | 1.52 | 2.04 | |
| | | $R_{ILIM}$ = 120 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.96 | — | 0.76 | 1.16 | |
| | | $R_{ILIM}$ = 250 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.50 | — | 0.35 | 0.65 | |
| | | $R_{ILIM}$ = 0 Ω, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.64 | — | — | — | |
| | | $R_{ILIM}$ = OPEN, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.64 | — | — | — | |
| Short-circuit current limit | $I_{SCL}$ | (Note 2),(Note 4) | — | 0.15 | — | 0.05 | 0.50 | A |
| Fast trip comparator level | $I_{FASTTRIP}$ ($I_{SHORT_TRIP}$) | — | — | $I_{LIM}$ × 1.6 | — | — | — | A |
| ILIM short resistor detect Threshold | $R_{SHORTLIM}$ | — | — | 11 | — | — | — | kΩ |
| **Thermal Protection** | | | | | | | | |
| Thermal shutdown Threshold | $T_{SD}$ | Tj | — | 160 | — | — | — | °C |
| Thermal shutdown Hysteresis | $T_{SDH}$ | Tj (Auto-retry Type) | — | 20 | — | — | — | °C |

Note 2: This parameter is warranted by design.

Note 3: Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

Note 4: Hard short less than 10 mΩ.


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## 11.2 TCKE805 AC Characteristics
## (Unless otherwise specified, Ta = -40 to 85°C, $V_{IN}$ = 5 V, $R_{ILIM}$ = 20 kΩ, $R_{LOAD}$ = 5 Ω, $C_{IN}$ = $C_{OUT}$ = 1 μF )

| Characteristics | Symbol | Test Condition | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ on time | $t_{ON}$ | $V_{EN}$↑ to $I_{IN}$ = 100 mA, 1 A resistive load at $V_{OUT}$, $C_{dV/dT}$ = OPEN (Note 5) | | — | 330 | — | μs |
| $V_{OUT}$ off time | $t_{OFF}$ | $V_{EN}$↓ to $V_{EFET}$↓, $C_{EFET}$ = OPEN (Note 5) | TCKE805NA | — | 1.0 | — | μs |
| | | | TCKE805NL | — | 0.5 | — | |
| Output ramp time | $t_{dV/dT}$ | $V_{EN}$↑ to $V_{OUT}$ become $V_{IN}$* 90%, $C_{dV/dT}$ = OPEN (Note 6) | | 200 | 400 | 700 | μs |
| | | $V_{EN}$↑ to $V_{OUT}$ become $V_{IN}$* 90%, $C_{dV/dT}$ = 1 nF (Note 5) | | — | 2.3 | — | ms |
| Fast trip comparator delay | $t_{FastOffDly}$ | $I_{OUT}$ > $I_{FASTTRIP}$ to $I_{OUT}$ = 0 (Switch off) (Note 5) | | — | 150 | — | ns |
| EFET on time | $t_{EFET-ON}$ | $V_{EN}$↑ to $V_{EFET}$ = $V_{IN}$, $C_{EFET}$ = 1 nF (Note 5) | | — | 2.6 | — | ms |
| | | $V_{EN}$↑ to $V_{EFET}$ = $V_{IN}$, $C_{EFET}$ = 10 nF (Note 5) | | — | 25 | — | ms |
| EFET off time | $t_{EFET-OFF}$ | $V_{EN}$↓ to $V_{EFET}$ = 1 V, $C_{EFET}$ = 1 nF (Note 5) | TCKE805NA | — | 1.2 | — | μs |
| | | | TCKE805NL | — | 0.8 | — | |
| | | $V_{EN}$↓ to $V_{EFET}$ = 1 V, $C_{EFET}$ = 10 nF (Note 5) | TCKE805NA | — | 2.9 | — | μs |
| | | | TCKE805NL | — | 2.5 | — | |

Note 5: This parameter is reference only.
Note 6: This parameter is warranted by design.


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## 11.3 TCKE800 & 812 DC Characteristics
## (Unless otherwise specified, $V_{IN}$ = 12 V, $R_{ILIM}$ = 20 kΩ)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40 to 85°C (Note 2) | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ. | Max | Min | Max | |
| **Basic operation** | | | | | | | | |
| VIN under voltage lockout (UVLO) threshold, rising | $V_{IN_UVLO}$ | — | — | 4.15 | — | 4.00 | 4.4 | V |
| VIN under voltage lockout (UVLO) hysteresis | $V_{IN_UVhyst}$ | — | — | 5 | — | — | — | % |
| EN threshold voltage, rising | $V_{ENR}$ | — | — | 1.1 | — | 1.0 | 1.2 | V |
| EN threshold voltage, falling | $V_{ENF}$ | — | — | 0.96 | — | 0.89 | 1.01 | V |
| On resistance | $R_{ON}$ | $I_{OUT}$ = 1.5 A | — | 28 | — | — | 38 | mΩ |
| Quiescent current (ON state) | $I_{Q(ON)}$ | $V_{EN}$ = 3 V, $R_{ILIM}$ = 120 kΩ, $I_{OUT}$ = 0 A | — | 0.49 | — | — | 0.64 | mA |
| Quiescent current (OFF state) | $I_{Q(OFF)}$ | $V_{EN}$ = 0 V | — | 46 | — | — | 67 | μA |
| **dV/dT control** | | | | | | | | |
| Capacitor Voltage | $V_{dV/dT}$ | — | — | 3 | — | — | — | V |
| Charging Current | $I_{dV/dT}$ | $V_{dV/dT}$ = 0 V | — | 250 | — | — | — | nA |
| Discharge resistance | $R_{dV/dT}$ | $V_{EN}$ = 0 V, $I_{dV/dT}$ = 10 mA | — | 5 | — | 3 | 9 | Ω |
| dV/dT to OUT gain | $GAIN_{dV/dT}$ | (Note 2) $V_{dV/dT}$ = 1.0 V | — | 10.5 | — | — | — | — |
| **External FET Gate driver** | | | | | | | | |
| Charging Current | $I_{EFET}$ | $V_{EFET}$ = 12 V (Note 2) | — | 2 | — | — | — | μA |
| Output voltage | $V_{EFET}$ | (Note 2) | — | $V_{IN}$+4.9 | — | $V_{IN}$+4.4 | $V_{IN}$+5.3 | V |
| Discharge resistance | $R_{EFET}$ | $V_{EN}$ = 0 V, $I_{EFET}$ = 20 mA | — | 24 | — | 12 | 40 | Ω |
| **Over-voltage Protection** | | | | | | | | |
| Over voltage clamp (OVC) | $V_{OC}$ | $V_{IN}$ = 17 V, $I_{OUT}$ = 1 A (TCKE812) | — | 15.10 | — | 14.11 | 16.14 | V |
| **Over-current Protection** | | | | | | | | |
| Over current limit (Note3) | $I_{LIM}$ ($I_{OUT_CL}$) | $R_{ILIM}$ = 20 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 5.15 | — | 4.44 | 5.87 | A |
| | | $R_{ILIM}$ = 24 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 4.38 | — | 3.88 | 4.88 | |
| | | $R_{ILIM}$ = 35.1 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 3.06 | — | 2.70 | 3.41 | |
| | | $R_{ILIM}$ = 62 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 1.78 | — | 1.52 | 2.04 | |
| | | $R_{ILIM}$ = 120 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.96 | — | 0.76 | 1.16 | |
| | | $R_{ILIM}$ = 250 kΩ, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.50 | — | 0.35 | 0.65 | |
| | | $R_{ILIM}$ = 0 Ω, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.64 | — | — | — | |
| | | $R_{ILIM}$ = OPEN, $V_{IN}$ - $V_{OUT}$ = 1 V | — | 0.64 | — | — | — | |
| Short-circuit current limit | $I_{SCL}$ | (Note 2),(Note 4) | — | 0.15 | — | 0.05 | 0.5 | A |
| Fast-trip comparator level | $I_{FASTTRIP}$ ($I_{SHORT_TRIP}$) | — | — | $I_{LIM}$ × 1.6 | — | — | — | A |
| ILIM short resistor detect Threshold | $R_{SHORTLIM}$ | — | — | 11 | — | — | — | kΩ |
| **Thermal Protection** | | | | | | | | |
| Thermal shutdown Threshold | $T_{SD}$ | Tj | — | 160 | — | — | — | °C |
| Thermal shutdown Hysteresis | $T_{SDH}$ | Tj (Auto-retry Type) | — | 20 | — | — | — | °C |

Note 2: This parameter is warranted by design.
Note 3: Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.
Note 4: Hard short less than 10 mΩ. .


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## 11.4 TCKE800 & 812 AC Characteristics
## (Unless otherwise specified,Ta = -40 to 85°C, $V_{IN}$ = 12 V, $R_{ILIM}$ = 20 kΩ, $R_{LOAD}$ = 12 Ω, $C_{IN}$ = $C_{OUT}$ = 1 μF )

| Characteristics | Symbol | Test Condition | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ on time | $t_{ON}$ | $V_{EN}$↑ to $I_{IN}$ = 100 mA, 1 A resistive load at $V_{OUT}$, $C_{dV/dT}$ = OPEN (Note 5) | | — | 270 | — | μs |
| $V_{OUT}$ off time | $t_{OFF}$ | $V_{EN}$↓ to $V_{EFET}$↓, $C_{EFET}$ = OPEN (Note 5) | TCKE800NA TCKE812NA | — | 1.0 | — | μs |
| | | | TCKE800NL TCKE812NL | — | 0.5 | — | |
| Output ramp time | $t_{dV/dT}$ | $V_{EN}$↑ to $V_{OUT}$ become $V_{IN}$* 90%, $C_{dV/dT}$ = OPEN (Note 6) | | 300 | 500 | 700 | μs |
| | | $V_{EN}$↑ to $V_{OUT}$ become $V_{IN}$* 90%, $C_{dV/dT}$ = 1 nF (Note 5) | | — | 4.8 | — | ms |
| Fast-trip comparator delay | $t_{FastOffDly}$ | $I_{OUT}$ > $I_{FASTRIP}$ to $I_{OUT}$ = 0 (Switch off) (Note 5) | | — | 150 | — | ns |
| EFET on time | $t_{EFET-ON}$ | $V_{EN}$↑ to $V_{EFET}$ = $V_{IN}$, $C_{EFET}$ = 1 nF (Note 5) | | — | 6.2 | — | ms |
| | | $V_{EN}$↑ to $V_{EFET}$ = $V_{IN}$, $C_{EFET}$ = 10 nF (Note 5) | | — | 60 | — | ms |
| EFET off time | $t_{EFET-OFF}$ | $V_{EN}$↓ to $V_{EFET}$ = 1 V, $C_{EFET}$ = 1 nF (Note 5) | TCKE800NA TCKE812NA | — | 1.5 | — | μs |
| | | | TCKE800NL TCKE812NL | — | 1.1 | — | |
| | | $V_{EN}$↓ to $V_{EFET}$ = 1 V, $C_{EFET}$ = 10 nF (Note 5) | TCKE800NA TCKE812NA | — | 3.9 | — | μs |
| | | | TCKE800NL TCKE812NL | — | 3.5 | — | |

Note 5: This parameter is reference only.
Note 6: This parameter is warranted by design.


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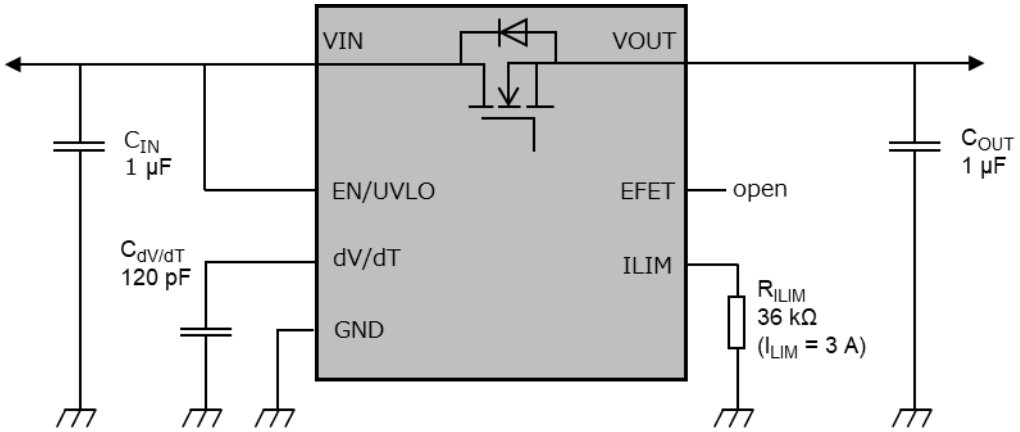
# 12. Application Note

## 1. Application circuit example




### 1) Peripheral circuits

Connect the power supply to the input terminal VIN. During normal operation, almost the same voltage as the $V_{IN}$ voltage is output from the output terminal VOUT through the internal MOSFET.

If the current suddenly decreases, for example, when short-circuiting or overcurrent is protected, high-spike voltages may be generated due to back electromotive force of inductance components such as wirings connected to the input/output terminals of the eFuse IC, causing damage to the eFuse IC and resulting damage. In this case, a positive spike voltage is generated on the input side and a negative spike voltage is generated on the output side.

When designing boards, design patterns so that the length of the wires on the input-side and output-side of the eFuse IC is as short as possible. Also, the GND wiring area should be as wide as possible to reduce the impedance. $C_{IN}$ functions to suppress the peak value against the positive spike voltage generated by the inputs. The peak value $V_{SPIKE}$ of the spike voltage and the capacitance value of the $C_{IN}$ have the following relationship. It can be understood that the spike voltage can be reduced by increasing the $C_{IN}$.

$$V_{SPIKE}\ (V) = V_{IN} + I_{OUT} \times \sqrt{\frac{L_{IN}}{C_{IN}}}$$

$L_{IN}$: effective inductance component of the input terminal (H), $I_{OUT}$: output current (A)
$V_{SPIKE}$: peak value of spiked voltage generated (V), $V_{IN}$: power supply voltage during normal operation (V)

Toshiba eFuse IC recommends 1 μF for $C_{IN}$ and $C_{OUT}$, and in most cases this value is effective enough. Be sure to measure it on the actual PCB board.

If the transient voltage at the input terminal of the eFuse IC exceeds the absolute maximum rating, connect a Zener diode between the input terminal and GND.

For negative spike voltage generated on the output side, SBD (Schottky barrier diode) can be connected to prevent the output potential from dropping below GND.

SBD is effective not only for protecting eFuse ICs, but also for protecting ICs and devices connected to the load side. Connect the SBD with the GND as the anode between the output terminal of the eFuse IC and the GND.

As noted above, Zener diode and SBD are recommended for eFuse IC because they can provide more robust protective features. The diagram below shows the peripheral circuit diagram when a Zener diode and a SBD are added.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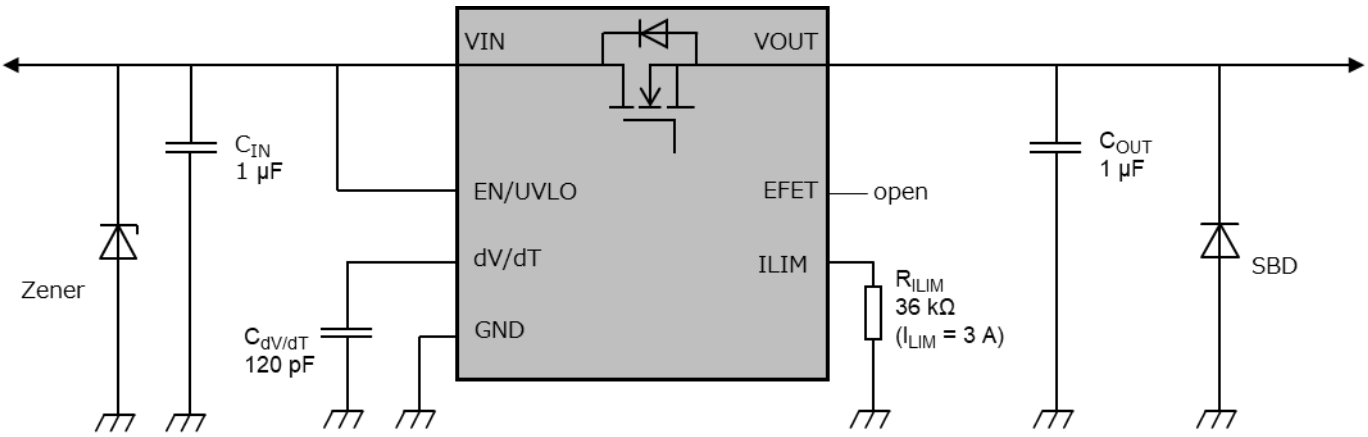


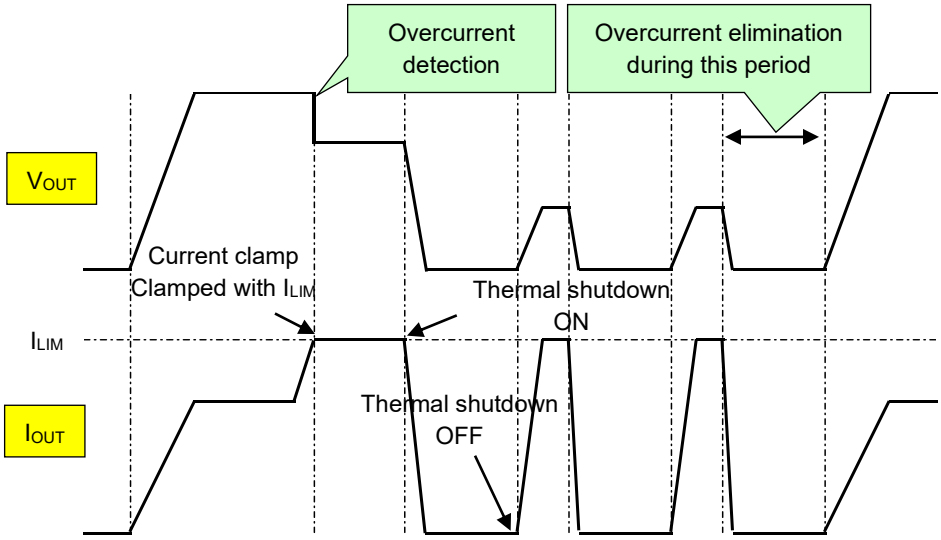

Toshiba recommends CUHZ20V as the Zener diode and CUHS20S30 as the SBD diode.

**2) Operation of the thermal shutdown function**

The overcurrent protection function prevents damage to the IC and load by suppressing power consumption in the event of an error. If the output current exceeds the limit current ($I_{LIM}$) due to a load error or short circuit, the output voltage and output current also decrease, thereby limiting the power consumed by the IC and the load.

In addition to the short-circuit protection function, which will be described later, it is double-protected against overcurrent, which greatly contributes to the prevention of ignition and smoke.

The timing chart of the auto-retry type overcurrent protection clamp operation is shown below.




**Timing chart of overcurrent protection operation (auto-retry type)**

When the output current reaches $I_{LIM}$ and overcurrent is detected, the output current is clamped so that no more current than $I_{LIM}$ flows. At this time, the output voltage drops slightly according to the relationship between the output voltage and the current, which will be described later. If the overcurrent is not resolved at this stage, this condition is maintained and the IC temperature continues to rise. Soon the IC reaches the operating temperature of the thermal shutdown function, the MOSFET is switched off, and the eFuse IC stops operating.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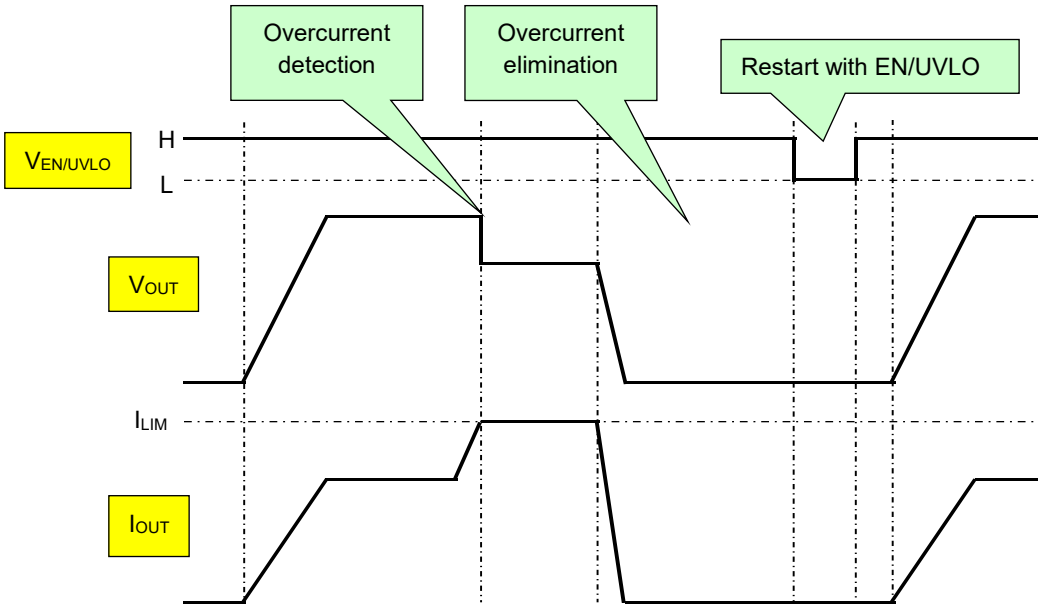
Next, the timing chart of the overcurrent protection clamp operation of the latch type is shown in the figure below.

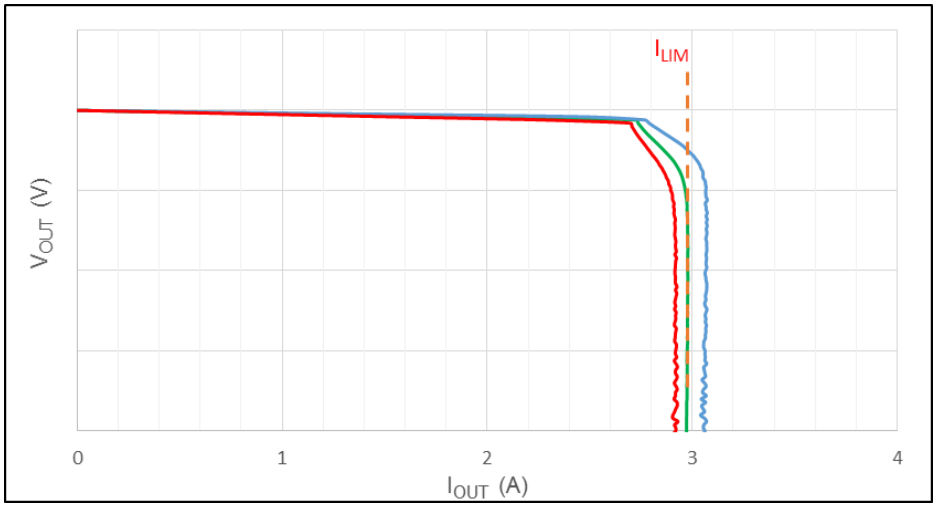
This condition is maintained until the latch type is restarted by the control signals of the EN/UVLO terminal. However, the auto-retry type repeats the restoration attempt by stopping the operation → lowering the temperature → releasing the thermal shutdown → clamping the current → protecting the overheat → raising the temperature → protecting the overheat → Stopping the operation until the overcurrent is eliminated.




**Timing chart of overcurrent protection operation (latch type)**

**3) Setting the overcurrent protection function**

The following figure shows the relationship between output voltage and current during overcurrent protection clamp operation.




**Output Voltage-Current Characteristics during Overcurrent Protection Clamp Operation**

Toshiba eFuse IC has a variable current limit. By selecting the external resistor $R_{ILIM}$ of the ILIM terminal appropriately, the current limit can be set to the optimum value for each application. The $I_{LIM}$ calculations are the same as those for the TCKE8xx series, and are as shown below. However, the deviation between the theoretical value and the measured value is large when the current is 1A or lower. Be sure to check the resistance value with the actual machine when selecting the resistance value.

$$I_{LIM}(A) = 0.13 + 101.8/R_{ILIM}(k\Omega)$$

$R_{ILIM}$: ILIM terminal external resistor (kΩ)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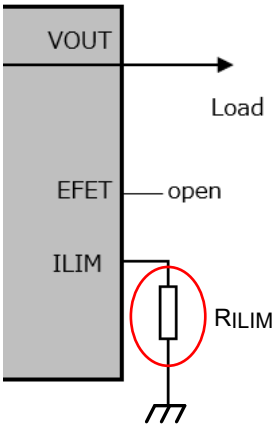
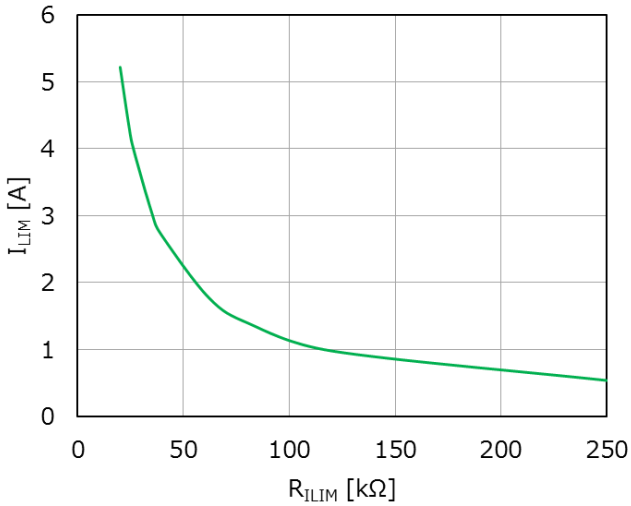
The following is a diagram of the peripheral circuitry of the ILIM terminal and the relation between $R_{ILIM}$ and $I_{LIM}$.




**ILIM Terminal External Circuits**




**$R_{ILIM}$-$I_{LIM}$ Characteristics**

For reference table below shows the resistivity of the $R_{ILIM}$ and the current $I_{LIM}$.

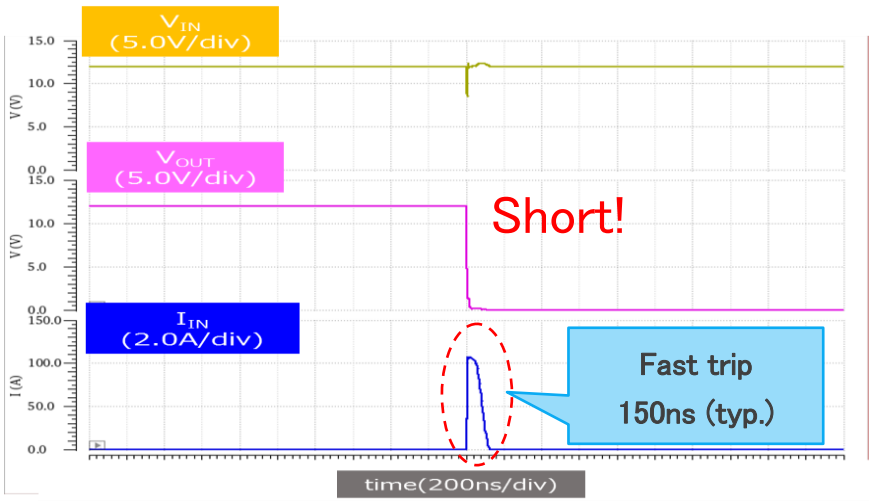
| $R_{ILIM}$ (kΩ) | $I_{LIM}$ (A) (typ.) | Conditions |
|---|---|---|
| 20 | 5.15 | $V_{IN}$-$V_{OUT}$=1 V |
| 24 | 4.38 | |
| 36 | 3.00 | |
| 62 | 1.78 | |
| 120 | 0.96 | |
| 250 | 0.5 | |
| 0 | 0.64 | |
| OPEN | 0.64 | |

**4) Short Circuit protection**

The short-circuit protection function prevents excessive current from flowing by stopping operation when the power supply line or load is short-circuited due to some kind of abnormality. If the output current is 1.6 times the current limit ($I_{LIM}$) for a very short period of time, the output is judged to be short-circuited and this function operates.

Toshiba eFuse IC employs an ultra-high-speed short-circuit protecting circuit (Fast trip function). Simulation results are shown to suppress the current to near zero at 150 ns (typ.) from the occurrence of the short-circuit.

The following figure shows the operating waveforms of the simulated Fast trip function.




**Output voltages and output current waveforms during fast trip operation**



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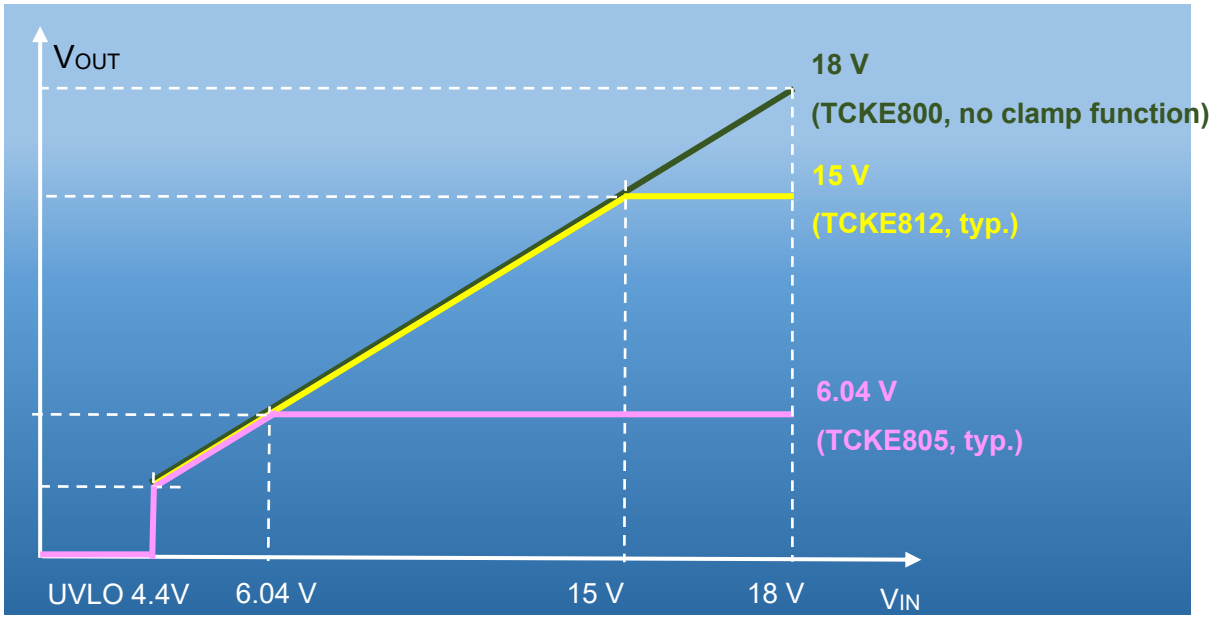
The short-circuit protection circuit performs the return operation 100 μs after Fast trip. If the short-circuit continues, the protection operation starts again. The latch type does not attempt to recover thereafter, but continues to be protected until it is restarted by the control signal. The auto-retry type attempts to recover until the short-circuit condition is resolved by using the thermal shutdown cycle.

**5) Overvoltage protection function**

The overvoltage clamp function clamps the output voltage with a limited voltage and prevents overvoltage from being applied to the load without outputting any more voltage. This function is available on the TCKE805/812 series and is not included in the TCKE800 series. The limit voltages are set to 6.04 V (typ.) for the TCKE805 series and 15 V (typ.) for the TCKE812 series. The diagram below shows the relation between the input voltage and the output voltage of TCKE800/805/812 series.




**Overvoltage Characteristics of TCKE800/805/812**

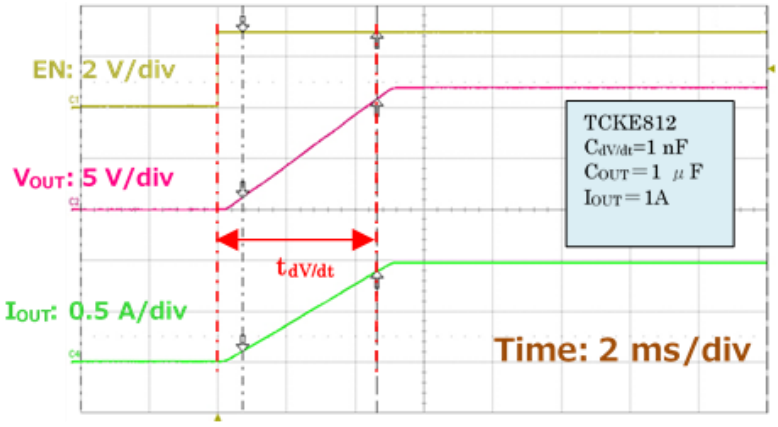
Similar to the overcurrent protection and short-circuit protection, the auto-retry type will attempt to recover from the overvoltage, but the latch type will retain this state until it is restarted.

**6) Inrush current reduction**

When the output is turned on, an inrush current flows to charge the capacitor connected to the load side. If this current is too large, the overcurrent protection circuit may malfunction, making it impossible to start up, or the output voltage may overshoot.

To prevent this, this function controls the slew rate when the output voltage rises by limiting the inrush current.

The following figure shows the rise of the output voltage ($V_{OUT}$) and the inrush current when the inrush current is limited by this function. As shown below, the output current at the start-up is gradually increasing.




**Inrush current reduction (slew rate control) function**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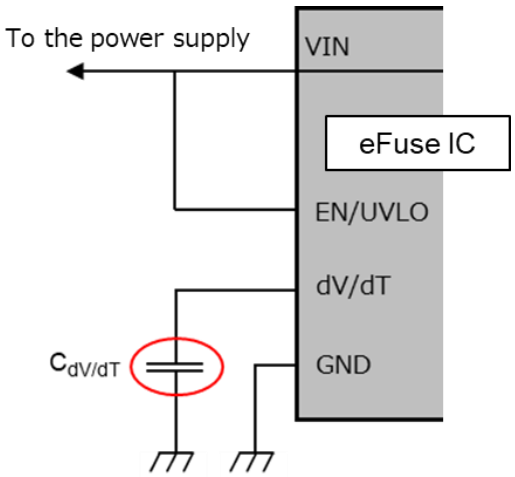
**7) Setting of slew rate control for inrush current reduction**

Toshiba eFuse IC has a variable inrush current function. The external capacitor at the dV/dT terminal can be used to appropriately set the rise time ($t_{dV/dT}$) of the output voltage. The formula for the rise time is as follows:

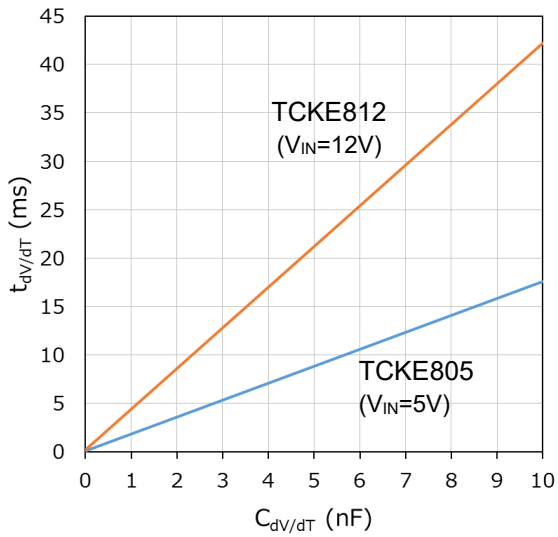
$$t_{dV/dT}\ (s) = 0.36 \times 10^{6} \times V_{IN} \times (C_{dV/dT} + 50 \times 10^{-12}) + 3.0 \times 10^{-4}$$

$V_{IN}$: input voltage (V), $C_{dV/dT}$: external capacitance of dV/dT terminal (F)

The following chart shows the peripheral circuit diagram of the dV/dT terminal and graphs showing the relation between $C_{dV/dT}$ and $t_{dV/dT}$.




**External Circuits around dV/dT Terminal**

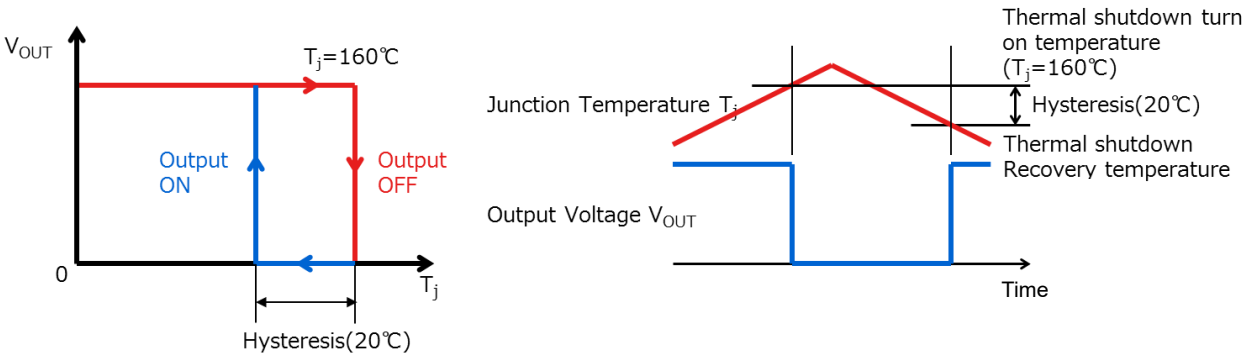



**$C_{dV/dT}$-$t_{dV/dT}$ Characteristics**

**8) Thermal shutdown function**

Thermal shutdown (overheat protection) is a function to shut off and protect the output by setting the IC to standby when a large current continues to flow to the output and the junction temperature of the eFuse IC exceeds the set temperature.

The following figure shows the operation image of the thermal shutdown function. When the thermal shutdown is activated, no current flows through the IC, and the junction temperature begins to drop. Hysteresis is given to the operating temperature and the recovery temperature of the thermal shutdown. The IC will not recover until the temperature drops after a certain period of time.




**Operation of thermal shutdown function**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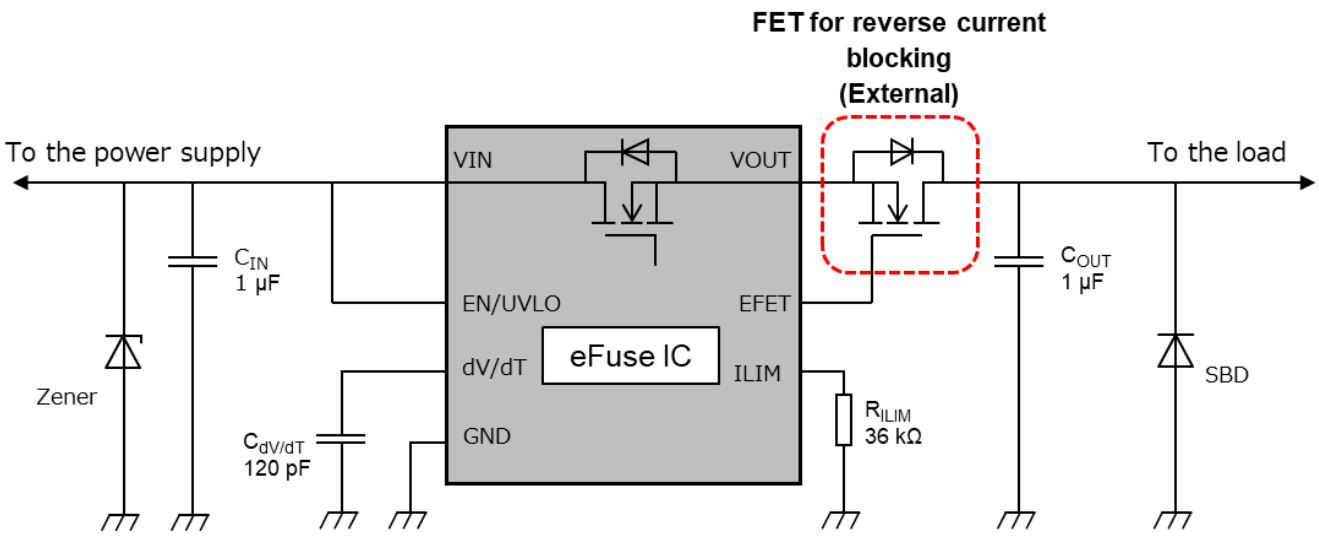
**9) Reverse current blocking**

As an option, Toshiba eFuse IC can prevent reverse current flow by attaching an N-channel MOSFET to the EFET terminal. The reverse current blocking function prevents reverse current from the output side to the input side when the operation of the eFuse IC is stopped, for example, by turning off the power supply of the VIN or controlling the input side by the EN/UVLO terminal.

The circuit for using the reverse current blocking function is shown in the figure below.




**Examples of eFuse IC Peripheral Circuits with Reverse current blocking Function**

Our SSM6K513NU is recommended as an external FET to prevent backflow. SSM6K513NU main characteristics are as follows:

- Drain-Source voltage: $V_{DSS}$ = 30 V
- Gate-Source Voltage: $V_{GSS}$ = 20 V
- Drain current: $I_D$ = 15 A
- Drain-Source on-resistance: $R_{DS\ (ON)}$ =8 mΩ @$V_{GS}$=4.5 V

When using other products, select a product with as low of on-resistance as possible, with sufficient $V_{DSS}$ and $I_D$ margins for the power supply voltage and the load current that is expected to be used.

The EFET terminal outputs the internally boosted voltage $V_{IN}$+4.9V (typ.). If this function is not used, open the terminal.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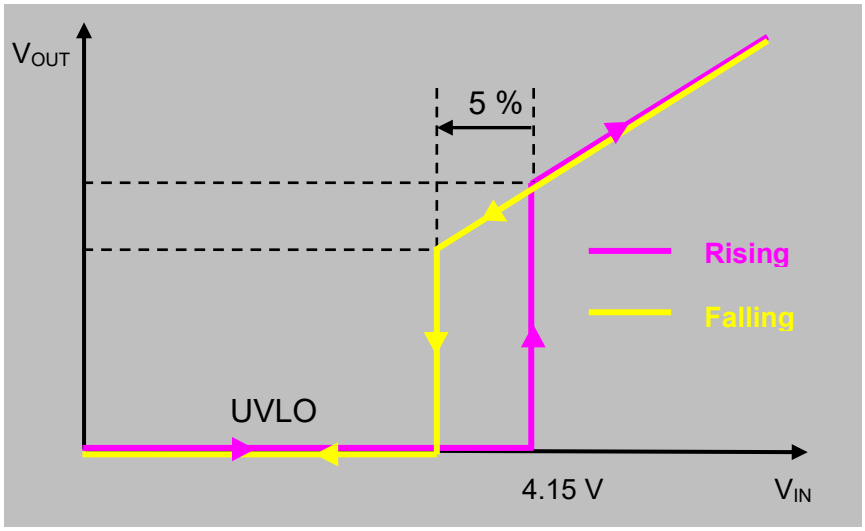
**10) Under voltage lockout function (UVLO)**

This function stops the operation of the eFuse IC when the input voltage is low and prevents malfunction of the load. The TCKE8xx series will not operate unless the input voltage exceeds 4.15 V (typ.). This voltage has hysteresis at the rising and falling edges. At the falling edge, the voltage stops at 5% (typ.) lower than 4.15 V at the rising edge (about 3.95 V).
The following figure shows the operation of this function.



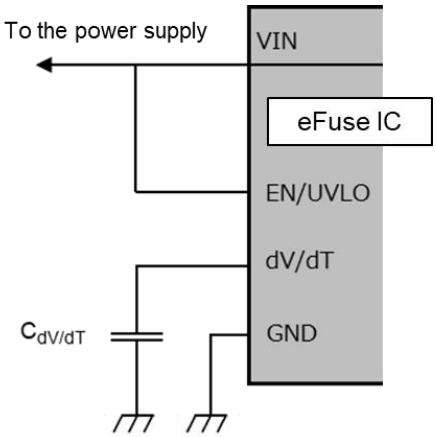

Operation of UVLO circuit

**11) EN/UVLO terminal function**

The TCKE8xx series is equipped with EN/UVLO terminal, and this terminal can be used to control the operation of the whole eFuse IC. It is also possible to set the operating voltage of the under voltage lockout function to the optimum value by externally attaching a resistor.

The following are examples of uses for this terminal.

(1) When the operating voltage of the under voltage lockout function is not changed or the operation control is not performed.




Connections of EN/UVLO terminals (Direct VIN connection)

Connect the EN/UVLO terminal directly to the VIN terminal. This eliminates the need for pull-up resistors in the TCKE8 series. The EN/UVLO terminal is designed to be breakdown-voltage 18 V, and the VIN terminal and the EN/UVLO terminal can be directly connected. This helps reduce the number of parts.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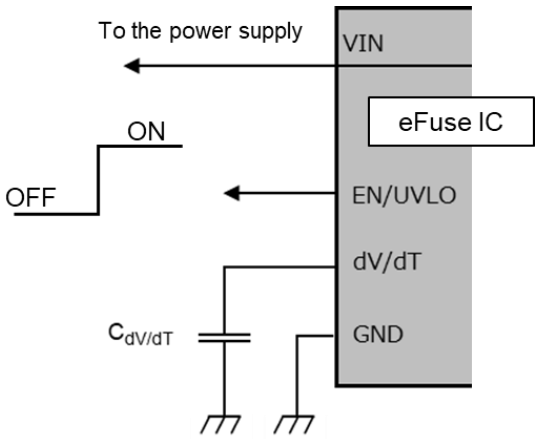
(2) When the operating voltage of the under voltage lockout function is not changed and the operation control is performed from the outside.

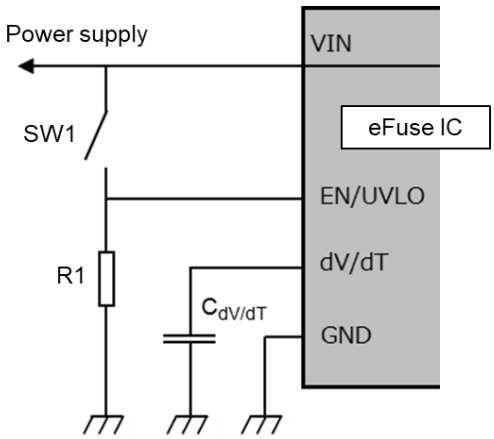



Connecting Examples of EN/UVLO Terminals (External Control)

Connect external control signals directly into the EN/UVLO terminal. Since the on/off threshold voltages of the EN/UVLO terminals are hysteretic, set the "H" level of the control signal to be 1.1 V (typ.) or higher and the "L" level of the control signal to be 0.96 V (typ.) or lower.

If the EN/UVLO terminal is open (indefinite), the eFuse IC operation may become abnormal. Be careful not to open this terminal even when it is at the "L" level.

(3) When the operating voltage of the under voltage lockout function is not changed and the operation is controlled by the short-circuit switch with the VIN terminal.




Connection examples of EN/UVLO terminals (connected by VIN and switches)

Switches can be directly connected to the VIN so that the operation can be controlled. A pull-down resistor is required to prevent the EN/UVLO terminal from being opened when the SW1 is opened. The value of the pull-down resistor may be any value that does not cause the EN/UVLO terminal to become indefinite. However, when the SW1 is conducting, consider the current flowing through R1, and check the value with the actual device to determine the value of the pull-down resistor.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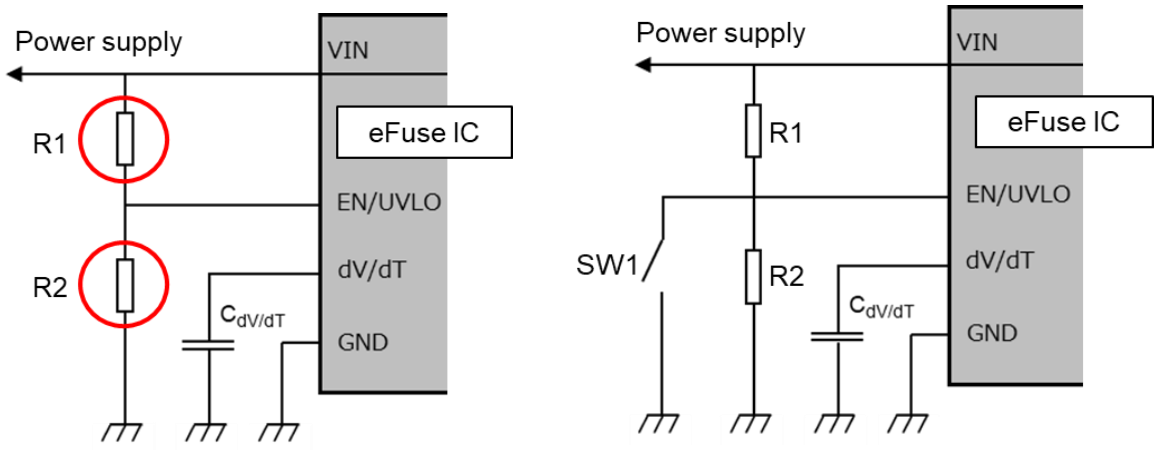
(4) To change the operating voltage of the under voltage lockout function

By adding an external resistor to the EN/UVLO terminal, the operating voltage of the under voltage lockout function can be changed to an optimum value. An example of the circuit is shown in the figure below.




**a)** In case of no operation control

**b)** in case of operation control

Connections of EN/UVLO terminals (VIN resistive division)

**a)** is an example of the circuit when the operation control is not performed by the EN/UVLO terminal, and **b)** is an example of the circuit when the operation control is performed.

As shown in the drawing, operation is stopped when the input voltage drops by controlling the operation of the EN/UVLO terminal with the voltage obtained by dividing the input voltage by external resistors. The operating voltage of the under voltage lockout function can be set to the optimum value by properly selecting the external resistance. However, the voltage cannot be set to 4.15 V or less.

The equation for setting $V_{IN_UVLO(fall)}$ by controlling the external resistors R1 and R2 of the EN/UVLO terminal is as follows.

$$V_{IN_UVLO_{(fall)}}(V) = \frac{R1 + R2}{R2} \times V_{ENF}(V)$$

$V_{ENF}$: EN threshold (falling) 0.96 V (typ.)

As described above, the control voltage of the EN/UVLO terminal is hysteretic, and therefore the voltage to be activated at the time of rising changes. The start-up voltage $V_{IN_UVLO(rise)}$ is calculated by the following equation.

$$V_{IN_UVLO_{(rise)}}(V) = \frac{R1 + R2}{R2} \times V_{ENR}(V)$$

$V_{ENR}$: EN Threshold Voltage (rising) 1.1 V (typ.)

As shown in **b)** above, the switch can be connected in parallel with R2 to control the operation. In this case, contrary to the case of (3), the eFuse IC stops operating at the time of SW1 conduction. At this time, R1 is the current limiting resistor. Be careful when selecting the resistors for R1 and R2.

**12) Precautions regarding protection functions**

Toshiba eFuse IC has various protection functions. Be aware that not every function will cause the eFuse IC to cease functioning. When using these products, please read through and understand the concepts described and follow absolute maximum ratings from the information above or from our 'Semiconductor Reliability Handbook'. Please operate these products below absolute maximum ratings in all instances. Furthermore, Toshiba highly recommends inserting failsafe systems into the design.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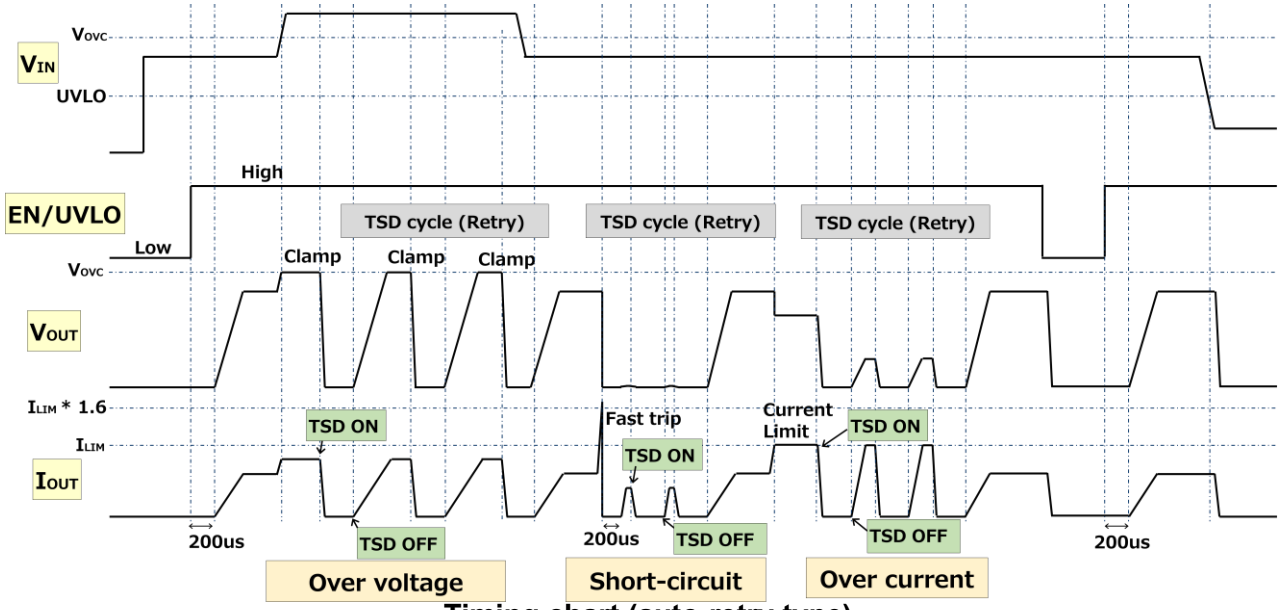
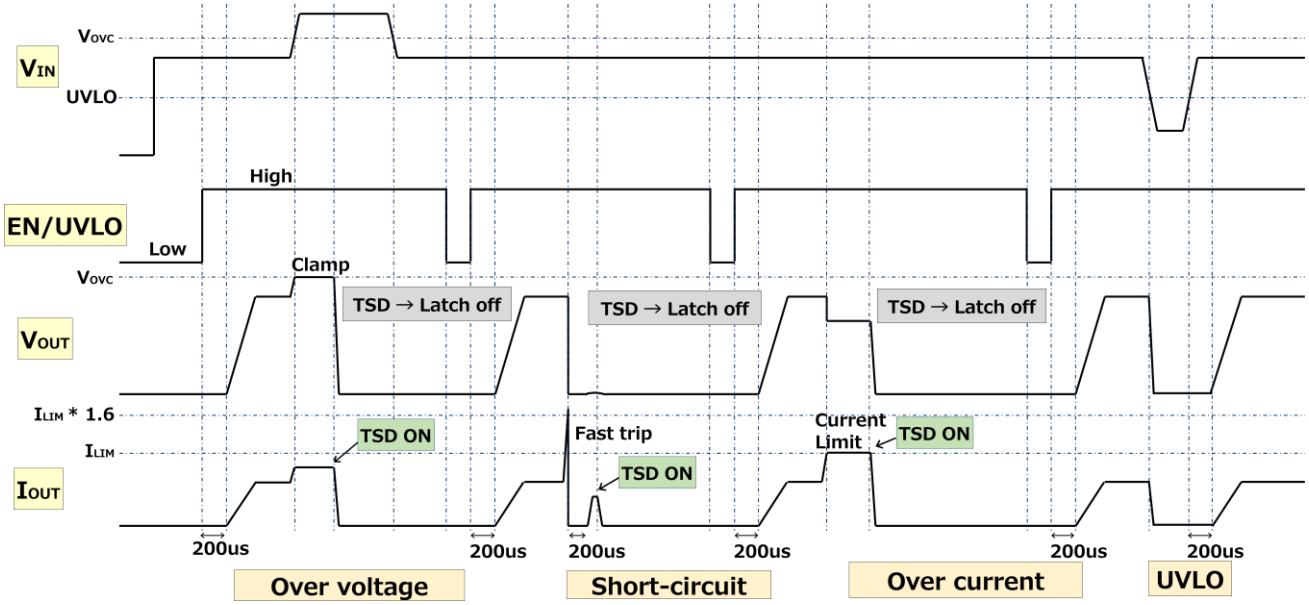
**13) Timing chart**

The timing chart of the auto-retry type is shown in the figure below.




**Timing chart (auto-retry type)**

The timing chart of the latch type is shown in the figure below.




**Timing chart (latch type)**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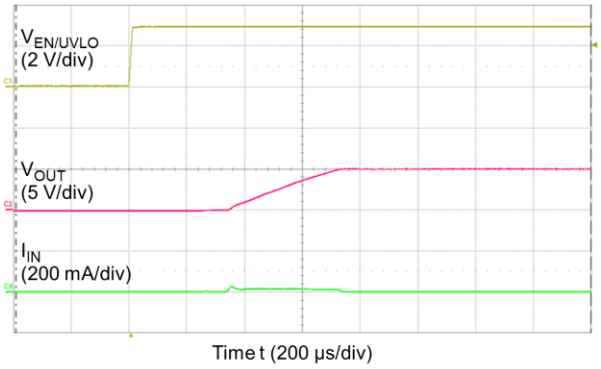
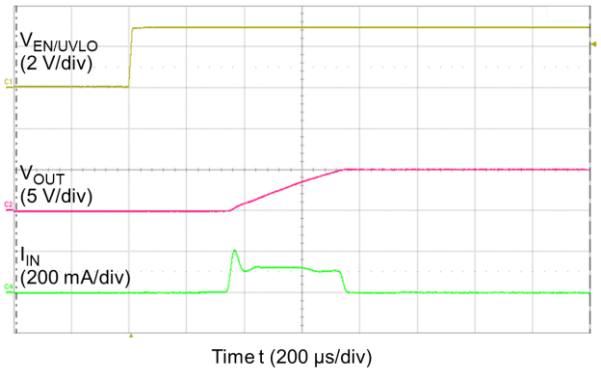
Representative Typical Characteristics

**$t_{ON}$ Response**

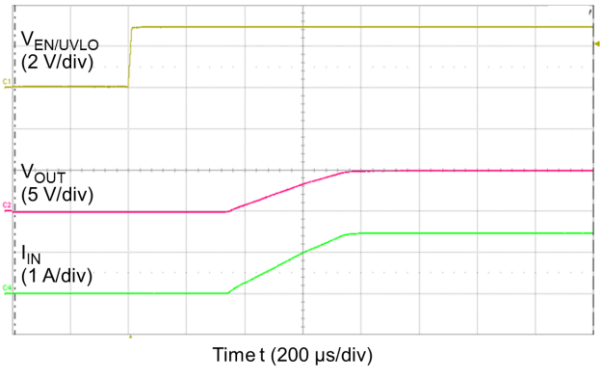
$V_{IN}$ = 5 V, $C_{dV/dT}$ = 120 pF, $C_{OUT}$ = 1 μF, $R_{LOAD}$ = OPEN



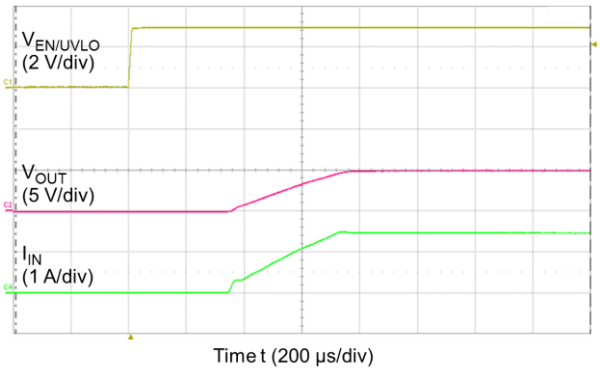

$V_{IN}$ = 5 V, $C_{dV/dT}$ = 120 pF, $C_{OUT}$ = 10 μF, $R_{LOAD}$ = OPEN




$V_{IN}$ = 5 V, $C_{dV/dT}$ = 120 pF, $C_{OUT}$ = 1 μF, $R_{LOAD}$ = 3.3 Ω

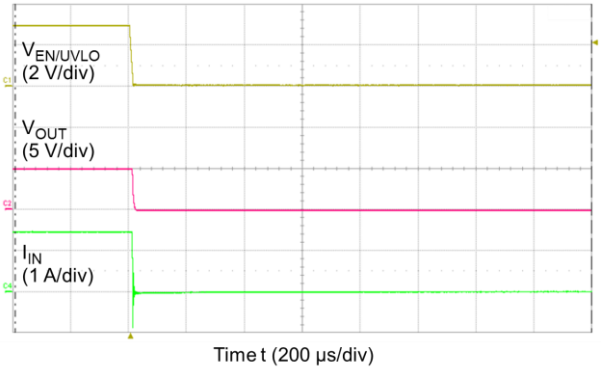



$V_{IN}$ = 5 V, $C_{dV/dT}$ = 120 pF, $C_{OUT}$ = 10 μF, $R_{LOAD}$ = 3.3 Ω



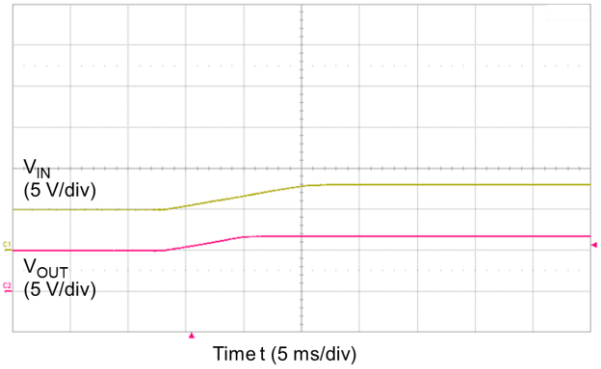

**$t_{OFF}$ Response**

$V_{IN}$ = 5 V, $C_{dV/dT}$ = 120 pF, $C_{OUT}$ = 1 μF, $R_{LOAD}$ = 3.3 Ω




**Over voltage clamp**

$C_{dV/dT}$ = Open, $C_{OUT}$ = 1 μF, $R_{LOAD}$ = Open
$V_{IN}$ 5V to 8V




Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.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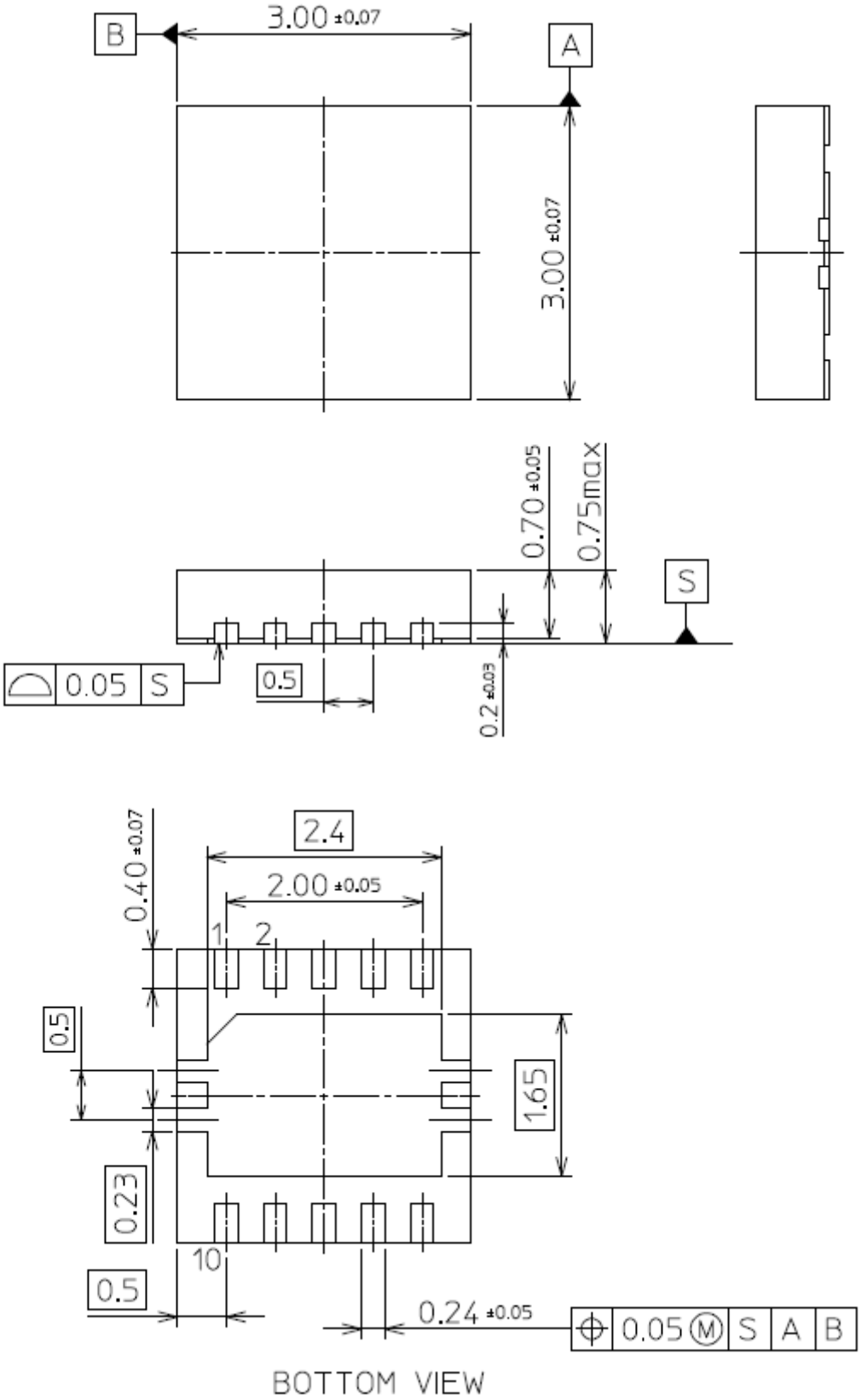
## 13. Package Dimensions

WSON10B

Unit: mm




Weight : 19.3 mg ( typ.)



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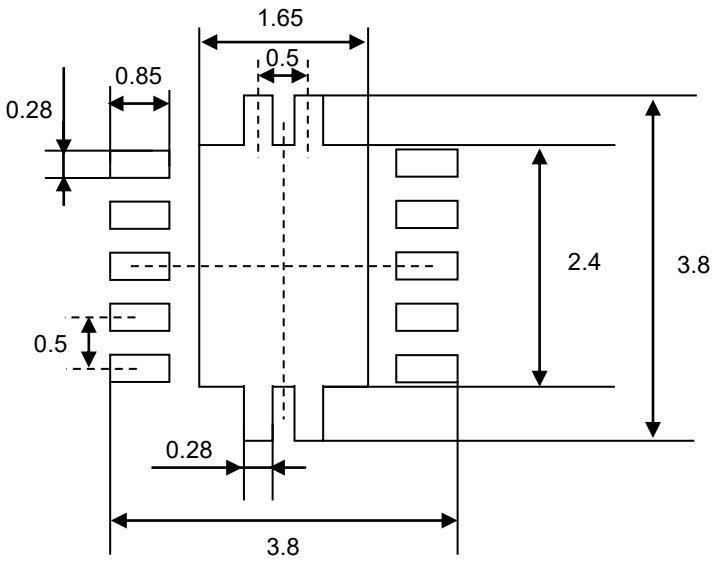
## 14. Land pattern dimensions for reference only

Unit: mm





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