

Triple-Output Step-Down Switching Regulator

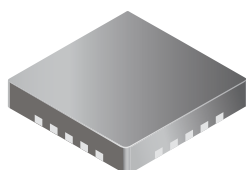
FEATURES AND BENEFITS

- Three buck converters
- 4.5 to 34 V input voltage range
- 550 kHz fixed frequency
- Multiphase switching
- Independent control of each converter
- Power-on-reset flag
- Internal compensation
- 4 × 4 mm QFN package, small PCB footprint

APPLICATIONS

- Photo, inkjet, and portable printers
- Industrial
- Handheld devices
- Portable devices

PACKAGE: 20-CONTACT QFN (SUFFIX ES)



Not to scale

DESCRIPTION

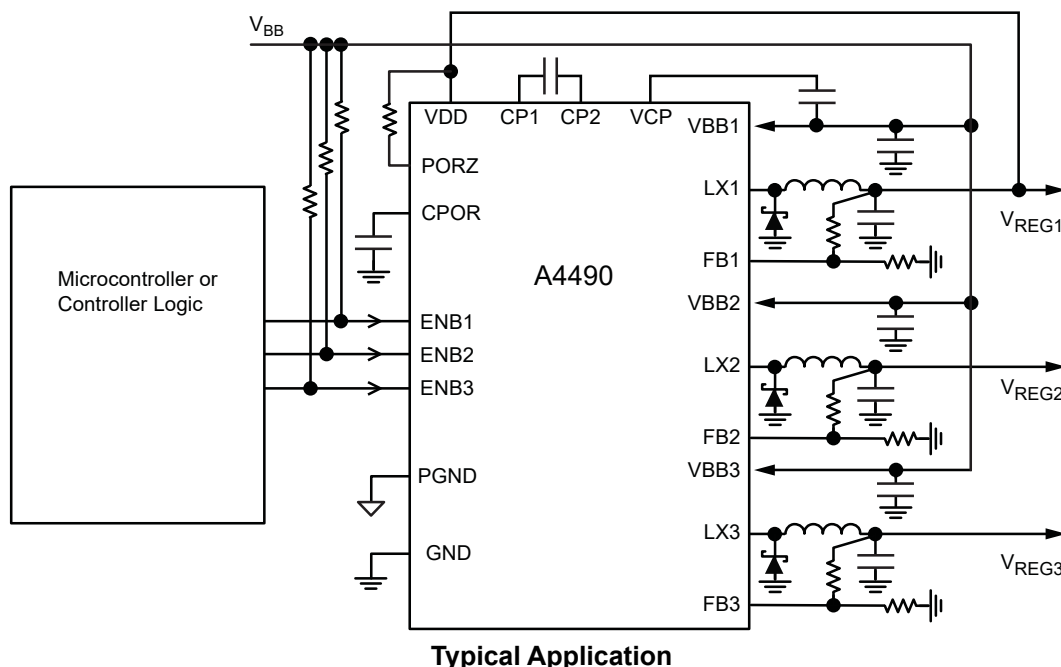
Designed to provide the power-supply requirements of printers, office automation, industrial, and portable equipment, the A4490 provides three high-current, high-performance, switching-regulator outputs with independent soft start.

High-frequency switching allows selection of inexpensive inductors and small ceramic output capacitors. The turn-on cycles of the regulators are interleaved to minimize stresses on the input capacitors and to reduce electromagnetic interference (EMI). A charge pump provides the supply to drive the power switches, which ensures operation at very-wide operating duty cycles and avoids the need for power-draining clamp circuits.

A power-on-reset (POR) circuit with user-configurable delay indicates when the enabled regulators are in specification. The POR flag also indicates when the input-voltage reduces to less than the specification, which gives the system controller advance warning while the switches continue to operate down to the shutdown level.

Internal diagnostics provide comprehensive protection against overloads, input undervoltages, and overtemperatures.

The A4490 is provided in a 20-contact, 4 mm × 4 mm, 0.75 mm nominal overall height quad-flat no lead (QFN) package, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.



SPECIFICATIONS

SELECTION GUIDE

Part Number	Packing	Operating Temperature Range (°C)
A4490EESTR-T	1500 pieces per 7-in. reel	–40 to 85



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		36	V
LX1, LX2, and LX3 Pins	V_{LXn}		–1 to 36	V
PORZ and VDD Pins	V_{IN}		–0.3 to 7	V
ENBx Pin Input Current	I_{ENBx}	Driven by a current-limited voltage source	1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

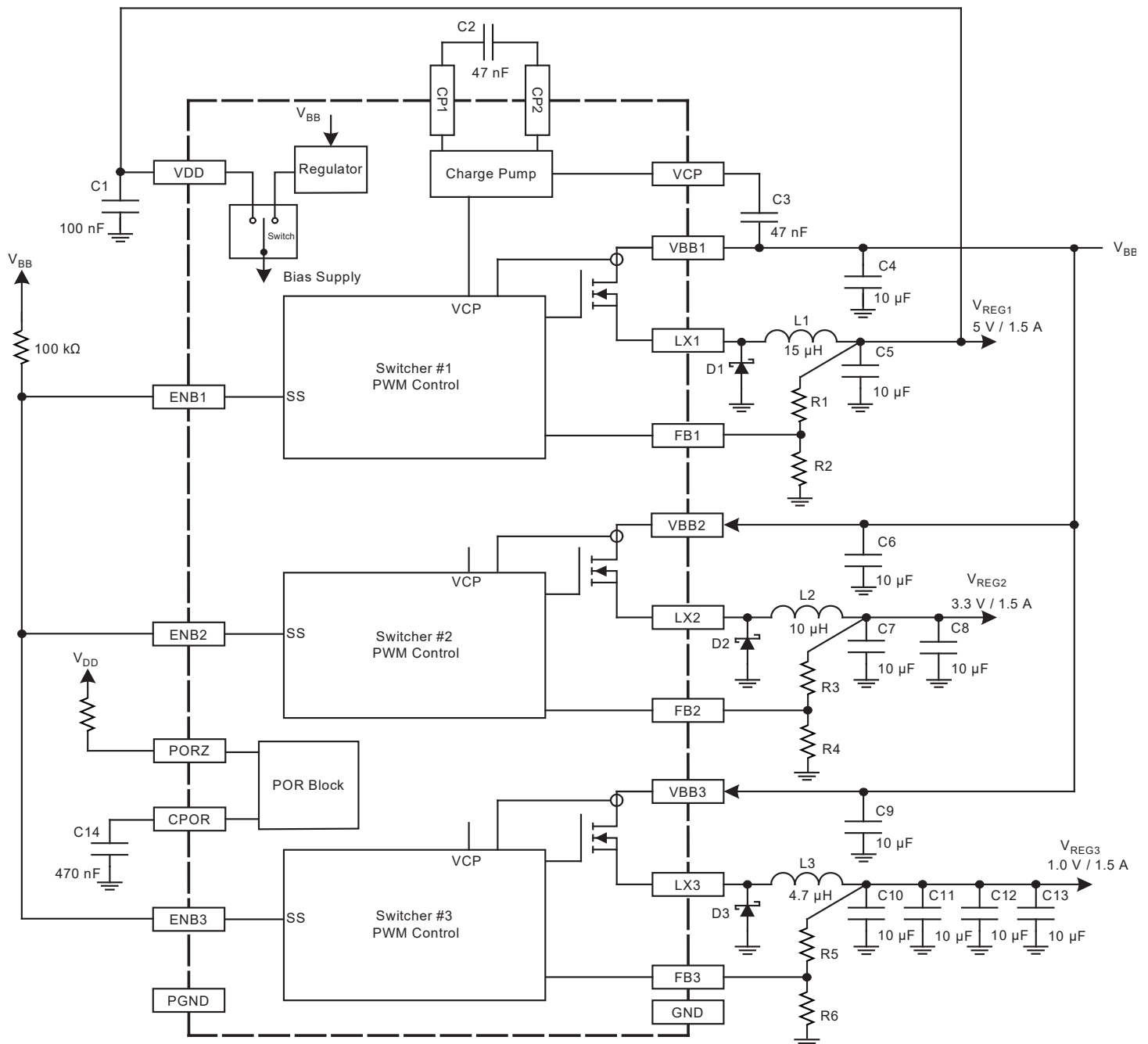
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
Load Supply Voltage	V_{BB}	To operate at $V_{BB} < 6$ V, connect V_{DD} supply to the V_{BB} supply. See the Power Configurations section.	4.5	–	34	V
LX1, LX2, and LX3 Pins	V_{LXn}		–0.7	–	34	V
Operating Ambient Temperature	T_A		–40	–	85	°C
Junction Temperature	T_J		–40	–	125	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	37	°C/W

[1] Additional thermal information is available on the Allegro website.

FUNCTIONAL BLOCK DIAGRAM

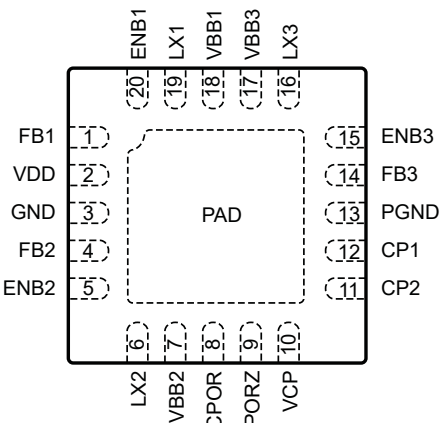


NOTE: All capacitors are ceramic X5R.

A4490

Triple-Output Step-Down Switching Regulator

PINOUT DIAGRAM AND TERMINAL LIST



Package ES Pinouts

Terminal List Table

Number	Name	Function
1	FB1	Feedback switching cycle 1 (REG1)
2	VDD	Bias supply
3	GND ^[1]	Ground
4	FB2	Feedback switching cycle 2 (REG2)
5	ENB2	Enable REG2, logic input, active high
6	LX2	Switch node REG2
7	VBB2 ^[2]	Input supply for REG2
8	CPOR	POR delay adjustment
9	PORZ	POR output, active low
10	VCP	Charge-pump reservoir
11	CP2	Charge-pump capacitor terminal
12	CP1	Charge-pump capacitor terminal
13	PGND ^[1]	Ground for charge-pump circuitry
14	FB3	Feedback switching cycle 3 (REG3)
15	ENB3	Enable REG3, logic input, active high
16	LX3	Switch node REG3
17	VBB3 ^[2]	Input supply for REG3
18	VBB1 ^[2]	Input supply for REG1
19	LX1	Switch node REG1
20	ENB1	Enable REG1, logic input, active high
–	PAD ^[3]	Exposed pad for enhanced thermal dissipation

^[1] GND and PGND should be connected externally.
^[2] The three VBBx pins should be connected together externally.
^[3] The thermal pad should be connected to the ground (0 V) plane using thermal vias.

ELECTRICAL CHARACTERISTICS [1][2]: Valid at $T_A = 25^\circ\text{C}$, $V_{BB} = 6$ to 34 V, V_{DD} supplied externally, unless noted otherwise.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
VBB Quiescent Current	I _{BBON}	ENBx = high, I _{LOAD} = 0 mA, V _{BB} = 12 V, current drawn by feedback resistors ignored	–	1	2	mA
	I _{BBOFF}	ENBx = 0 V	–	1	–	μA
VDD Supply Range	V _{DD}		3.3	–	5.5	V
VDD Quiescent Current	I _{DD}	ENBx = high	–	–	6	mA
		ENBx = 0 V	–	1	–	μA
REG1, REG2, AND REG3						
Feedback Input Bias Current	I _{BIAS}		–400	–100	100	nA
Feedback Voltage	V _{FB}	With respect to 0.8 V target voltage	–	±1.5	–	%
Output Voltage Regulation ^[3]	V _{OUT}	V _{REGx} = 5 V, I _{OUT} = 0 to 1.5 A, T _A = –20°C to 85°C	–2.5	–	2.5	%
		V _{REGx} = 5 V, I _{OUT} = 0 to 1.5 A, T _A = –40°C to 85°C	–3.5	–	3.5	%
PWM Frequency	f _{SW}		470	550	630	kHz
Maximum Duty Cycle	D _{max}		90	–	–	%
Minimum Duty Cycle	D _{min}		–	5	–	%
Buck Switch On-Resistance	R _{DS(on)}	T _J = 25°C, I _{LOAD} = 1.5 A, V _{BB} = 6 V	–	450	–	mΩ
		T _J = 125°C, I _{LOAD} = 1.5 A, V _{BB} = 6 V	–	700	–	mΩ
		T _J = 25°C, I _{LOAD} = 1.5 A, V _{BB} = 4.5 V	–	560	–	mΩ
		T _J = 125°C, I _{LOAD} = 1.5 A, V _{BB} = 4.5 V	–	870	–	mΩ
Current Limit Threshold	I _{LIM}	Peak current through switch with D = 0.9	2	–	–	A
Soft Start Duration	t _{ss}		0.625	1.25	1.875	ms
LOGIC INPUTS AND OUTPUTS						
ENBx Input Voltage	V _{IL}		–	–	0.8	V
	V _{IH}		2	–	–	V
ENBx Input Hysteresis	V _{I(hys)}		300	500	–	mV
ENBx Input Current	I _{IL}	V _{IH} ≤ 5 V	–1	–	1	μA
PORZ Output (Open Drain)	V _{PORZL}	I _{PORZL} = 1 mA, fault asserted	–	–	0.4	V
PORZ Output Leakage Current	I _{PORZH}	V _{PORZ} = 5 V, fault not asserted	–1	–	1	μA
Power-On-Reset (POR) Duration	t _{POR}	C _{POR} = 470 nF	75	115	155	ms

Continued on the next page...

ELECTRICAL CHARACTERISTICS [1][2]: Valid at $T_A = 25^\circ\text{C}$, $V_{BB} = 6$ to 34 V , V_{DD} supplied externally, unless noted otherwise.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
VREGx Undervoltage Lockout Startup	$V_{REGUV(su)}$	FB1, FB2, and FB3 rising	–	85	–	%VFB
VREGx Undervoltage Lockout Shutdown	$V_{REGUV(sd)}$	FB1, FB2, and FB3 falling	–	80	–	%VFB
VREGx Undervoltage Lockout Startup Hysteresis	$V_{REGUV(suhys)}$		–	5	–	%
VBB Undervoltage Lockout Startup	$V_{BBUV(su)}$	External VDD supply not used, V_{BB} rising	3.7	4.3	4.7	V
	$V_{BBCPUV(su)}$	External VDD supply used, V_{BB} rising	3.8	4.2	4.6	V
VBB Undervoltage Lockout Shutdown	$V_{BBUV(sd)}$	External VDD supply not used, V_{BB} falling	3.6	4.1	4.7	V
	$V_{BBCPUV(sd)}$	External VDD supply used, V_{BB} falling	3	3.5	4.3	V
VBB Undervoltage Lockout Shutdown Hysteresis	$V_{BBUV(sd)hys}$	External VDD supply not used	–	500	–	mV
	$V_{BBCPUV(sd)hys}$	External VDD supply used	–	600	–	mV
VBB Undervoltage Warning Threshold	$V_{BBUV(por)}$	V_{BB} falling (forces PORZ low); switches continue to operate	–	3.6	–	V
Junction Overtemperature Shutdown	T_{JTSD}	Temperature rising	–	165	–	$^\circ\text{C}$
Junction Overtemperature Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = $T_{JTSD} - T_{JTSD(hys)}$	–	15	–	$^\circ\text{C}$

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified pin.

[2] Specifications throughout the junction temperature range of -40°C to 125°C are assured by design and characterization.

[3] Average value of V_{OUT} relative to target voltage. The effects of the feedback resistors are not taken into account.

FUNCTIONAL DESCRIPTION

Basic Operation

The A4490 contains three fixed-frequency buck switching converters with peak current-mode control, including slope compensation. Each converter can be independently turned on and off via the enable inputs (EN1, EN2, and EN3), which are active high. When enabled, the corresponding output is brought up under the control of a soft-start routine, which avoids output voltage overshoot and minimizes input inrush current.

The output voltage is typically divided by an external potential divider and compared to an internal reference voltage to produce an error signal, also known as the current demand signal. The current signal through the buck switch is converted into a voltage. This signal is then compared to the current demand signal to create the required duty cycle.

At the beginning of each switching cycle, the buck switch turns on. When the current signal through the switch reaches the level of the current demand signal, the on time of the switch terminates. On the next switching cycle, the switch again turns on, and the cycle repeats.

One shared clock defines the switching frequency for each regulator. To minimize the pulsed current drawn from the input filter capacitors, each of the three switching cycles (REG1, REG2, and REG3) is phase-shifted by 120 degrees with respect to the others. In certain conditions—for example, a low V_{BB} condition and a relatively high user-set output voltage—switching overlap between channels is inevitable.

For a condition that causes a duty cycle (DC) of less than the minimum value, such as a light load or a high V_{BB} voltage, the converter enters a pulse-skipping mode that ensures regulation is maintained.

A charge-pump regulator is provided to ensure a sufficient gate drive is available for all three power switches across the full input-voltage range. This regulator allows operation even at very-wide operating duty cycles. Upon initial power-up, an internal regulator is used to provide the bias supply for on-chip control functions.

In a short-circuit or overload event, each regulator channel uses pulse-by-pulse current limiting. Depending on the duration of the overload, the IC temperature might rise sufficiently to cause the thermal shutdown circuit to operate. After the thermal disable condition is removed, and assuming all other conditions are met, the part automatically restarts under control of the soft-start circuit. For more information, see the Shutdown section.

Power Configuration

The A4490 supports alternative schemes to provide a logic supply voltage on the VDD pin. In addition, power-up and power-down of the integrated circuit (IC) can be performed using either the V_{BB} pin or the ENB pin.

POWERING VDD

To minimize power dissipation, especially at high input voltages, application of an external supply to the VDD input pin is recommended. Typically, this voltage derives from the setup of one of the three regulated outputs, between 3.3 and 5 V (V_{REGx}).

Another advantage of an externally powered VDD is that it lowers the V_{BB} undervoltage lockout level. To maximize switch runtime during a V_{BB} power-down condition, two alternative undervoltage shutdown conditions are supported based on which VDDower configuration is implemented. When an external V_{DD} is not applied, the minimum V_{BB} ($V_{BBUV(sd)}$) is 4.1 V (typical). When an external V_{DD} is applied, the minimum V_{BB} ($V_{BBCPUV(sd)}$) is 3.5 V (typical).

CAUTION: When deriving VDD from a VREG output, during initial application of V_{BB} , the internal bias supply automatically starts from the internal regulator. This occurs because VREG has not yet reached regulation. Because there is no external VDD, the startup threshold is determined by $V_{BBUV(su)}$ (4.3 V typical). When VREG begins to supply VDD externally, the shutdown threshold reduces to $V_{BBCPUV(sd)}$ (3.5 V typical). This assumes that V_{REG} is present.

POWER-UP AND POWER-DOWN WITH V_{BB}

Each enable input (ENBx) is tied to the V_{BB} rail via a 100 k Ω resistor and the VDD is supplied from one of the regulator outputs, as shown in Figure 1. This holds each enable input in the high state. When the V_{BB} voltage reaches the minimum threshold ($V_{BBUV(su)}$), ramp-up of the charge-pump supply (V_{CP}) occurs. When V_{BB} plus V_{CP} reaches the minimum threshold ($V_{BBCPUV(su)}$), the soft start routines initiate (t_{SS}) for all three regulator channels (V_{REGx}). When all three regulators reach the 85% FBx threshold, the POR timer is initiated. After the POR period (t_{POR}) elapses, PORZ transitions to the high state, which indicates that all the regulators and V_{BB} are within specification.

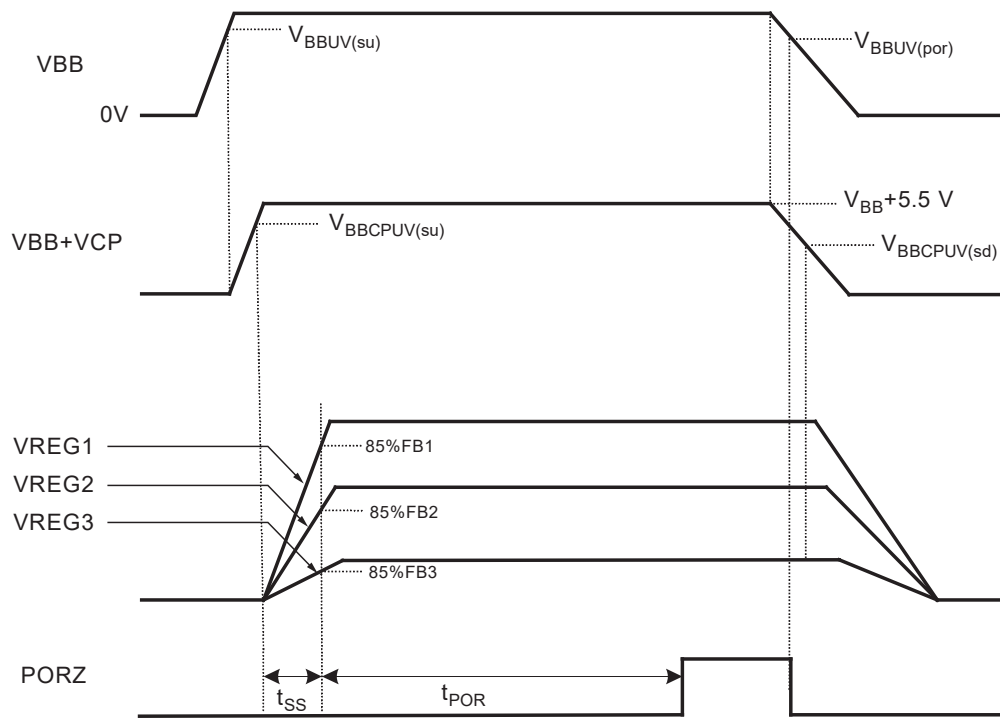


Figure 1: Timing Diagram for Power-Up and Power-Down Using the VBB Pin

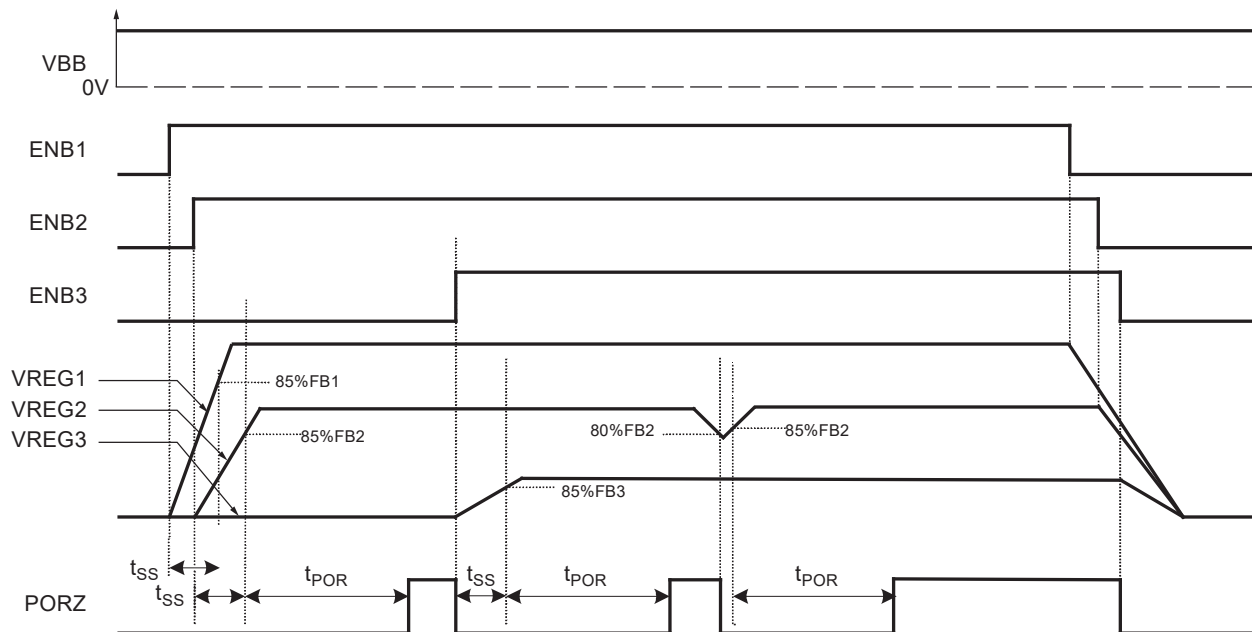


Figure 2: Timing Diagram for Power-Up and Power-Down Using the ENB Pin

When the V_{BB} voltage reduces to less than the undervoltage warning level ($V_{BBUV(por)}$) of 3.6 V (typical), the PORZ flag resets. This provides advance warning to the system controller that the V_{BB} voltage is falling.

NOTE: This feature is only guaranteed when V_{DD} is supplied externally. During this interval, the three switches continue to operate.

While V_{BB} falls further, the V_{CP} supply also tends to fall, which degrades the drive voltage to the series switches. In addition, the higher-voltage rails start to fall out of regulation first, as the corresponding maximum duty cycle (D_{max}) for these particular converters is reached.

When all regulator V_{BB} undervoltage thresholds are reached before power-down of the A4490 occurs, the regulators that have the lower output voltages achieve some level of steady state. For example, if the V_{DD} supply is derived externally, it might be possible for a 1 V output to continue to operate down to a V_{BB} of 3.4 V (typical). The extent of this effect depends on myriad factors, including input and output filter capacitances, output loads, gate drive amplitudes, MOSFET $R_{DS(on)}$, and so forth.

POWER-UP AND POWER-DOWN WITH ENABLE

Power-up with the EN pin, as shown in Figure 2, occurs when V_{BB} is present and the UVLO startup thresholds ($V_{BBUV(su)}$ and $V_{BBCPUV(su)}$) are reached. In turn, each of the regulators are enabled. Initially, V_{REG1} is enabled and is brought-up under the control of the soft-start circuit (t_{SS}). Before V_{REG1} reaches 85% of FB1, V_{REG2} is enabled and is brought-up under a separate soft start control.

When both regulators have reached their respective 85% FB thresholds, the POR timer is initiated.

NOTE: The POR timer is enabled only after all enabled regulators reach their corresponding 85% FB levels. After the POR time (t_{POR}) elapses, if the FB levels of V_{REG1} and V_{REG2} are not less than their respective 80% FB levels, then the PORZ signal transitions to the high state.

At some point later, if V_{REG3} is enabled, PORZ is reset and V_{REG3} is brought-up under the control of the soft-start circuit. When the 85% FB3 threshold is reached, the POR timer is initi-

ated. After t_{POR} elapses, if all FB levels exceed their respective 80% FB levels, the PORZ signal transitions to the high state.

NOTE: If any regulator channel is not enabled, the channel does not influence PORZ. To avoid multiple signal changes of the PORZ signal, a system design where all three regulator channels are within specification before t_{POR} elapses is recommended.

If any regulator channel reduces to less than 80% of FB, the PORZ signal is reset. If the voltage then recovers to within 85% of FB, the POR timer is reinitiated.

NOTE: When the feedback voltage reduces to less than 80% of FB, a soft start is not initiated. This feature allows a rapid autorestart in the event of an overload or similar fault. If a soft start is required, it is recommended for the system controller to disable then re-enable the relevant regulator channels upon receipt of the PORZ reset signal. As soon as the last regulator is disabled, the PORZ signal is reset.

If a soft start is required upon receipt of the PORZ reset signal, it is recommended for the system controller to disable then re-enable the relevant regulator channels. As soon as the last regulator is disabled, the PORZ signal is reset.

POWER ON RESET

The POR duration, t_{POR} , is determined by the capacitor connected to the CPOR pin. The value of this capacitor must be selected appropriately. The value of t_{POR} can be determined by:

Equation 1:

$$t_{POR} = 2.131 \times 10^5 \times C_{POR}$$

When both V_{BB} exceeds the undervoltage warning levels and the FB pins of the regulators that are enabled exceed 85% of the V_{REG} voltage, the PORZ output transitions to the high state.

Because the external capacitor is charged via a 5 μ A current source, care must be taken in the layout to avoid additional leakage paths. The capacitor should be positioned adjacent to the CPOR pin, and the ground connection to the A4490 GND pin should be as short as practicable.

To avoid the possibility of multiple triggerings of the PORZ output, it is recommended that the t_{POR} period be set to exceed the startup phases of all three regulators.

OUTPUT VOLTAGE SELECTION

The output voltage on each of the three regulators is set by the following relationship, shown here for the V_{REG1} channel:

Equation 2:

$$R_1 = R_2 [(V_{REG1}/V_{FB}) - 1]$$

where R_2 (connected between the GND and FB1 pins) should be a value between 4.7 and 12 k Ω , R_1 is connected between the output rail and the FB1 pin, V_{REG1} is the set output regulator voltage, and V_{FB} is the reference voltage.

The tolerances of the feedback resistors influence the voltage set point. Therefore, to target an overall regulation value, it is important to consider the tolerance selection.

The bias current, I_{BIAS} , that flows out of the FB1 node into R_2 introduces a small voltage offset to the output.

ENABLE

Each regulator channel can be individually enabled via the corresponding ENBx pin. After the application of the V_{BB} voltage, if automatic startup of any channel is required, that particular channel should have the ENB pin tied to the V_{BB} rail via a pull-up resistor. To prevent turn-on of the internal protection clamps, this resistor should be selected to limit the current to less than the maximum specified value, 1 mA. A 100 k Ω pull-up resistor is recommended: This value ensures that, when $V_{BB} = 36$ V, the current remains at less than the maximum value.

SOFT START

Each regulator channel contains a soft-start circuit. A soft-start cycle is initiated when: the appropriate regulator enable input is set to high; the V_{BB} , charge pump, and bias supply voltages exceed the minimum values; and a thermal shutdown condition does not exist.

NOTE: Except in the case of thermal shutdown event, an over-load or short circuit does not cause a soft-start cycle.

During a soft-start cycle, the reference voltage ramps from 0 to 0.8 V (typical), which forces the current demand signal to increase in a linear fashion.

SHUTDOWN

In the event of a thermal shutdown event or an undervoltage on V_{BB} ($V_{BBUV(sd)}$ or $V_{BBCPUV(sd)}$), all converter channels are disabled.

If the ENB inputs are enabled, upon removal of the above fault conditions, the appropriate channels autorestart under control of the soft-start circuit.

CURRENT LIMIT

The typical peak current limit for each channel is specified as 2.5 A minimum, with a duty cycle of 0.9. The minimum current limit occurs at the maximum duty cycle (0.9) because the slope compensation has a maximum effect under this condition. As the duty cycle reduces, the current limit increases. This means that an application that operates with a narrow duty cycle can operate with a load current of greater than 2 A.

The typical peak current limit versus duty cycle is shown in Figure 3. For example, it is possible to operate with a peak current limit of 3.75 A with a duty cycle of 0.3.

Under the worst-case load and input voltage conditions, in addition to ensuring that the peak current limit is not exceeded, it is important to check thermal-performance implications, as described in the Thermal Considerations section.

Component Selection

INDUCTOR

The inductance value, L , determines the ripple current. It is important to ensure that the minimum current limit is not exceeded for the worst-case conditions: $V_{BB(min)}$, $I_{LOAD(max)}$, $f_{SW(min)}$, and $L_{(min)}$.

Because powdered iron solutions exhibit relatively high core losses that can have a large impact on long-term reliability, gapped ferrite solutions are recommended.

Inductors are typically specified at two current levels: the root mean square (rms) current level and the saturation current level. With regard to the rms current, it is important to understand how the rms current level is specified, in terms of ambient temperature. Some manufacturers provide an ambient-only specification, while others provide a temperature specification that includes a self-induced temperature rise. For example, if an inductor is rated for 85°C and includes a self-induced temperature rise of 25°C at maximum load, the inductor cannot be safely operated beyond an ambient temperature of 60°C at full load. The rms current can be assumed to be simply the maximum load current, with perhaps some margin to allow for overloads, and so forth.

To determine the inductor value, the first step is to specify a peak-to-peak ripple current, typically about 20% to 25% of the maximum load.

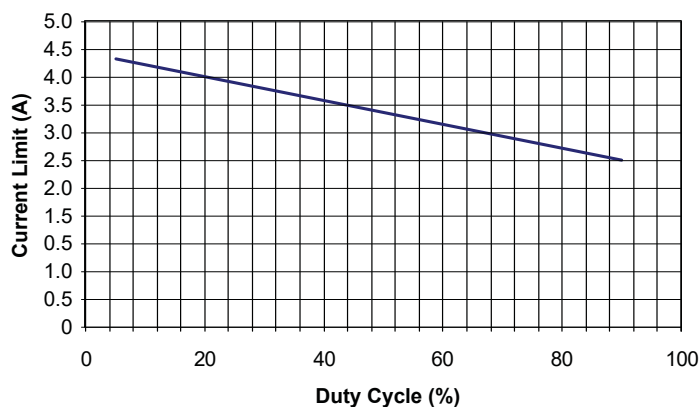


Figure 3: Current Limit vs. Duty Cycle

The maximum peak-to-peak ripple current, I_{RIPPLE} , occurs at the maximum input voltage. Therefore, the duty cycle (D) should be found under these conditions (for the V_{REG1} channel):

Equation 3:

$$D(min) = \frac{V_{REG1} + V_f}{V_{BB(max)} + V_f}$$

where V_f is the forward voltage reduction of the recirculation diode.

The required inductance can be determined by:

Equation 4:

$$L(min) = \frac{V_{BB(max)} - V_{REG1}}{I_{RIPPLE}} \times D(min) \times \frac{1}{f_{SW(min)}}$$

NOTE: The manufacturer-provided inductance tolerance should also be taken into account. This value might be as high as $\pm 20\%$. To avoid instability in the innermost circuit loops due to insufficient slope compensation, the peak-to-peak current should not exceed 1 A.

To ensure that the saturation current level of the chosen inductor is not exceeded, The maximum peak current can be found from:

Equation 5:

$$I_{sat} = I_{LOAD} + \frac{I_{RIPPLE}}{2}$$

The recommended inductor manufacturers and ranges are:

- Taiyo Yuden: NR6045 series for 1.5 A outputs
- Taiyo Yuden: NRG4026 series for 1.0 A outputs
- Sumida: CDH74 series for 1.5 A outputs

OUTPUT CAPACITOR

In the interests of size, cost, and performance, use of ceramic X5R or X7R capacitor types is highly recommended. When using ceramic capacitors, another important consideration is the electric field (e-field) effects on the actual value of the capacitor. To minimize the effects of the capacitance reducing with output voltage, the working voltage of the capacitor should be considerably more than the set output voltage. For output voltages of 3.3 V and less, 6.3 V-rated capacitors are recommended. For output voltages of 5 V, 10 V-rated capacitors are recommended.

The output capacitor determines the output voltage ripple and is used to close the control loop. To guarantee stability, the capacitance must increase as the output voltage reduces. Because the ripple voltage is typically specified as a percentage of output voltage, this requirement is reasonable from a ripple-voltage point of view.

The minimum output capacitance for a given output voltage is:

Output Voltage (V)	Minimum Output Capacitance (μF)
15	3.3
12	4.7
5	10
3.3	20
1.8 to 2.5	30
<1.8	40

Use of a capacitance value that exceeds the above value reduces the bandwidth. This might be necessary in a system that has extremely low ripple/noise requirements.

The output ripple is largely determined by the output capacitance, and the effects of the equivalent series resistance (ESR) and equivalent series inductance (ESL) can largely be ignored, assuming good layout practices are observed.

The output voltage ripple can be approximated as:

Equation 6:

$$V_{\text{RIPPLE}} \approx \frac{I_{\text{RIPPLE}}}{8 \times f_{\text{SW}} \times C_{\text{OUT}}}$$

Use of ceramic capacitors generally prevents the need to consider the current-carrying capability due to the negligible heating effects of the ESR. Also, the flow of rms current into the output capacitor is extremely low.

INPUT CAPACITOR

Use of a ceramic X5R or X7R capacitor is highly recommended.

The value of the input capacitance determines the amount of current ripple (i.e., electromagnetic interference, EMI) that appears at the source (V_{BB} supply) terminals. The amount of current flow in and out of the input capacitor depends on the relative impedance between the input capacitor impedance and the source impedance. To achieve a low-impedance filter solution, placement of at least two capacitors in parallel is recommended.

Generally, the heating effects of the rms current flow through the ESR do not need to be considered. Also, the phase-shift of the input current drawn by each of the regulators helps to reduce the overall rms current.

FLYBACK DIODE

This diode conducts during the off-time of the switch. To minimize both the forward drop and switching losses, a Schottky diode is recommended.

The worst-case dissipation occurs at the maximum V_{BB} , when the duty cycle (D) is at the minimum. The average current through the diode can be determined by:

Equation 7:

$$I_{\text{DIODE(av)}} = I_{\text{LOAD}} \times (1 - D_{(\text{min})})$$

The forward voltage drop (V_f) can be determined from the diode characteristics by use of the actual load current (not the average current).

The static power dissipation can be determined by:

Equation 8:

$$P_{\text{STAT}} = I_{\text{LOAD(av)}} \times V_f$$

To ensure that enough heat-sink capability is provided to maintain the diode junction temperature within the safe operation area for the device, it is also important to account for the thermal rating of the package ($R_{\theta\text{JA}}$) and the ambient temperature.

To minimize the effects of heat from the A4490 on the diode, and vice versa, diode mounting on the reverse side of the printed circuit board (PCB) is recommended.

SUPPORT COMPONENTS

The POR capacitor (C11), charge-pump capacitor (C1), reservoir capacitor (C2), and V_{DD} filter capacitor (C12) should be ceramic X5R or X7R.

Thermal Considerations

To ensure the A4490 operates in the safe operation area, which effectively means the junction temperature is restricted to less than 150°C, several checks should be made. The general approach is to determine the thermal impedance ($R_{\theta JA}$) required to maintain the junction temperature at a given level, for a particular power dissipation.

Another factor worth consideration is that other power-dissipating components on the system PCB might influence the thermal performance of the A4490. For example, the power loss contribution from the recirculation diode and the sense resistor might cause the junction temperature of the A4490 exceed the expected temperature.

The steps that follow provide guidelines to determine a suitable thermal solution.

NOTE: The optimal solution usually requires an iterative process.

1. Estimate the maximum ambient temperature, $T_{A(max)}$, of the application.
2. Define the maximum junction temperature, $T_{J(max)}$.
NOTE: The absolute maximum is 150°C.
3. Determine the worst-case power dissipation, $P_{D(max)}$.

The evaluation should consider these factors at the maximum load and minimum V_{BB} . Contributors are switch static losses, dynamic losses, and control losses, as described in the steps that follow.

1. Switch Static Losses

Determine the switch static losses as follows

- A. Estimate the maximum duty cycle as:

Equation 9:

$$D_{(max)} = (V_{REG} + V_f) / (V_{BB(min)} + V_f)$$

where V_f is the forward voltage drop of the Schottky diode under the given load current.

- B. Estimate the $R_{DS(on)}$ of the each regulator switch at the given junction temperature as:

Equation 10:

$$R_{DS(on)TJ} = R_{DS(on)25C} [1 + (T_J - 25) / 200]$$

NOTE: If the V_{BB} range is restricted to between 4.5 and 5.5 V, $R_{DS(on)}$ increases. For example, at 25°C:

- When $V_{BB} > 6$ V, $R_{DS(on)}$ is 450 mΩ (typical), as stated in the Electrical Characteristics table.
- When $V_{BB} = 4.5$ V, $R_{DS(on)}$ is 560 mΩ (typical).
- When V_{BB} is between 4.5 and 6 V, $R_{DS(on)}$ can be determined by linear approximation.

For more information about operation of the A4490 at a V_{BB} voltage between 4.5 and 5.5 V, see the Power Configurations section.

- C. Determine the static loss for each switch as:

Equation 11:

$$P_{STAT} = I_{LOAD}^2 \times D_{(max)} \times R_{DS(on)TJ}$$

where I_{LOAD} is the load for that particular regulator channel.

2. Switch Dynamic Losses

To determine the switch dynamic losses, estimate the turn-on and turn-off losses as:

Equation 12:

$$P_{DYN} = V_{BB(min)} \times (I_{LOAD}/2) \times 30 \times 10^{-9} \times f_{SW}$$

where f_{SW} is the switching frequency.

3. Control Losses

Determine control losses as:

Equation 13:

$$P_{VBB} = I_{BBON} \times V_{BB}$$

where I_{BBON} is the quiescent current assuming all three regulators are on.

Equation 14:

$$P_{VDD} = I_{VDD} \times V_{DD}$$

where I_{VDD} and is the quiescent current on VDD.

4. Total Losses

Estimate the total losses as:

Equation 15:

$$P_{TOTAL} = P_{STAT1} + P_{STAT2} + P_{STAT3} + P_{DYN1} + P_{DYN2} + P_{DYN3} + P_{VBB} + P_{VDD}$$

5. Thermal Impedance

Determine the thermal impedance required for the solution as:

Equation 16:

$$R_{\theta JA} = (T_J - T_A) / P_{TOTAL}$$

Example

Selected parameters:

- $V_{BB(min)} = 6 \text{ V}$
- $V_{REG1} = 5 \text{ V at } 1 \text{ A}$
- $V_{REG2} = 3.3 \text{ V at } 1 \text{ A}$
- $V_{REG3} = 1.8 \text{ V at } 800 \text{ mA}$
- $T_A = 70^\circ\text{C}$
- $T_J = 115^\circ\text{C}$
- $V_f = 0.4 \text{ V}$

1. Switch static losses:

$$V_{REG1} \text{ duty cycle } (D_1) = (5 + 0.4) / (6 + 0.4) = 0.84$$

$$V_{REG2} \text{ duty cycle } (D_2) = (3.3 + 0.4) / (6 + 0.4) = 0.58$$

$$V_{REG3} \text{ duty cycle } (D_3) = (1.8 + 0.4) / (6 + 0.4) = 0.34$$

The $R_{DS(on)}$ of each switch can be determined by:

$$R_{DS(on)TJ} = 450 \times 10^{-3} [1 + (115 - 25) / 200] = 0.653 \Omega$$

The static loss of each switch can be determined by:

$$P_{STAT1} = I^2 \times 0.84 \times 0.653 = 0.55 \text{ W}$$

$$P_{STAT2} = I^2 \times 0.58 \times 0.653 = 0.379 \text{ W}$$

$$P_{STAT3} = 0.8^2 \times 0.34 \times 0.653 = 0.14 \text{ W}$$

2. Switch dynamic losses:

$$P_{DYN1} = 6 \times (1/2) \times 30 \times 10^{-9} \times 500 \times 10^3 = 0.045 \text{ W}$$

$$P_{DYN2} = 6 \times (1/2) \times 30 \times 10^{-9} \times 500 \times 10^3 = 0.045 \text{ W}$$

$$P_{DYN3} = 6 \times (0.8/2) \times 30 \times 10^{-9} \times 500 \times 10^3 = 0.036 \text{ W}$$

3. Control losses:

$$P_{VBB} = 0.005 \times 6 = 0.03 \text{ W}$$

$$P_{VDD} = 0.001 \times 3.3 = 0.003 \text{ W}$$

4. The total power dissipation can now be determined by:

$$P_{TOTAL} = 0.55 + 0.379 + 0.14 + 0.045 + 0.045 + 0.036 + 0.03 + 0.003 = 1.228 \text{ W}$$

5. The thermal impedance required for the solution can be determined by:

$$R_{\theta JA} = (115 - 70) / 1.228 = 36.6^\circ\text{C/W}$$

To ensure the junction temperature remains at less than 115°C , this particular solution requires a board with a high thermal efficiency. For maximum effectiveness, the material of the PCB pad area underneath the thermal pad of the A4490 should be exposed copper. Several thermal vias (typically, between 4 and 8) should be used to connect the thermal pad to the internal ground plane. If possible, an additional thermal copper plane should be applied to the bottom side of the PCB and connected to the thermal pad of the A4490 through the vias.

This calculation assumes thermal influence from other components is not present. If possible, flyback-diode mounting is recommended on the reverse side of the PCB. Ensure low impedance electrical connections are implemented between board layers.

PCB LAYOUT GUIDELINES

The ground plane is largely dictated by the thermal requirements described previously. The ground-referenced power components should be referenced to a star ground, located away from the A4490 to minimize ground bounce issues.

A small, local, relatively quiet ground plane near the A4490 should be used for the ground-referenced support components, to minimize interference effects of ground noise from the power circuitry. The recommended grounding architecture is illustrated in Figure 4.

To avoid ground bounce and offset issues, the connection for the ground-referenced feedback resistors (R2, R4, and R6) is highly recommended to be placed as close as practicable to the A4490 GND connection.

A local quiet ground plane around these components can be implemented. However, this ground plane should have a high-impedance connection to the star connection of the power stages.

If a ground plane is used, to avoid the possibility of noise pickup, overlap of the switching nodes (LX1, LX2, and LX3) is not recommended. To minimize the possibility of noise-injection issues, isolation of the ground plane around high-impedance nodes (such as FBx, ENBx, and CPOR) is recommended.

In terms of grounding the power components, a star connection should be made to minimize the ground-loop impedances.

IMPORTANT: Although the thermal characteristics of the solution might require a ground plane, implementation of a ground star connection for the power components remains imperative. The ground for the charge pump (PGND) should be connected to the thermal vias.

The importance of ground connections that are as short as practicable and form good star connections is illustrated in Figure 5 and Figure 6.

The current conduction paths during the on-cycle of the switching FET are also shown in Figure 5. The following points should be noted:

- The C_{IN} capacitor should be placed as close as practicable to the VBB terminals.
- The capacitance of the C_{IN} capacitor should be split between the VBB terminals for V_{REG1} and V_{REG3} and the VBB terminal for V_{REG2} .
- The VBB terminals for V_{REG1} and V_{REG2} should be connected via short and wide traces to the VBB terminal for V_{REG3} .
- Each inductor should be connected as close as practicable to the respective switching FET (LX1, LX2, and LX3) and output capacitors.

The current conduction path during the off-cycle of the switching FET is shown in Figure 6. The following points should be noted:

- The diode (D) should be placed as close as practicable to both the switching FET and the inductor.
- Support components POR capacitor (C11), charge pump capacitor (C1), reservoir capacitor (C2), and VDD filter capacitor (C12) should be located as close as practicable to their respective terminal connections. The ground-referenced capacitors should be connected as close as practicable to the GND terminal.

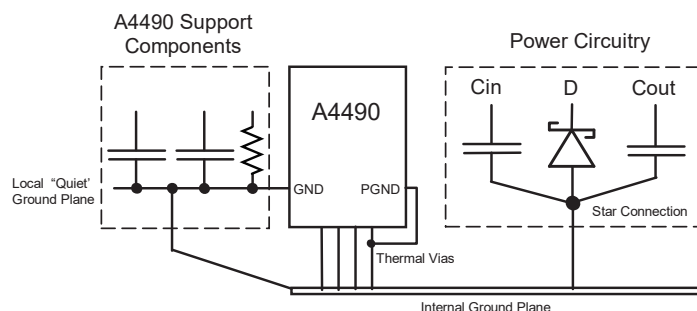


Figure 4: Ground Plane Configurations

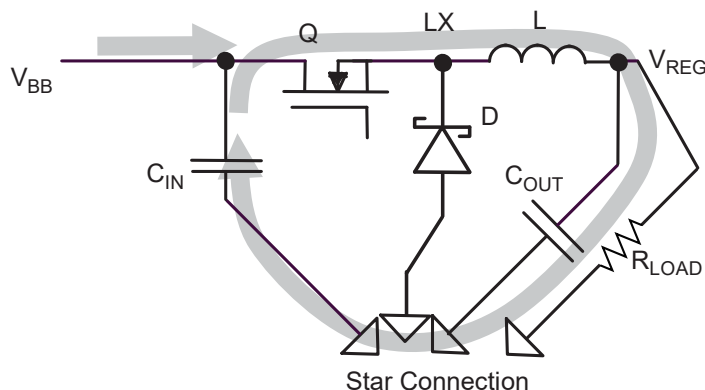


Figure 5: FET On-Cycle Current Conduction Paths

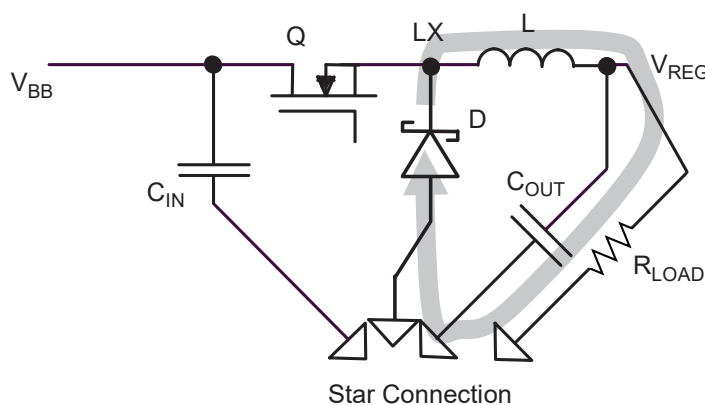
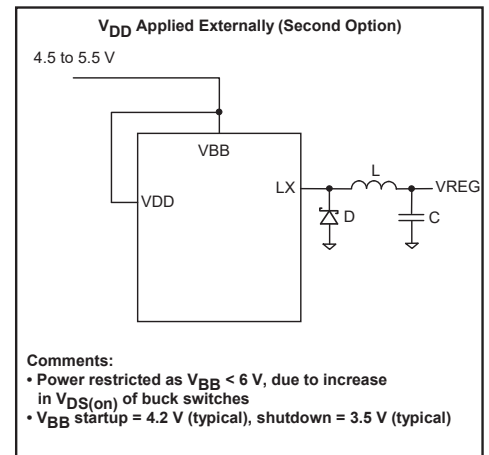
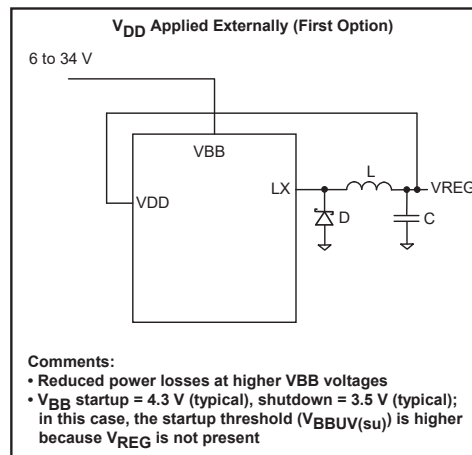
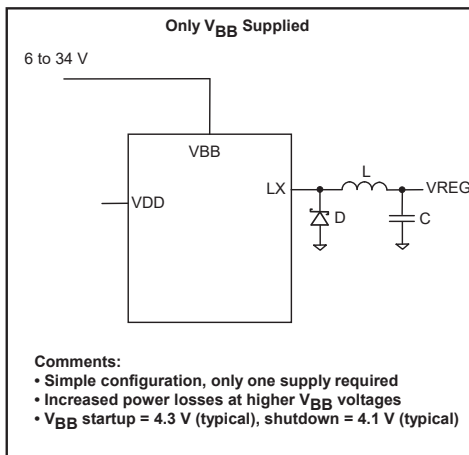


Figure 6: FET Off-Cycle Current Conduction Paths

POWER CONFIGURATIONS

The following three diagrams show typical configurations to provide power to the application. The center diagram corresponds to the Typical Application diagram.



PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-220WGGD)

Dimensions in millimeters – NOT TO SCALE

Exact case and lead configuration at supplier discretion within limits shown

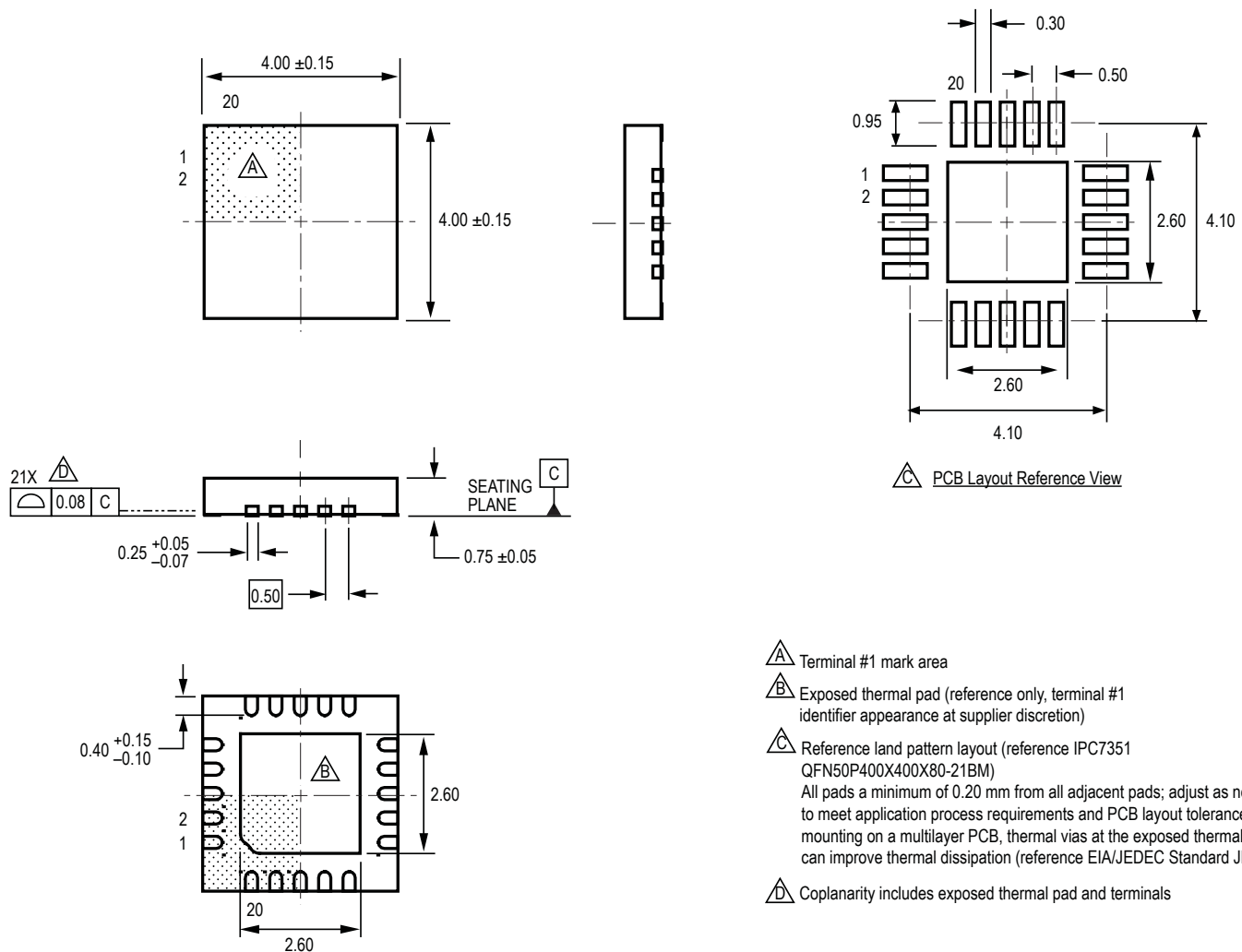


Figure 7: Package ES, 20-Pin QFN

REVISION HISTORY

Number	Date	Description
10	June 26, 2012	Update IDD and undervoltage lockout
11	July 24, 2026	Overhauled web-published document, including a template update and editorial and formatting modifications throughout, and submitted for initial release to document control.

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