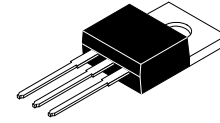


# MOSFET – N-Channel, POWERTRENCH®

105 V, 41 A, 33 mΩ

FDP3672



TO-220-3LD  
CASE 340AT

## Features

- $R_{DS(on)} = 25 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 41 \text{ A}$
- $Q_{G(tot)} = 28 \text{ nC}$  (Typ.) @  $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low  $Q_{rr}$  Body Diode
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

## Applications

- Consumer Appliances
- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

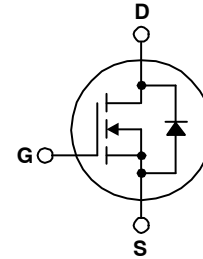
## MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain to Source Voltage	105	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		A
	Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10 \text{ V}$ )	41	
	Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10 \text{ V}$ )	31	
	Continuous Pulsed ( $T_{amb} = 25^\circ\text{C}$ , $V_{GS} = 10 \text{ V}$ , $R_{\theta JA} = 62^\circ\text{C/W}$ )	5.9 Fig. 4	
$E_{AS}$	Single Pulsed Avalanche Energy (Note 1)	48	mJ
$P_D$	Power Dissipation Derate above $25^\circ\text{C}$	135	W
		0.9	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

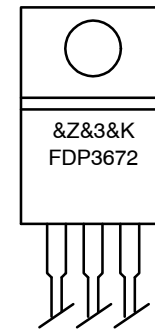
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.11	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	62	



## MARKING DIAGRAM



&Z = Assembly Location  
&3 = Date Code (Year & Week)  
&K = Lot Run Traceability Code  
FDP3672 = Specific Device Code

## ORDERING INFORMATION

Device	Package	Shipping
FDP3672	TO-220-3LD	800 Units / Tube

# FDP3672

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

B <sub>V</sub> DSS	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	105	–	–	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DSS</sub> = 80 V	–	–	1	μA
		V <sub>GS</sub> = 0 V, T <sub>C</sub> = 150°C	–	–	250	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±20	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DSS</sub> , I <sub>D</sub> = 250 μA	2	–	4	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 41 A, V <sub>GS</sub> = 10 V I <sub>D</sub> = 21 A, V <sub>GS</sub> = 6 V I <sub>D</sub> = 41 A, V <sub>GS</sub> = 10 V, T <sub>C</sub> = 175°C	– – –	0.025 0.031 0.063	0.033 0.055 0.070	Ω

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	1670	–	pF
C <sub>oss</sub>	Output Capacitance		–	240	–	
C <sub>rss</sub>	Reverse Transfer Capacitance		–	55	–	
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 41 A, I <sub>G</sub> = 1.0 mA	–	28	37	nC
Q <sub>g(th)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 V to 2 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 41 A, I <sub>G</sub> = 1.0 mA	–	3.9	5	
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 41 A, I <sub>G</sub> = 1.0 mA	–	12	–	
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau		–	8.0	–	
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	6.5	–	

### RESISTIVE SWITCHING CHARACTERISTICS (V<sub>GS</sub> = 10 V)

t <sub>(on)</sub>	Turn-On Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 41 A, V <sub>GS</sub> = 10 V, R <sub>GS</sub> = 11.0 Ω	–	–	90	ns
t <sub>d(on)</sub>	Turn-On Delay Time		–	12	–	
t <sub>r</sub>	Rise Time		–	48	–	
t <sub>d(off)</sub>	Turn-Off Delay Time		–	24	–	
t <sub>f</sub>	Fall Time		–	27	–	
t <sub>(off)</sub>	Turn-Off Time		–	–	77	

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = 41 A	–	–	1.25	V
		I <sub>SD</sub> = 21 A	–	–	1.0	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>SD</sub> = 41 A, dI <sub>SD</sub> /dt = 100 A/μs	–	–	39	ns
Q <sub>rr</sub>	Reverse Recovered Charge	I <sub>SD</sub> = 41 A, dI <sub>SD</sub> /dt = 100 A/μs	–	–	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

- Starting T<sub>J</sub> = 25°C, L = 0.11 mH, I<sub>AS</sub> = 30 A.
- Pulse Width = 100 s.

TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

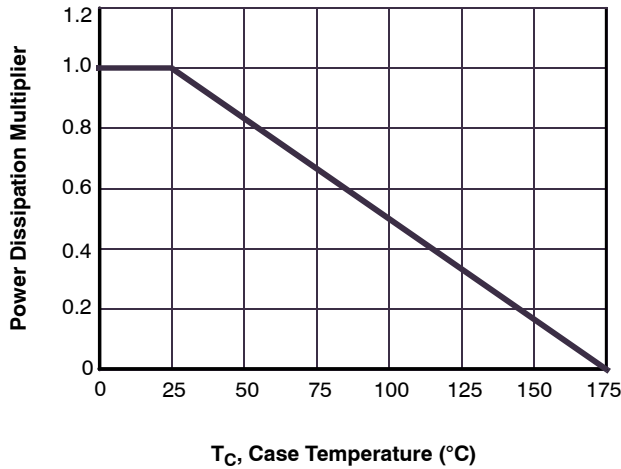


Figure 2. Normalized Power Dissipation vs Ambient Temperature

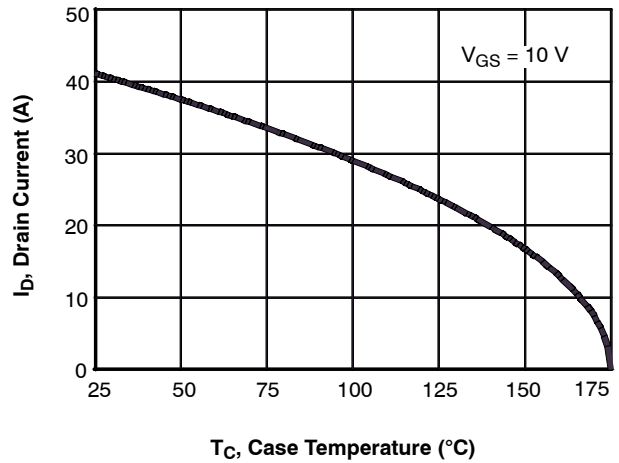


Figure 1. Maximum Continuous Drain Current vs Case Temperature

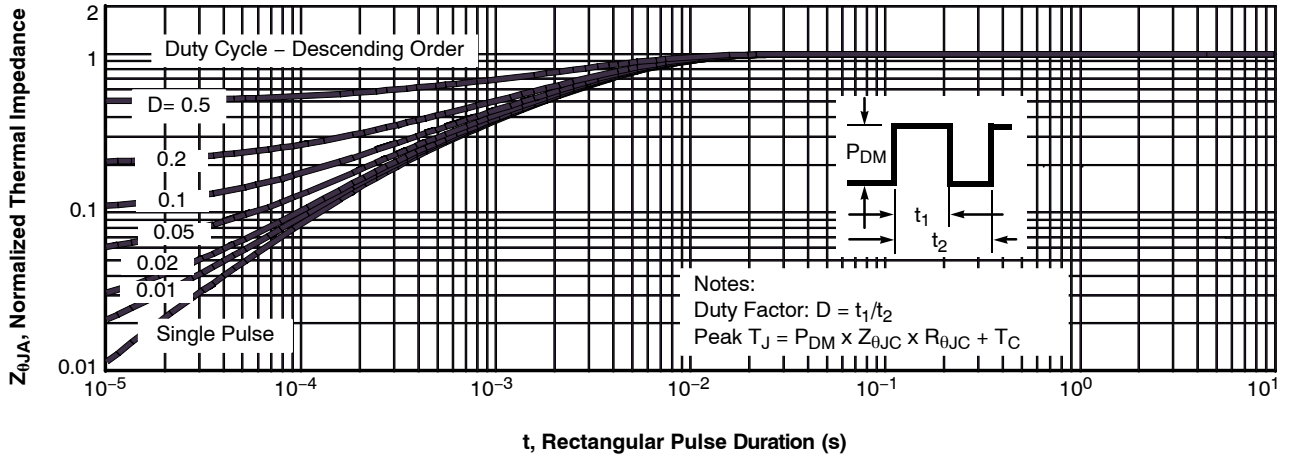


Figure 3. Normalized Maximum Transient Thermal Impedance

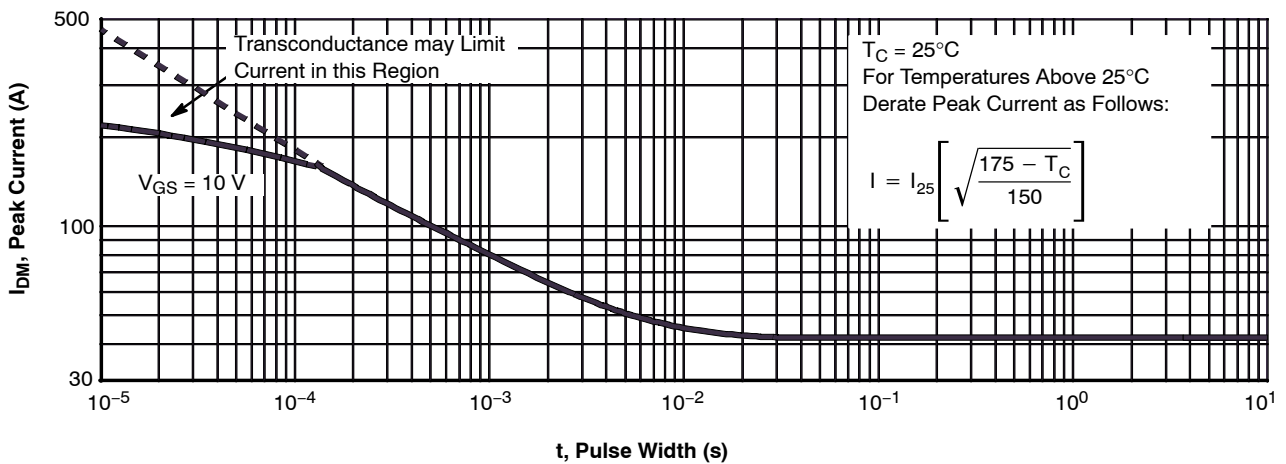


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

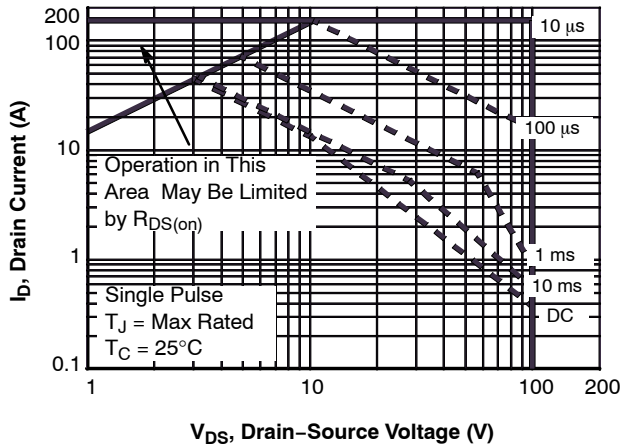


Figure 5. Forward Bias Safe Operating Area

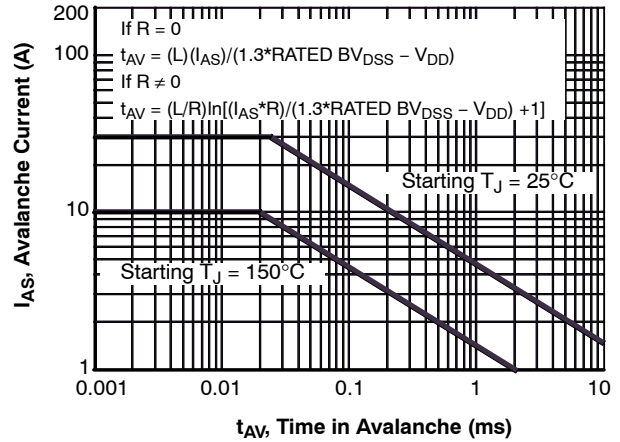


Figure 6. Unclamped Inductive Switching Capability

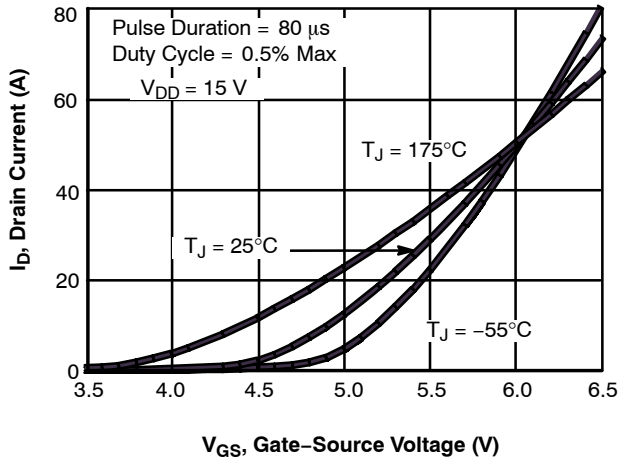


Figure 7. Transfer Characteristics

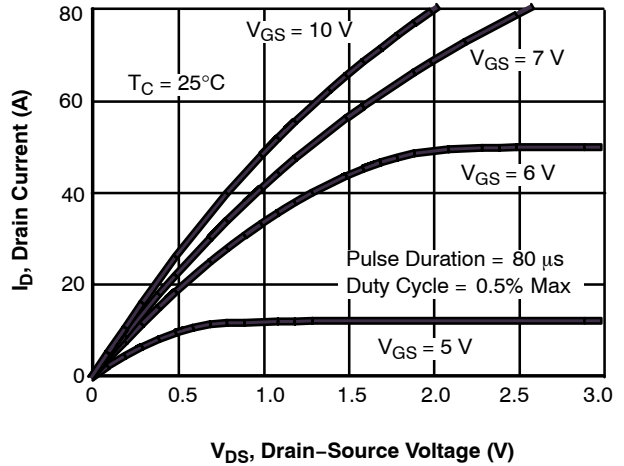


Figure 8. Saturation Characteristics

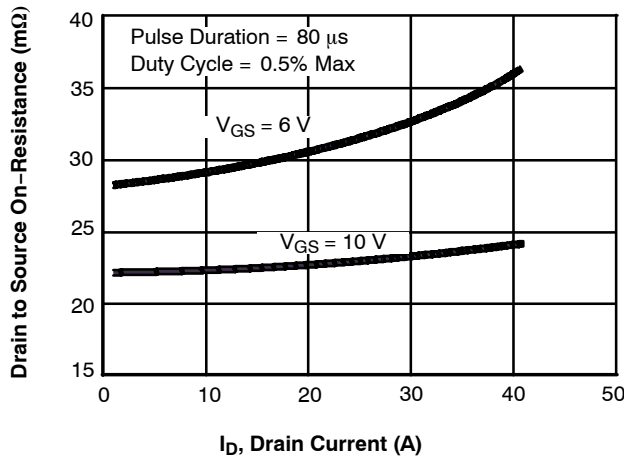


Figure 9. Drain to Source On Resistance vs. Drain Current

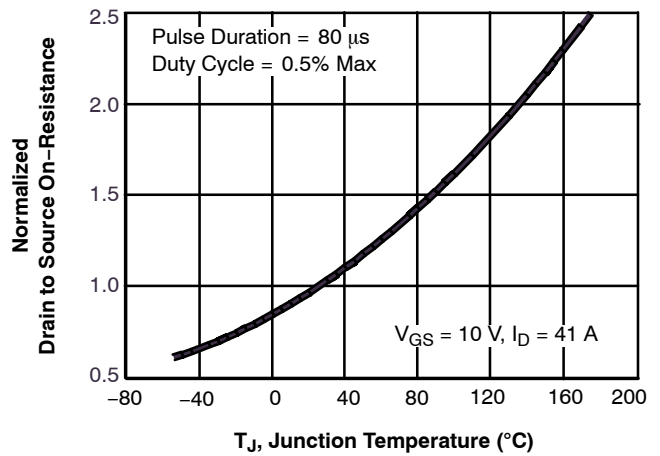


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

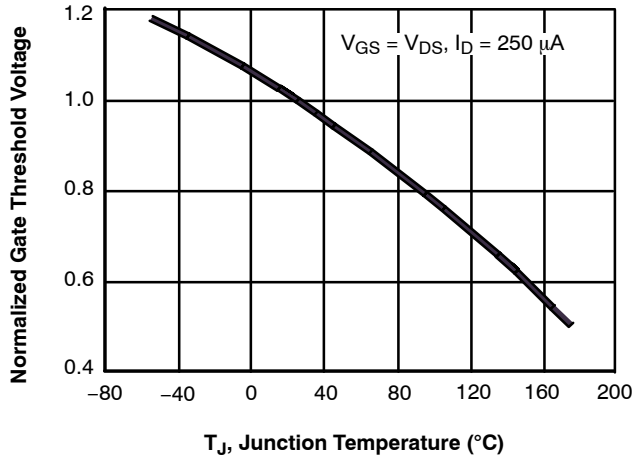


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

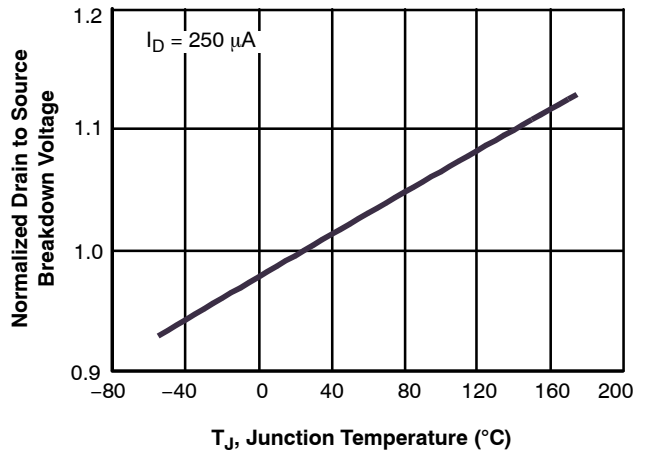


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

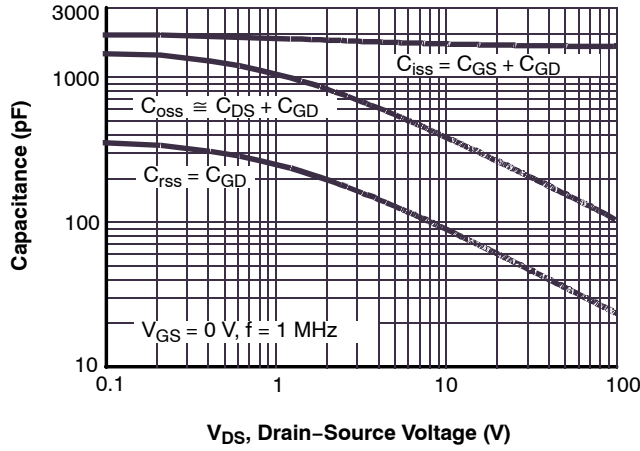


Figure 13. Capacitance vs Drain to Source Voltage

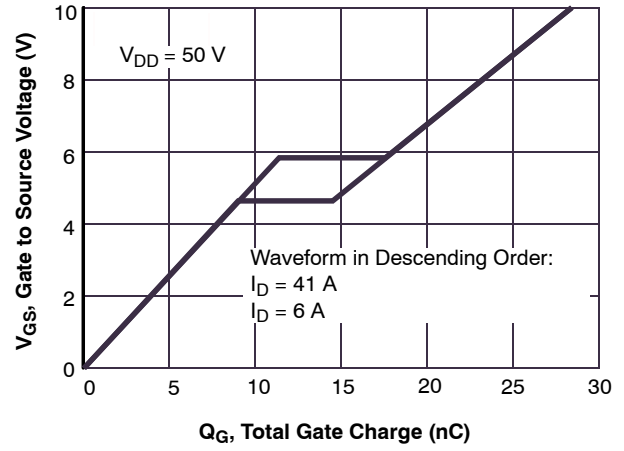


Figure 14. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

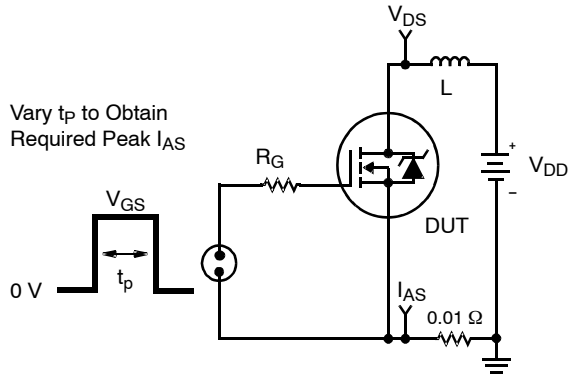


Figure 15. Unclamped Energy Test Circuit

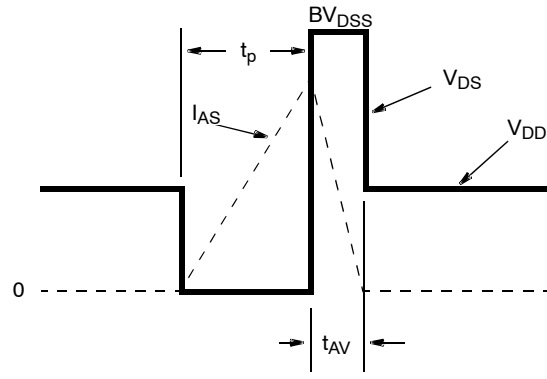


Figure 16. Unclamped Energy Waveforms

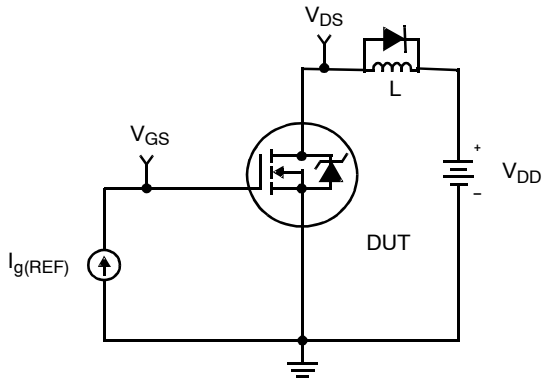


Figure 17. Gate Charge Test Circuit

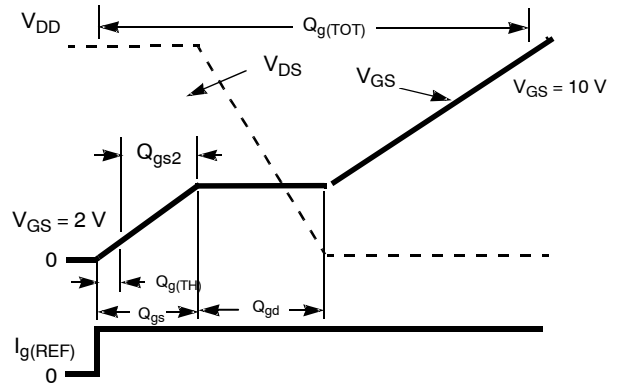


Figure 18. Gate Charge Waveforms

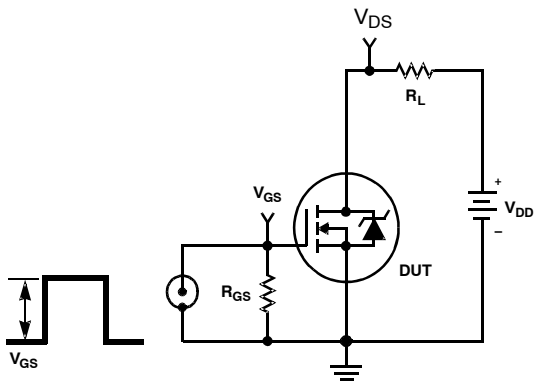


Figure 19. Switching Time Test Circuit

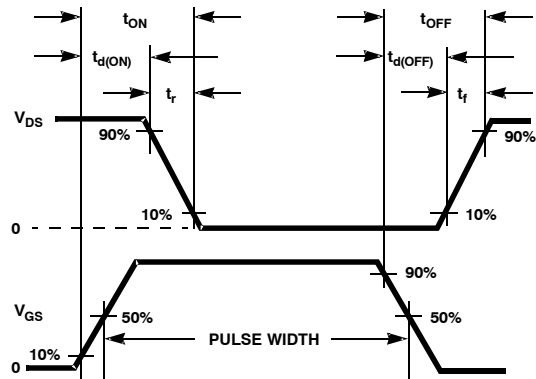


Figure 20. Switching Time Waveforms

# FDP3672

## PSPICE ELECTRICAL MODEL

.SUBCKT FDP3672 2 1 3 ; rev October 2002

Ca 12 8 5.8e-10  
Cb 15 14 6.8e-10  
Cin 6 8 1.6e-9

Dbody 7 5 DbodyMOD  
Dbreak 5 11 DbreakMOD  
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 105  
Eds 14 8 5 8 1  
Egs 13 8 6 8 1  
Esg 6 10 6 8 1  
Evthres 6 21 19 8 1  
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 9.56e-9  
Ldrain 2 5 1.0e-9  
Lsource 3 7 4.45e-9

RLgate 1 9 95.6  
RLdrain 2 5 10  
RLsource 3 7 44.5

Mmed 16 6 8 8 MmedMOD  
Mstro 16 6 8 8 MstroMOD  
MweakMOD 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
Rdrain 50 16 RdrainMOD 6.0e-3  
Rgate 9 20 1.5  
RSLC1 5 51 RSLCMOD 1.0e-6  
RSLC2 5 50 1.0e3  
Rsource 8 7 RsourceMOD 9.5e-3  
Rvthres 22 8 RvthresMOD 1  
Rvtemp 18 19 RvtempMOD 1  
S1a 6 12 13 8 S1AMOD  
S1b 13 12 13 8 S1BMOD  
S2a 6 15 14 13 S2AMOD  
S2b 13 15 14 13 S2BMOD

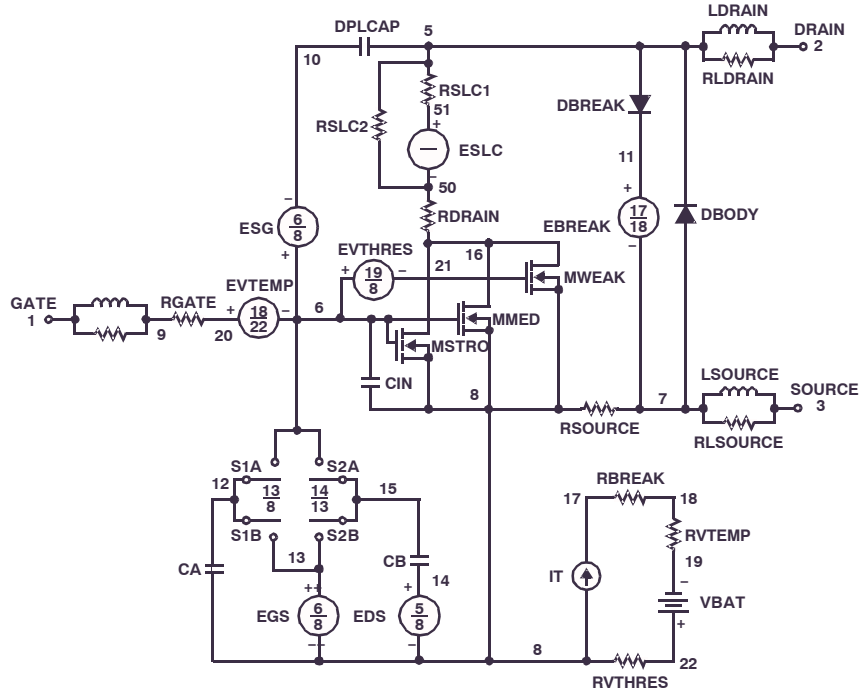
Vbat 22 19 DC 1

ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) \* (PWR(V(5,51)/(1e-6\*98),3)) }

.MODEL DbodyMOD D (IS=1.0E-11 N=1.05 RS=3.7e-3 TRS1=2.5e-3 TRS2=1.0e-6  
+ CJO=1.2e-9 M=0.58 TT=3.75e-8 XTI=4.0)  
.MODEL DbreakMOD D (RS=15 TRS1=4.0e-3 TRS2=-5.0e-6)  
.MODEL DplcapMOD D (CJO=3.8e-10 IS=1.0e-30 N=10 M=0.60)

.MODEL MmedMOD NMOS (VTO=3.6 KP=3 IS=1e-40 N=10 TOX=1 L=1u W=1u RG=1.5)  
.MODEL MstroMOD NMOS (VTO=4.3 KP=59 IS=1e-30 N=10 TOX=1 L=1u W=1u)  
..MODEL MweakMOD NMOS (VTO=3.09 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=15 RS=0.1)

.MODEL RbreakMOD RES (TC1=9.0e-4 TC2=-1.0e-7)  
.MODEL RdrainMOD RES (TC1=11.0e-3 TC2= 6.1e-5)  
.MODEL RSLCMOD RES (TC1=3.0e-3 TC2=1.0e-6)  
.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6)  
.MODEL RvthresMOD RES (TC1=-3.5e-3 TC2=-1.5e-5)  
.MODEL RvtempMOD RES (TC1=-4.3e-3 TC2=1.5e-6)



## FDP3672

```
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-3.5)  
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-5.0)  
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)  
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)
```

.ENDS

For further discussion of the PSPICE model, consult *A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options*; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



**SPICE THERMAL MODEL**

REV October 2002  
FDP3672

CTHERM1 TH 6 3.2e-3  
CTHERM2 6 5 3.3e-3  
CTHERM3 5 4 3.4e-3  
CTHERM4 4 3 3.5e-3  
CTHERM5 3 2 6.4e-3  
CTHERM6 2 TL 1.9e-2

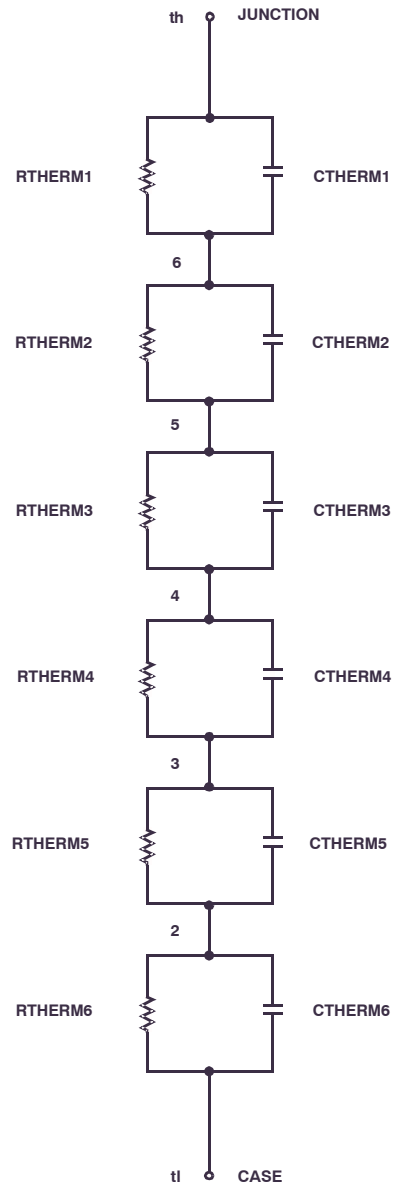
RTHERM1 TH 6 5.5e-4  
RTHERM2 6 5 5.0e-3  
RTHERM3 5 4 4.5e-2  
RTHERM4 4 3 10.5e-2  
RTHERM5 3 2 3.4e-1  
RTHERM6 2 TL 3.5e-1

**SABER THERMAL MODEL**

SABER thermal model FDP3672  
template thermal\_model th tl  
thermal\_c th, tl

```
{
cctherm.ctherm1 th 6 =3.2e-3
ctherm.ctherm2 6 5 =3.3e-3
ctherm.ctherm3 5 4 =3.4e-3
ctherm.ctherm4 4 3 =3.5e-3
ctherm.ctherm5 3 2 =6.4e-3
ctherm.ctherm6 2 tl =1.9e-2
```

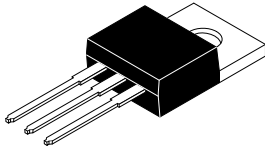
```
rtherm.rtherm1 th 6 =5.5e-4
rtherm.rtherm2 6 5 =5.0e-3
rtherm.rtherm3 5 4 =4.5e-2
rtherm.rtherm4 4 3 =10.5e-2
rtherm.rtherm5 3 2 =3.4e-1
rtherm.rtherm6 2 tl =3.5e-1
}
```



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

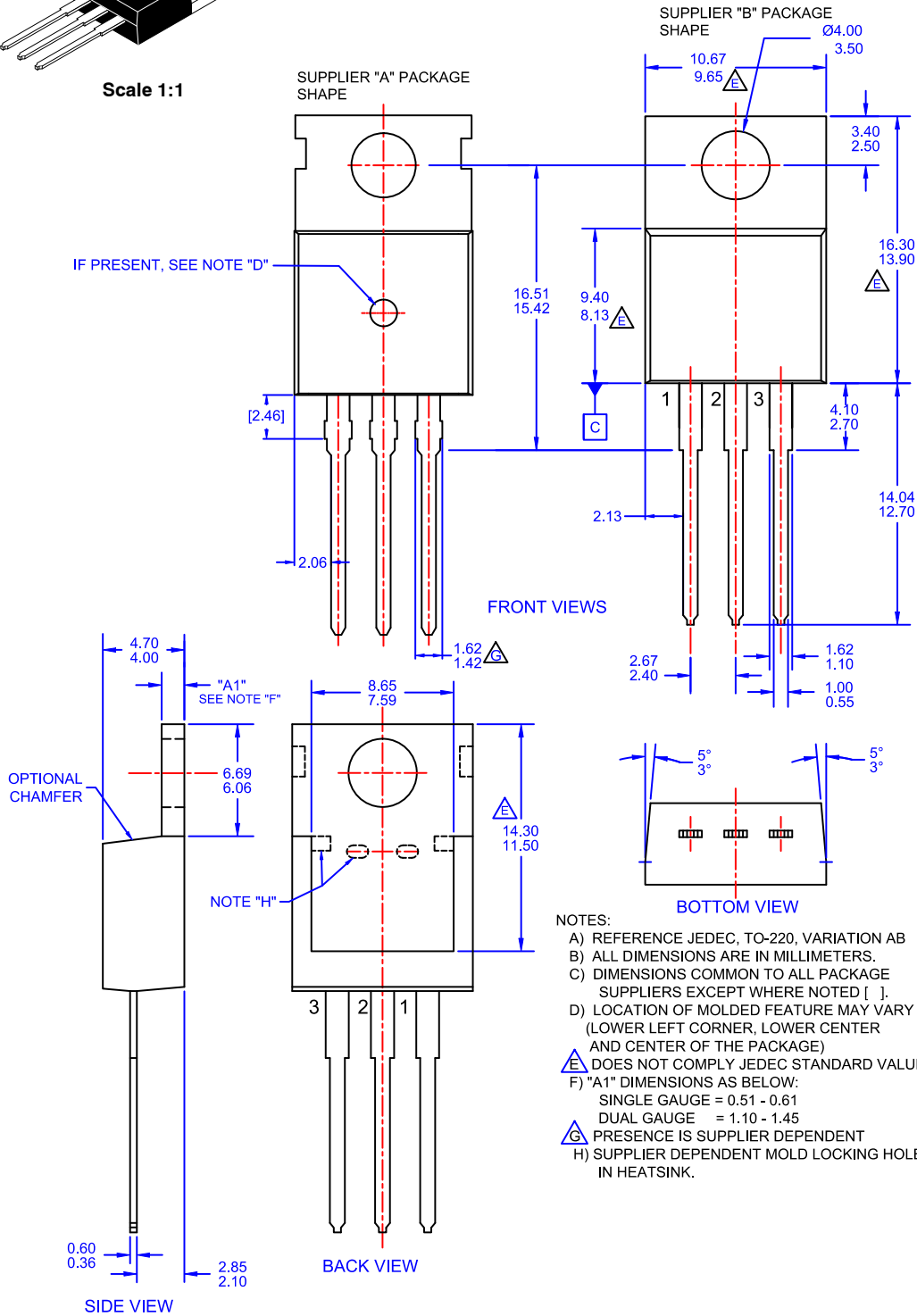
ON Semiconductor®



Scale 1:1

### TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



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