NTLJD3119C

MOSFET – Power, Complementary, WDFN 2X2 mm
20 V/-20 V, 4.6 A/-4.1 A

ON Semiconductor®

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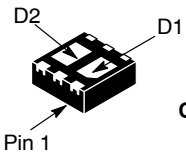
Features

- Complementary N−Channel and P−Channel MOSFET
- WDFN Package with Exposed Drain Pad for Excellent Thermal Conduction
- Footprint Same as SC−88 Package
- Leading Edge Trench Technology for Low On Resistance
- 1.8 V Gate Threshold Voltage
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb−Free Device

Applications

- Synchronous DC−DC Conversion Circuits
- Load/Power Management of Portable Devices like PDA's, Cellular Phones and Hard Drives
- Color Display and Camera Flash Regulators

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
N−Channel 20 V	65 mΩ @ 4.5 V	3.8 A
	85 mΩ @ 2.5 V	2.0 A
	120 mΩ @ 1.8 V	1.7 A
P−Channel −20 V	100 mΩ @ −4.5 V	−4.1 A
	135 mΩ @ −2.5 V	−2.0 A
	200 mΩ @ −1.8 V	−1.6 A



WDFN6
CASE 506AN

MARKING DIAGRAM

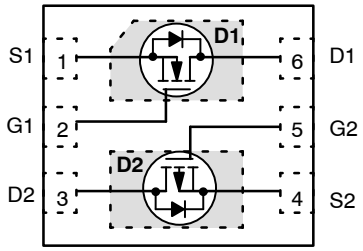
JM = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage		N−Ch	V_{DSS}	20	V
		P−Ch		−20	
Gate−to−Source Voltage		N−Ch	V_{GS}	±8.0	V
		P−Ch			
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	3.8	A
		T_A = 85°C		2.8	
	t ≤ 5 s	T_A = 25°C		4.6	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−3.3	A
		T_A = 85°C		−2.4	
	t ≤ 5 s	T_A = 25°C		−4.1	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.5	W
	t ≤ 5 s			2.3	
N−Channel Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	2.6	A
		T_A = 85°C		1.9	
P−Channel Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−2.3	A
		T_A = 85°C		−1.6	
Power Dissipation (Note 2)	Steady State	T_A = 25°C	P_D	0.71	W
Pulsed Drain Current	N−Ch	t_p = 10 μs	I_{DM}	18	A
	P−Ch			−20	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJD3119CTAG	WDFN6 (Pb−Free)	3000/Tape & Reel
NTLJD3119CTBG	WDFN6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm^2, 2 oz Cu.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
SINGLE OPERATION (SELF−HEATED)			
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction−to−Ambient − Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	54	
DUAL OPERATION (EQUALLY HEATED)			
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction−to−Ambient − Steady State Min Pad (Note 4)	$R_{\theta JA}$	133	
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm^2, 2 oz Cu).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = −250 μA	−20			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N				10.4		mV/°C
		P				9.95		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25 °C			1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −16 V				−1.0	
		N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 85 °C			10	
		P	V_{GS} = 0 V, V_{DS} = −16 V				−10	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
		P	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.4	0.7	1.0	V
		P		I_D = −250 μA	−0.4	−0.7	−1.0	
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	N				−3.0		mV/°C
		P				2.44		
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V , I_D = 3.8 A			37	65	mΩ
		P	V_{GS} = −4.5 V , I_D = −4.1 A			75	100	
		N	V_{GS} = 2.5 V , I_D = 2.0 A			46	85	
		P	V_{GS} = −2.5 V, I_D = −2.0 A			101	135	
		N	V_{GS} = 1.8 V , I_D = 1.7 A			65	120	
		P	V_{GS} = −1.8 V, I_D = −1.6 A			150	200	
Forward Transconductance	g_{FS}	N	V_{DS} = 10 V, I_D = 1.7 A			4.2		S
		P	V_{DS} = −5.0 V , I_D = −2.0 A			3.1		
CHARGES, CAPACITANCES AND GATE RESISTANCE								
Input Capacitance	C_{ISS}	N	f = 1.0 MHz, V_{GS} = 0 V	V_{DS} = 10 V		271		pF
		P		V_{DS} = −10 V		531		
Output Capacitance	C_{OSS}	N		V_{DS} = 10 V		72		
		P		V_{DS} = −10 V		91		
Reverse Transfer Capacitance	C_{RSS}	N		V_{DS} = 10 V		43		
		P		V_{DS} = −10 V		56		
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			3.7		nC
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −2.0 A			5.5		
Threshold Gate Charge	$Q_{G(TH)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			0.3		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −2.0 A			0.7		
Gate−to−Source Charge	Q_{GS}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			0.6		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −2.0 A			1.0		
Gate−to−Drain Charge	Q_{GD}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.8 A			1.0		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −2.0 A			1.4		

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 16 V, I_D = 1.0 A, R_G = 2.0 Ω			3.8		ns
Rise Time	t_r					4.7		
Turn−Off Delay Time	$t_{d(OFF)}$					11.1		
Fall Time	t_f					5.8		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −2.0 A, R_G = 2.0 Ω			5.2		
Rise Time	t_r					13.2		
Turn−Off Delay Time	$t_{d(OFF)}$					13.7		
Fall Time	t_f					19.1		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25 °C	I_S = 1.0 A		0.69	1.0	V
		P		I_S = −1.0 A		−0.75	−1.0	
		N	V_{GS} = 0 V, T_J = 125 °C	I_S = 1.0 A		0.52		
		P		I_S = −1.0 A		−0.64		
Reverse Recovery Time	t_{RR}	N	V_{GS} = 0 V, dI_S / dt = 100 A/μs	I_S = 1.0 A		10.2		ns
		P		I_S = −1.0 A		16.2		
Charge Time	t_a	N		I_S = 1.0 A		6.0		
		P		I_S = −1.0 A		10.6		
Discharge Time	t_b	N		I_S = 1.0 A		4.2		
		P		I_S = −1.0 A		5.6		
Reverse Recovery Charge	Q_{RR}	N		I_S = 1.0 A		3.0		nC
		P		I_S = −1.0 A		5.7		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES – N–CHANNEL (T_J = 25°C unless otherwise noted)

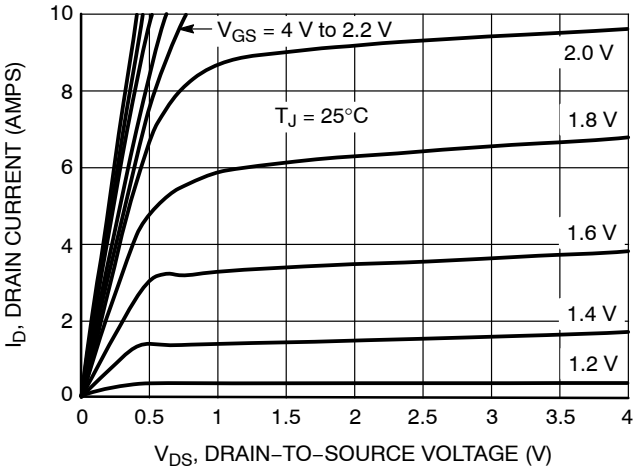


Figure 1. On–Region Characteristics

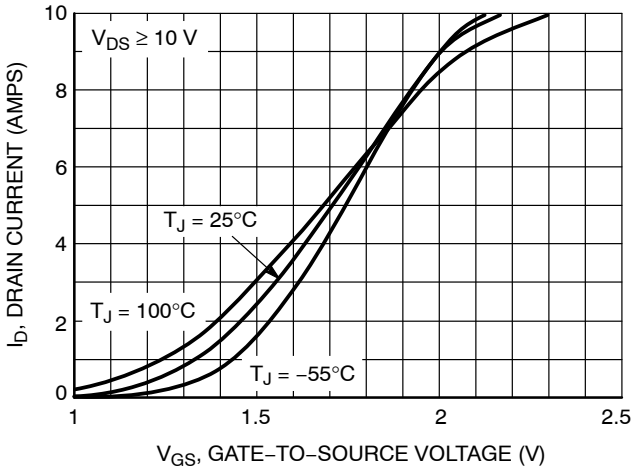


Figure 2. Transfer Characteristics

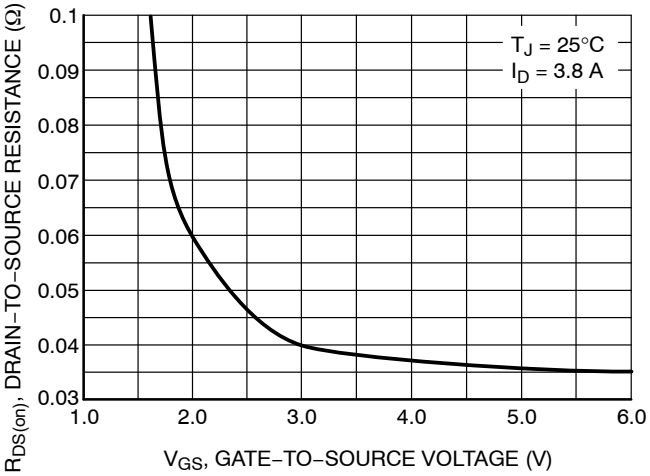


Figure 3. On–Resistance versus Drain Current

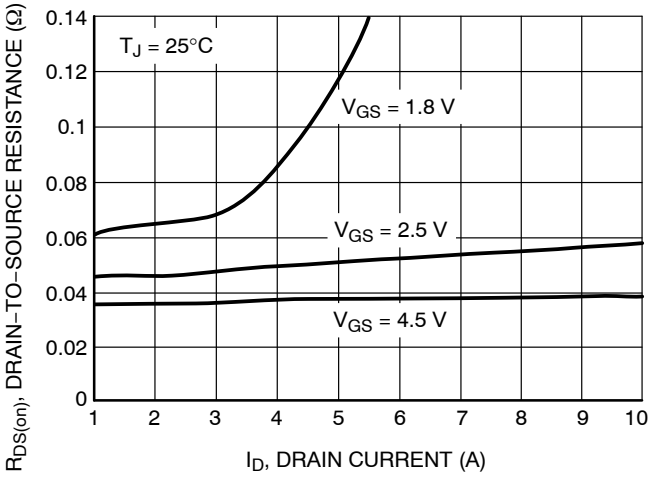


Figure 4. On–Resistance versus Drain Current and Gate Voltage

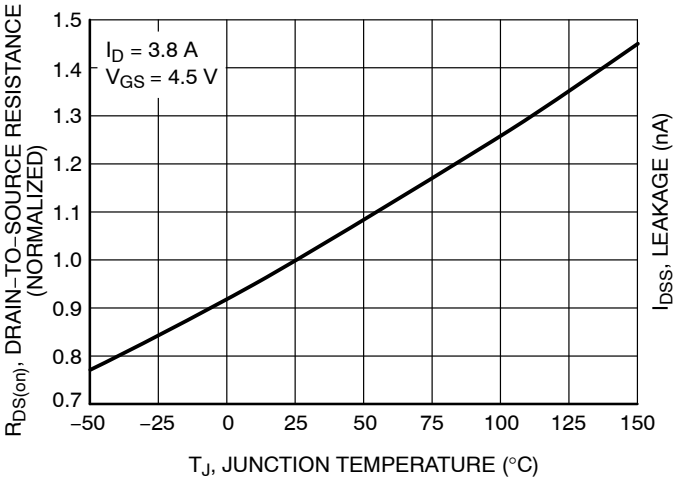


Figure 5. On–Resistance Variation with Temperature

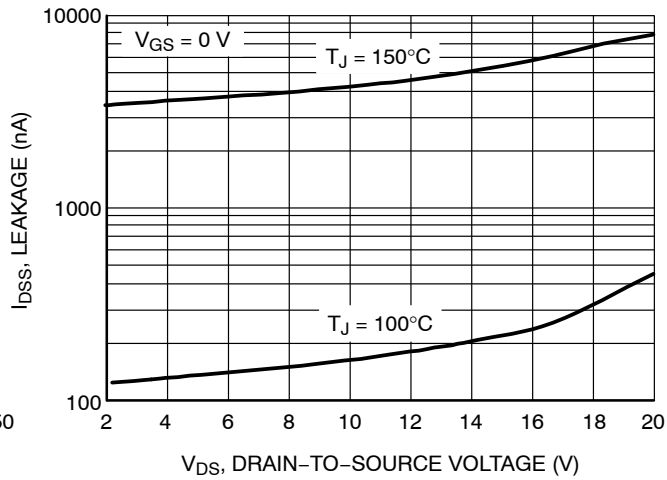


Figure 6. Drain–to–Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES – N–CHANNEL (T_J = 25°C unless otherwise noted)

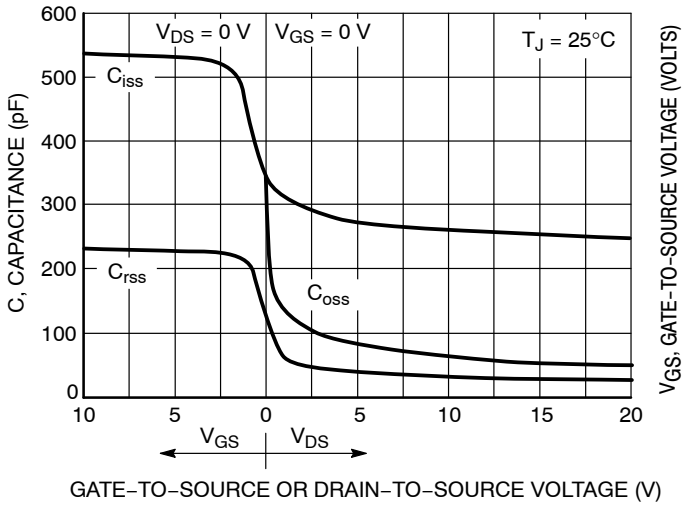


Figure 7. Capacitance Variation

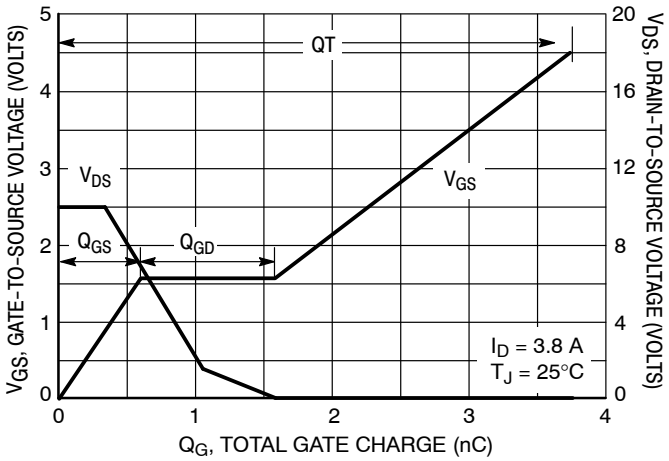


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

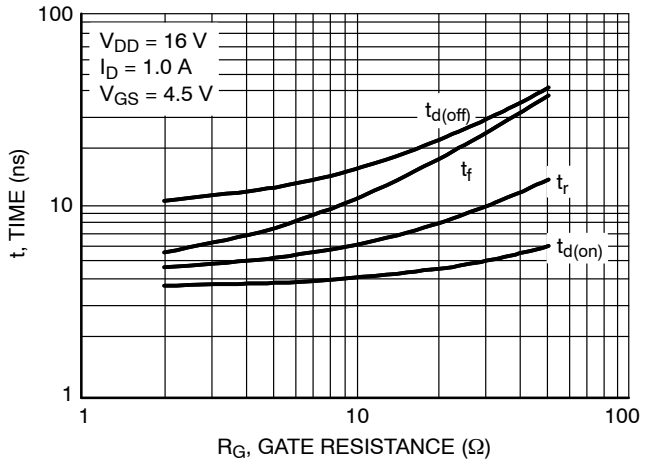


Figure 9. Resistive Switching Time Variation versus Gate Resistance

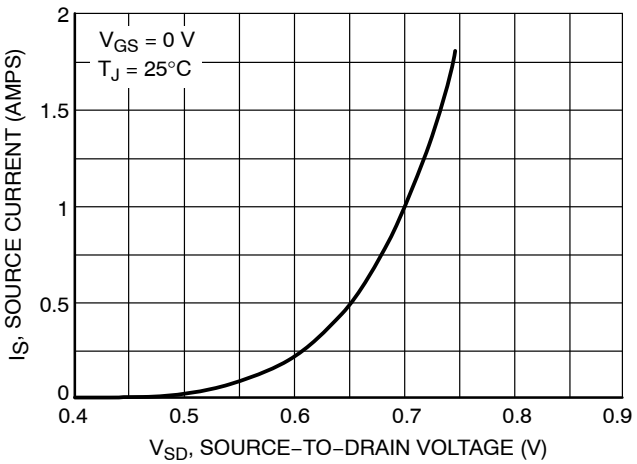


Figure 10. Diode Forward Voltage versus Current

TYPICAL PERFORMANCE CURVES – P–CHANNEL (T_J = 25°C unless otherwise noted)

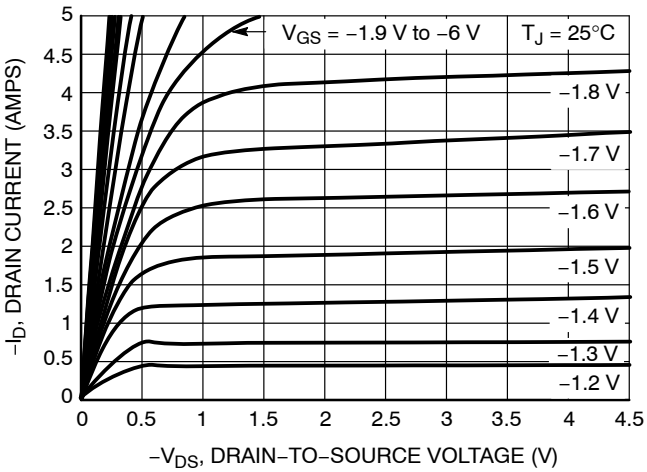


Figure 11. On–Region Characteristics

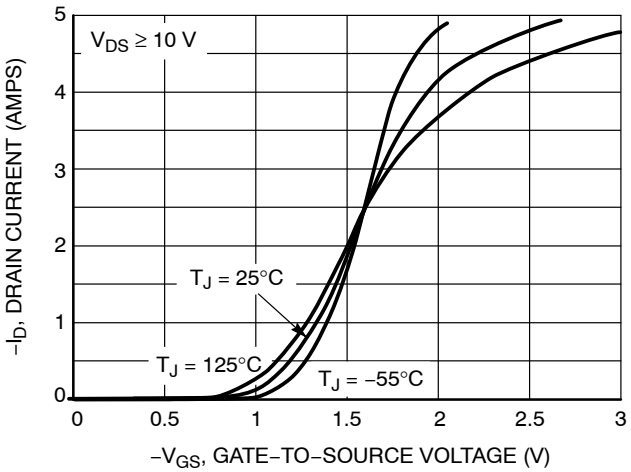


Figure 12. Transfer Characteristics

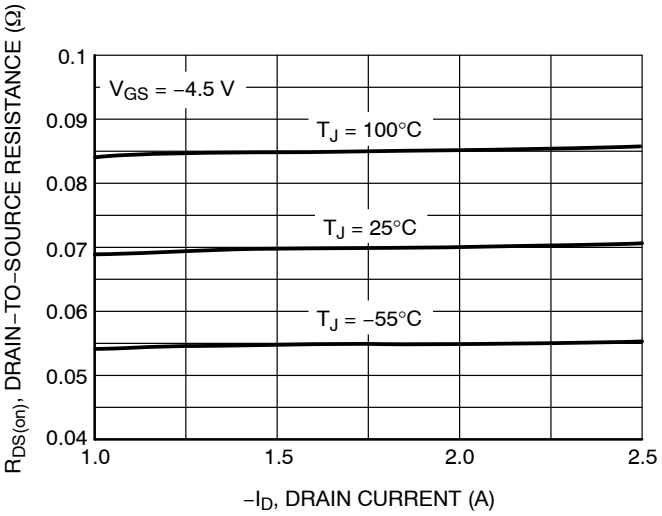


Figure 13. On–Resistance versus Drain Current

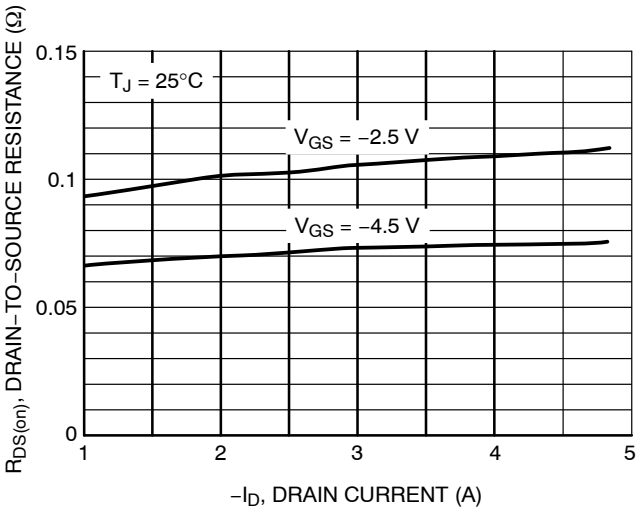


Figure 14. On–Resistance versus Drain Current and Gate Voltage

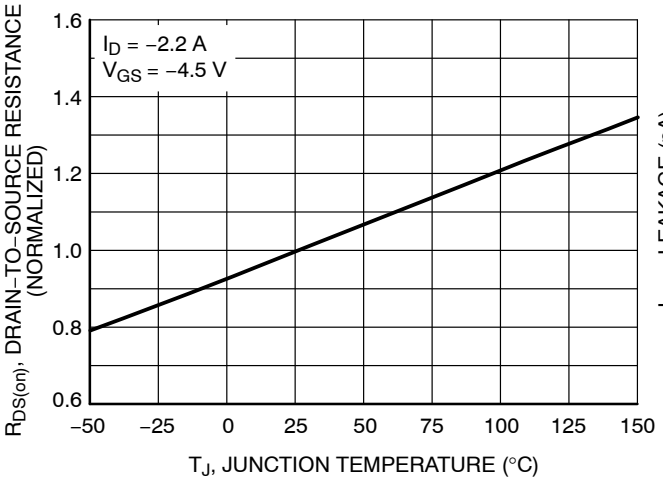


Figure 15. On–Resistance Variation with Temperature

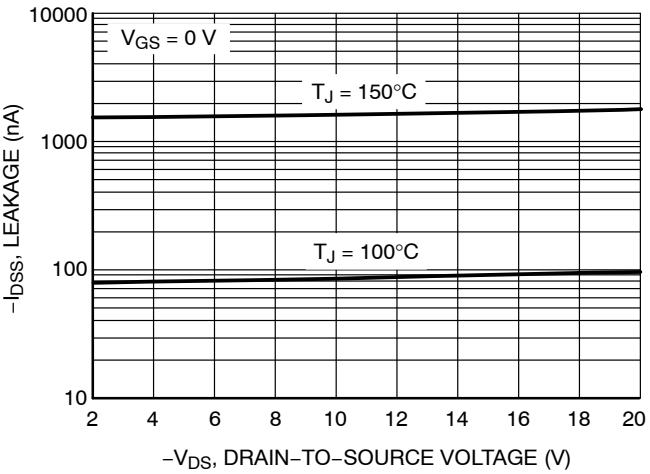


Figure 16. Drain–to–Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES – P–CHANNEL (T_J = 25°C unless otherwise noted)

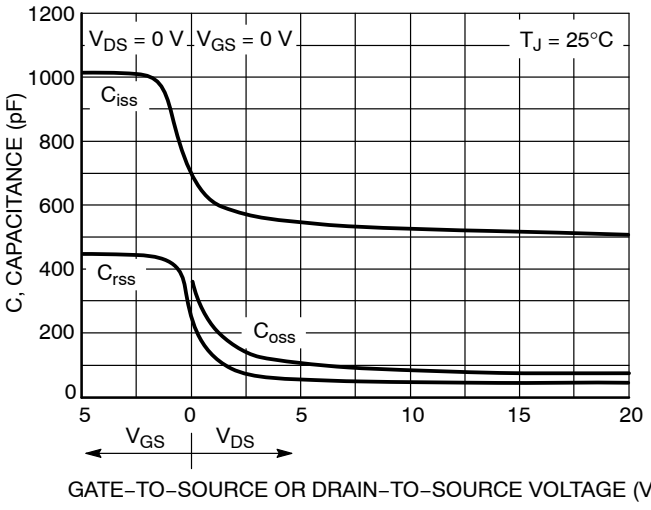


Figure 17. Capacitance Variation

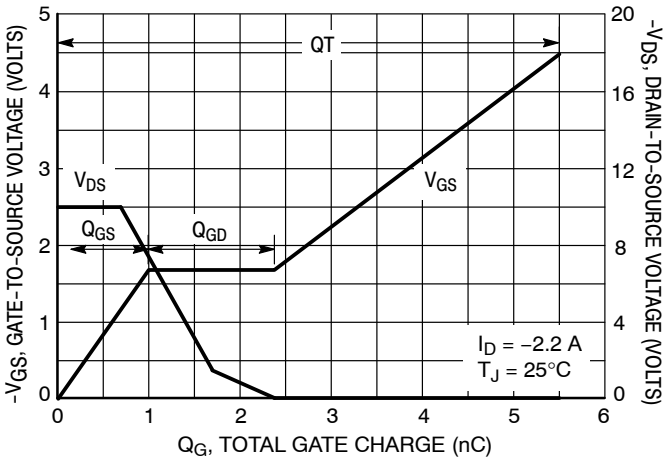


Figure 18. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

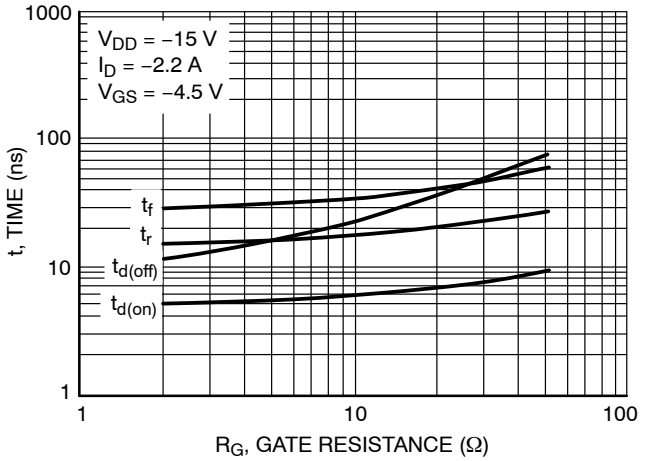


Figure 19. Resistive Switching Time Variation versus Gate Resistance

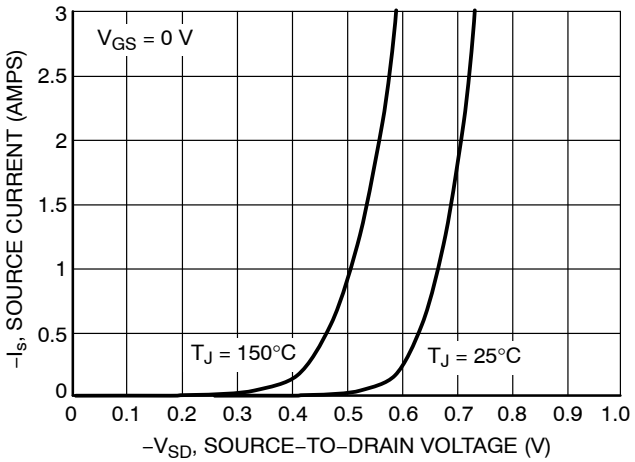


Figure 20. Diode Forward Voltage versus Current

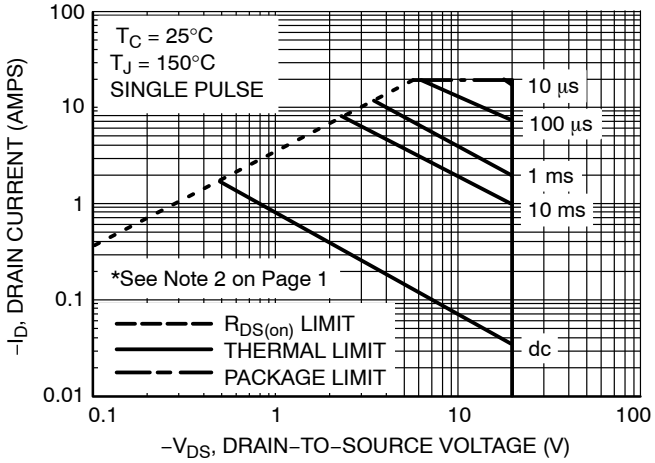


Figure 21. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

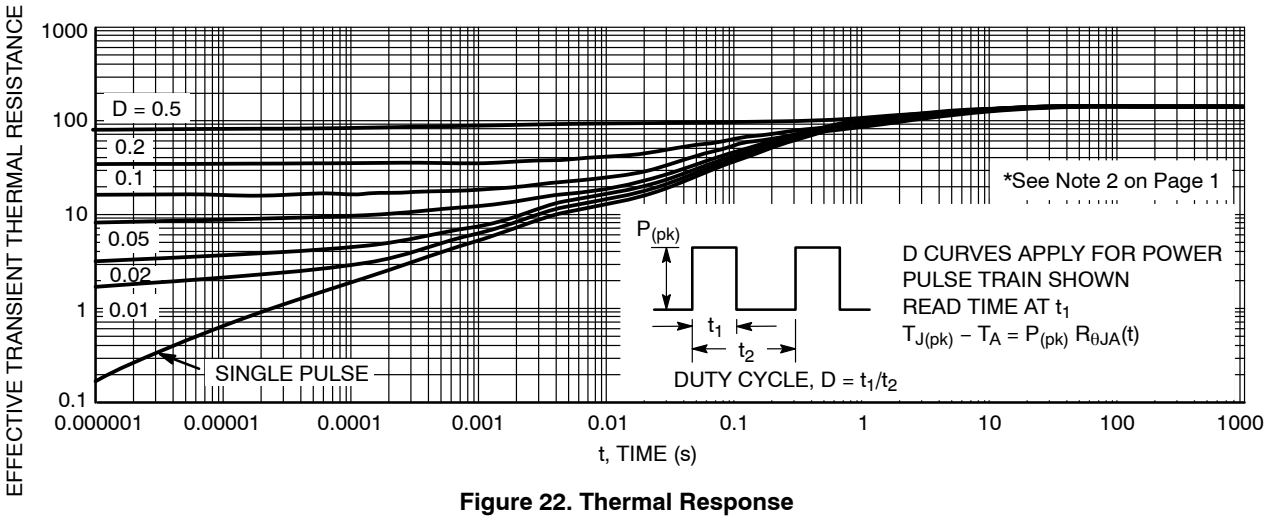
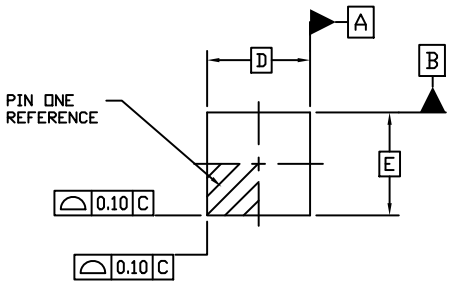


Figure 22. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P
CASE 506AN
ISSUE H

DATE 25 JAN 2022

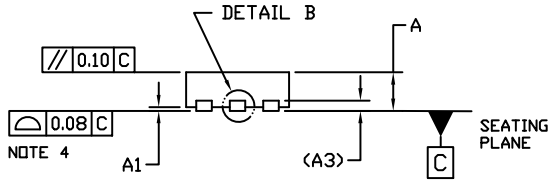


TOP VIEW

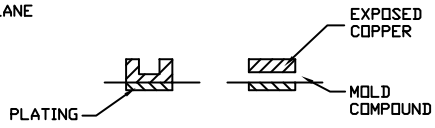
DETAIL A
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

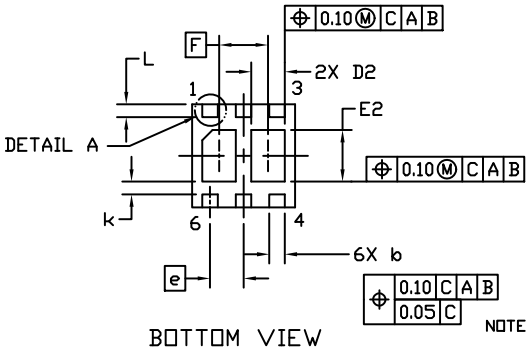


SIDE VIEW

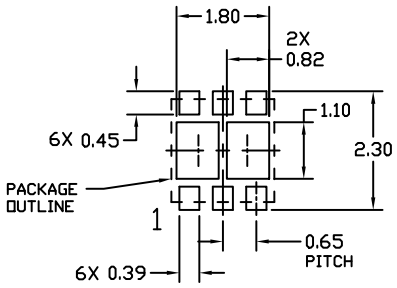


DETAIL B
OPTIONAL CONSTRUCTIONS

DIM	MILLIMETERS	
	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
k	0.25 REF	
L	0.20	0.30
L1	---	0.10



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT
SOLDERMASK DEFINED

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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