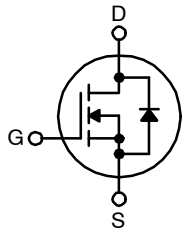
MOSFET – N-Channel, UniFET™

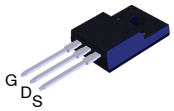
250 V, 33 A, 94 mΩ

FDPF33N25T

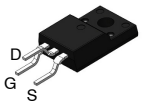
V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
250 V	94 mΩ @ 10 V	33 A



N−Channel MOSFET



TO−220 Fullpack, 3−Lead / TO−220F−3SG CASE 221AT



TO−220−3LD LF (LG−formed) CASE 340BL

Description

UniFET MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

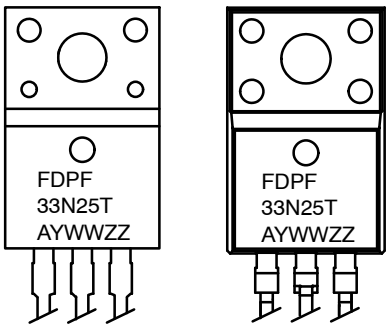
Features

- $R_{DS(on)}$ = 94 mΩ (Max.) @ V_{GS} = 10 V, I_D = 16.5 A
- Low Gate Charge (Typ. 36.8 nC)
- Low C_{rss} (Typ. 39 pF)
- 100% Avalanche Tested

Applications

- PDP TV
- Lighting
- Uninterruptible Power Supply
- AC−DC Power Supply

MARKING DIAGRAM



FDPF33N25T	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDPF33N25T FDPF33N25TRDTU	Unit
V_{DSS}	Drain−Source Voltage		250	V
I_D	Drain Current	− Continuous (T_C = 25°C) − Continuous (T_C = 100°C)	33* 20.4*	A A
I_{DM}	Drain Current	− Pulsed (Note 1)	132*	A
V_{GSS}	Gate−Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		918	mJ
I_{AR}	Avalanche Current (Note 1)		33	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		23.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C) − Derate Above 25°C	37 0.29	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 1.35 mH, I_{AS} = 33 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 33 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDPF33N25T FDPF33N25TRDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_J = 25°C	250	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.25	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 250 V, V_{GS} = 0 V V_{DS} = 200 V, T_C = 125°C	– –	– –	1 10	μA μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 16.5 A	–	0.077	0.094	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 16.5 A	–	26.6	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	1640	2135	pF
C_{oss}	Output Capacitance		–	330	430	pF
C_{rss}	Reverse Transfer Capacitance		–	39	59	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 125 V, I_D = 33 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	–	35	80	ns
t_r	Turn−On Rise Time		–	230	470	ns
$t_{d(off)}$	Turn−Off Delay Time		–	75	160	ns
t_f	Turn−Off Fall Time		–	120	250	ns
Q_g	Total Gate Charge	V_{DS} = 200 V, I_D = 33 A, V_{GS} = 10 V (Note 4)	–	36.8	48	nC
Q_{gs}	Gate−Source Charge		–	10	–	nC
Q_{gd}	Gate−Drain Charge		–	17	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	33	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	132	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 33 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 33 A, dI_F/dt = 100 A/μs	–	220	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.71	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping
FDPF33N25T	FDPF33N25T	TO−220 Fullpack, 3−Lead / TO−220F−3SG CASE 221AT	1000 Units / Tube
FDPF33N25TRDTU	FDPF33N25T	TO−220−3LD LF (LG−formed) CASE 340BL	800 Units / Tube

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TYPICAL PERFORMANCE CHARACTERISTICS

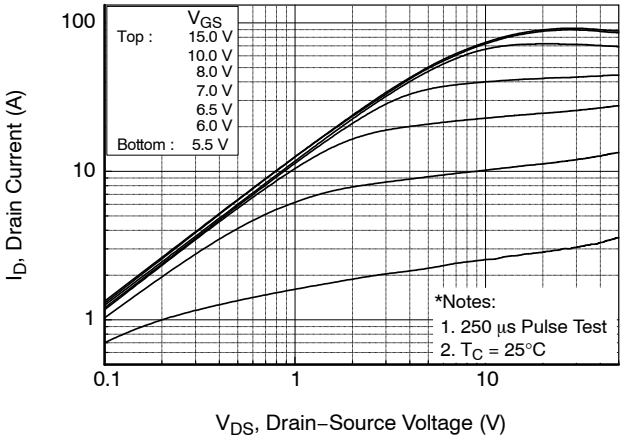


Figure 1. On−Region Characteristics

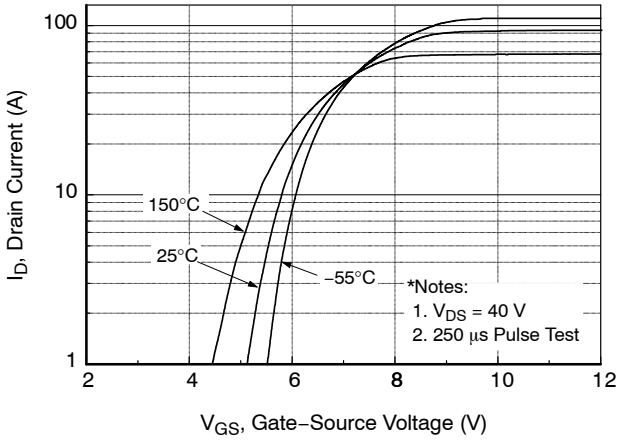


Figure 2. Transfer Characteristics

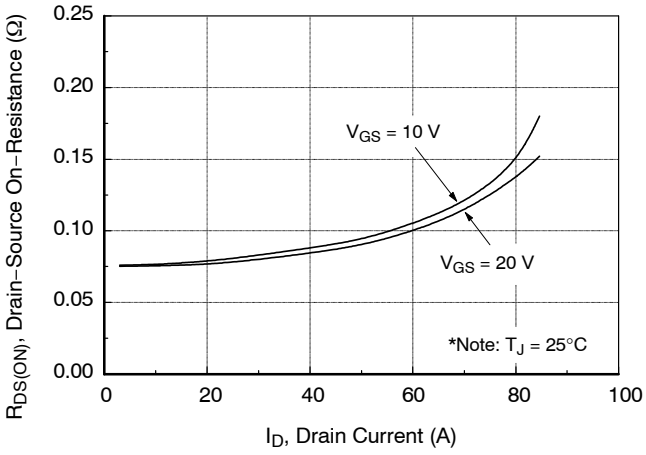


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

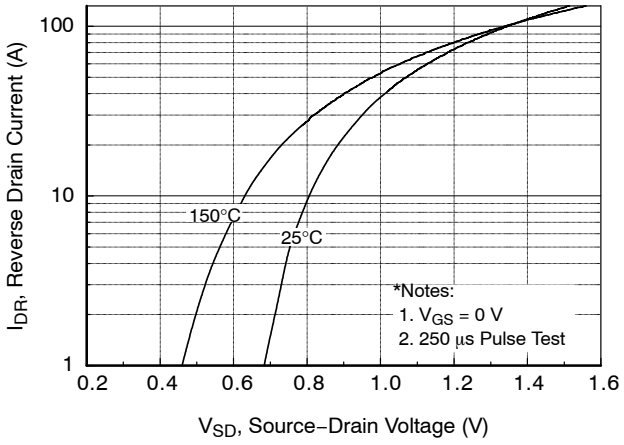


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

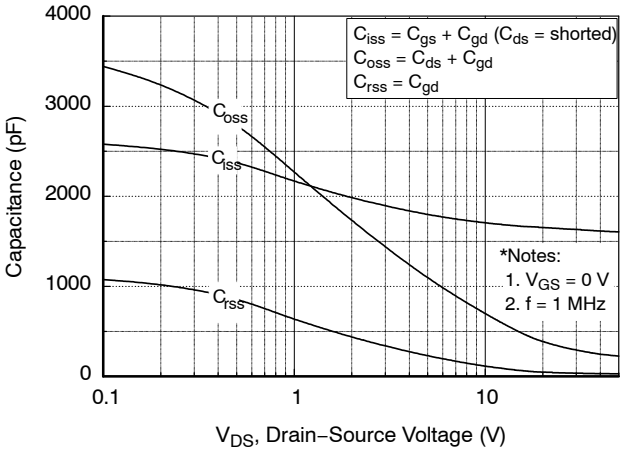


Figure 5. Capacitance Characteristics

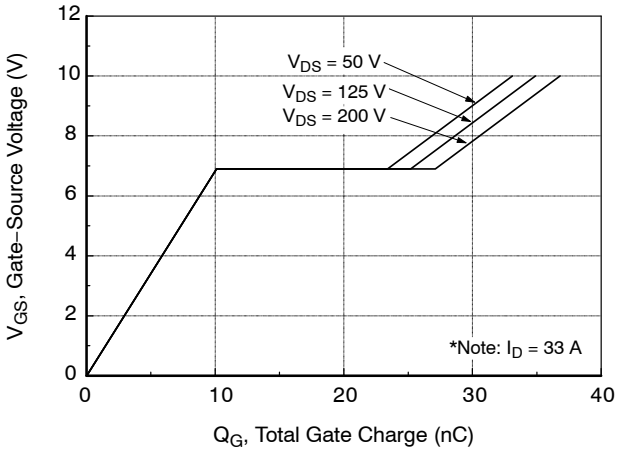


Figure 6. Gate Charge Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

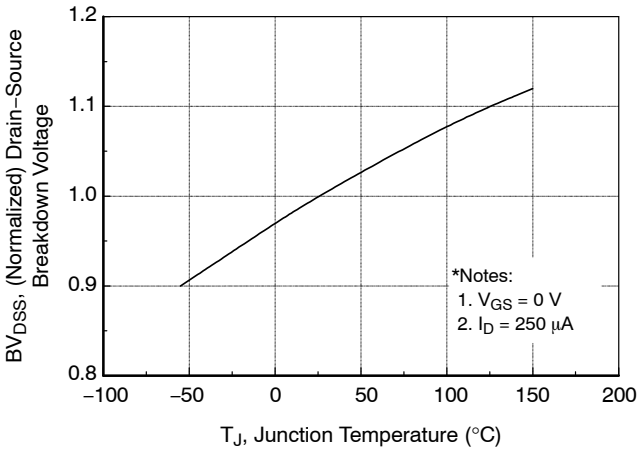


Figure 7. Breakdown Voltage Variation vs. Temperature

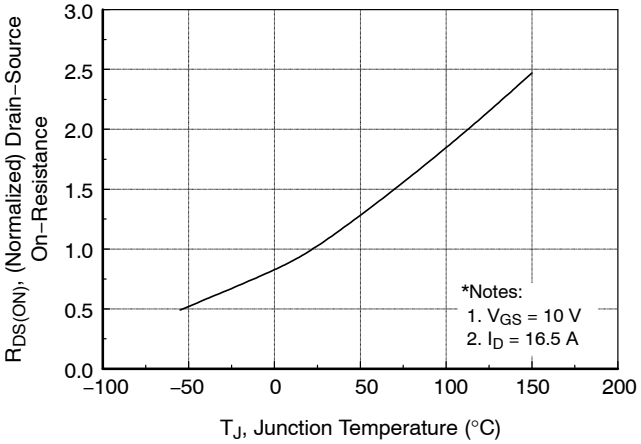


Figure 8. On−Resistance Variation vs. Temperature

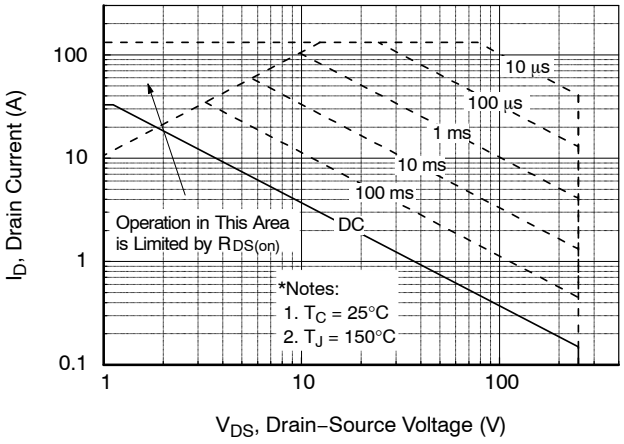


Figure 9. Maximum Safe Operating Area

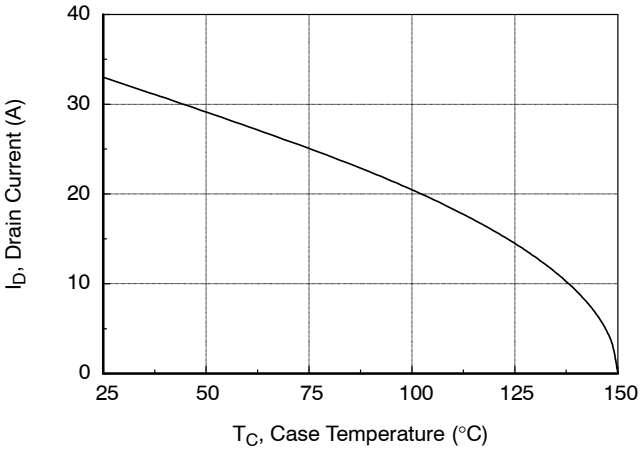


Figure 10. Maximum Drain Current vs. Case Temperature

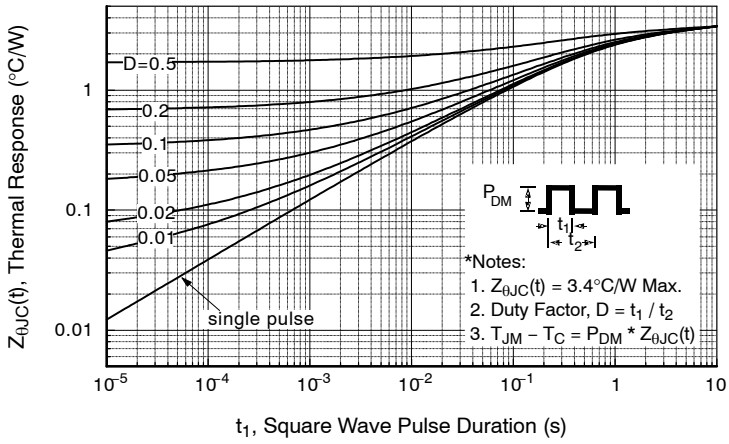


Figure 11. Transient Thermal Response Curve

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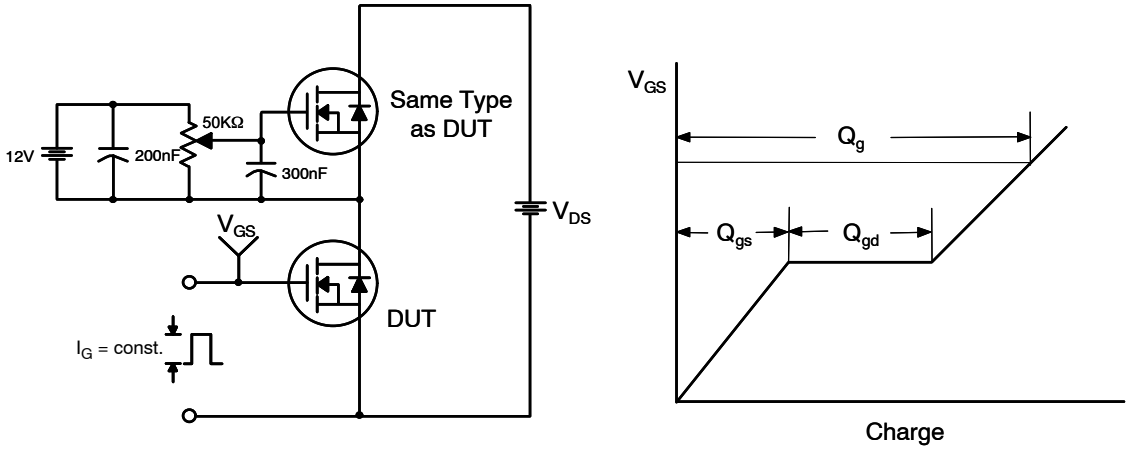


Figure 12. Gate Charge Test Circuit & Waveform

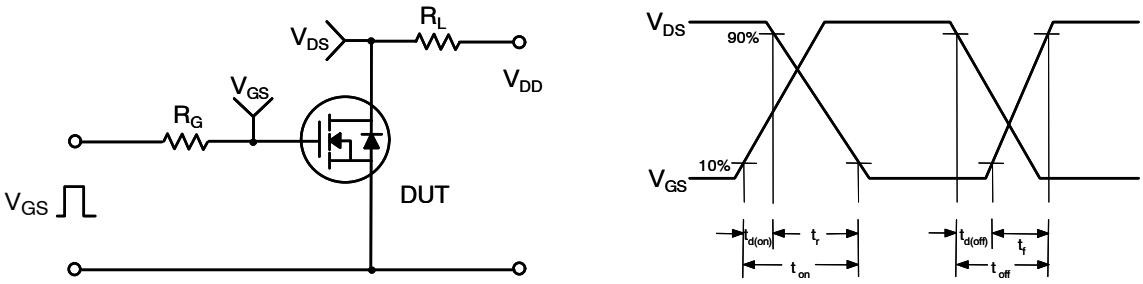


Figure 13. Resistive Switching Test Circuit & Waveforms

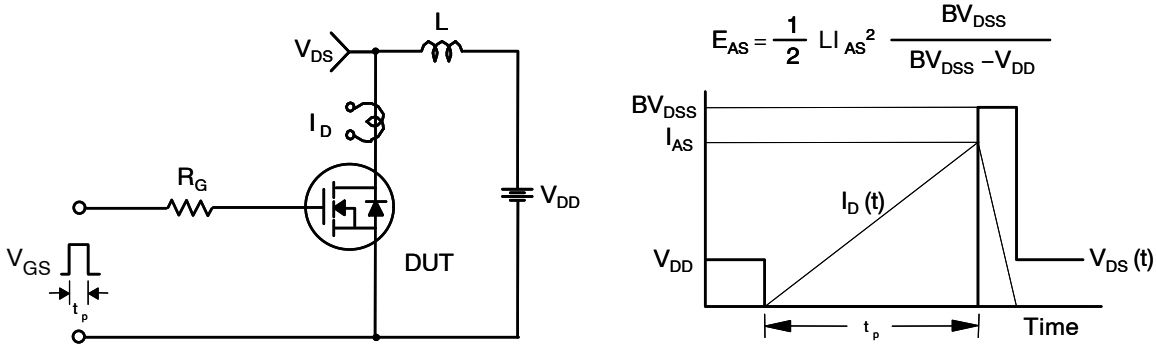


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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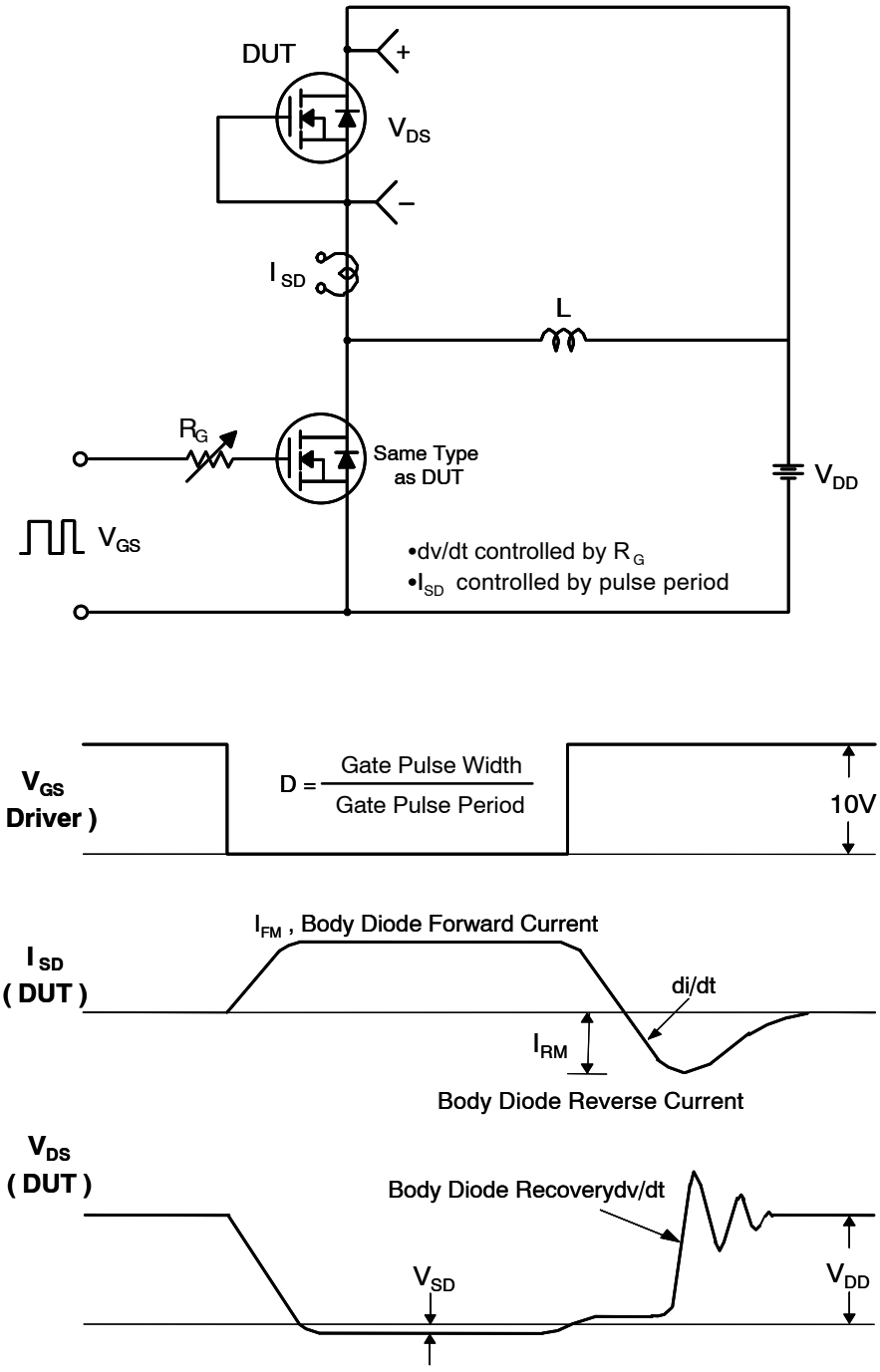


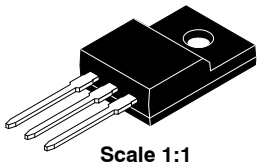
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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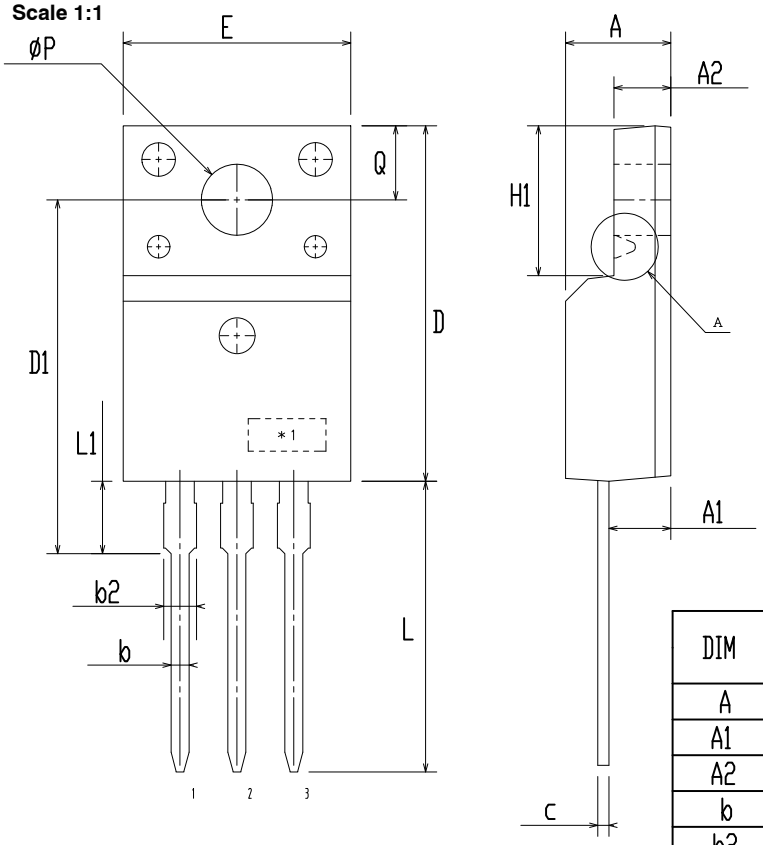
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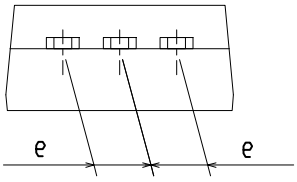
TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE B

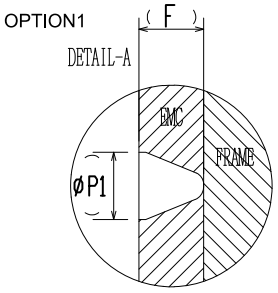
DATE 19 JAN 2021



Scale 1:1







DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
ø P	2.98	3.18	3.38
ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

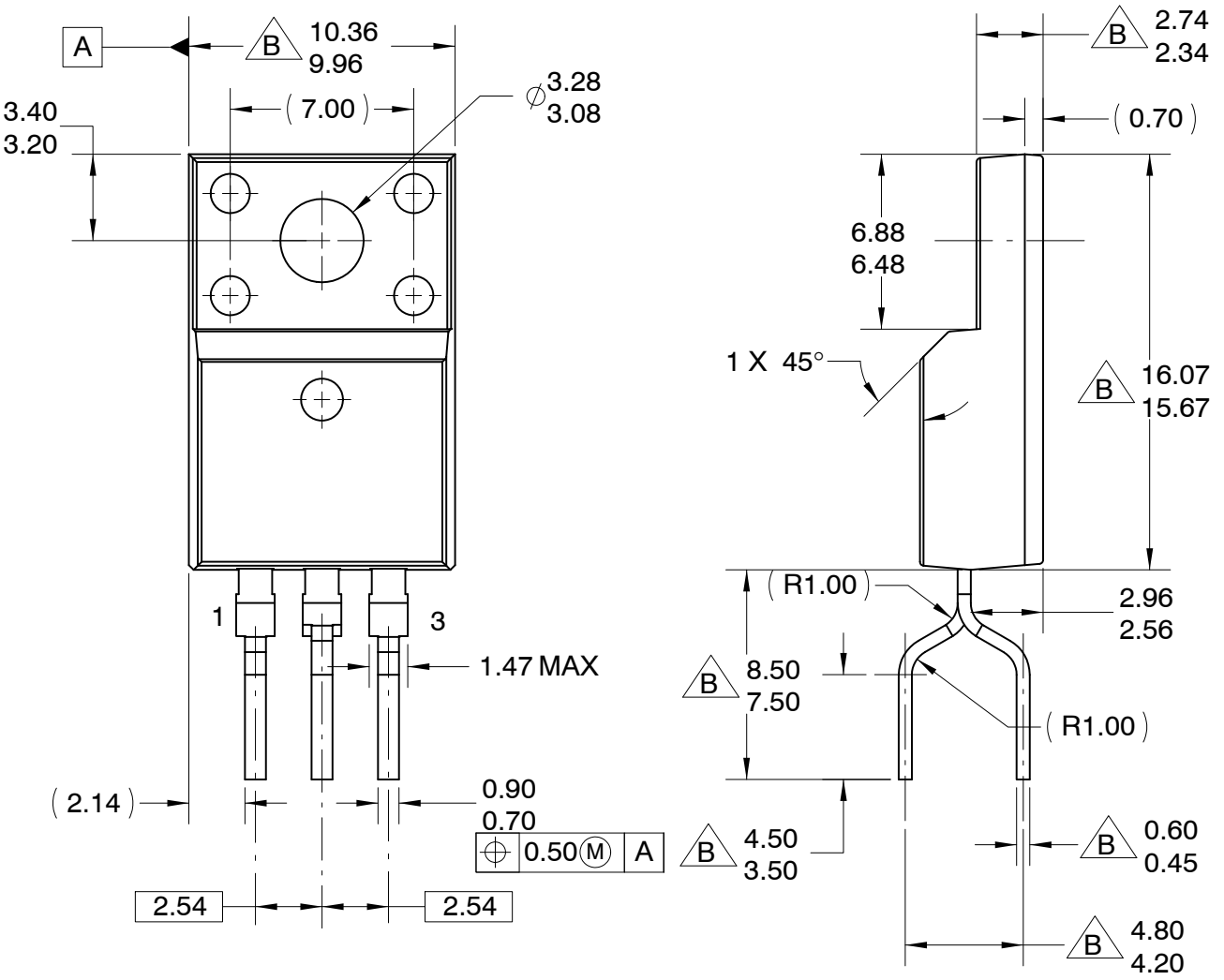
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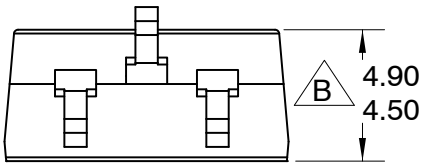
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NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
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C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5−1994.

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