RX140 Group

Renesas MCUs

R01DS0379EJ0120
Rev.1.20
Nov 22, 2024

48-MHz, 32-bit RX MCUs, on-chip FPU, 204 Coremark, up to 256-KB flash memory, up to 36 pins capacitive touch sensing unit, up to 9 comms channels, 12-bit A/D, D/A, RTC, IEC60730 compliance, 1.8-V to 5.5-V single supply, Encryption functions (optional)

Features

■ 32-bit RXv2 CPU core

- Maximum operating frequency: 48 MHz
  Capable of 204 Coremark in operation at 48 MHz
- Enhanced DSP instructions: 32-bit multiply-accumulate instructions, and 16-bit multiply-subtract instructions are supported.
- On-chip FPU: 32-bit single-precision floating point compliant with IEEE-754
- On-chip divider that operated at the fastest of two clock cycles
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit

■ Low power design and architecture

- Operation from a single 1.8-V to 5.5-V supply
- Four low power consumption modes
- Low power timer (LPT) that operates during the software standby state
- Supply current
  High-speed operating mode: 58 µA/MHz
  Supply current in software standby mode: 0.25 µA (typ.) (T_a = 25°C)
- Recovery time from software standby mode: 6.2 µs (typ.) (Clock Source: HOCO 32 MHz, T_a = 25°C)

■ On-chip flash memory for code

- 64 K/128 K/256 Kbytes size capacities
- User code is programmable by on-board programming.
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory

- 4K/8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states

- 16 K/32 K/64 Kbytes size capacities

■ DTC

- Five transfer modes

■ ELC

- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

■ Reset and supply management

- Seven types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- External clock input frequency: Up to 20 MHz
- Main clock oscillator frequency: 1 to 20 MHz
- Sub clock oscillator frequency: 32.768 kHz
- PLL circuit input: 4 MHz to 12 MHz
- Low-speed on-chip oscillator: 4 MHz
- High-speed on-chip oscillator: 24/32/48 MHz ± 1%
- IWDT-dedicated on-chip oscillator: 15 kHz
- Generate a 32.768 kHz clock for the real-time clock
- On-chip clock frequency accuracy measurement circuit (CAC)

■ Realtime clock

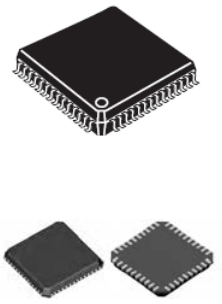
- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable

■ Independent watchdog timer

- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance

- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.



PLQP0080KB-B 12 × 12mm, 0.5mm pitch
PLQP0064GA-A 14 × 14mm, 0.8mm pitch
PLQP0064KB-C 10 × 10mm, 0.5mm pitch
PLQP0048KB-B 7 × 7mm, 0.5mm pitch
PLQP0032GB-A 7 × 7mm, 0.8mm pitch

PWQN0048KC-A 7 × 7mm, 0.5mm pitch
PWQN0032KE-A 5 × 5mm, 0.5mm pitch

■ MPC

- Input/output functions selectable from multiple pins

■ Up to 9 communication functions

- One channel of CAN module compliant with ISO11898-1: Transfer at up to 1 Mbps
- SCI with many useful functions (up to 6 channels)
  Asynchronous mode (Fine adjustable baud rate: 0 to 255/255), clock synchronous mode, smart card interface mode
- I^2C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI (one channel): Transfer at up to 16 Mbps

■ Up to 12 extended-function timers

- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (two channels)

■ 12-bit A/D converter

- Capable of conversion within 0.67 µs
- 17 (external pin input) +1 (internal input) channels
- Sampling time can be set for each channel
- Conversion results compare features
- Self-diagnostic function and analog input disconnection detection assistance function
- Double trigger (data duplication) function for motor control

■ D/A converter

- Two channels

■ Capacitive touch sensing unit

- Self-capacitance method: A single pin configures a single key, supporting up to 36 keys
- Mutual capacitance method: Matrix configuration with 8 × 8, supporting up to 64 keys

■ Comparator B

- Two channels

■ General I/O ports

- 5-V tolerant, open drain, input pull-up

■ Encryption functions (optional)

- AES (key lengths: 128 and 256 bits)
- RNG (True random number generator)

■ Temperature sensor

■ Unique ID

- 32-byte ID code for the MCU

■ Operating temperature range

- –40 to +85°C
- –40 to +105°C

■ Applications

- General industrial and consumer equipment

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1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages in the RX140 Group.

Table 1.1 Outline of Specifications (1/4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 48 MHz • 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 (variable-length instruction format) • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 64 K/128 K/256 Kbytes • 32 MHz ≤: No-wait cycle access • 32 MHz to 48 MHz: One-wait cycle access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 16 K/32 K/64 Kbytes • No-wait memory access
	E2 DataFlash	• Capacity: 4 K/8 Kbytes • Number of erase/write cycles: 1,000,000 (typ.)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 48 MHz (at max.) Peripheral modules run in synchronization with the PCLKB: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 48 MHz (at max.) • ADCLK in the S12AD runs in synchronization with PCLKD: Up to 48 MHz • The ICLK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1, 2, 4, 8, 16, 32, 64)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels

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Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	• Module stop function • Four low power consumption modes Sleep mode, deep sleep mode, software standby mode, and snooze mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, middle-speed operating mode 2 and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 256 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (The NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	Data transfer controller (DTCb)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Sequence transfer
I/O ports	General I/O ports	80-pin/64-pin (ROM capacity: product with 128 Kbytes or more)/64-pins (ROM capacity: product with 64 Kbytes)/48-pin/32-pin • I/O: 69/53/53/39/23 • Input: 3/3/1/1/1 • Pull-up resistors: 69/53/53/39/23 • Open-drain outputs: 47/35/35/27/20 • 5-V tolerance: 4/2/2/2/2
Event link controller (ELC)		• Event signals of 48 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 unit • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed clock for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCB)	• Clock source: Sub-clock • Calendar count mode or binary count mode selectable • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt
	Low power timer (LPTa)	• 16 bits × 1 channel • Clock source: Sub-clock, LOCO clock divided by 4, or dedicated low-speed clock for the IWDT selectable • Clock division ratio: Frequency divided by 1, 2, 4, 8, 16, or 32 selectable • PWM output mode
	8-bit timer (TMRa)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer

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Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (SCIg, SCIh, SCIk)	• 6 channels (channel 1, 5: SCIk, 6, 8, 9: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 7, 8, or 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on SCI5) • SCIk (the following functions are added) Data matching detection Adjustment function of the asynchronous RXD sampling • SCIh (the following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
Communication functions	Serial peripheral interface (RSPIc)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Transit/receive data can be swapped in byte units • Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception.
	CAN module (RSCAN)	• 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 mailboxes
12-bit A/D converter (S12ADE)		• 12 bits (18 channels × 1 unit*1) • 12-bit resolution • Minimum conversion time: 0.67 μs per channel when the ADCLK is operating at 48 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Conversion results compare features • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0 V to AVCC0
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable

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Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
Capacitive touch sensing unit (CTSU2SL, CTSU2L)		• CTSU2L Self-capacitance method: A single pin configures a single key, supporting up to 36 keys Mutual capacitance method: Matrix configuration with 8 × 8, supporting up to 64 keys • CTSU2SL (The following functions are added to CTSU2L) Automatic correction Automatic judgment
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Encryption function	Advanced encryption standard hardware accelerator (AESA)	• Key lengths: 128 and 256 bits • Support for ECB, CBC, and CTR operating modes • Speed of calculations: 128-bit key length in 176 cycles 256-bit key length in 240 cycles • Compliant with FIPS PUB 197
	True random number generator (RNGA)	• Length of random numbers: 32 bits • Generation of random-number-generated interrupts after a number is generated
Power supply voltages/Operating frequencies		VCC = 1.8 to 5.5 V: 48 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KC-A) 7 × 7 mm, 0.5 mm pitch 32-pin LQFP (PLQP0032GB-A) 7 × 7 mm, 0.8 mm pitch 32-pin HWQFN (PWQN0032KE-A) 5 × 5 mm, 0.5 mm pitch
Debugging interfaces		FINE interface

Note 1. The 12-bit A/D converter has 17 external input channels and a single internal input channel. For details, refer to section 35, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.

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Table 1.2 Comparison of Functions for Different Packages in the RX140 Group

Module/Functions		Products with 128-Kbyte or larger ROM			Products with 64-Kbyte ROM		
		80 Pins	**64 Pins**	**48 Pins**	**64 Pins**	**48 Pins**	**32 Pins**
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0 to IRQ2, IRQ5 to IRQ7
DTC	Data transfer controller	Available			Available		
Timers	Multi-function timer pulse unit 2	6 channels			6 channels		
	Port output enable 2	POE0# to POE3#, POE8#			POE0# to POE3#, POE8#		POE0#, POE8#
	8-bit timer	2 channels × 2 units			2 channels × 2 units		
	Compare match timer	2 channels × 1 unit			2 channels × 1 unit		
	Low power timer	1 channel			1 channel		
	Realtime clock	Available		Not supported	Available	Not supported	
	Independent watchdog timer	Available			Available		
Communication functions	Serial communications interfaces (SCIk)	2 channels (SCI1, 5)			2 channels (SCI1, 5)		
	Serial communications interfaces (SCIg)	3 channels (SCI6, 8, 9)		2 channels (SCI6, 8)	Not supported		
	Serial communications interfaces (SCIh)	1 channel (SCI12)			1 channel (SCI12)		
Communication functions	I^2C bus interface	1 channel			1 channel		
	Serial peripheral interface	1 channel			1 channel		
	CAN module	1 channel			Not supported		
Capacitive touch sensing unit (CTSU2SL)		36 channels	32 channels	24 channels	Not supported		
Capacitive touch sensing unit (CTSU2L)		Not supported			12 channels	12 channels	12 channels
12-bit A/D converter		18 channels *1	15 channels *1	11 channels *1	15 channels *1	11 channels *1	8 channels *1
Temperature sensor		Available			Available		
D/A converter		2 channels		Not supported	2 channels	Not supported	
CRC calculator		Available			Available		
Event link controller		Available			Available		
Comparator B		2 channels			2 channels		
Encryption function	Advanced encryption standard hardware accelerator (AESA)	Available/Not supported			Not supported		
	True random number generator (RNGA)	Available/Not supported			Not supported		
Packages		80-pin LFQFP (0.5 mm)	64-pin LQFP (0.8 mm) 64-pin LFQFP (0.5 mm)	48-pin LFQFP (0.5 mm) 48-pin HWQFN (0.5 mm)	64-pin LQFP (0.8 mm) 64-pin LFQFP (0.5 mm)	48-pin LFQFP (0.5 mm) 48-pin HWQFN (0.5 mm)	32-pin LQFP (0.8 mm) 32-pin HWQFN (0.5 mm)

Note 1. This number includes a single internal input channel. For details, refer to section 35, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.

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1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Encryption Module	Operating Temperature
RX140	R5F51406ADFN	R5F51406ADFN#30	PLQP0080KB-B	256 Kbytes	64 Kbytes	8 Kbytes	48 MHz	Not supported	–40 to +85°C
	R5F51406ADFM	R5F51406ADFM#30	PLQP0064KB-C						
	R5F51406ADFK	R5F51406ADFK#30	PLQP0064GA-A						
	R5F51406ADFL	R5F51406ADFL#30	PLQP0048KB-B						
	R5F51406ADNE	R5F51406ADNE#30	PWQN0048KC-A						
	R5F51406AGFN	R5F51406AGFN#30	PLQP0080KB-B						–40 to +105°C
	R5F51406AGFM	R5F51406AGFM#30	PLQP0064KB-C						
	R5F51406AGFK	R5F51406AGFK#30	PLQP0064GA-A						
	R5F51406AGFL	R5F51406AGFL#30	PLQP0048KB-B						
	R5F51406AGNE	R5F51406AGNE#30	PWQN0048KC-A						
	R5F51405ADFN	R5F51405ADFN#30	PLQP0080KB-B	128 Kbytes	32 Kbytes				–40 to +85°C
	R5F51405ADFM	R5F51405ADFM#30	PLQP0064KB-C						
	R5F51405ADFK	R5F51405ADFK#30	PLQP0064GA-A						
	R5F51405ADFL	R5F51405ADFL#30	PLQP0048KB-B						
	R5F51405ADNE	R5F51405ADNE#30	PWQN0048KC-A						
	R5F51405AGFN	R5F51405AGFN#30	PLQP0080KB-B						–40 to +105°C
	R5F51405AGFM	R5F51405AGFM#30	PLQP0064KB-C						
	R5F51405AGFK	R5F51405AGFK#30	PLQP0064GA-A						
	R5F51405AGFL	R5F51405AGFL#30	PLQP0048KB-B						
	R5F51405AGNE	R5F51405AGNE#30	PWQN0048KC-A						
	R5F51403ADFM	R5F51403ADFM#30	PLQP0064KB-C	64 Kbytes	16 Kbytes	4 Kbytes			–40 to +85°C
	R5F51403ADFK	R5F51403ADFK#30	PLQP0064GA-A						
	R5F51403ADFL	R5F51403ADFL#30	PLQP0048KB-B						
	R5F51403ADNE	R5F51403ADNE#30	PWQN0048KC-A						
	R5F51403ADFJ	R5F51403ADFJ#30	PLQP0032GB-A						
	R5F51403ADNH	R5F51403ADNH#30	PWQN0032KE-A						
	R5F51403AGFM	R5F51403AGFM#30	PLQP0064KB-C						–40 to +105°C
	R5F51403AGFK	R5F51403AGFK#30	PLQP0064GA-A						
	R5F51403AGFL	R5F51403AGFL#30	PLQP0048KB-B						
	R5F51403AGNE	R5F51403AGNE#30	PWQN0048KC-A						
	R5F51403AGFJ	R5F51403AGFJ#30	PLQP0032GB-A						
	R5F51403AGNH	R5F51403AGNH#30	PWQN0032KE-A						

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Table 1.3 List of Products (2/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Encryption Module	Operating Temperature
RX140	R5F51406BDFN	R5F51406BDFN#30	PLQP0080KB-B	256 Kbytes	64 Kbytes	8 Kbytes	48 MHz	Available	–40 to +85°C
	R5F51406BDFM	R5F51406BDFM#30	PLQP0064KB-C						
	R5F51406BDFK	R5F51406BDFK#30	PLQP0064GA-A						
	R5F51406BDFL	R5F51406BDFL#30	PLQP0048KB-B						
	R5F51406BDNE	R5F51406BDNE#30	PWQN0048KC-A						
	R5F51406BGFN	R5F51406BGFN#30	PLQP0080KB-B						–40 to +105°C
	R5F51406BGFM	R5F51406BGFM#30	PLQP0064KB-C						
	R5F51406BGFK	R5F51406BGFK#30	PLQP0064GA-A						
	R5F51406BGFL	R5F51406BGFL#30	PLQP0048KB-B						
	R5F51406BGNE	R5F51406BGNE#30	PWQN0048KC-A						
	R5F51405BDFN	R5F51405BDFN#30	PLQP0080KB-B	128 Kbytes	32 Kbytes				–40 to +85°C
	R5F51405BDFM	R5F51405BDFM#30	PLQP0064KB-C						
	R5F51405BDFK	R5F51405BDFK#30	PLQP0064GA-A						
	R5F51405BDFL	R5F51405BDFL#30	PLQP0048KB-B						
	R5F51405BDNE	R5F51405BDNE#30	PWQN0048KC-A						
	R5F51405BGFN	R5F51405BGFN#30	PLQP0080KB-B						–40 to +105°C
	R5F51405BGFM	R5F51405BGFM#30	PLQP0064KB-C						
	R5F51405BGFK	R5F51405BGFK#30	PLQP0064GA-A						
	R5F51405BGFL	R5F51405BGFL#30	PLQP0048KB-B						
	R5F51405BGNE	R5F51405BGNE#30	PWQN0048KC-A						

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.

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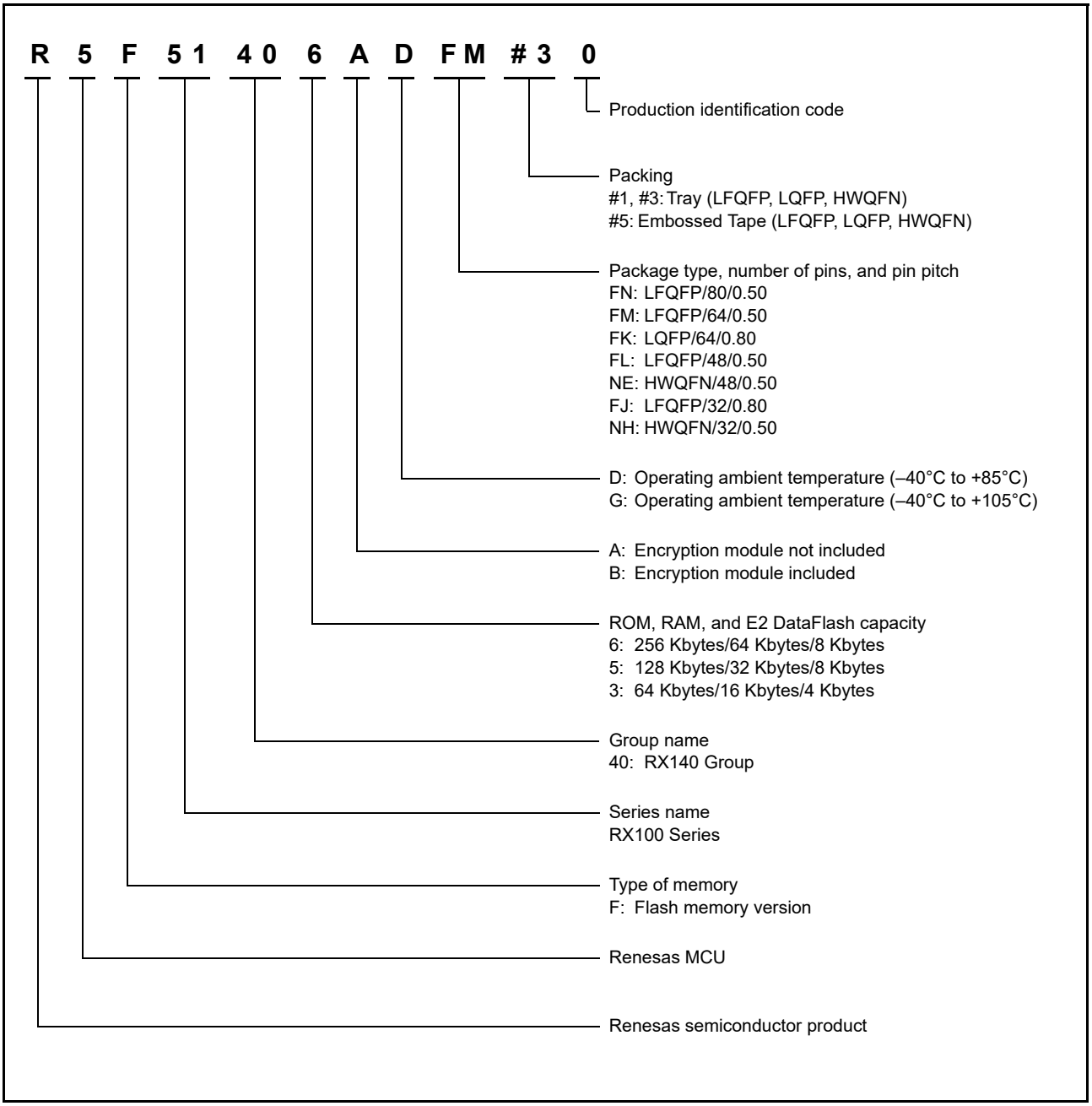

Figure 1.1 How to Read the Product Part Number

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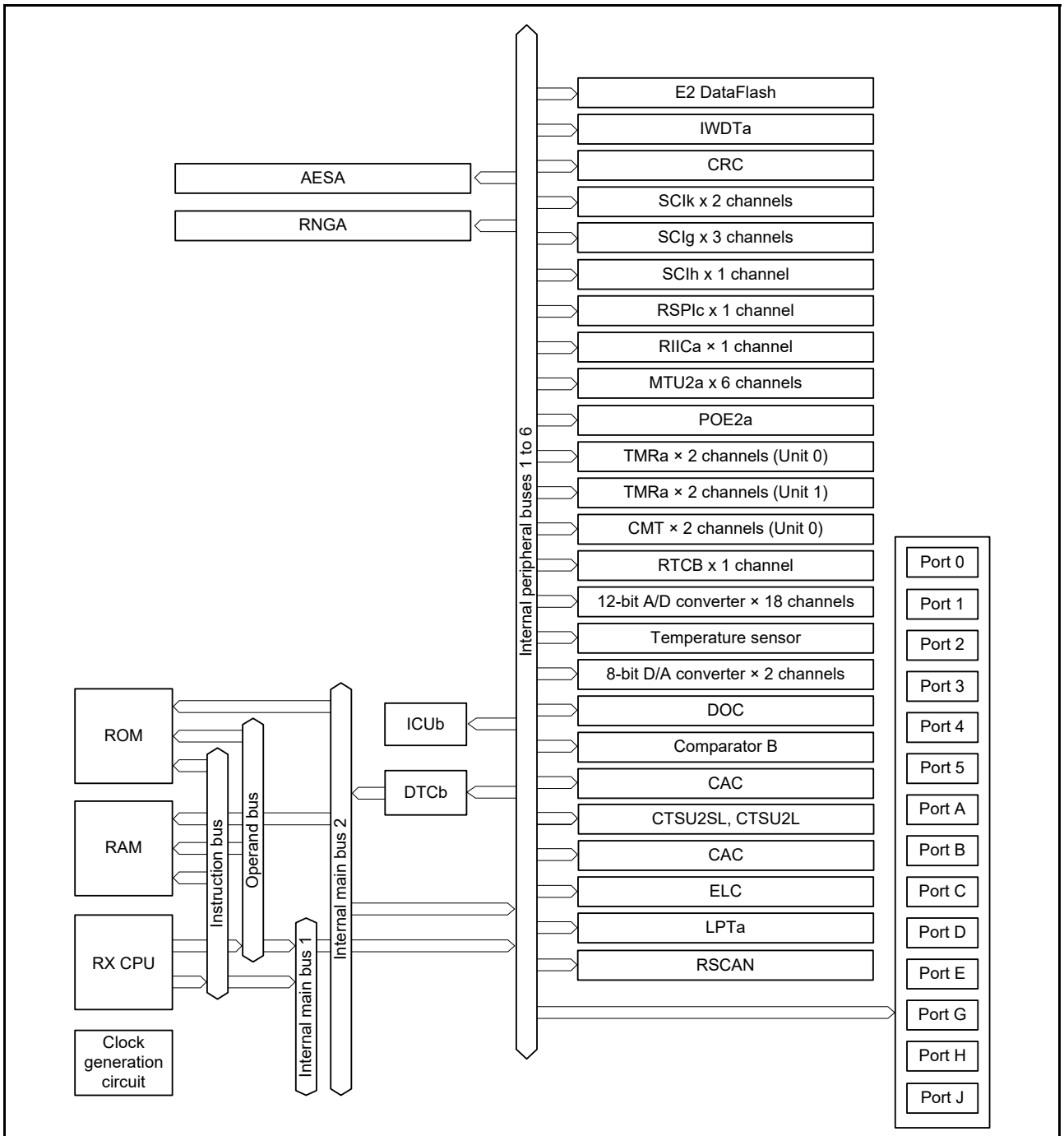
1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCb: Data transfer controller
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIk, SCIg, SCIh: Serial communications interface
RSPIc: Serial peripheral interface
RIICa: I²C bus interface
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
RTCB: Realtime clock

DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit
CTSU2SL, CTSU2L: Capacitive touch sensing unit
TMRa: 8-bit timer
LPTa: Low power timer
RSCAN: CAN module
AESA: Advanced encryption standard hardware accelerator
RNGA: True-random number generator

Note: Available functions depend on the product.

Figure 1.2 Block Diagram

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1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. For usage, refer to section 3.1, Operating Mode Types and Selection in the User's Manual: Hardware.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
Voltage detection circuit	CMPA2	Input	Detection target voltage pin for voltage detection 2.
Clock frequency accuracy measurement circuit	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.
Low power timer	LPTO	Output	PWM output pin

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Table 1.4 Pin Functions (2/3)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg, SCIk)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#, SS8#, SS9#	Input	Slave-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I^2C bus interface	SCL0	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.

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Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
CAN module	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
12-bit A/D converter	AN000 to AN007, AN016 to AN021, AN024 to AN026	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0, CMPB1	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0, CVREFB1	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0, CMPOB1	Output	Output pin for comparator B.
Capacitive touch sensing unit	TS0 to TS35	I/O	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	—	Connect to the VSS via a decoupling capacitor (10 nF) for stabilizing the internal voltage
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
I/O ports	P03 to P07	I/O	5-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20, P21, P26, P27	I/O	4-bit input/output pins.
	P30 to P32, P34 to P37	I/O	7-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P54, P55	I/O	2-bit input/output pins.
	PA0 to PA6	I/O	7-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC2 to PC7	I/O	6-bit input/output pins.
	PD0 to PD2	I/O	3-bit input/output pins.
	PE0 to PE5	I/O	6-bit input/output pins.
	PG7	I/O	1-bit input/output pin.
	PH0 to PH3, PH6*1, PH7*1	I/O	6-bit input/output pins (PH6, PH7: input pins).
	PJ1, PJ6, PJ7	I/O	3-bit input/output pins.

Note 1. This is not supported by products with 64 Kbytes of ROM.

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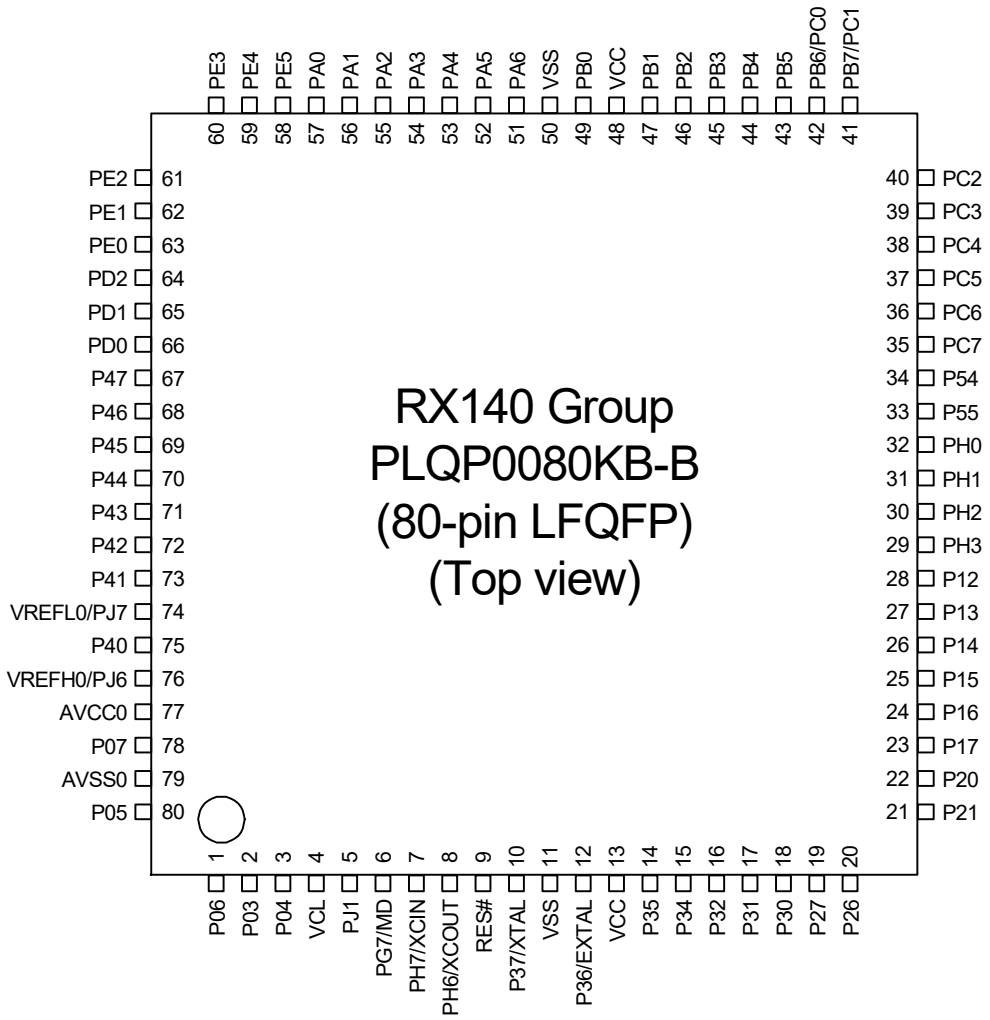
1.5 Pin Assignments

1.5.1 80-pin LFQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LFQFP)”.

Figure 1.3 Pin Assignments of the 80-Pin LFQFP

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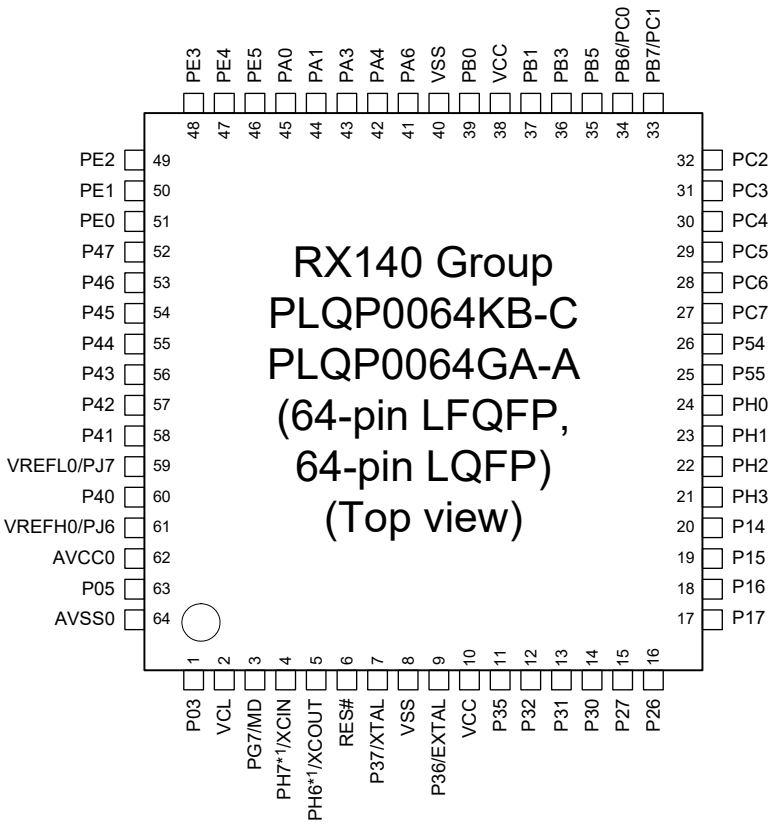
1.5.2 64-pin LFQFP, 64-pin LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP)”.
Note 1. This is not supported by products with 64 Kbytes of ROM.

Figure 1.4 Pin Assignments of the 64-Pin LFQFP, 64-Pin LQFP

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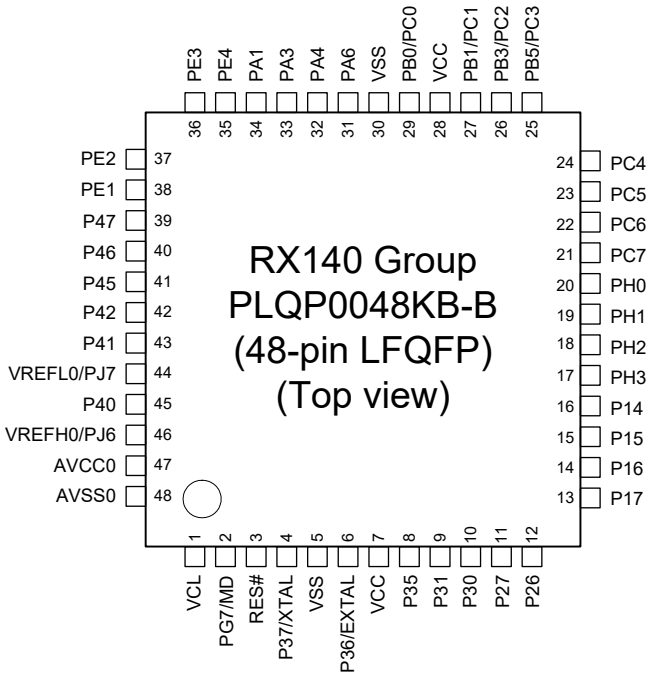
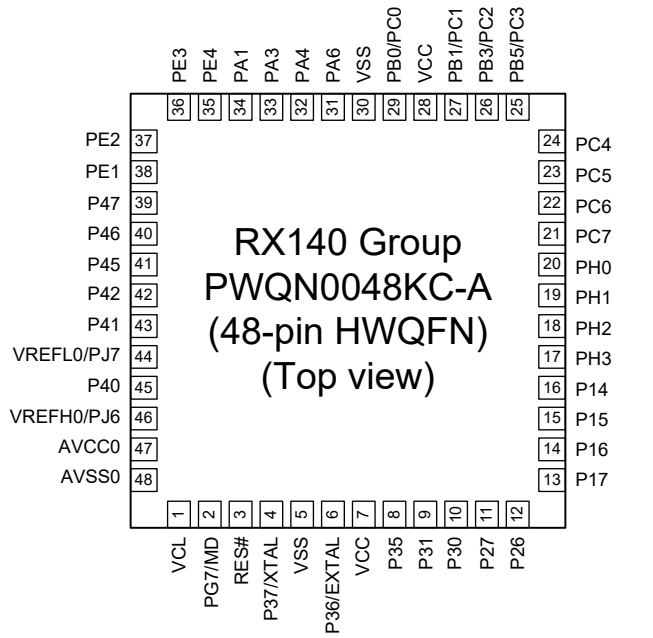
1.5.3 48-pin LFQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN)”.

Figure 1.5 Pin Assignments of the 48-Pin LQFP

1.5.4 48-pin HWQFN



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN)”.

Figure 1.6 Pin Assignments of the 48-Pin HWQFN

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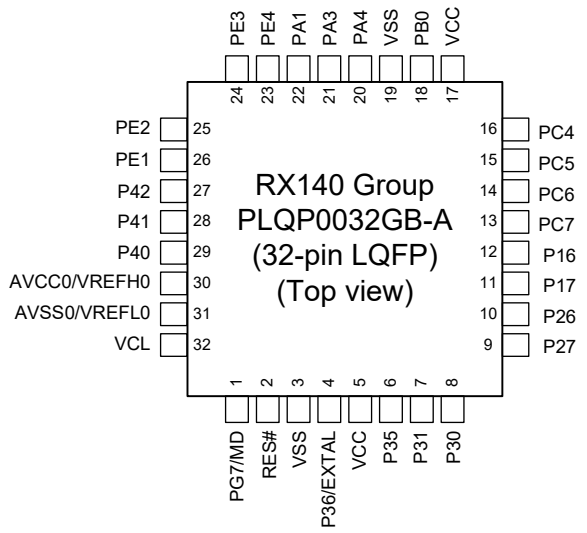
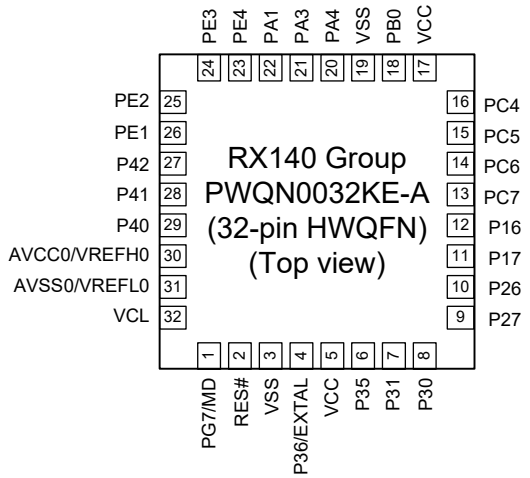
1.5.5 32-pin LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (32-Pin LQFP, 32-Pin HWQFN)”.

Figure 1.7 Pin Assignments of the 32-Pin LQFP

1.5.6 32-pin HWQFN



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (32-Pin LQFP, 32-Pin LQFPHWQFN)”.

Figure 1.8 Pin Assignments of the 32-Pin HWQFN

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1.6 List of Pins and Pin Functions

1.6.1 80-pin LFQFP

Table 1.5 List of Pins and Pin Functions (80-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, LPT)	Communications (SCIg, SCIh, SCIk, RSPI, RIIC, RSCAN)	Touch sensing	Others
1		P06*1				
2		P03*1				DA0
3		P04*1				
4	VCL					
5		PJ1	MTIOC3A			
6	MD	PG7				FINED
7	XCIN	PH7				
8	XCOUT	PH6				
9	RES#					
10	XTAL	P37				IRQ4
11	VSS					
12	EXTAL	P36				IRQ2
13	VCC					
14		P35				NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6		IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
19		P27	MTIOC2B/TMCI3	SCK1	TS3	
20		P26	MTIOC2A/TMO1/LPTO	TXD1/SMOSI1/SSDA1	TS4	
21		P21	MTIOC1B/TMCI0			
22		P20	MTIOC1A/TMRI0			
23	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0		IRQ7
24	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0		IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1/CRXD0	TS5	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/CTXD0	TS6	IRQ4
27	(5V tolerant)	P13	MTIOC0B/TMO3	SDA0		IRQ3
28	(5V tolerant)	P12	TMCI1	SCL0		IRQ2
29		PH3	MTIOC4D/TMCI0		TS7	
30		PH2	MTIOC4C/TMRI0		TS8	IRQ1
31		PH1	MTIOC3D/TMO0		TS9	IRQ0
32		PH0	MTIOC3B		TS10	CACREF
33		P55	MTIOC4A/MTIOC4D/TMO3	CRXD0	TS11	
34		P54	MTIOC4B/TMCI1	CTXD0	TS12	
35		PC7	MTCLKB/MTIOC3A/TMO2/ LPTO	MISOA/TXD8/SMOSI8/SSDA8	TS13	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA/RXD8/SMISO8/SSCL8	TS14	
37		PC5	MTIOC0C/MTIOC3B/ MTCLKD/TMRI2	RSPCKA/SCK8	TS15	
38		PC4	MTIOC0A/MTIOC3D/ MTCLKC/TMCI1/POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	TSCAP	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
41		PB7/ PC1*2	MTIOC3B	TXD9/SMOSI9/SSDA9	TS18	
42		PB6/ PC0*2	MTIOC3D	RXD9/SMISO9/SSCL9	TS19	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	TS20	
44		PB4		CTS9#/RTS9#/SS9#	TS21	

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Table 1.5 List of Pins and Pin Functions (80-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, LPT)	Communications (SCIg, SCIh, SCIk, RSPI, RIIC, RSCAN)	Touch sensing	Others
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#/LPTO	SCK6	TS22	
46		PB2		CTS6#/RTS6#/SS6#	TS23	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
48	VCC					
49		PB0	MTIOC3D/MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
50	VSS					
51		PA6	MTIOC3D/MTIC5V/ MTCLKB/TMCI3/POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
52		PA5		RSPCKA	TS27	
53		PA4	MTIOC4C/MTIC5U/ MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
54		PA3	MTIOC0D/MTIOC4D/ MTIC5V/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/SSLA3	TS30	
56		PA1	MTIOC0B/MTIOC3B/ MTCLKC	SCK5/SSLA2	TS31	
57		PA0	MTIOC4A	SSLA1	TS32	CACREF
58		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
59		PE4	MTIOC4D/MTIOC1A/ MTIOC4A		TS33	AN020/CMPA2/ CLKOUT
60		PE3	MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT
61		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
62		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
63		PE0		SCK12		AN016
64		PD2	MTIOC4D	SCK6		IRQ2/AN026
65		PD1	MTIOC4B	RXD6/SMISO6/SSCL6		IRQ1/AN025
66		PD0		TXD6/SMOSI6/SSDA6		IRQ0/AN024
67		P47*1				AN007
68		P46*1				AN006
69		P45*1				AN005
70		P44*1				AN004
71		P43*1				AN003
72		P42*1				AN002
73		P41*1				AN001
74	VREFL0	PJ7*1				
75		P40*1				AN000
76	VREFH0	PJ6*1				
77	AVCC0					
78		P07*1				ADTRG0#
79	AVSS0					
80		P05*1				DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. PC0 and PC1 are valid only when the port switching function is selected.

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1.6.2 64-pin LFQFP, 64-pin LQFP

Table 1.6 List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, LPT)	Communications (SCIg, SCIh, SCIk, RSPI, RIIC, RSCAN)	Touch sensing	Others
1		P03*1				DA0
2	VCL					
3	MD	PG7				FINED
4	XCIN	PH7*3				
5	XCOUT	PH6*3				
6	RES#					
7	XTAL	P37				IRQ4
8	VSS					
9	EXTAL	P36				IRQ2
10	VCC					
11		P35				NMI
12		P32	MTIOC0C/TMO3	TXD6*3/SMOSI6*3/SSDA6*3	TS0*3	IRQ2/RTCOUT
13		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1*3	IRQ1
14		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2*3	IRQ0
15		P27	MTIOC2B/TMCI3	SCK1	TS3	
16		P26	MTIOC2A/TMO1/LPTO	TXD1/SMOSI1/SSDA1	TS4	
17	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0		IRQ7
18	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0		IRQ6/RTCOUT/ ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1/CRXD0	TS5*3	IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/CTXD0	TS6*3	IRQ4
21		PH3	MTIOC4D/TMCI0		TS7*3	
22		PH2	MTIOC4C/TMRI0		TS8*3	IRQ1
23		PH1	MTIOC3D/TMO0		TS9*3	IRQ0
24		PH0	MTIOC3B		TS10*3	CACREF
25		P55	MTIOC4A/MTIOC4D/TMO3	CRXD0*3	TS11*3	
26		P54	MTIOC4B/TMCI1	CTXD0*3	TS12*3	
27		PC7	MTIOC3A/MTCLKB/TMO2/ LPTO	TXD8*3/SMOSI8*3/SSDA8*3/MISOA	TS13	CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8*3/SMISO8*3/SSCL8*3/MOSIA	TS14	
29		PC5	MTIOC0C/MTIOC3B/ MTCLKD/TMRI2	SCK8*3/RSPCKA	TS15	
30		PC4	MTIOC0A/MTIOC3D/ MTCLKC/TMCI1/POE0#	SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0	TSCAP	
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16*3	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17*3	
33		PB7/ PC1*2	MTIOC3B	TXD9*3/SMOSI9*3/SSDA9*3	TS18*3	
34		PB6/ PC0*2	MTIOC3D	RXD9*3/SMISO9*3/SSCL9*3	TS19*3	
35		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9*3	TS20*3	
36		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#/LPTO	SCK6*3	TS22*3	
37		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6*3/SMOSI6*3/SSDA6*3	TS24*3	IRQ4/CMPOB1
38	VCC					
39		PB0	MTIOC3D/MTIC5W	RXD6*3/SMISO6*3/SSCL6*3/RSPCKA	TS25	
40	VSS					
41		PA6	MTIOC3D/MTIC5V/ MTCLKB/TMCI3/POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26*3	
42		PA4	MTIOC4C/MTIC5U/ MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
43		PA3	MTIOC0D/MTIOC4D/ MTIC5V/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1

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Table 1.6 List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, LPT)	Communications (SCIg, SCIh, SCIk, RSPI, RIIC, RSCAN)	Touch sensing	Others
44		PA1	MTIOC0B/MTIOC3B/ MTCLKC	SCK5/SSLA2	TS31	
45		PA0	MTIOC4A	SSLA1	TS32*3	CACREF
46		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
47		PE4	MTIOC4D/MTIOC1A/ MTIOC4A		TS33	AN020/CMPA2/ CLKOUT
48		PE3	MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
51		PE0		SCK12		AN016
52		P47*1				AN007
53		P46*1				AN006
54		P45*1				AN005
55		P44*1				AN004
56		P43*1				AN003
57		P42*1				AN002
58		P41*1				AN001
59	VREFL0	PJ7*1				
60		P40*1				AN000
61	VREFH0	PJ6*1				
62	AVCC0					
63		P05*1				DA1
64	AVSS0					

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. PC0 and PC1 are valid only when the port switching function is selected.
Note 3. This is not supported by products with 64 Kbytes of ROM.

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1.6.3 48-pin LFQFP, 48-pin HWQFN

Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, LPT)	Communications (SCIg, SCIh, SCIk, RSPI, RIIC, RSCAN)	Touch sensing	Others
1	VCL					
2	MD	PG7				FINED
3	RES#					
4	XTAL	P37				IRQ4
5	VSS					
6	EXTAL	P36				IRQ2
7	VCC					
8		P35				NMI
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1*3	IRQ1
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2*3	IRQ0
11		P27	MTIOC2B/TMCI3	SCK1	TS3	
12		P26	MTIOC2A/TMO1/LPTO	TXD1/SMOSI1/SSDA1	TS4	
13	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/POE8#	SCK1/MISOA/SDA0		IRQ7
14	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0		IRQ6/ ADTRG0#/ RTCOUT
15		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1/CRXD0*3	TS5*3	IRQ5
16		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/CTXD0*3	TS6*3	IRQ4
17		PH3	MTIOC4D/TMCI0		TS7*3	
18		PH2	MTIOC4C/TMRI0		TS8*3	IRQ1
19		PH1	MTIOC3D/TMO0		TS9*3	IRQ0
20		PH0	MTIOC3B		TS10*3	CACREF
21		PC7	MTIOC3A/TMO2/MTCLKB/LPTO	TXD8*3/SMOSI8*3/SSDA8*3/MISOA	TS13	CACREF
22		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8*3/SMISO8*3/SSCL8*3/MOSIA	TS14	
23		PC5	MTIOC0C/MTIOC3B/MTCLKD/ TMRI2	SCK8*3/RSPCKA	TS15	
24		PC4	MTIOC0A/MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0	TSCAP	
25		PB5/PC3*1	MTIOC2A/MTIOC1B/TMRI1/POE1#		TS20*3	
26		PB3/PC2*1	MTIOC0A/MTIOC4A/TMO0/POE3#/ LPTO	SCK6*3	TS22*3	
27		PB1/PC1*1	MTIOC0C/MTIOC4C/TMCI0	TXD6*3/SMOSI6*3/SSDA6*3	TS24*3	IRQ4/CMPOB1
28	VCC					
29		PB0/PC0*1	MTIOC3D/MTIC5W	RXD6*3/SMISO6*3/SSCL6*3/ RSPCKA	TS25	
30	VSS					
31		PA6	MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26*3	
32		PA4	MTIOC4C/MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/ CVREFB1
33		PA3	MTIOC0D/MTIOC4D/MTIC5V/ MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
34		PA1	MTIOC0B/MTIOC3B/MTCLKC	SCK5/SSLA2	TS31	
35		PE4	MTIOC4D/MTIOC1A/MTIOC4A		TS33	AN020/ CMPA2/ CLKOUT
36		PE3	MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#	TS34	AN019/ CLKOUT
37		PE2	MTIOC4A	RXD12/RXDX12/SSCL12	TS35	IRQ7/AN018/ CVREFB0
38		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SSDA12		AN017/CMPB0
39		P47*2				AN007
40		P46*2				AN006
41		P45*2				AN005
42		P42*2				AN002
43		P41*2				AN001

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Table 1.7 List of Pins and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, LPT)	Communications (SCIg, SCIh, SCIk, RSPI, RIIC, RSCAN)	Touch sensing	Others
44	VREFL0	PJ7*2				
45		P40*2				AN000
46	VREFH0	PJ6*2				
47	AVCC0					
48	AVSS0					

Note 1. PC0 to PC3 are valid only when the port switching function is selected.
Note 2. The power source of the I/O buffer for these pins is AVCC0.
Note 3. This is not supported by products with 64 Kbytes of ROM.

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1.6.4 32-pin LQFP, 32-pin HWQFN

Table 1.8 List of Pins and Pin Functions (32-Pin LQFP, 32-Pin HWQFN)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, LPT)	Communications (SCIg, SCIh, SCIk, RSPI, RIIC)	Touch sensing	Others
1	MD	PG7				FINED
2	RES#					
3	VSS					
4	EXTAL	P36				IRQ2
5	VCC					
6		P35				NMI
7		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#		IRQ1
8		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1		IRQ0
9		P27	MTIOC2B/TMCI3	SCK1	TS3	
10		P26	MTIOC2A/TMO1/LPTO	TXD1/SMOSI1/SSDA1	TS4	
11	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0		IRQ7
12	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0		IRQ6/ADTRG0#/ RTCOUT
13		PC7	MTIOC3A/MTCLKB/TMO2/ LPTO	MISOA	TS13	CACREF
14		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
15		PC5	MTIOC0C/MTIOC3B/ MTCLKD/TMRI2	RSPCKA	TS15	
16		PC4	MTIOC0A/MTIOC3D/ MTCLKC/TMCI1/POE0#	SCK5/SSLA0	TSCAP	
17	VCC					
18		PB0	MTIOC3D/MTIC5W	RSPCKA	TS25	
19	VSS					
20		PA4	MTIOC4C/MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
21		PA3	MTIOC0D/MTIOC4D/ MTIC5V/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
22		PA1	MTIOC0B/MTIOC3B/ MTCLKC	SCK5/SSLA2	TS31	
23		PE4	MTIOC1A/MTIOC4A/ MTIOC4D		TS33	AN020/CMPA2/ CLKOUT
24		PE3	MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#	TS34	AN019/CLKOUT
25		PE2	MTIOC4A	RXD12/SSCL12/RXDX12	TS35	IRQ7/AN018/CVREFB0
26		PE1	MTIOC4C	TXD12/SSDA12/TXDX12/SIOX12		AN017/CMPB0
27		P42*1				AN002
28		P41*1				AN001
29		P40*1				AN000
30	AVCC0/VREFH0					
31	AVSS0/VREFL0					
32	VCL					

Note 1. The power source of the I/O buffer for these pins is AVCC0.

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2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Ports for 5 V tolerant: P12, P13, P16, P17	V_{in}	–0.3 to +6.5	V
	P03 to P07, P40 to P47, PJ6, PJ7		–0.3 to AVCC0 + 0.3	V
	Ports other than above		–0.3 to VCC + 0.3	
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN016 to AN021, AN024 to AN026 used		–0.3 to VCC + 0.3	
Junction temperature	D-version	T_j	–40 to +105	°C
	G-version		–40 to +112	
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 μF capacitor. The capacitor must be placed close to the pin, refer to section 2.15.1, Connecting VCL Capacitor and Bypass Capacitors.
Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

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2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item	Symbol	Symbol	Min.	Typ.	Max.	Unit
Power supply voltages		VCC*1, *2	1.8	—	5.5	V
		VSS	—	0	—	
Analog power supply voltages		AVCC0*1	1.8	—	5.5	V
		AVSS0	—	0	—	
		VREFH0	1.8	—	AVCC0	
		VREFL0	—	0	—	
Input voltage	Ports for 5 V tolerant: P12, P13, P16, P17	V_{in}	–0.3	—	5.8	V
	P03 to P07, P40 to P47, PJ6, PJ7		–0.3	—	AVCC0 + 0.3	
	Ports other than above		–0.3	—	VCC + 0.3	
Operating temperature*3	D version	T_{opr}	–40	—	85	°C
	G version		–40	—	105	

Note 1. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.
Note 2. When VCC < 2.4 V, normal operating mode functions of the CTSU are restricted. For details, refer to section 32, Capacitive Touch Sensing Unit (CTSU2SL, CTSU2L) in the User's Manual: Hardware.
Note 3. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance for stabilizing the internal voltage	C_{VCL}	4.7μF ± 30%*1

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 4.7 μF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

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2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—	V	
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	IRQ input pin, MTU2 input pin, POE2 input pin, TMR input pin, SCI input pin, RSPI input pin, CAC input pin, CAN input pin, ADTRG0# input pin*1, RES#, NMI, MD	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.1 × VCC	—	—		
	ADTRG0# input pin*2	V_{IH}	0.8 × AVCC0	—	—		
		V_{IL}	—	—	0.2 × AVCC0		
		ΔV_T	0.1 × AVCC0	—	—		
Input level voltage (except for schmitt trigger input pins)	EXTAL (external clock input)	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
	RIIC input pin (SMBus)	V_{IH}	2.2	—	—		VCC = 3.6 to 5.5 V
			2.0	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.8		VCC = 3.6 to 5.5 V
			—	—	0.5		VCC = 2.7 to 3.6 V
	P12 to P17, P20, P21, P26, P27, P30 to P32, P34 to P37, P54, P55, PA0 to PA6, PB0 to PB7, PC2 to PC7, PD0 to PD2, PE0 to PE5, PH0 to PH3, PH6*3, PH7*3 PJ1, PG7	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	P03 to P07, P40 to P47, PJ6, PJ7	V_{IH}	0.8 × AVCC	—	—		
		V_{IL}	—	—	0.2 × AVCC		

Note 1. The ADTRG0# input pin is assigned to P16.
Note 2. The ADTRG0# input pin is assigned to P07.
Note 3. This pin function is not provided for products with 64 Kbytes of ROM.

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Table 2.5 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin, MTU2 input pin, POE2 input pin, TMR input pin, SCI input pin, RSPI input pin, CAC input pin, CAN input pin, ADTRG0# input pin*1, RES#, NMI, MD	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.01 × VCC	—	—		
	ADTRG0# input pin*2	V_{IH}	0.8 × AVCC0	—	—		
		V_{IL}	—	—	0.2 × AVCC0		
		ΔV_T	0.01 × AVCC0	—	—		
Input level voltage (except for schmitt trigger input pins)	EXTAL (external clock input)	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
	P12 to P17, P20, P21, P26, P27, P30 to P32, P34 to P37, P54, P55, PA0 to PA6, PB0 to PB7, PC2 to PC7, PD0 to PD2, PE0 to PE5, PH0 to PH3, PH6*3, PH7*3 PJ1, PG7	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	P03 to P07, P40 to P47, PJ6, PJ7	V_{IH}	0.8 × AVCC	—	—		
		V_{IL}	—	—	0.2 × AVCC		

Note 1. The ADTRG0# input pin is assigned to P16.
Note 2. The ADTRG0# input pin is assigned to P07.
Note 3. This pin function is not provided for products with 64 Kbytes of ROM.

Table 2.6 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, P35, PH6*1, PH7*1	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports for 5-V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V, 5.8 V
	PJ6, PJ7		—	—	1.0		V_{in} = 0 V, VCC
	Other than ports for 5 V tolerant and PJ6, PJ7		—	—	0.2		V_{in} = 0 V, VCC
Input capacitance	All input pins (except for P35)	C_{in}	—	—	15	pF	V_{in} = 0 mV, f = 1 MHz, T_a = 25°C
	P35		—	—	30		

Note 1. This pin function is not provided for products with 64 Kbytes of ROM.

Table 2.7 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC < 5.5 V, 1.8 V ≤ AVCC0 < 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for P35, PH6*1, PH7*1)	R_U	10	20	50	kΩ	V_{in} = 0 V

Note 1. This pin function is not provided for products with 64 Kbytes of ROM.

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[Products with 64-Kbyte ROM]

Table 2.8 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ. *4	Max.		Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 48 MHz	I_{CC}	2.5	—	mA	
				ICLK = 32 MHz		1.8	—		
				ICLK = 16 MHz		1.3	—		
				ICLK = 8 MHz		1.0	—		
			All peripheral operation: Normal*3	ICLK = 48 MHz		9.0	—		
				ICLK = 32 MHz		7.4	—		
				ICLK = 16 MHz		4.2	—		
				ICLK = 8 MHz		2.5	—		
			All peripheral operation: Max.*3	ICLK = 48 MHz		—	20.1		
		Sleep mode	No peripheral operation*2	ICLK = 48 MHz		1.4	—		
				ICLK = 32 MHz		1.1	—		
				ICLK = 16 MHz		0.8	—		
				ICLK = 8 MHz		0.7	—		
			All peripheral operation: Normal*3	ICLK = 48 MHz		4.0	—		
				ICLK = 32 MHz		4.0	—		
				ICLK = 16 MHz		2.3	—		
				ICLK = 8 MHz		1.5	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 48 MHz		1.0	—		
				ICLK = 32 MHz		0.8	—		
				ICLK = 16 MHz		0.7	—		
				ICLK = 8 MHz		0.6	—		
			All peripheral operation: Normal*3	ICLK = 48 MHz		3.1	—		
				ICLK = 32 MHz		3.1	—		
				ICLK = 16 MHz		1.9	—		
				ICLK = 8 MHz		1.2	—		
		Increase during flash rewrite*5				2.1	—		
	Middle-speed operating mode	Normal operating mode	No peripheral operation*6	ICLK = 24 MHz		1.6	—		
				ICLK = 8 MHz		0.8	—		
				ICLK = 4 MHz		0.3	—		
				ICLK = 1 MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 24 MHz		5.8	—		
				ICLK = 8 MHz		2.3	—		
				ICLK = 4 MHz		1.5	—		
				ICLK = 1 MHz		0.8	—		
			All peripheral operation: Max.*7	ICLK = 24 MHz		—	13.1		
		Sleep mode	No peripheral operation*6	ICLK = 24 MHz		1.1	—		
				ICLK = 8 MHz		0.6	—		
				ICLK = 4 MHz		0.2	—		
				ICLK = 1 MHz		0.2	—		

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Item					Symbol	Typ. *4	Max.		Test Conditions
Supply current*1	Middle-speed operating mode	Sleep mode	All peripheral operation: Normal*7	ICLK = 24 MHz	I_{CC}	3.3	—	mA	
				ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.0	—		
				ICLK = 1 MHz		0.7	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 24 MHz		0.8	—		
				ICLK = 8 MHz		0.5	—		
				ICLK = 4 MHz		0.1	—		
				ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*7	ICLK = 24 MHz		2.6	—		
				ICLK = 8 MHz		1.3	—		
				ICLK = 4 MHz		0.9	—		
				ICLK = 1 MHz		0.7	—		
		Increase during flash rewrite*5				2.1	—		
	Middle-speed operating mode 2	Normal operating mode	No peripheral operation*8	ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		0.8	—		
			All peripheral operation: Max.*9	ICLK = 1 MHz		—	3.0		
		Sleep mode	No peripheral operation*8	ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		0.7	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		0.7	—		
		Increase during flash rewrite*5				1.4	—		
	Low-speed operating mode	Normal operating mode	No peripheral operation*10	ICLK = 32.768 kHz		2.4	—	μA	
			All peripheral operation: Normal*11, *12	ICLK = 32.768 kHz		7.5	—		
			All peripheral operation: Max. *11, *12	ICLK = 32.768 kHz		—	88.4		
		Sleep mode	No peripheral operation*10	ICLK = 32.768 kHz		1.4	—		
			All peripheral operation: Normal*11	ICLK = 32.768 kHz		3.8	—		
		Deep sleep mode	No peripheral operation*10	ICLK = 32.768 kHz		1.0	—		
			All peripheral operation: Normal*11	ICLK = 32.768 kHz		2.8	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK is set to the same frequency as ICLK and PCLK is set to divided by 2 when ICLK is 48 MHz. FCLK and PCLK are set to the same frequency as ICLK when ICLK is 32 MHz or less.

Note 4. Values when VCC = 3.3 V.

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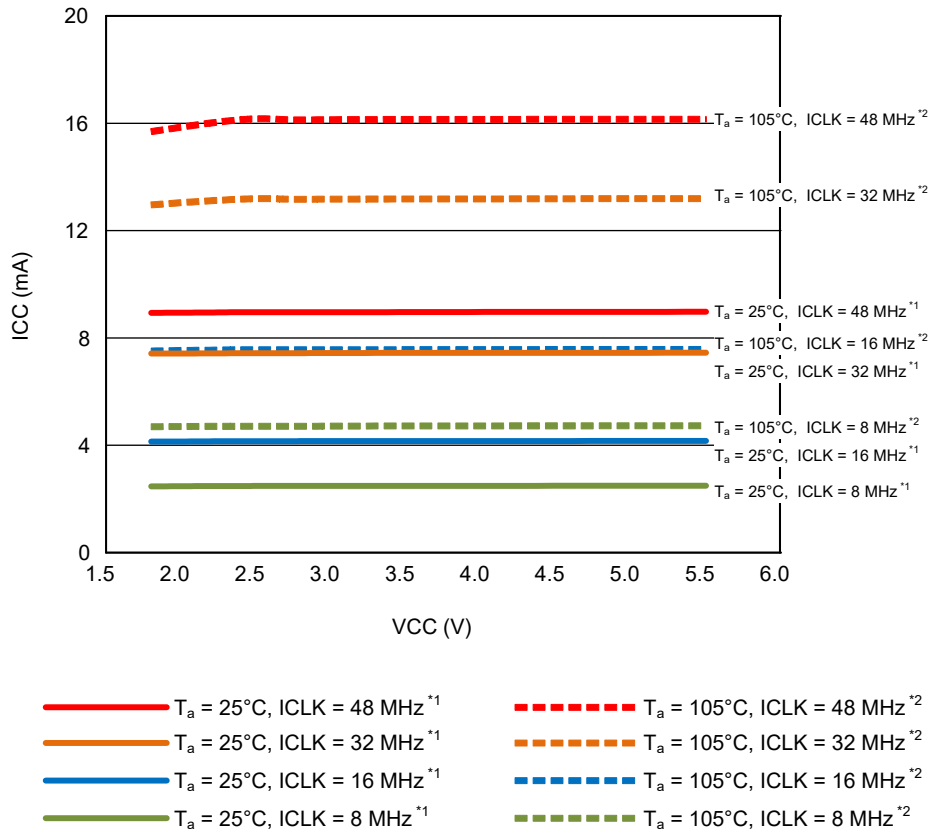
Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.
Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 24 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 24 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.
Note 8. Clock supply to the peripheral function is stopped. The clock source is LOCO when ICLK is 1 MHz, FCLK and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is LOCO when ICLK is 1 MHz, FCLK and PCLK are set to the same frequency as ICLK.
Note 10. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 11. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 12. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.1 Voltage Dependency in High-Speed Operating Mode (Reference Data for Products with 64-Kbyte ROM)

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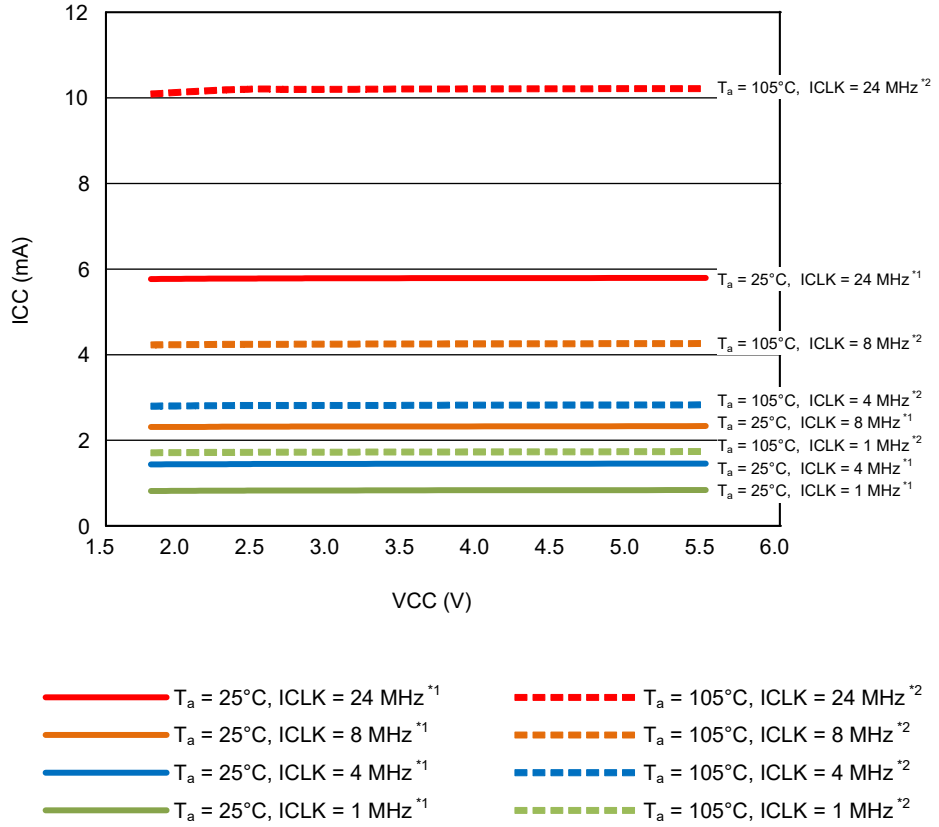

Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data for Products with 64-Kbyte ROM)

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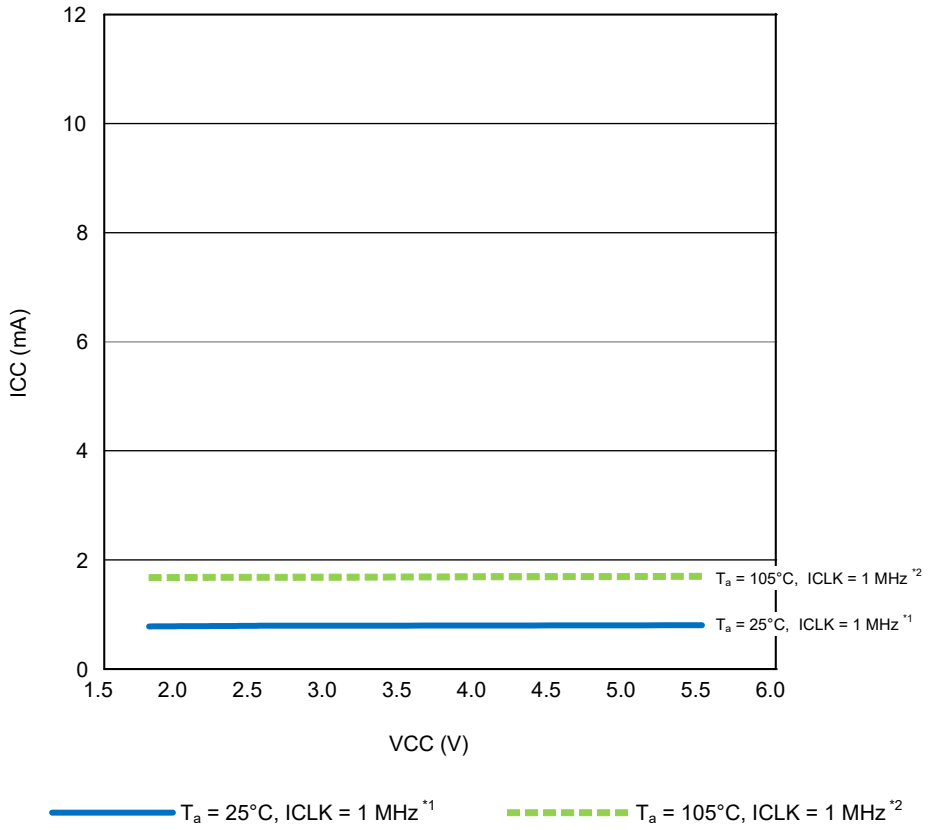

Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.3 Voltage Dependency in Middle-Speed Operating Mode 2 (Reference Data for Products with 64-Kbyte ROM)

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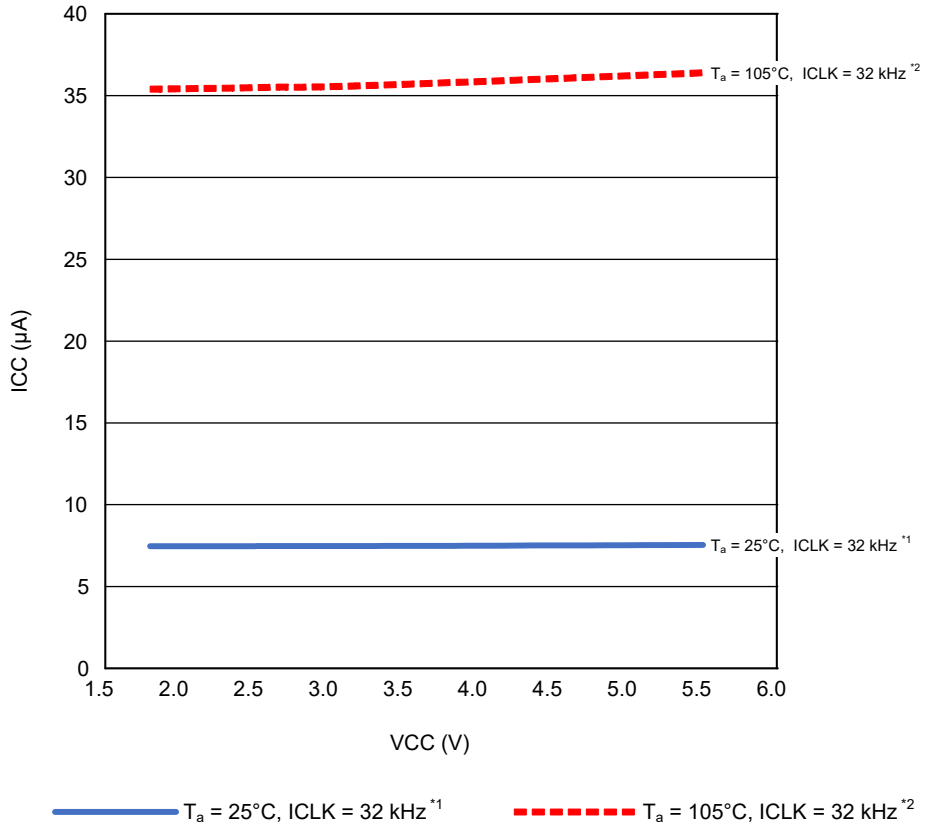

Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.4 Voltage Dependency in Low-Speed Operating Mode (Reference Data for Products with 64-Kbyte ROM)

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[Products with 128-Kbyte or larger ROM]

Table 2.9 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 48 MHz	I_{CC}	2.6	—	mA	
				ICLK = 32 MHz		1.9	—		
				ICLK = 16 MHz		1.3	—		
				ICLK = 8 MHz		1.0	—		
			All peripheral operation: Normal*3	ICLK = 48 MHz		10.4	—		
				ICLK = 32 MHz		8.9	—		
				ICLK = 16 MHz		4.9	—		
				ICLK = 8 MHz		2.9	—		
			All peripheral operation: Max.*3	ICLK = 48 MHz		—	22.8		
		Sleep mode	No peripheral operation*2	ICLK = 48 MHz		1.4	—		
				ICLK = 32 MHz		1.1	—		
				ICLK = 16 MHz		0.8	—		
				ICLK = 8 MHz		0.7	—		
			All peripheral operation: Normal*3	ICLK = 48 MHz		4.7	—		
				ICLK = 32 MHz		4.9	—		
				ICLK = 16 MHz		2.8	—		
				ICLK = 8 MHz		1.7	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 48 MHz		1.0	—		
				ICLK = 32 MHz		0.8	—		
				ICLK = 16 MHz		0.7	—		
				ICLK = 8 MHz		0.6	—		
			All peripheral operation: Normal*3	ICLK = 48 MHz		3.7	—		
				ICLK = 32 MHz		3.9	—		
				ICLK = 16 MHz		2.3	—		
				ICLK = 8 MHz		1.4	—		
		Increase during flash rewrite*5				2.1	—		
		Increase during encryption function operation				—	3.9		
	Middle-speed operating mode	Normal operating mode	No peripheral operation*6	ICLK = 24 MHz		1.7	—		
				ICLK = 8 MHz		0.9	—		
				ICLK = 4 MHz		0.3	—		
				ICLK = 1 MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 24 MHz		6.9	—		
				ICLK = 8 MHz		2.8	—		
				ICLK = 4 MHz		1.7	—		
				ICLK = 1 MHz		0.9	—		
			All peripheral operation: Max.*7	ICLK = 24 MHz		—	15.4		
		Sleep mode	No peripheral operation*6	ICLK = 24 MHz		1.1	—		
				ICLK = 8 MHz		0.7	—		
				ICLK = 4 MHz		0.2	—		
				ICLK = 1 MHz		0.2	—		

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Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating mode	Sleep mode	All peripheral operation: Normal*7	ICLK = 24 MHz	I_{CC}	4.0	—	mA	
				ICLK = 8 MHz		1.8	—		
				ICLK = 4 MHz		1.2	—		
				ICLK = 1 MHz		0.8	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 24 MHz		0.8	—		
				ICLK = 8 MHz		0.6	—		
				ICLK = 4 MHz		0.1	—		
				ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*7	ICLK = 24 MHz		3.2	—		
				ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.0	—		
				ICLK = 1 MHz		0.7	—		
		Increase during flash rewrite*5				2.1	—		
	Middle-speed operating mode 2	Normal operating mode	No peripheral operation*8	ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		0.9	—		
			All peripheral operation: Max.*9	ICLK = 1 MHz		—	3.3		
		Sleep mode	No peripheral operation*8	ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		0.7	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		0.7	—		
		Increase during flash rewrite*5				1.4	—		
	Low-speed operating mode	Normal operating mode	No peripheral operation*10	ICLK = 32.768 kHz		2.6	—	μA	
			All peripheral operation: Normal*11, *12	ICLK = 32.768 kHz		9.4	—		
			All peripheral operation: Max. *11, *12	ICLK = 32.768 kHz		—	175.4		
		Sleep mode	No peripheral operation*10	ICLK = 32.768 kHz		1.5	—		
			All peripheral operation: Normal*11	ICLK = 32.768 kHz		5.1	—		
		Deep sleep mode	No peripheral operation*10	ICLK = 32.768 kHz		1.3	—		
			All peripheral operation: Normal*11	ICLK = 32.768 kHz		4.1	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK is set to the same frequency as ICLK and PCLK is set to divided by 2 when ICLK is 48 MHz. FCLK and PCLK are set to the same frequency as ICLK when ICLK is 32 MHz or less.

Note 4. Values when VCC = 3.3 V.

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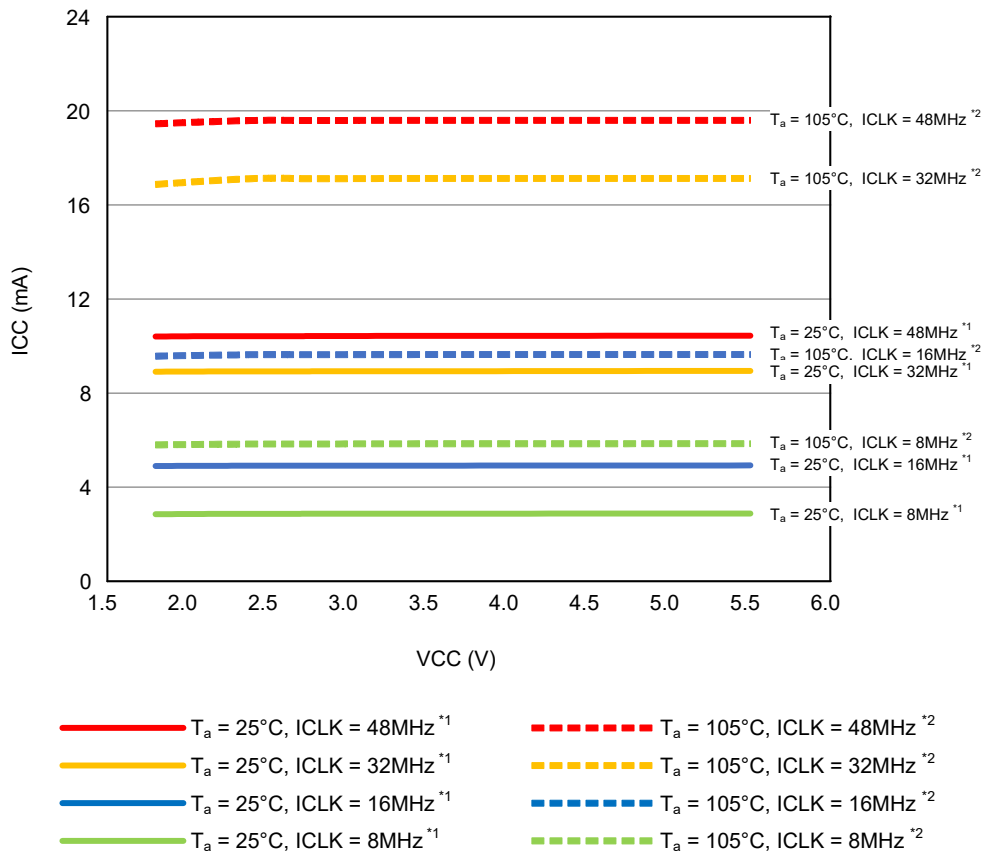
Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.
Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 24 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 24 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.
Note 8. Clock supply to the peripheral function is stopped. The clock source is LOCO when ICLK is 1 MHz, FCLK and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is LOCO when ICLK is 1 MHz, FCLK and PCLK are set to the same frequency as ICLK.
Note 10. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 11. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 12. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.5 Voltage Dependency in High-Speed Operating Mode (Reference Data for Products with 128-Kbyte or Larger ROM)

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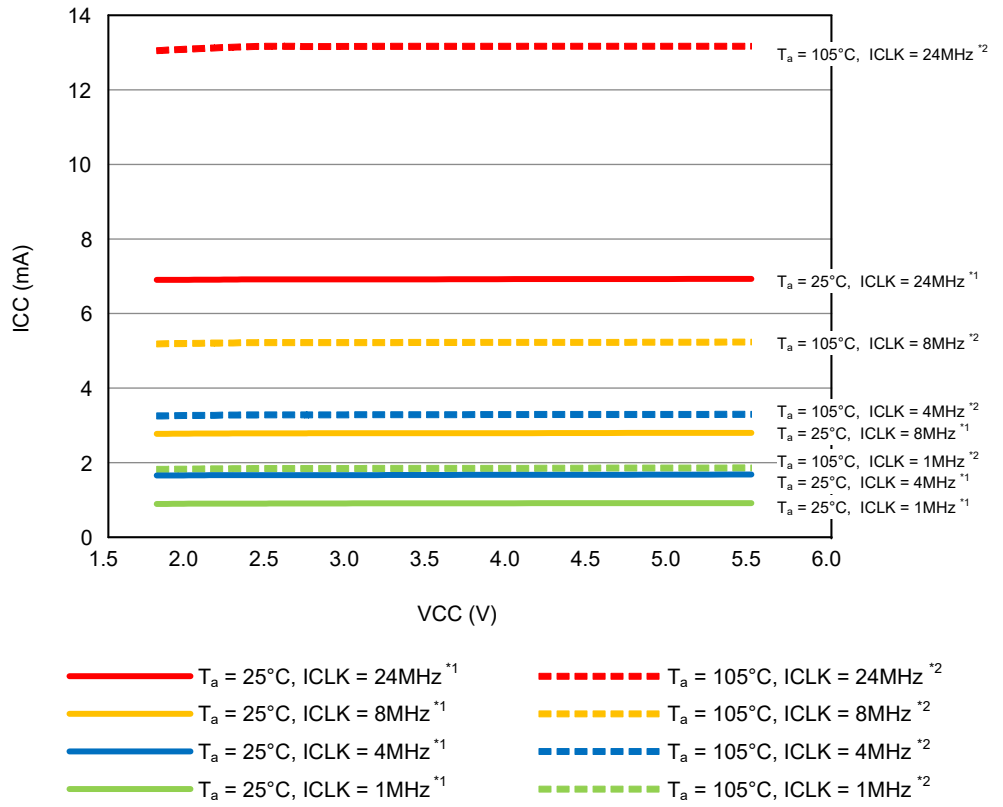

Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.6 Voltage Dependency in Middle-Speed Operating Mode (Reference Data for Products with 128-Kbyte or Larger ROM)

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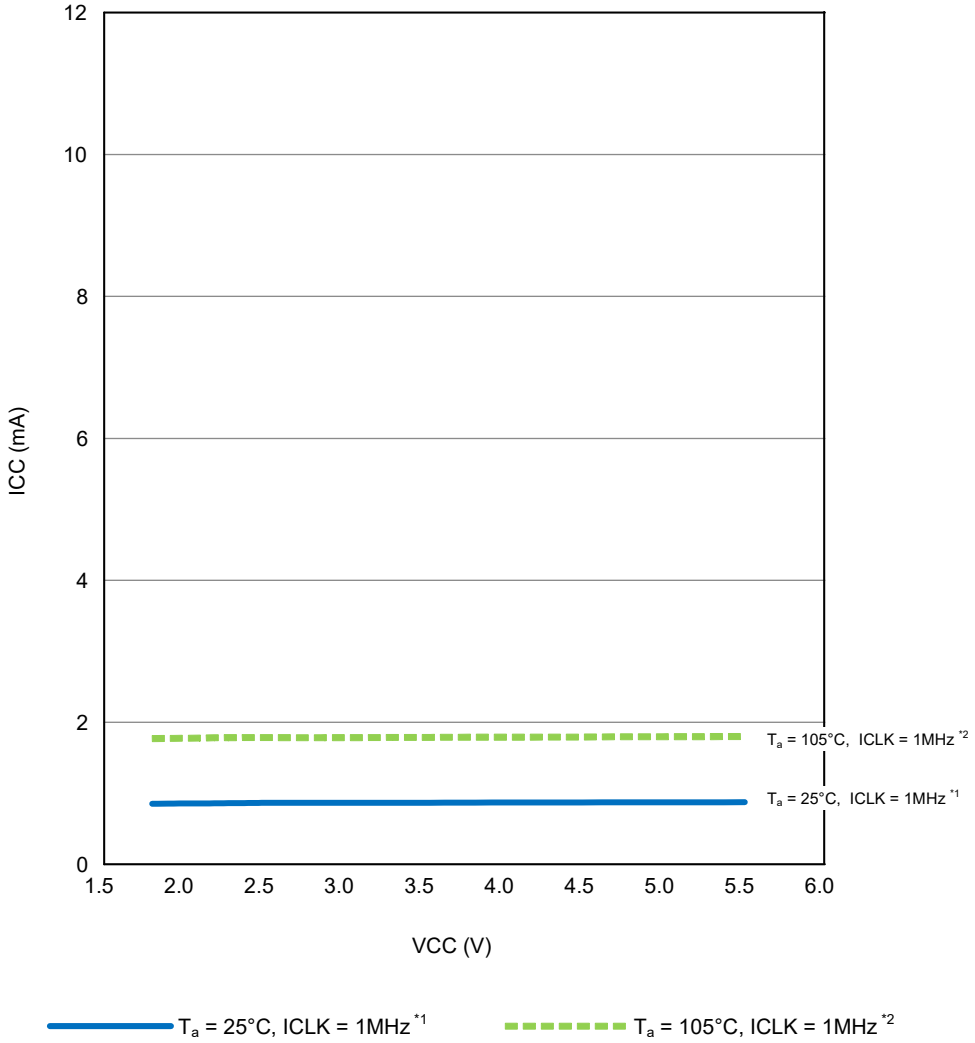

Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.7 Voltage Dependency in Middle-Speed Operating Mode 2 (Reference Data for Products with 128-Kbyte or Larger ROM)

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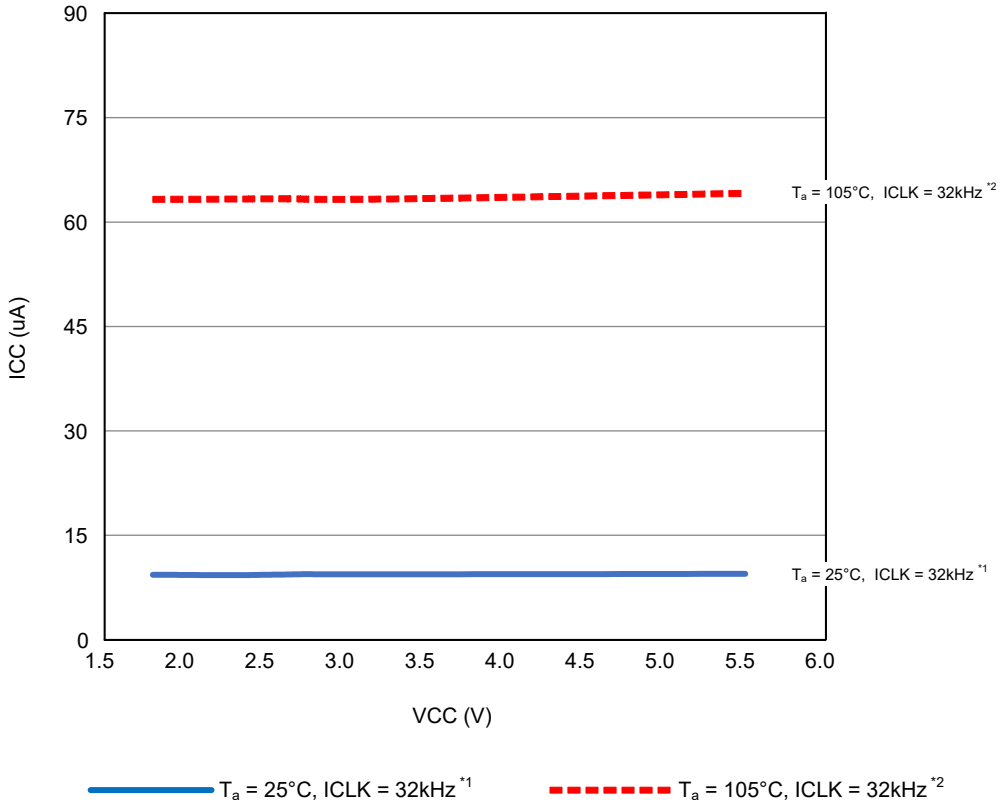

Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.8 Voltage Dependency in Low-Speed Operating Mode (Reference Data for Products with 128-Kbyte or Larger ROM)

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[Products with 64-Kbyte ROM]

Table 2.10 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.25	1.56	μA	
		T_a = 55°C		0.54	4.66		
		T_a = 85°C		1.86	18.09		
		T_a = 105°C		4.72	43.74		
	Increment for RTC operation*4			0.97	—		SOMCR.SODRV[1:0] set to drive capacity for standard CL
				0.52	—		SOMCR.SODRV[1:0] set to high drive capacity for low CL
				0.27	—		SOMCR.SODRV[1:0] set to middle drive capacity for low CL
				0.17	—		SOMCR.SODRV[1:0] set to low drive capacity for low CL
	Increment for low-power timer operation			0.28	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
				15.97	—		LPTCR1.LPCNTCKSEL 2 set to Low-speed on-chip oscillator
	Increment for independent watchdog timer operation			0.26	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.

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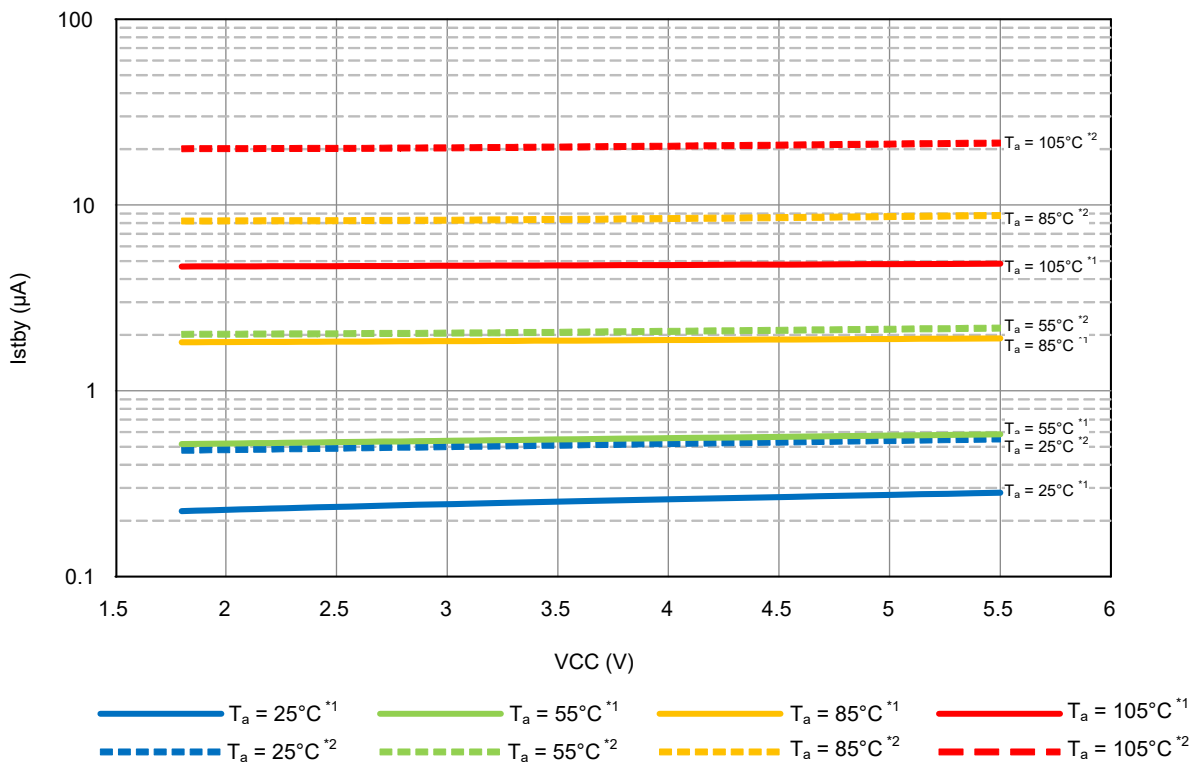
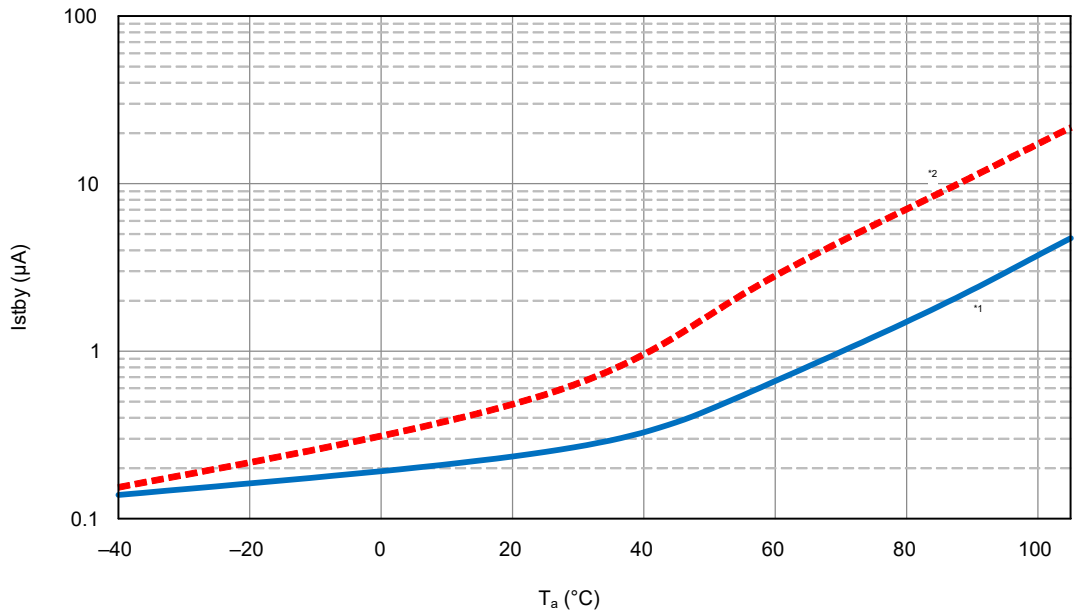


Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 2.9 Voltage Dependency in Software Standby Mode (Reference Data for Products with 64-Kbyte ROM)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 2.10 Temperature Dependency in Software Standby Mode (Reference Data for Products with 64-Kbyte ROM)

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[Products with 128-Kbyte or larger ROM]

Table 2.11 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Typ.*3	Max.		Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.43	2.07	μA	
		T_a = 55°C		1.00	8.46		
		T_a = 85°C		3.30	31.14		
		T_a = 105°C		7.76	71.36		
	Increment for RTC operation*4			0.99	—		SOMCR.SODRV[1:0] set to drive capacity for standard CL
				0.55	—		SOMCR.SODRV[1:0] set to high drive capacity for low CL
				0.32	—		SOMCR.SODRV[1:0] set to middle drive capacity for low CL
				0.22	—		SOMCR.SODRV[1:0] set to low drive capacity for low CL
	Increment for low-power timer operation			0.33	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
				15.89	—		LPTCR1.LPCNTCKSEL 2 set to Low-speed on-chip oscillator
	Increment for independent watchdog timer operation			0.32	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.

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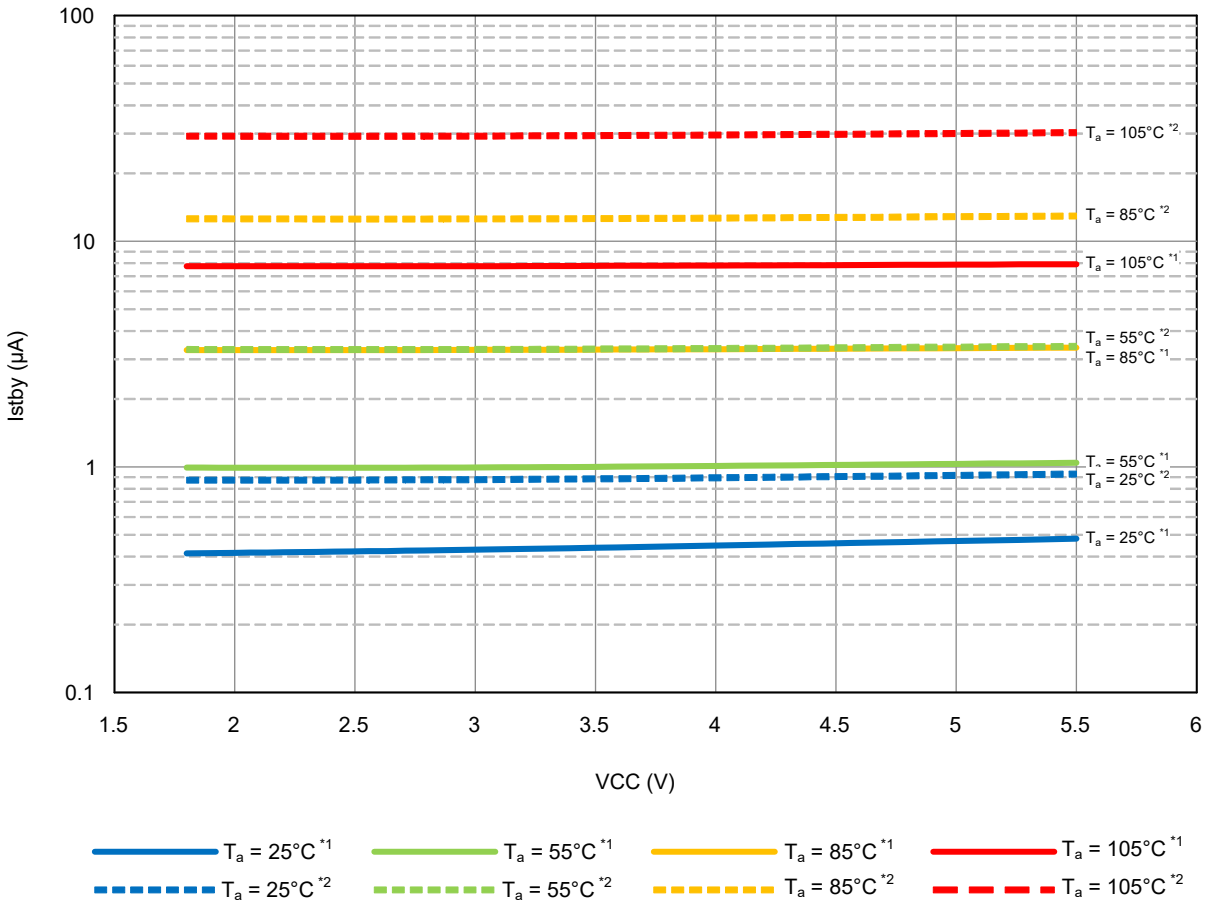

Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 2.11 Voltage Dependency in Software Standby Mode (Reference Data for Products with 128-Kbyte or Larger ROM)

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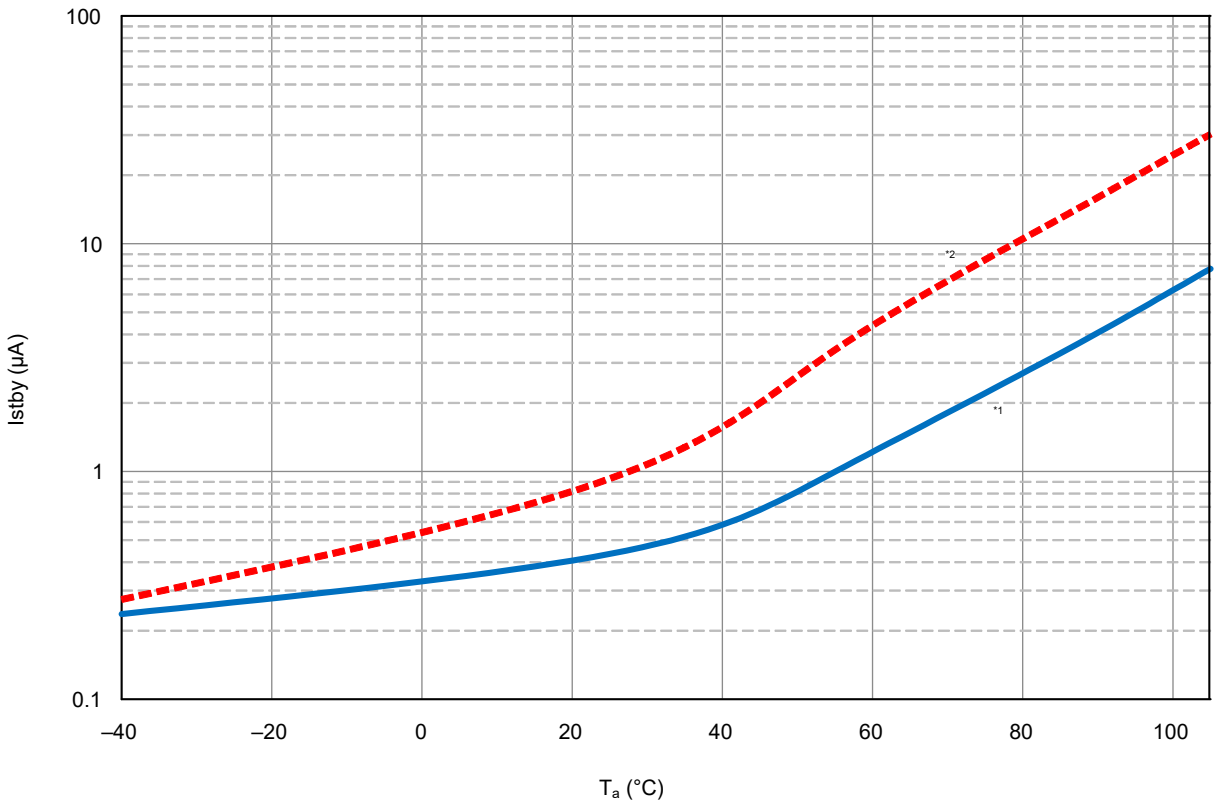

Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 2.12 Temperature Dependency in Software Standby Mode (Reference Data for Products with 128-Kbyte or Larger ROM)

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Table 2.12 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*4	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.6	1.3	mA	
	During A/D conversion (at low-speed conversion)		—	0.3	0.7		
	During D/A conversion (per channel)*1		—	—	0.5		
	Waiting for A/D and D/A conversion		—	—	2.0	μA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	49.6	120	μA	
	Waiting for A/D conversion		—	—	0.3	nA	
LVD0	—	I_{LVD}	—	0.04	—	μA	
LVD1, 2	Per channel		—	0.12	—	μA	
Temperature sensor*3	—	I_{TEMP}	—	120	—	μA	
Comparator B operating current*3	Window function enabled	I_{CMP}*2	—	7.5	12.5	μA	
	Comparator high-speed mode (per channel)		—	5.0	10.0	μA	
	Comparator low-speed mode (per channel)		—	1.5	3.0	μA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. Current consumed only by the comparator B module.
Note 3. ICurrent consumed by the power supply (VCC).
Note 4. When VCC = AVCC0 = 3.3 V.

Table 2.13 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 2.14 DC Characteristics (9)

Conditions: 0 V ≤ VCC ≤ 5.5 V, 0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) = 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) = 01b.
Note 3. When OFS1.LVDAS = 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

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Table 2.15 DC Characteristics (10)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit and lower limit. When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 2.13 $V_{r\,(VCC)}$ ≤ 0.2 × VCC
		—	—	1	MHz	Figure 2.13 $V_{r\,(VCC)}$ ≤ 0.08 × VCC
		—	—	10	MHz	Figure 2.13 $V_{r\,(VCC)}$ ≤ 0.06 × VCC
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

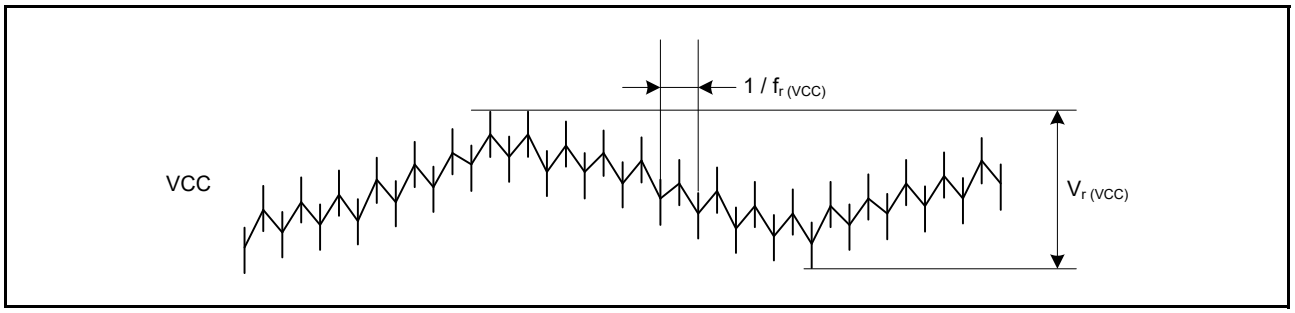

Figure 2.13 Ripple Waveform

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Table 2.16 Permissible Output Currents (1)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OL}	8.0	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		8.0	
	Ports other than above		8.0	
Permissible output low current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OL}	40	
	Total of P12 to P17, P20, P21, P26 to P27, P30 to P32, P34 to P37, PG7, PH2, PH3, PJ1		40	
	Total of P54, P55, PB0 to PB7, PC2 to PC7, PH0, PH1		40	
	Total of PA0 to PA6, PD0 to PD2, PE0 to PE5		40	
	Total of all output pins		80	
Permissible output high current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OH}	–4.0	
	Ports other than above		–4.0	
Permissible output high current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		–4.0	
	Ports other than above		–4.0	
Permissible output high current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OH}	–40	
	Total of P12 to P17, P20, P21, P26 to P27, P30 to P32, P34 to P37, PG7, PH2, PH3, PJ1		–40	
	Total of P54, P55, PB0 to PB7, PC2 to PC7, PH0, PH1		–40	
	Total of PA0 to PA6, PD0 to PD2, PE0 to PE5		–40	
	Total of all output pins		–80	

Note: Do not exceed the permissible total supply current.

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Table 2.17 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OL}	8.0	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		8.0	
	Ports other than above		8.0	
Permissible output low current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OL}	30	
	Total of P12 to P17, P20, P21, P26 to P27, P30 to P32, P34 to P37, PG7, PH2, PH3, PJ1		30	
	Total of P54, P55, PB0 to PB7, PC2 to PC7, PH0, PH1		30	
	Total of PA0 to PA6, PD0 to PD2, PE0 to PE5		30	
	Total of all output pins		60	
Permissible output high current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OH}	–4.0	
	Ports other than above		–4.0	
Permissible output high current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		–4.0	
	Ports other than above		–4.0	
Permissible output high current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OH}	–30	
	Total of P12 to P17, P20, P21, P26 to P27, P30 to P32, P34 to P37, PG7, PH2, PH3, PJ1		–30	
	Total of P54, P55, PB0 to PB7, PC2 to PC7, PH0, PH1		–30	
	Total of PA0 to PA6, PD0 to PD2, PE0 to PE5		–30	
	Total of all output pins		–60	

Note: Do not exceed the permissible total supply current.

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Table 2.18 Output Values of Voltage (1)

Conditions: 1.8 V ≤ VCC < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)		V_{OL}	—	0.3	V	I_{OL} = 1.0 mA
Output high	All output ports	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.3	—	V	I_{OH} = –0.5 mA
		Ports other than above		VCC – 0.3	—	V	

Table 2.19 Output Values of Voltage (2)

Conditions: 2.7 V ≤ VCC < 4.0 V, 2.7 V ≤ AVCC0 < 4.0 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)		V_{OL}	—	0.5	V	I_{OL} = 2.0 mA
	RIIC pins			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.5	—	V	I_{OH} = –1.0 mA
		Ports other than above		VCC – 0.5	—		

Table 2.20 Output Values of Voltage (3)

Conditions: 4.0 V ≤ VCC ≤ 5.5 V, 4.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)		V_{OL}	—	0.8	V	I_{OL} = 4.0 mA
	RIIC pins			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –2.0 mA
		Ports other than above		VCC – 0.8	—		

Table 2.21 Thermal Resistance Value (Reference Values)

Item	Package	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal resistance	80-pin LFQFP (PLQP0080KB-B)	θja	—	—	52.60	°C/W	JESD51-2 and JESD51-7 compliant
	64-pin LFQFP (PLQP0064KB-C)		—	—	54.70		
	64-pin LQFP (PLQP0064GA-A)		—	—	54.30		
	48-pin LFQFP (PLQP0048KB-B)		—	—	63.50		
	48-pin HWQFN (PWQN0048KC-A)		—	—	21.20*1		
	32-pin LQFP (PLQP0032GB-A)		—	—	62.20		
	32-pin HWQFN (PWQN0032KE-A)		—	—	23.60*1		
	80-pin LFQFP (PLQP0080KB-B)	Ψjt	—	—	1.54		
	64-pin LFQFP (PLQP0064KB-C)		—	—	2.29		
	64-pin LQFP (PLQP0064GA-A)		—	—	2.29		
	48-pin LFQFP (PLQP0048KB-B)		—	—	2.78		
	48-pin HWQFN (PWQN0048KC-A)		—	—	0.21*1		
	32-pin LQFP (PLQP0032GB-A)		—	—	2.78		
	32-pin HWQFN (PWQN0032KE-A)		—	—	0.23*1		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

Note 1. This value applies when the exposed die pad for this purpose is connected to VSS.

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2.4 Normal I/O Pin Output Characteristics

Table 2.22 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.05	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.09	—		I_{OH} = –1.0 mA
			—	VCC – 0.20	—		I_{OH} = –2.0 mA
			—	VCC – 0.49	—		I_{OH} = –4.0 mA

Table 2.23 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.02	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.05	—		I_{OH} = –1.0 mA
			—	VCC – 0.10	—		I_{OH} = –2.0 mA
			—	VCC – 0.22	—		I_{OH} = –4.0 mA

Table 2.24 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.02	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.04	—		I_{OH} = –1.0 mA
			—	VCC – 0.08	—		I_{OH} = –2.0 mA
			—	VCC – 0.15	—		I_{OH} = –4.0 mA

Table 2.25 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
			—	0.04	—		I_{OL} = 1.0 mA
			—	0.08	—		I_{OL} = 2.0 mA
			—	0.17	—		I_{OL} = 4.0 mA
			—	0.43	—		I_{OL} = 8.0 mA

Table 2.26 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.04	—		I_{OL} = 2.0 mA
			—	0.08	—		I_{OL} = 4.0 mA
			—	0.17	—		I_{OL} = 8.0 mA

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Table 2.27 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.01	—		I_{OL} = 1.0 mA
			—	0.03	—		I_{OL} = 2.0 mA
			—	0.06	—		I_{OL} = 4.0 mA
			—	0.12	—		I_{OL} = 8.0 mA

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2.5 AC Characteristics

2.5.1 Clock Timing

Table 2.28 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency*4	System clock (ICLK)	f	—	—	48	MHz
	FlashIF clock (FCLK)*1, *2		—	—	48	
	Peripheral module clock (PCLKB)		—	—	32	
	Peripheral module clock (PCLKD)*3		—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 2.35, HOCO Clock Timing (ROM capacity: product with 128 Kbytes or more) or Table 2.36, HOCO Clock Timing (ROM capacity: product with 64 Kbytes).

Table 2.29 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency*4	System clock (ICLK)	f	—	—	24	MHz
	FlashIF clock (FCLK)*1, *2		—	—	24	
	Peripheral module clock (PCLKB)		—	—	24	
	Peripheral module clock (PCLKD)*3		—	—	24	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 2.35, HOCO Clock Timing (ROM capacity: product with 128 Kbytes or more) or Table 2.36, HOCO Clock Timing (ROM capacity: product with 64 Kbytes).

Table 2.30 Operating Frequency Value (Middle-Speed Operating Mode 2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency*4	System clock (ICLK)	f	—	—	1	MHz
	FlashIF clock (FCLK)*1, *2		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKD)*3		—	—	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz when the A/D converter is in use.

Table 2.31 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency	System clock (ICLK)	f	—	—	32.768	kHz
	FlashIF clock (FCLK)*1		—	—	32.768	
	Peripheral module clock (PCLKB)		—	—	32.768	
	Peripheral module clock (PCLKD)*2		—	—	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

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Table 2.32 EXTAL Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.14
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

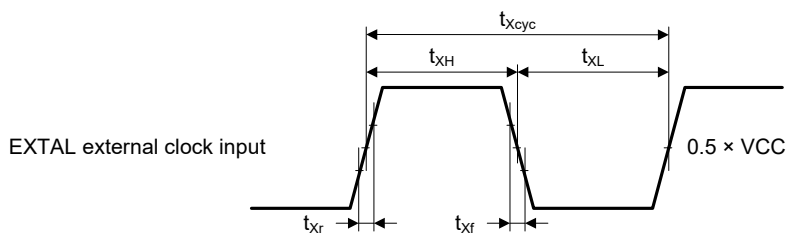

Figure 2.14 EXTAL External Clock Input Timing

Table 2.33 Main Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*1	$t_{MAINOSC}$	—	3	—	ms	Figure 2.15
Main clock oscillation stabilization time (ceramic resonator)*1	$t_{MAINOSC}$	—	50	—	μs	

Note 1. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

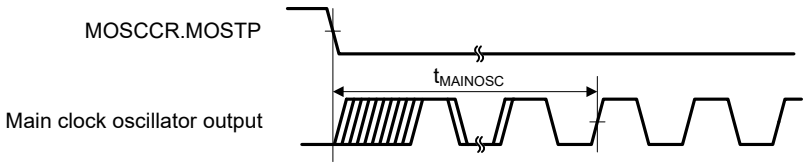

Figure 2.15 Main Clock Oscillation Start Timing

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Table 2.34 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation frequency error	Δf_{LOCO}	—	—	±14	%	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 2.16
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation frequency error	Δf_{ILOCO}	—	—	±15	%	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	80	μs	Figure 2.17

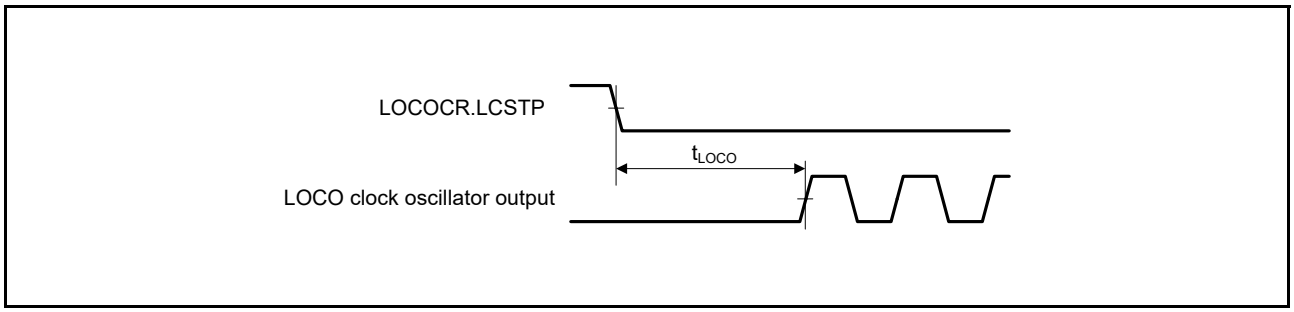

Figure 2.16 LOCO Clock Oscillation Start Timing

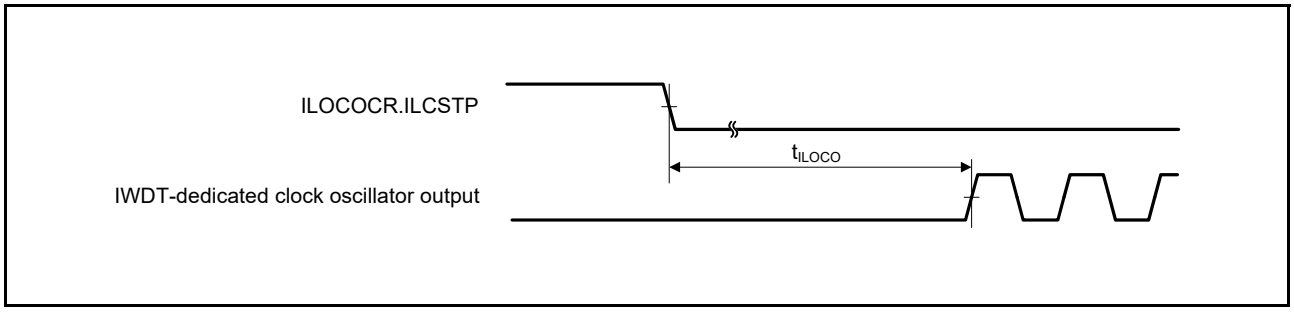

Figure 2.17 IWDT-Dedicated Clock Oscillation Start Timing

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Table 2.35 HOCO Clock Timing (ROM capacity: product with 128 Kbytes or more)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency*1	f_{HOCO}	23.76	24	24.24	MHz	T_a = –40 to +105°C
		31.68	32	32.32		
		47.52	48	48.48		
HOCO oscillation frequency error*1	Δf_{HOCO}	—	—	±1.0	%	T_a = –40 to +105°C
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	4.95	μs	Figure 2.19

Note 1. Accuracy at production test.

Table 2.36 HOCO Clock Timing (ROM capacity: product with 64 Kbytes)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency*1	f_{HOCO}	23.64	24	24.36	MHz	T_a = –40 to –20°C
		23.76		24.24		T_a = –20 to +85°C
		23.52		24.48		T_a = +85 to +105°C
		31.52	32	32.48	MHz	T_a = –40 to –20°C
		31.68		32.32		T_a = –20 to +85°C
		31.36		32.64		T_a = +85 to +105°C
		47.28	48	48.72	MHz	T_a = –40 to –20°C
		47.52		48.48		T_a = –20 to +85°C
		47.04		48.96		T_a = +85 to +105°C
HOCO oscillation frequency error*1	Δf_{HOCO}	—	—	±1.5	%	T_a = –40 to –20°C
		—	—	±1.0		T_a = –20 to +85°C
		—	—	±2.0		T_a = +85 to +105°C
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	4.95	μs	Figure 2.19

Note 1. Accuracy at production test.

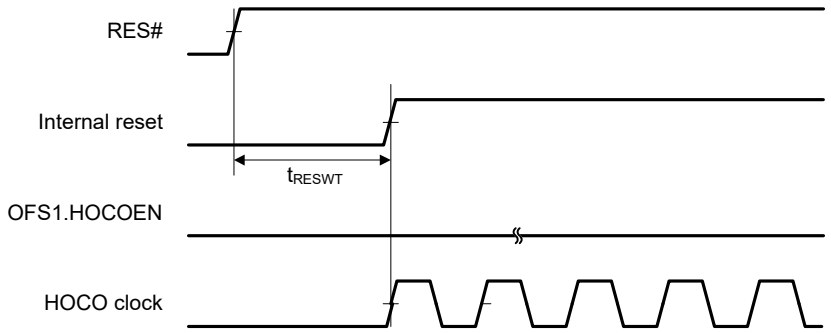

Figure 2.18 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

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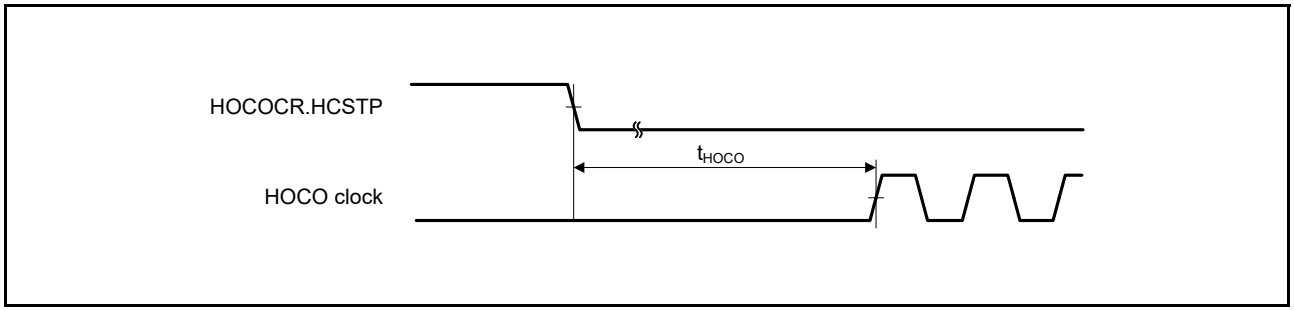

Figure 2.19 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

Table 2.37 PLL Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL input frequency	f_{PLLIN}	4	—	12	MHz	
PLL circuit oscillation frequency	f_{PLL}	24	—	48	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	81.4	μs	Figure 2.20
PLL free-running oscillation frequency	f_{PLLFR}	—	9	—	MHz	

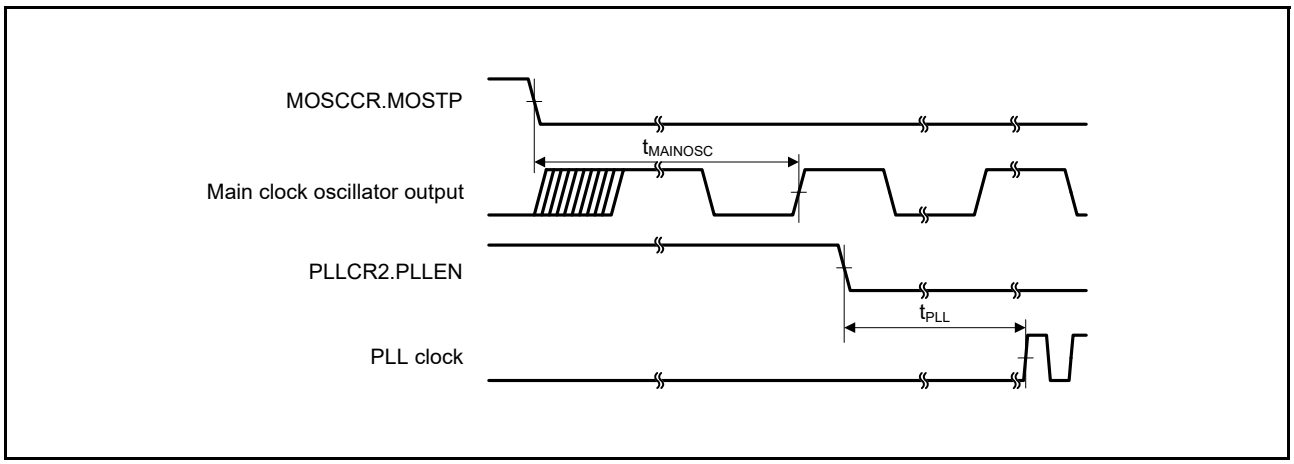

Figure 2.20 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

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Table 2.38 Sub-Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillator oscillation frequency*2	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*1	t_{SUBOSC}	—	0.5	—	s	Figure 2.21

Note 1. Reference value when a 32.768-kHz resonator is used.
After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 2. Only 32.768-kHz can be used.

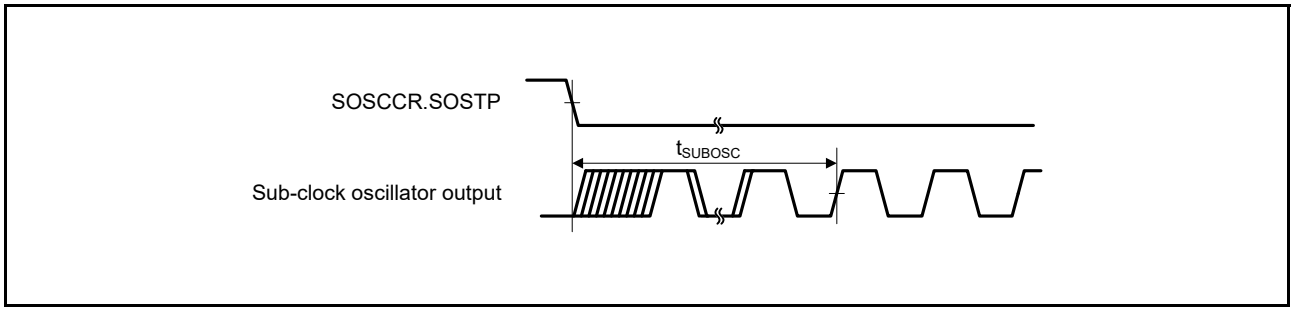

Figure 2.21 Sub-Clock Oscillation Start Timing

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2.5.2 Reset Timing

Table 2.39 Reset Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	10.5	—	—	ms	Figure 2.22
	Other than above	t_{RESW}	30	—	—	μs	Figure 2.23
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 2.22
	During fast startup time*2	t_{RESWT}	—	850	—	μs	
Wait time after RES# cancellation (during powered-on state)	LVD0 disabled*3	t_{RESWT}	—	120	—	μs	Figure 2.23
	LVD0 enabled*4		—	850	—	μs	
Internal reset time (independent watchdog timer reset, software reset)	LVD0 disabled*3	t_{RESWT2}	—	190	—	μs	
	LVD0 enabled*4		—	890	—	μs	

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) = a value other than 11b.
Note 3. When OFS1.LVDAS = 1b.
Note 4. When OFS1.LVDAS = 0b.

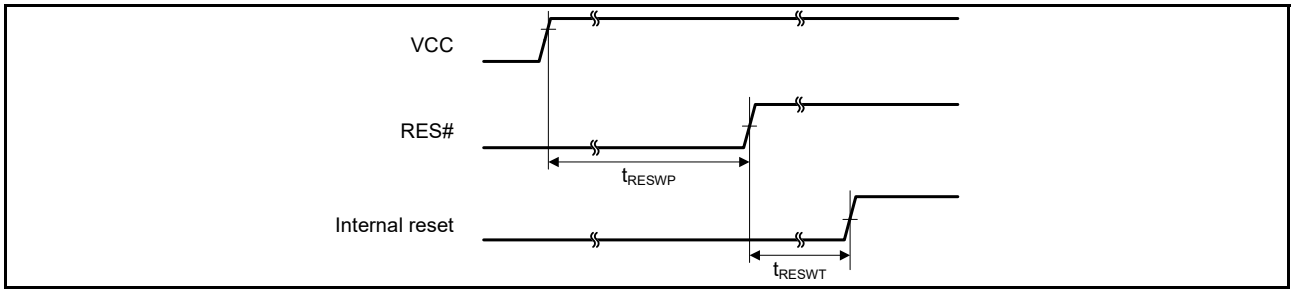

Figure 2.22 Reset Input Timing at Power-On

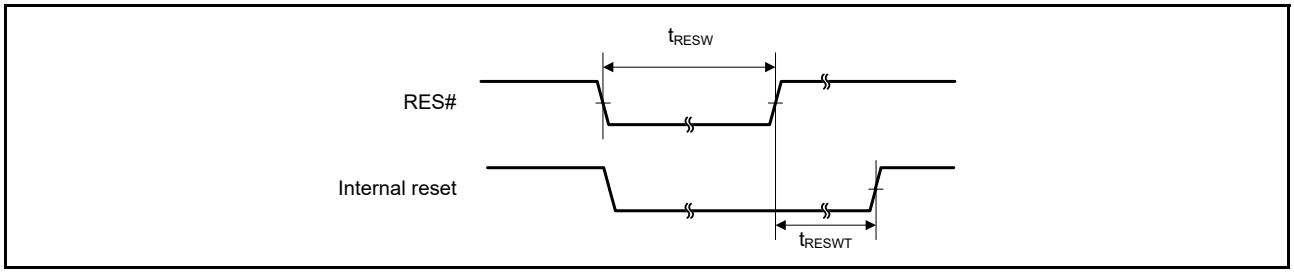

Figure 2.23 Reset Input Timing (1)

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2.5.3 Timing of Recovery from Low Power Consumption Modes

Table 2.40 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time*1	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	$t_{SBYOSCWTMC}$	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 1 / f_{ICLK}	μs	
			Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}		
		Sub-clock oscillator operating		$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}		
		High-speed on-chip oscillator operating		$t_{SBYOSCWTHO}$	—	—	t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
		Low-speed on-chip oscillator operating		$t_{SBYOSCWTLO}$	—	—	t_{LOCO} + 1 / f_{ICLK}		
Time required for operations by the sequencer before release from software standby mode*2				t_{SBYSEQ}	—	—	4 / f_{LOCO} + 11 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*3	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	t_{SBYMC}	—	—	$t_{SBYOSCWTMC}$ + t_{SBYSEQ}		Figure 2.24
			Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		
		Sub-clock oscillator operating		t_{SBYSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
		High-speed on-chip oscillator operating		t_{SBYHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
		Low-speed on-chip oscillator operating		t_{SBYLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entry to software standby mode, the oscillation stabilization wait time will be selected as the largest value among those for the operating oscillators.

Note 2. For n, the largest value is selected from among the internal clock division settings.

Note 3. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

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Table 2.41 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time*1	Middle-speed operating mode 2	Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}	μs	
		Sub-clock oscillator operating	$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}		
		High-speed on-chip oscillator operating	$t_{SBYOSCWTHO}$	—	—	t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
		Low-speed on-chip oscillator operating	$t_{SBYOSCWTLO}$	—	—	t_{LOCO} + 1 / f_{ICLK}		
Time required for operations by the sequencer before release from software standby mode*2			t_{SBYSEQ}	—	—	9 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*3	Middle-speed operating mode 2	Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		Figure 2.24
		Sub-clock oscillator operating	t_{SBYSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
		High-speed on-chip oscillator operating	t_{SBYHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
		Low-speed on-chip oscillator operating	t_{SBYLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entry to software standby mode, the oscillation stabilization wait time will be selected as the largest value among those for the operating oscillators.

Note 2. For n, the largest value is selected from among the internal clock division settings.

Note 3. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

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Table 2.42 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time	Low-speed operating mode	Sub-clock oscillator operating	$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}	μs	
Time required for operations by the sequencer before release from software standby mode*1			t_{SBYSEQ}	—	—	9 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*2	Low-speed operating mode	Sub-clock oscillator operating	t_{SBYSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		Figure 2.24

Note 1. For n, the largest value is selected from among the internal clock division settings.

Note 2. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

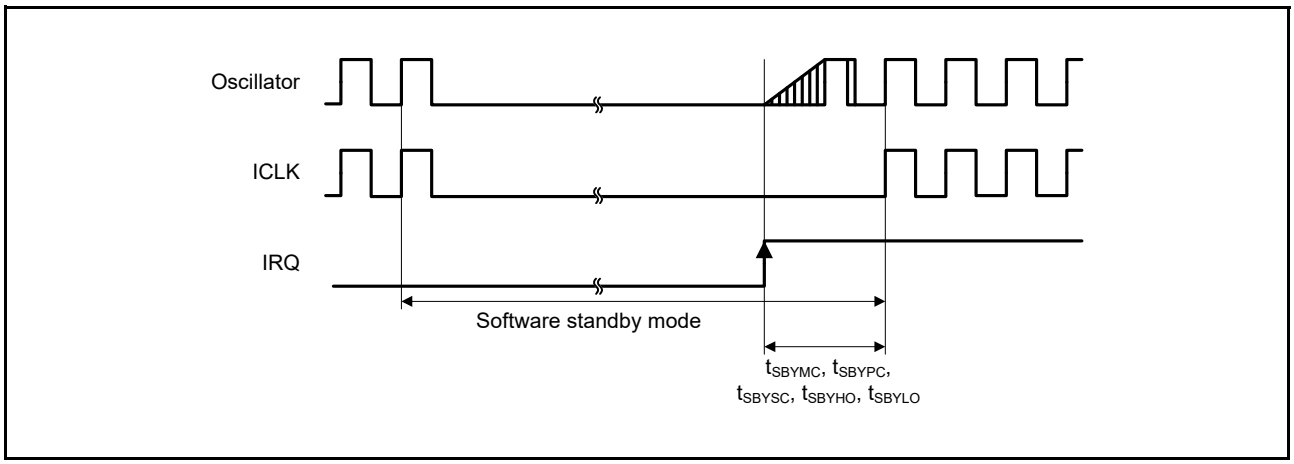

Figure 2.24 Software Standby Mode Recovery Timing

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Table 2.43 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time*1	Main clock oscillator operating	Main clock oscillator operating	$t_{SBYOSCWTMC}$	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 1 / f_{ICLK}	μs	
		Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}		
	Sub-clock oscillator operating		$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}		
	High-speed on-chip oscillator operating		$t_{SBYOSCWTHO}$	—	—	t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
	Low-speed on-chip oscillator operating		$t_{SBYOSCWTLO}$	—	—	t_{LOCO} + 1 / f_{ICLK}		
Time required for operations by the sequencer before release from software standby mode*2			t_{SBYSEQ}	—	—	3 / f_{ICLK} + 2n / $f_{source\ clock}$		
Time to shift to the snooze mode from the software standby mode*3	Main clock oscillator operating	Main clock oscillator operating	t_{SNZMC}	—	—	$t_{SBYOSCWTMC}$ + t_{SBYSEQ}		Figure 2.25
		Main clock oscillator and PLL circuit operating	t_{SNZPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		
	Sub-clock oscillator operating		t_{SNZSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
	High-speed on-chip oscillator operating		t_{SNZHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
	Low-speed on-chip oscillator operating		t_{SNZLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entry to software standby mode, the oscillation stabilization wait time will be selected as the largest value among those for the operating oscillators.

Note 2. For n, the largest value is selected from among the internal clock division settings.

Note 3. The time to shift to the snooze mode from the software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

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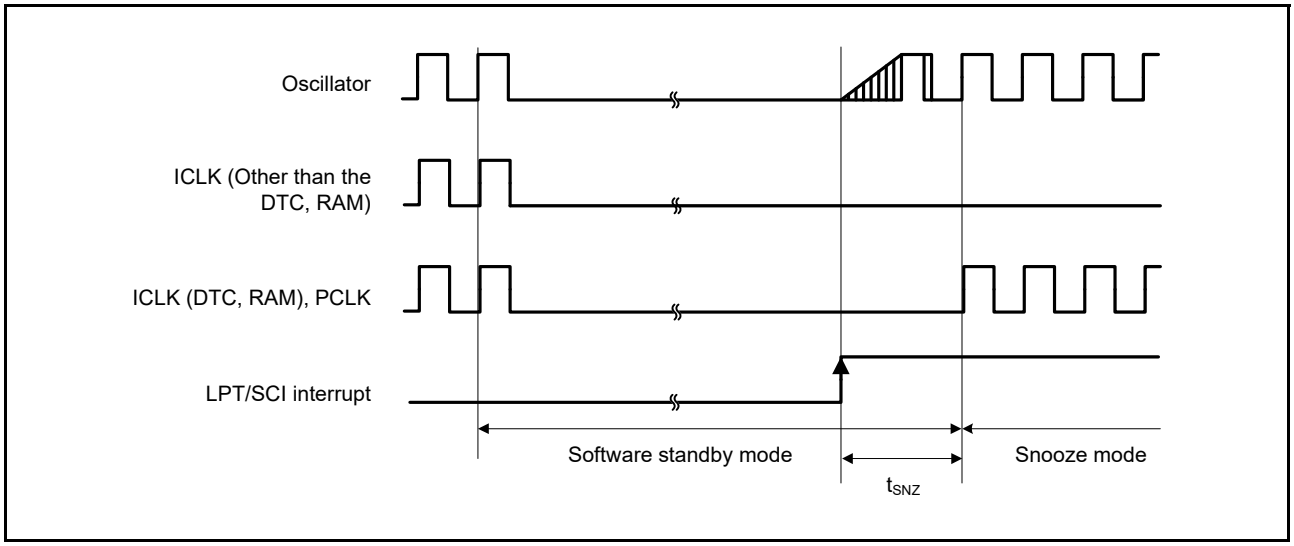

Figure 2.25 Timing to shift to the Snooze Mode from the Software Standby Mode

Table 2.44 Timing of Recovery from Low Power Consumption Modes (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.*2	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed operating mode	t_{DSLP}	—	—	$4 / f_{LOCO} + 8 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$	μs	Figure 2.26
	Middle-speed operating mode				$4 / f_{LOCO} + 8 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$		
	Middle-speed operating mode 2				$6 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$		
	Low-speed operating mode				$6 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$		

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. For n, the largest value is selected from among the internal clock division settings.

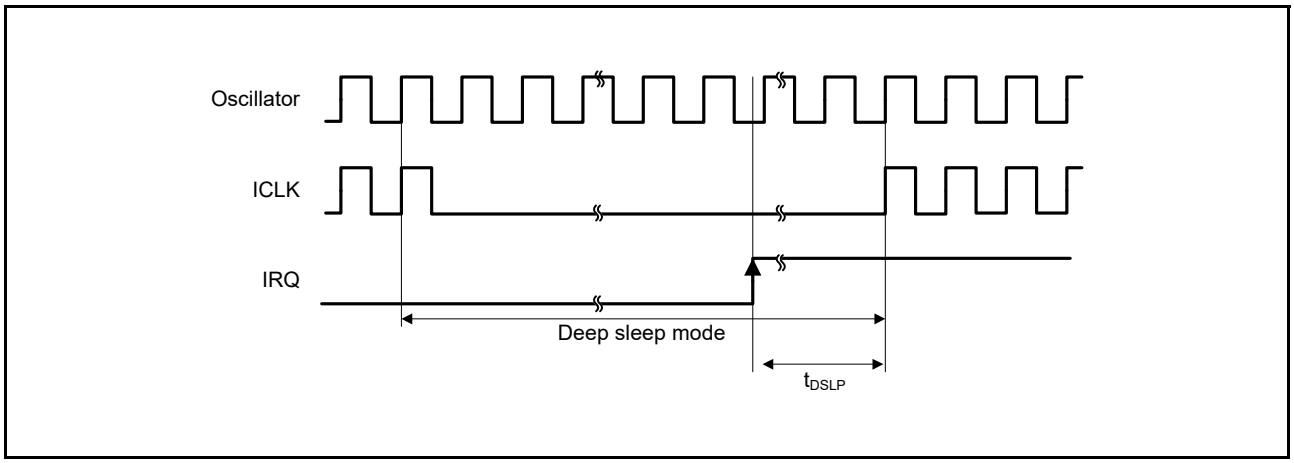

Figure 2.26 Deep Sleep Mode Recovery Timing

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Table 2.45 Operating Mode Transition Time

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating mode	24 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	μs
	Middle-speed operating mode 2	1 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	
	Low-speed operating mode	32.768 kHz	—	3 / f_{ICLK} + 2 / f_{FCLK}	—	
Middle-speed operating mode	High-speed operating mode	24 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	
	Middle-speed operating mode 2	1 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	
	Low-speed operating mode	32.768 kHz	—	3 / f_{ICLK} + 2 / f_{FCLK}	—	
Middle-speed operating mode 2	High-speed operating mode	1 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	
	Middle-speed operating mode	1 MHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	
	Low-speed operating mode	32.768 kHz	—	3 / f_{ICLK} + 2 / f_{FCLK}	—	
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	5 / f_{ICLK} + 3 / f_{FCLK}	—	
	Middle-speed operating mode	32.768 kHz	—	3 / f_{ICLK} + 3 / f_{FCLK}	—	
	Middle-speed operating mode 2	32.768 kHz	—	3 / f_{ICLK} + 3 / f_{FCLK}	—	

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2.5.4 Control Signal Timing

Table 2.46 Control Signal Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

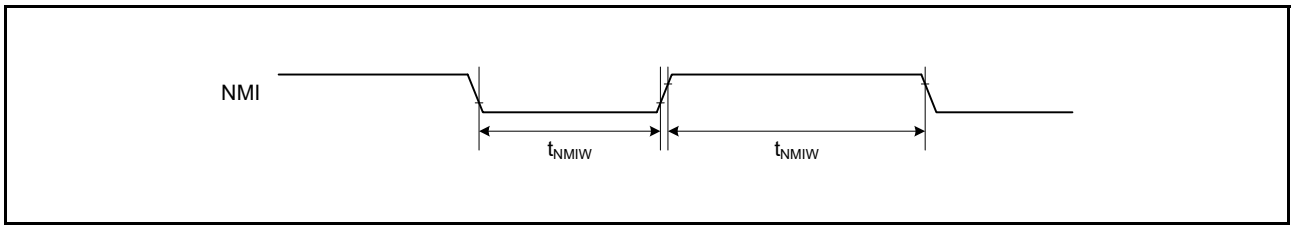

Figure 2.27 NMI Interrupt Input Timing

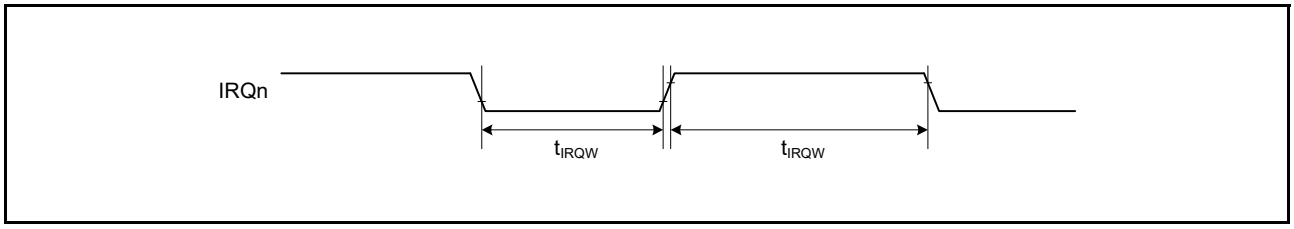

Figure 2.28 IRQ Interrupt Input Timing

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2.5.5 Timing of On-Chip Peripheral Modules

2.5.5.1 I/O Port Input Timing

Table 2.47 I/O Port Input Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{Pcyc}	Figure 2.29

Note 1. t_{Pcyc}: PCLK cycle

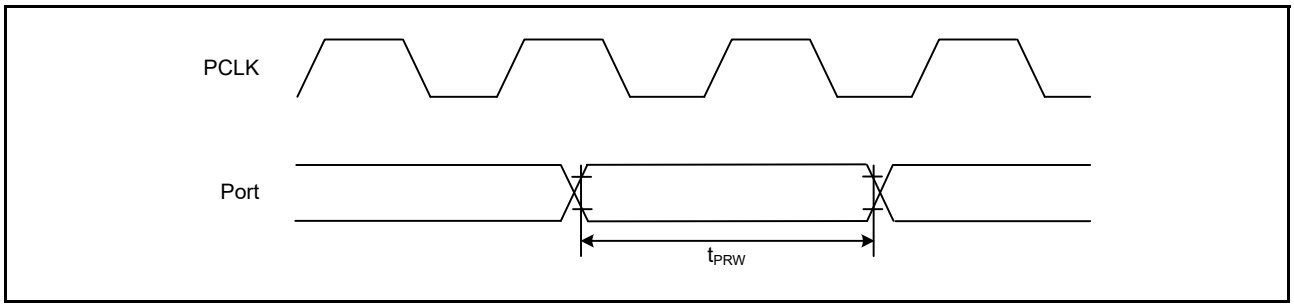

Figure 2.29 I/O Port Input Timing

2.5.5.2 MTU2

Table 2.48 MTU2 Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
MTU2	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 2.30
		Both-edge setting		2.5	—		
	Input capture input rise/fall time		t_{TICr}, t_{TICf}	—	0.1	μs/V	
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 2.31
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
	Timer clock rise/fall time		t_{TCKr}, t_{TCKf}	—	0.1	μs/V	

Note 1. t_{Pcyc}: PCLK cycle

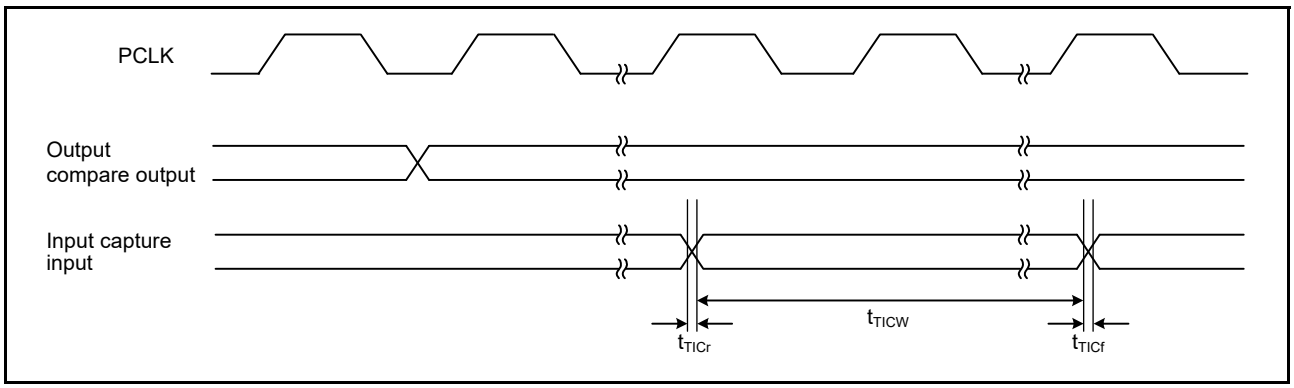

Figure 2.30 MTU2 Input/Output Timing

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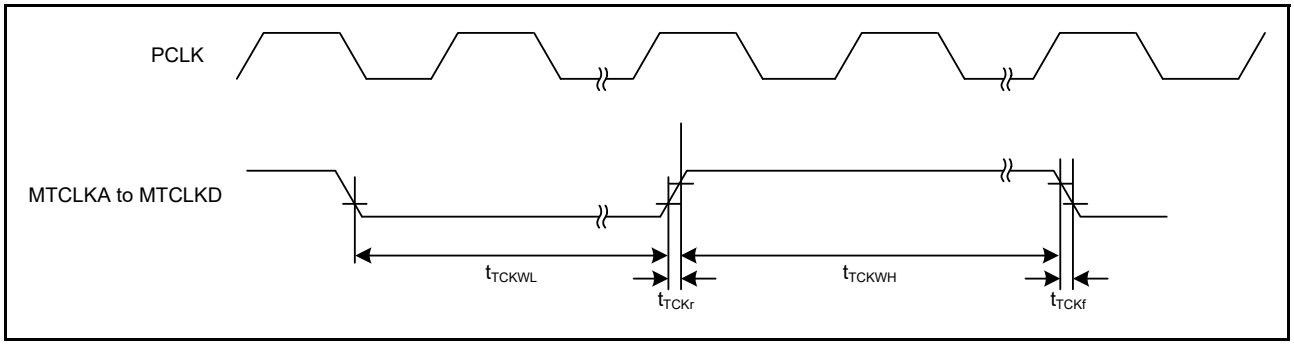

Figure 2.31 MTU2 Clock Input Timing

2.5.5.3 POE2

Table 2.49 POE2 Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
POE2	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 2.32
	POE# input rise/fall time		t_{POEr}, t_{POEf}	—	0.1	μs/V	
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	$5t_{Pcyc}$ + 0.24	μs	Figure 2.33 When detecting falling edges (ICSRm.POEnM[3:0] = 0000 (m =1, 2; n = 0, 1, 2,3,8))
		Simultaneous conduction of output pins	t_{POEDO}	—	$3t_{Pcyc}$ + 0.2		Figure 2.34
		Register setting	t_{POEDS}	—	$1t_{Pcyc}$ + 0.2		Figure 2.35 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	21		Figure 2.36

Note 1. t_{Pcyc}: PCLK cycle

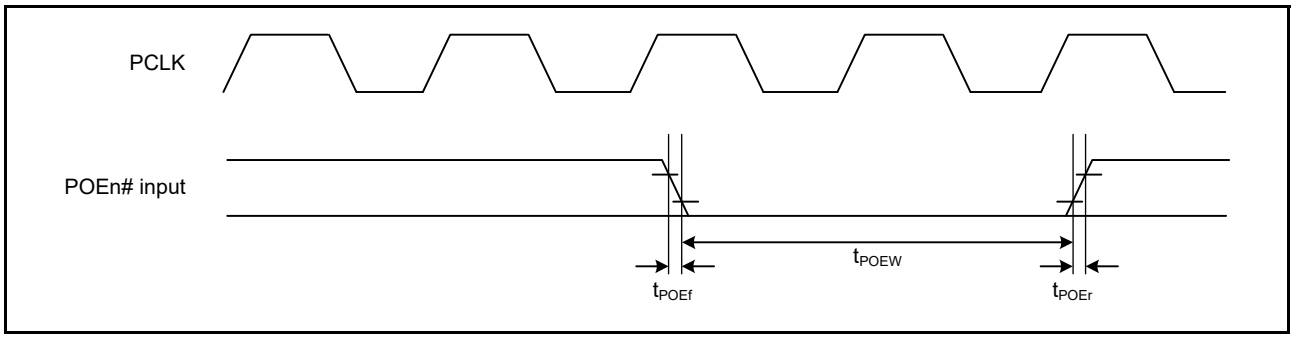

Figure 2.32 POE# Input Timing

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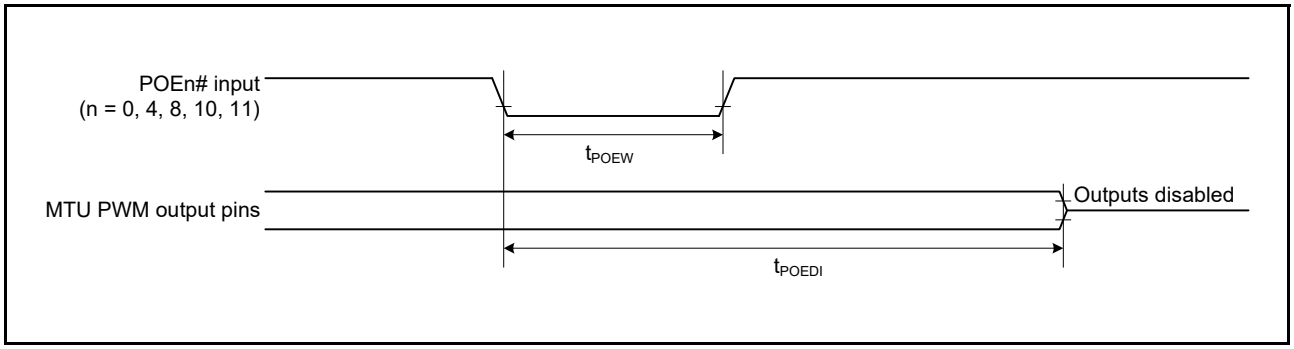

Figure 2.33 Output Disable Time for POE in Response to Transition of the POEn# Signal Level

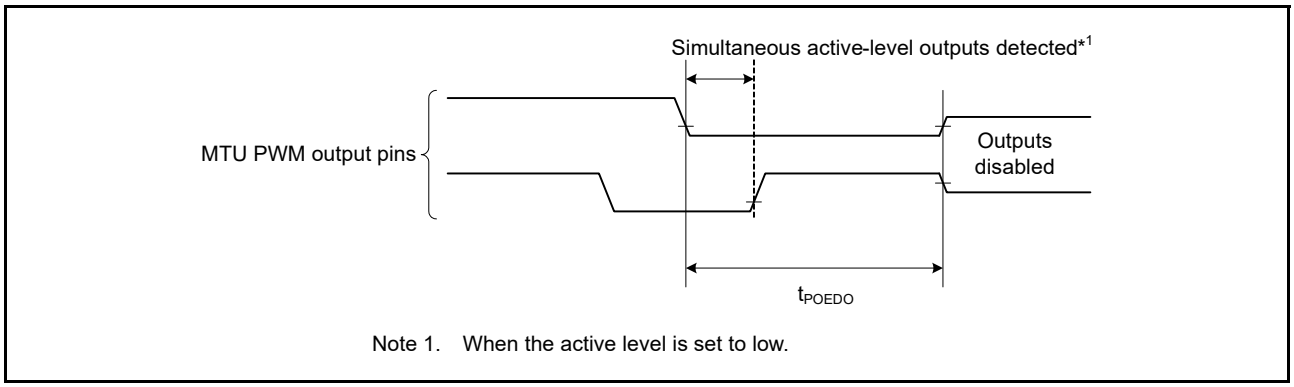

Figure 2.34 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

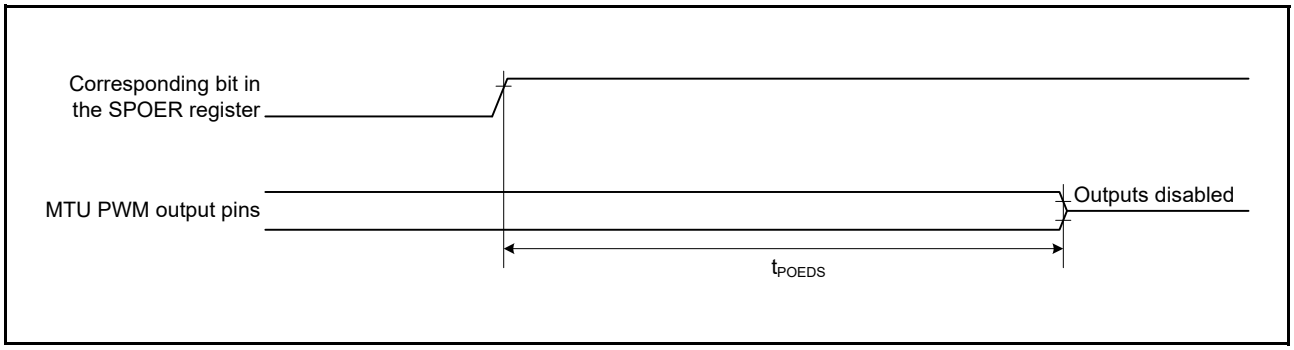

Figure 2.35 Output Disable Time for POE in Response to the Register Setting

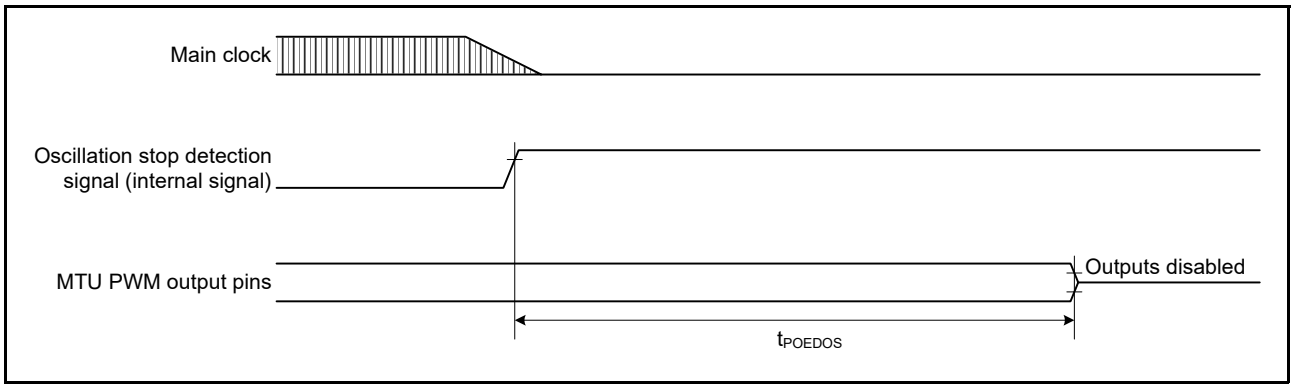

Figure 2.36 Output Disable Time for POE in Response to the Oscillation Stop Detection

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2.5.5.4 TMR

Table 2.50 TMR Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 2.37
		Both-edge setting		2.5	—		
	Timer clock rise/fall time		t_{TMCr}, t_{TMCf}	—	0.1	μs/V	

Note 1. t_{Pcyc}: PCLK cycle

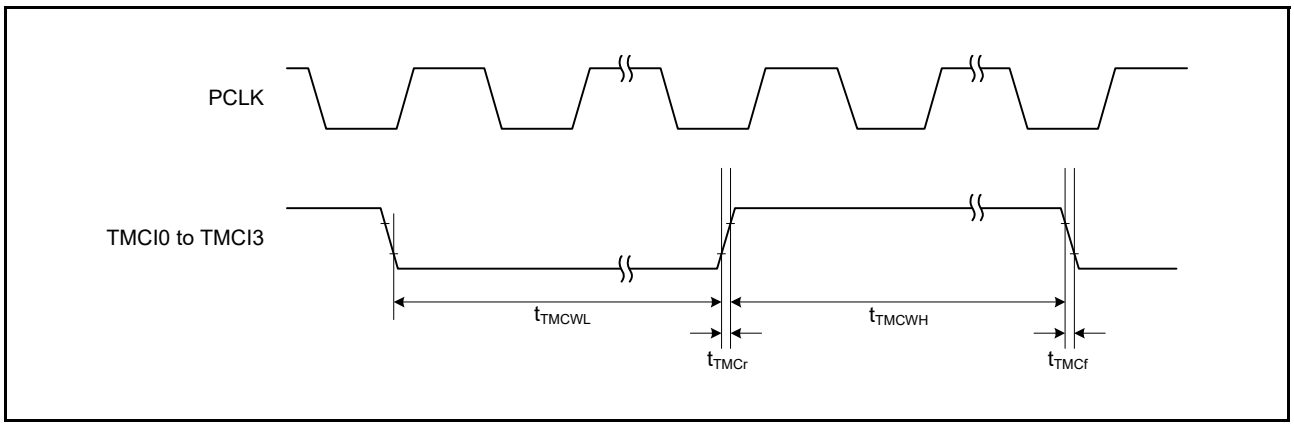

Figure 2.37 TMR Clock Input Timing

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2.5.5.5 SCI

Table 2.51 SCI Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF

Item					Symbol	Min.	Max.	Unit *1	Test Conditions
SCI (channel 1, 5)	Input clock cycle time			Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.38
				Clock synchronous		6	—		
	Input clock pulse width				t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time				t_{SCKr}	—	20	ns	
	Input clock fall time				t_{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous			t_{Scyc}	6	—	t_{Pcyc}	Figure 2.39
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V			4	—		
			1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		8	—		
				PCLKB ≤ 24 MHz		4	—		
	Output clock pulse width				t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time				t_{SCKr}	—	20	ns	
	Output clock fall time				t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous			t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous		2.7 V or above		—	55	ns	
				2.4 V or above		—	60	ns	
				1.8 V or above		—	100	ns	
	Receive data setup time (master)	Clock synchronous		2.7 V or above	t_{RXS}	45	—	ns	
				2.4 V or above		55	—	ns	
				1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchronous				40	—	ns	
	Receive data hold time	Clock synchronous			t_{RXH}	40	—	ns	
SCI (channel 6,8,9,12)	Input clock cycle time			Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.38
				Clock synchronous		6	—		
	Input clock pulse width				t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time				t_{SCKr}	—	20	ns	
	Input clock fall time				t_{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous			t_{Scyc}	8	—	t_{Pcyc}	Figure 2.39
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V			4	—		
			1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		8	—		
				PCLKB ≤ 24 MHz		4	—		
	Output clock pulse width				t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time				t_{SCKr}	—	20	ns	
	Output clock fall time				t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous			t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous		2.7 V or above		—	65	ns	
				1.8 V or above		—	100	ns	
	Receive data setup time (master)	Clock synchronous		2.7 V or above	t_{RXS}	65	—	ns	
				1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchronous				40	—	ns	
	Receive data hold time	Clock synchronous			t_{RXH}	40	—	ns	

Note 1. t_{Pcyc}: PCLK cycle

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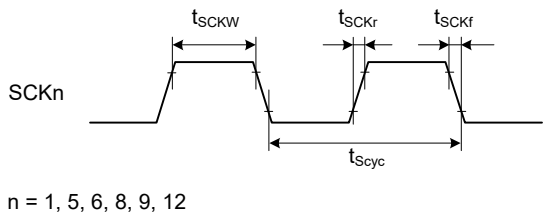

Figure 2.38 SCK Clock Input Timing

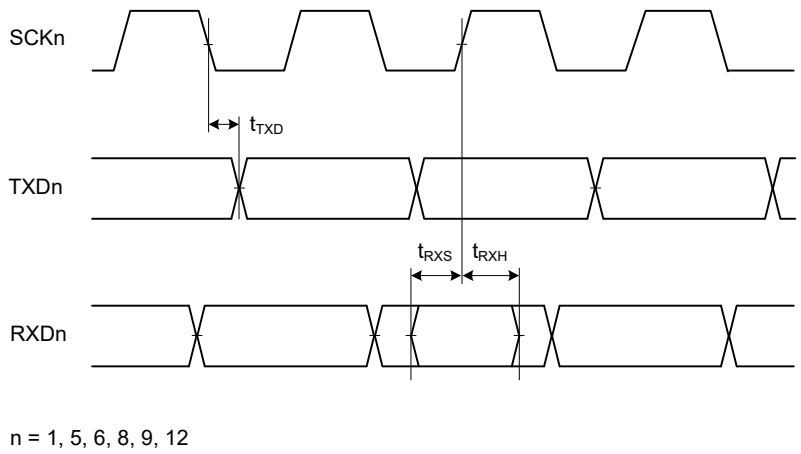

Figure 2.39 SCI Input/Output Timing: Clock Synchronous Mode

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Table 2.52 Simple I²C Timing

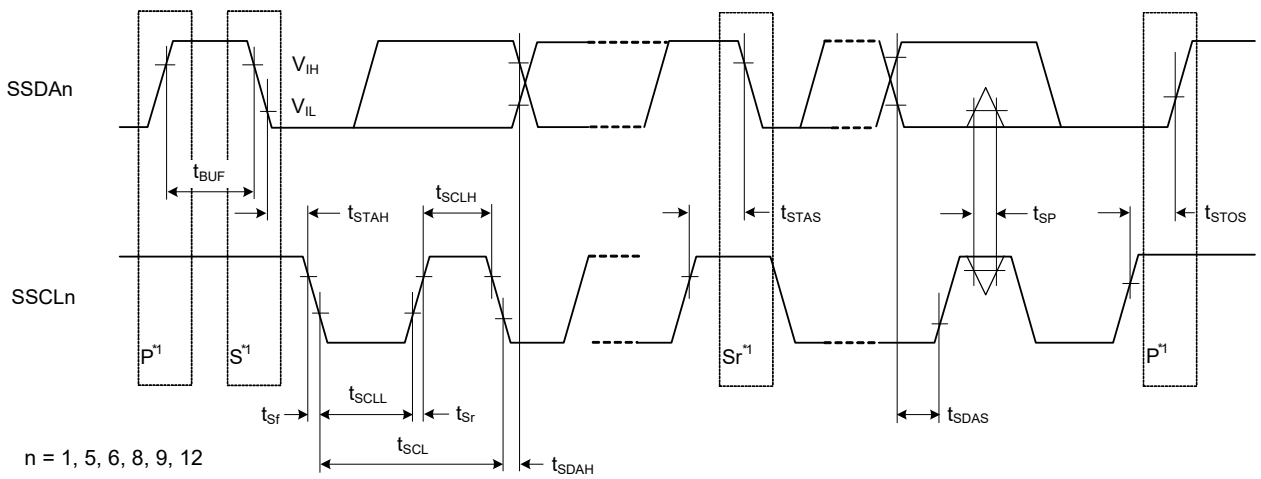
Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I²C (standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 2.40
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple I²C (fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 2.40
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{Pcyc}: PCLK cycle

Note 1. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.40 Output Timing and Simple I²C Bus Interface Input/Output Timing

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Table 2.53 Simple SPI Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	2.4 V ≤ VCC ≤ 5.5 V		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.41
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		8	65536		
			PCLKB ≤ 24 MHz		4	65536		
	SCK clock cycle input (slave)				6	—	t_{Pcyc}	
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time			t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)		2.7 V or above	t_{SU}	45	—	ns	Figure 2.42, Figure 2.43
			2.4 V or above		55	—		
			1.8 V or above		80	—		
	Data input setup time (slave)				40	—		
	Data input hold time			t_H	40	—	ns	
	SSL input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SSL input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time (master)			t_{OD}	—	40	ns	
	Data output delay time (slave)		2.7 V or above		—	65		
			1.8 V or above		—	100		
	Data output hold time (master)		2.7 V or above	t_{OH}	–10	—	ns	
			1.8 V or above		–20	—		
	Data output hold time (slave)				–10	—		
	Data rise/fall time			t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time			t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 2.44, Figure 2.45
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		—	7		
			PCLKB ≤ 24 MHz		—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		—	7		
			PCLKB ≤ 24 MHz		—	6		

Note 1. t_{Pcyc}: PCLK cycle

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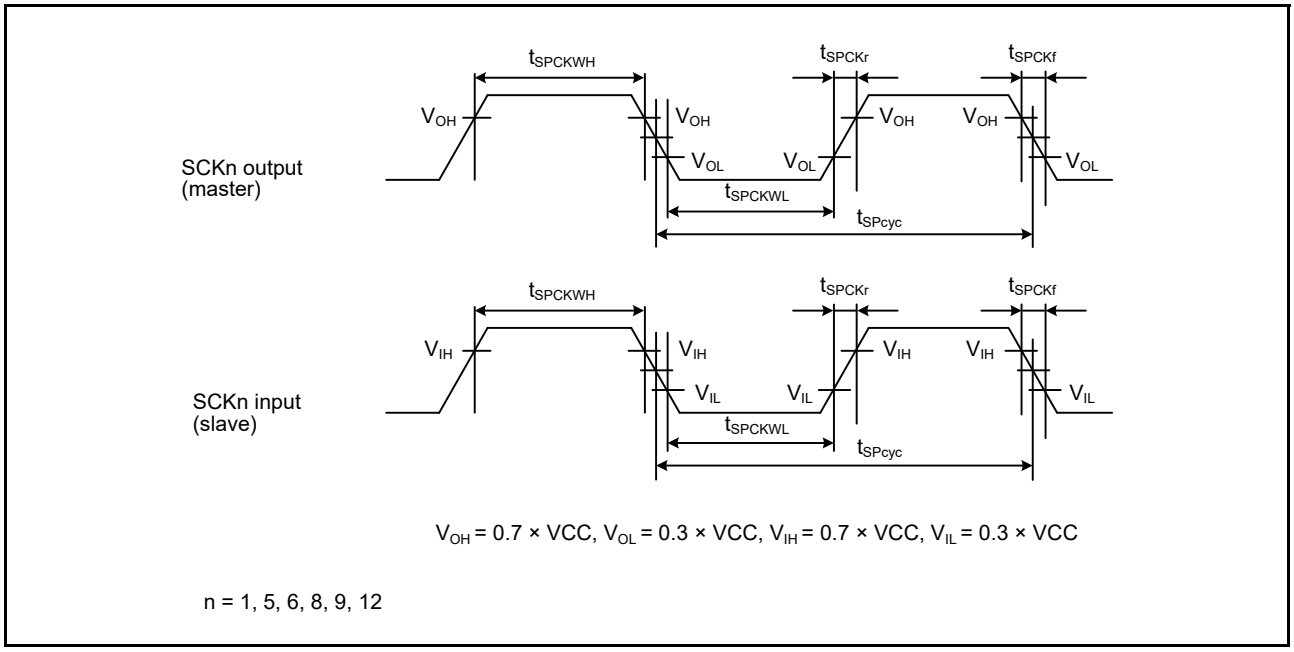

Figure 2.41 Simple SPI Clock Timing

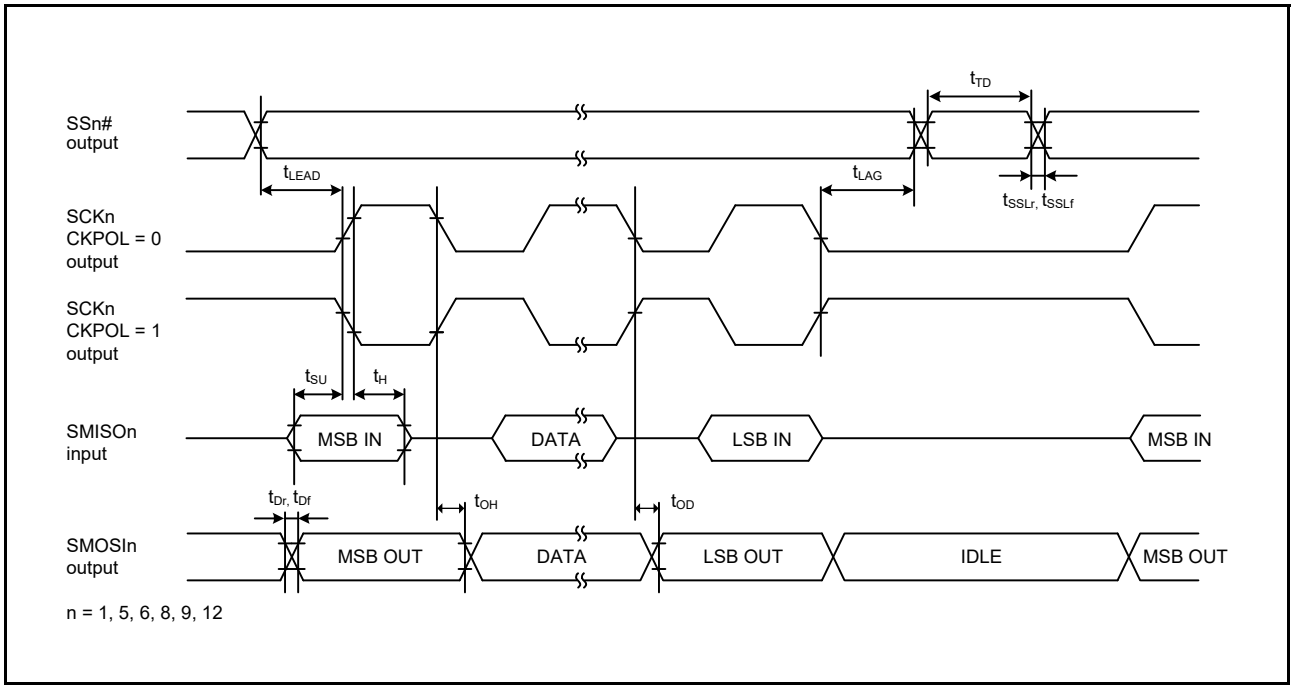

Figure 2.42 Simple SPI Clock Timing (Master, CKPH = 1)

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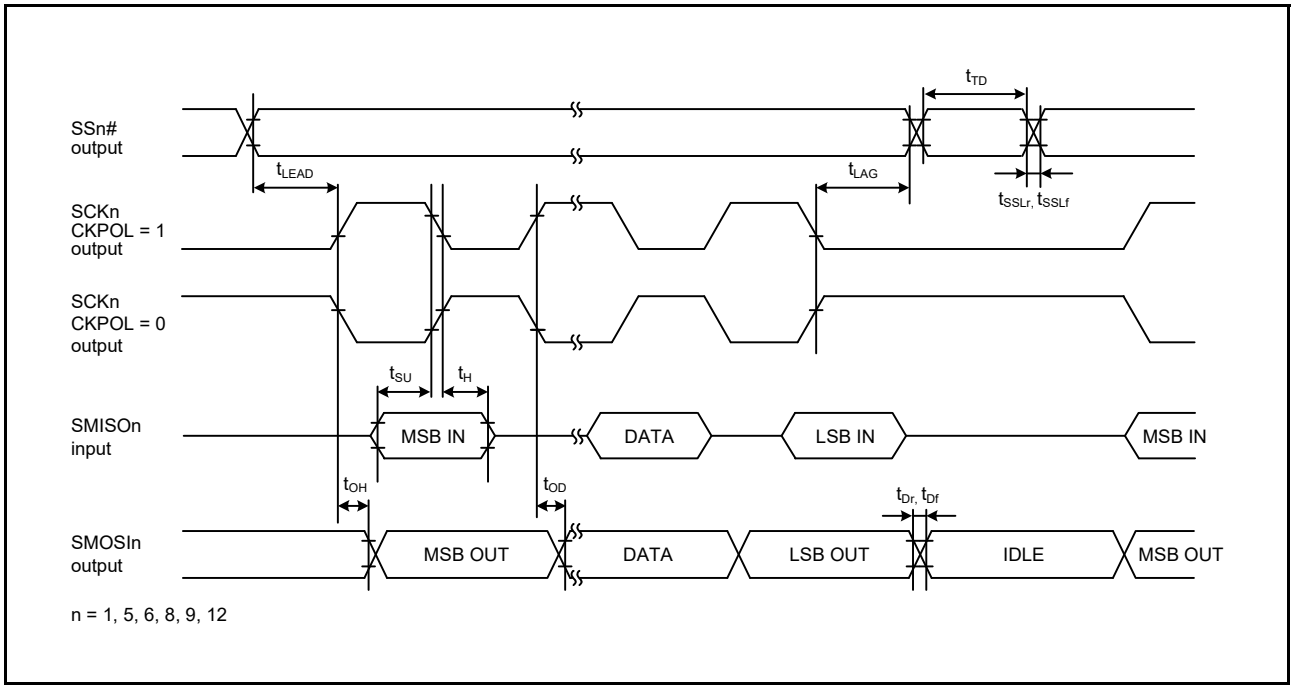

Figure 2.43 Simple SPI Clock Timing (Master, CKPH = 0)

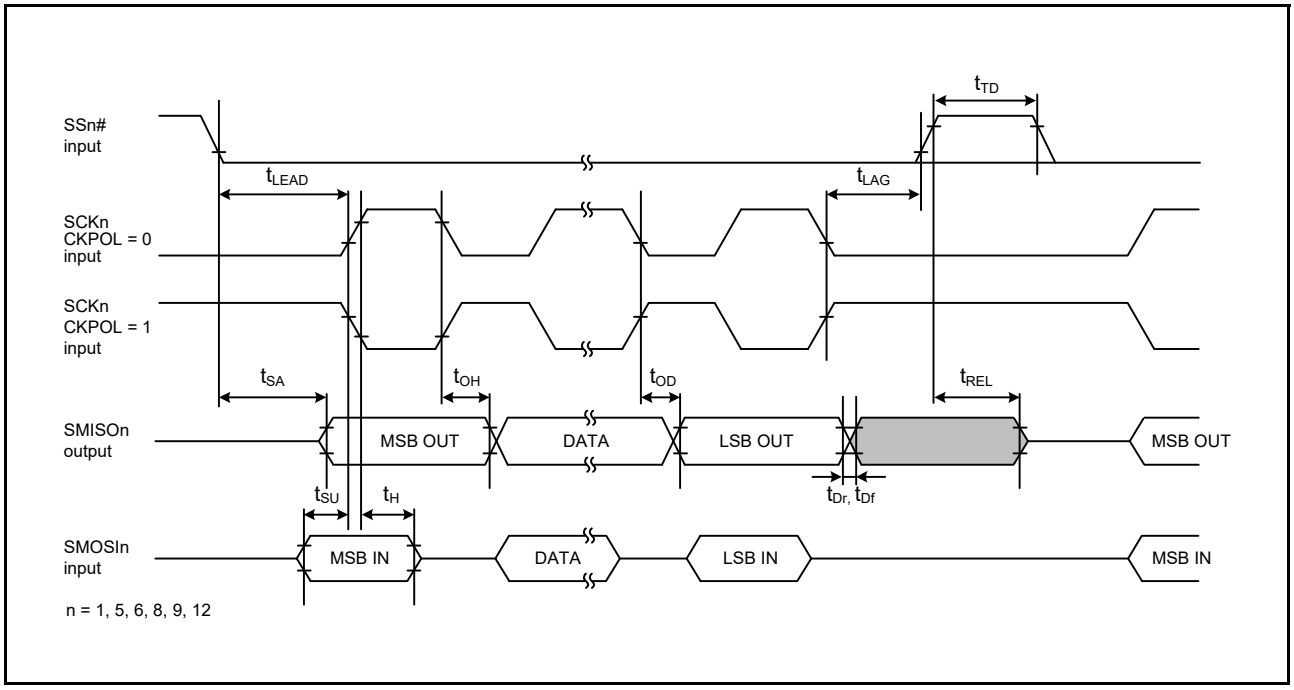

Figure 2.44 Simple SPI Clock Timing (Slave, CKPH = 1)

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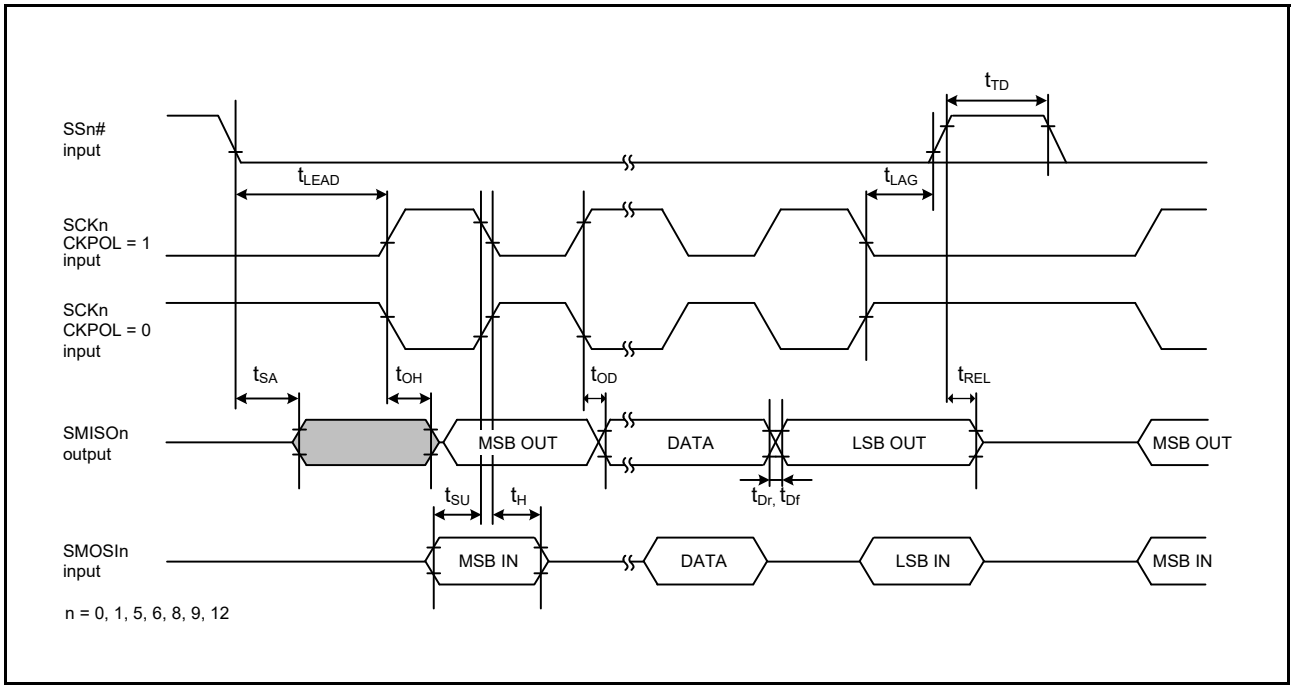

Figure 2.45 Simple SPI Clock Timing (Slave, CKPH = 0)

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2.5.5.6 RIIC

Table 2.54 RIIC Timing

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.46
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.46
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

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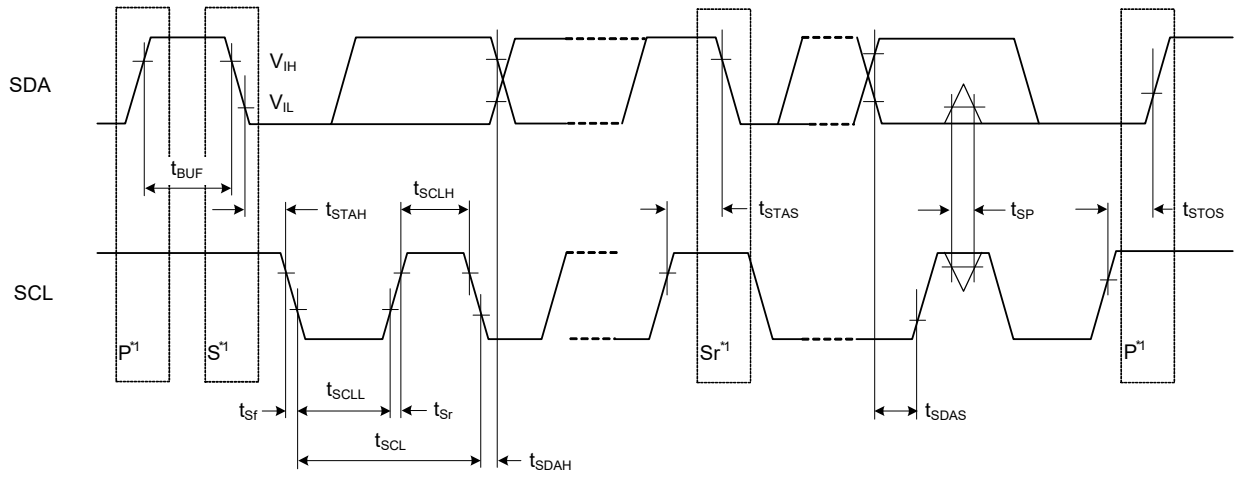

Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.46 RIIC Bus Interface Input/Output Timing

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2.5.5.7 RSPI

Table 2.55 RSPI Timing (1/2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 2.47
		Slave			4	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave			(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave			(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2	—		
	RSPCK clock rise/ fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V or above		—	15		
			1.8 V or above		—	20		
		Input			—	0.1	μs/V	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 2.48 to Figure 2.51
			1.8 V or above		30	—		
		Slave	2.7 V or above		10	—		
			1.8 V or above		15	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	20	—		
	SSL setup time	Master		t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			2.4 V or above		—	20		
			1.8 V or above		—	25		
		Slave	2.7 V or above		—	50		
			2.4 V or above		—	60		
			1.8 V or above		—	85		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			6 × t_{Pcyc}	—		
	MOSI and MISO rise/ fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			2.4 V or above		—	15		
			1.8 V or above		—	20		
		Input			—	1	μs	

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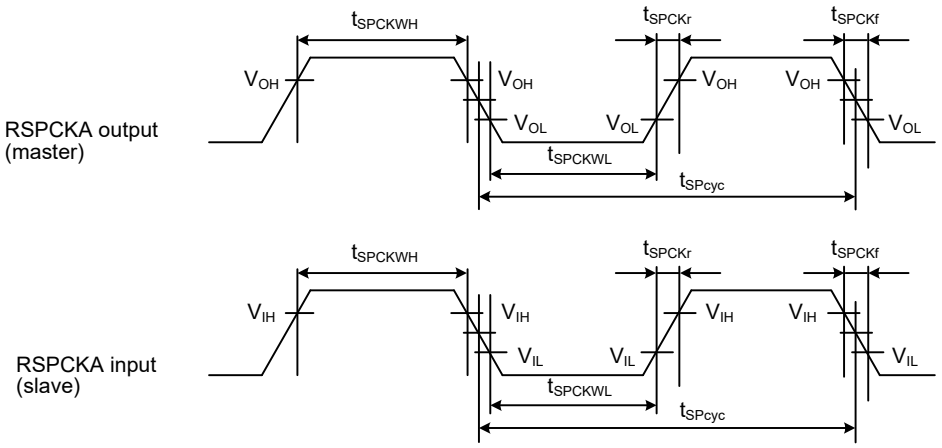
Table 2.55 RSPI Timing (2/2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	SSL rise/fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	—	10	ns	Figure 2.48 to Figure 2.51
			2.4 V or above		—	15	ns	
			1.8 V or above		—	20	ns	
		Input			—	1	μs	
	Slave access time		2.4 V or above	t_{SA}	—	2 × t_{Pcyc} + 100	ns	Figure 2.50, Figure 2.51
			1.8 V or above		—	2 × t_{Pcyc} + 140	ns	
	Slave output release time		2.4 V or above	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V or above		—	2 × t_{Pcyc} + 140	ns	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.47 RSPI Clock Timing

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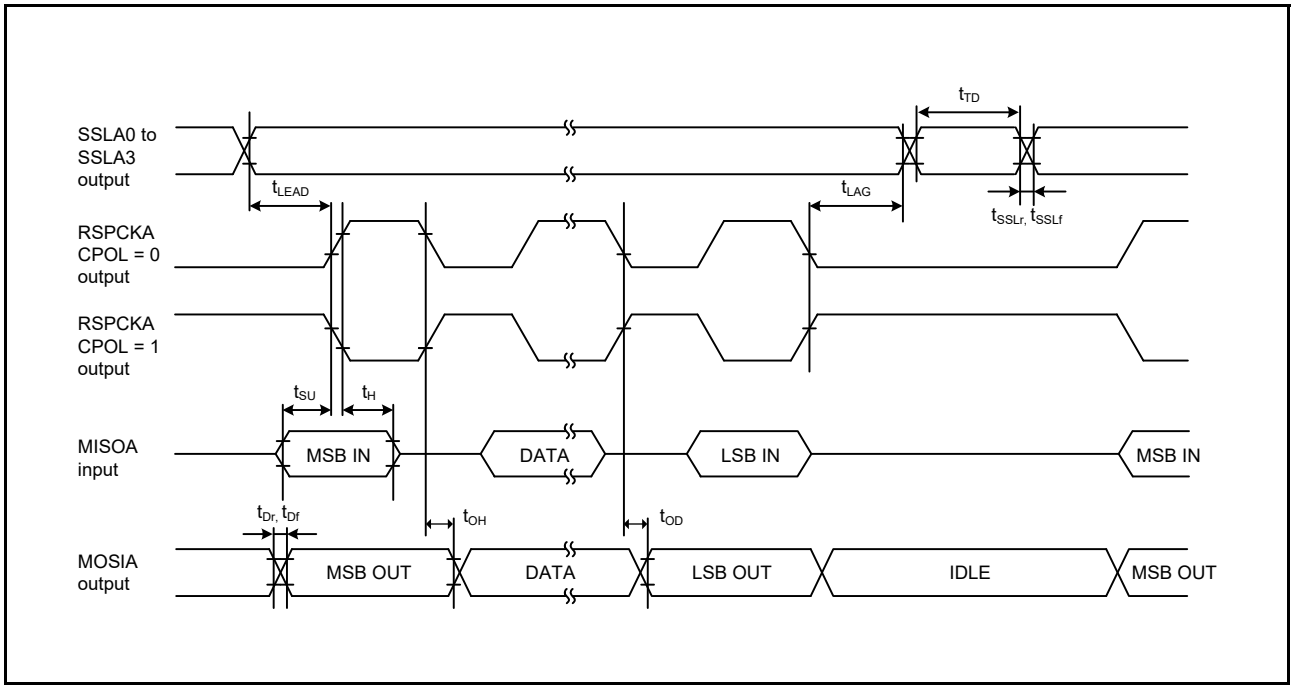

Figure 2.48 RSPI Timing (Master, CPHA = 0)

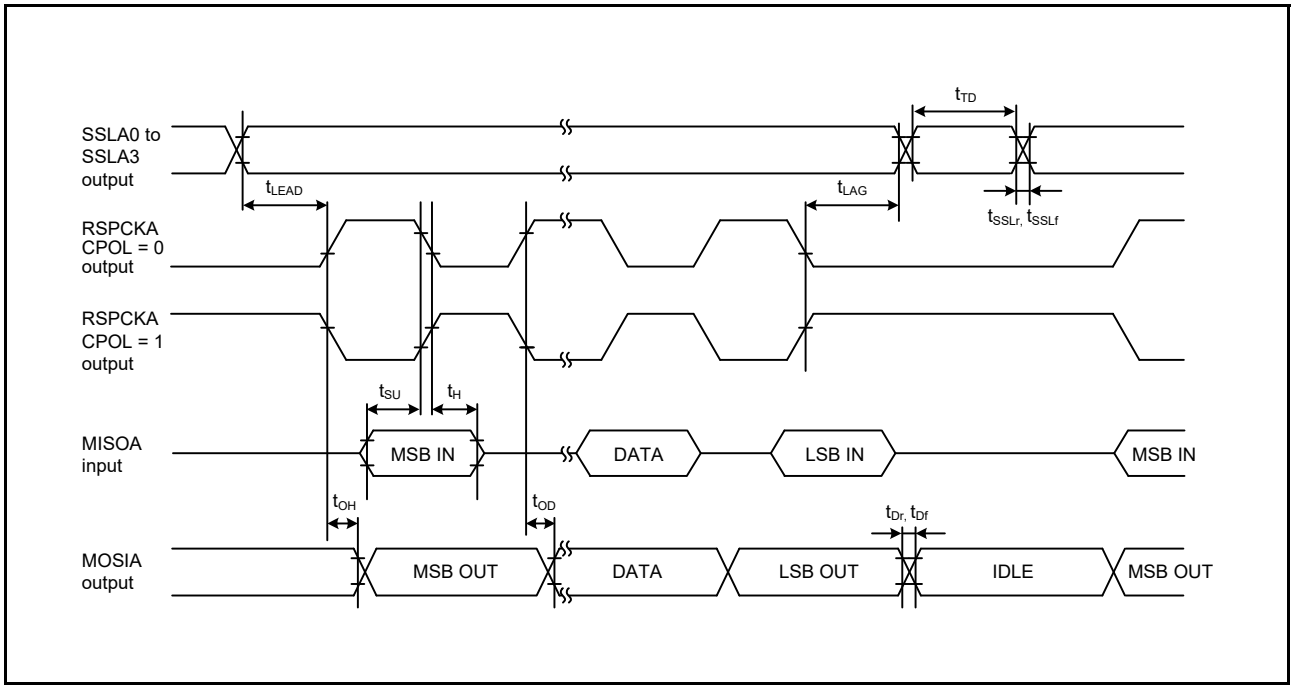

Figure 2.49 RSPI Timing (Master, CPHA = 1)

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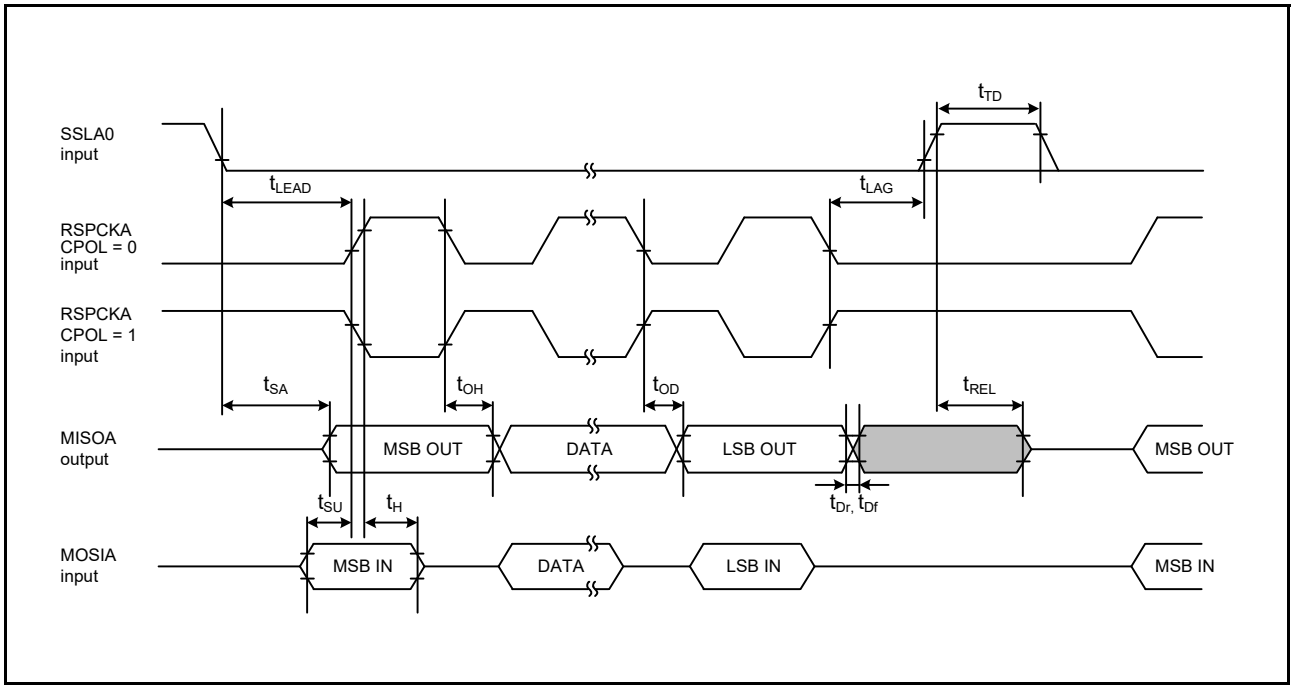

Figure 2.50 RSPI Timing (Slave, CPHA = 0)

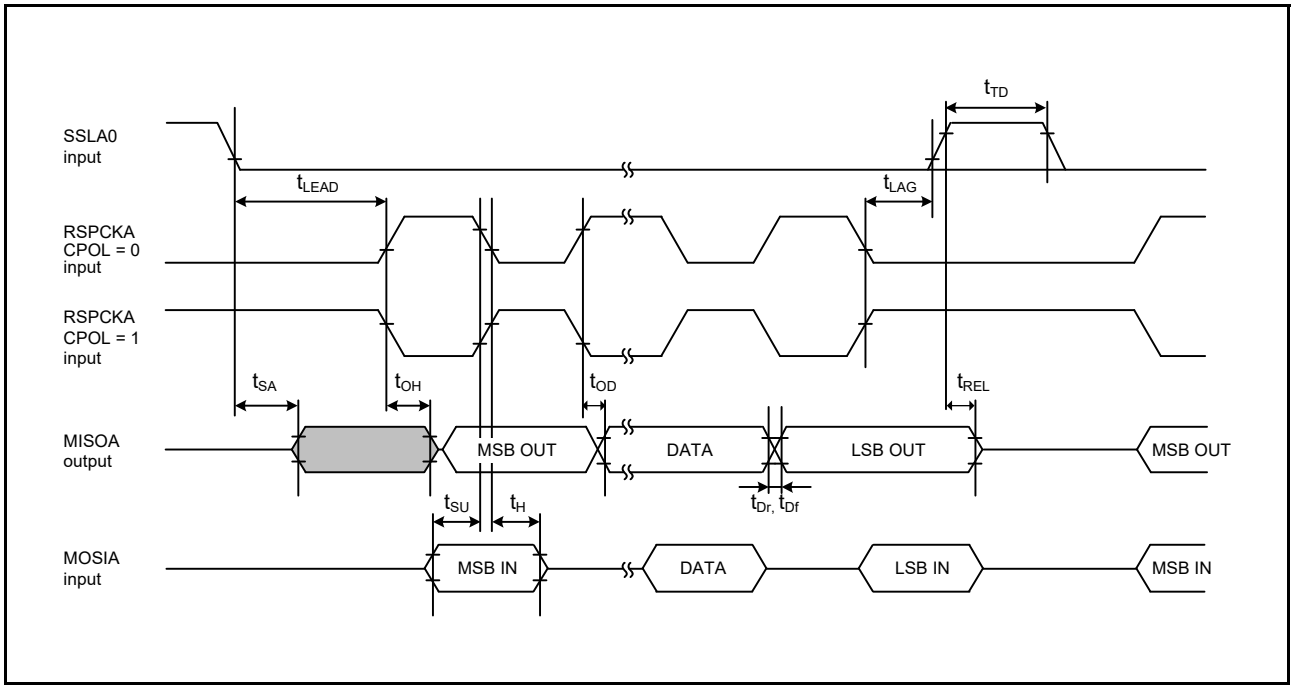

Figure 2.51 RSPI Timing (Slave, CPHA = 1)

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2.5.5.8 A/D Converter Trigger

Table 2.56 A/D Converter Trigger Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
A/D converter	Trigger input pulse width	t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.52

Note 1. t_{Pcyc}: PCLK cycle

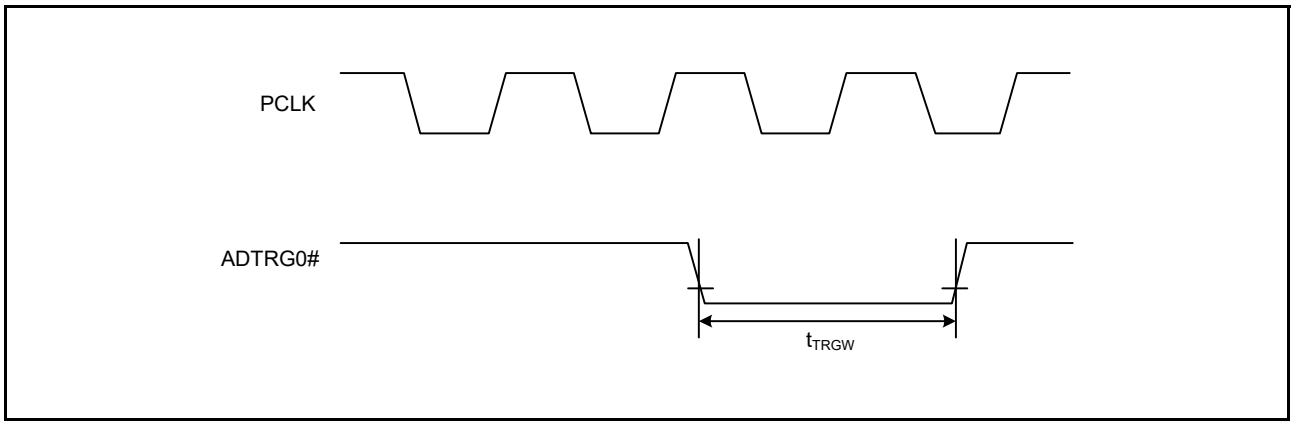

Figure 2.52 A/D Converter External Trigger Input Timing

2.5.5.9 CAC

Table 2.57 CAC Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			
	CACREF input rise/fall time		$t_{CACREFr}$, $t_{CACREFf}$	—	0.1	μs/V	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle

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2.5.5.10 CLKOUT

Table 2.58 CLKOUT Timing

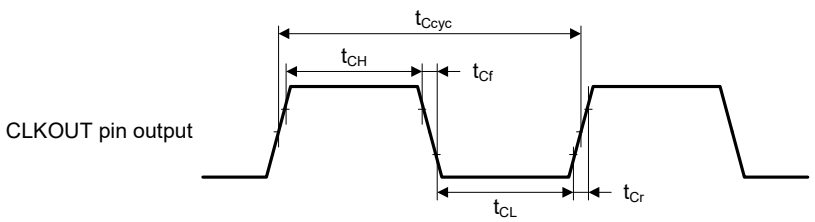
Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
CLKOUT	CLKOUT pin output cycle*2	VCC = 2.7 V or above	t_{Ccyc}	62.5	—	ns	Figure 2.53
		VCC = 1.8 V or above		125			
	CLKOUT pin high pulse width*1	VCC = 2.7 V or above	t_{CH}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin low pulse width*1	VCC = 2.7 V or above	t_{CL}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	—	12	ns	
		VCC = 1.8 V or above			25		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	—	12	ns	
		VCC = 1.8 V or above			25		

Note 1. When the LOCO is selected as the clock output source (CKOCR.CKOSEL[3:0] bits = 0000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).

Note 2. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSEL[3:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.



Test conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.53 CLKOUT Output Timing

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2.6 A/D Conversion Characteristics

Table 2.59 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ VREFH0 = AVCC0 ≤ 5.5 V*1, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, signal source impedance = 0.3 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	48	MHz	
Resolution		—	—	12	Bit	
Conversion time*2 (operation at PCLKD = 48 MHz)		0.67 (0.208)*3	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Ah ADCCR.CCS = 1
		1.29 (0.833)*3	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*4	pF	High-precision channel
		—	—	10*4		Normal-precision channel
Analog input resistance	Rs	—	—	1.9*4	kΩ	High-precision channel
		—	—	6.0*4		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. For 32-pin products, VREFH0 = AVCC0.

Note 2. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 3. The values in ( ) show the sampling times.

Note 4. The values are reference values.

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Table 2.60 A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ VREFH0 = AVCC0 ≤ 5.5 V*1, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, signal source impedance = 1.3 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*2 (Operation at PCLKD = 32 MHz)		1.00 (0.313)*3	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Ah ADCCR.CCS = 1
		1.94 (1.250)*3	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*4	pF	High-precision channel
		—	—	10*4		Normal-precision channel
Analog input resistance	Rs	—	—	2.2*4	kΩ	High-precision channel
		—	—	7.0*4		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. For 32-pin products, VREFH0 = AVCC0.

Note 2. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 3. The values in ( ) show the sampling times.

Note 4. The values are reference values.

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Table 2.61 A/D Conversion Characteristics (3)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ VREFH0 = AVCC0 ≤ 5.5 V*1, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, signal source impedance = 1.1 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	24	MHz	
Resolution		—	—	12	Bit	
Conversion time*2 (operation at PCLKD = 24 MHz)		1.58 (0.417)*3	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Ah ADCCR.CCS = 1
		2.00 (0.833)*3	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 14h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*4	pF	High-precision channel
		—	—	10*4		Normal-precision channel
Analog input resistance	Rs	—	—	1.9*4	kΩ	High-precision channel
		—	—	6*4		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.25	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. For 32-pin products, VREFH0 = AVCC0.

Note 2. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 3. The values in ( ) show the sampling times.

Note 4. The values are reference values.

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Table 2.62 A/D Conversion Characteristics (4)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ VREFH0 = AVCC0 ≤ 5.5 V*1, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, signal source impedance = 2.2 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*2 (operation at PCLKD = 16 MHz)		2.38 (0.625)*3	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Ah ADCCR.CCS = 1
		3.00 (1.250)*3	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 14h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*4	pF	High-precision channel
		—	—	10*4		Normal-precision channel
Analog input resistance	Rs	—	—	2.2*4	kΩ	High-precision channel
		—	—	7*4		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.25	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. or 32-pin products, VREFH0 = AVCC0.

Note 2. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 3. The values in ( ) show the sampling times.

Note 4. The values are reference values.

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Table 2.63 A/D Conversion Characteristics (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ VREFH0 = AVCC0 ≤ 5.5 V*1, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, signal source impedance = 5 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*2 (operation at PCLKD = 8 MHz)		4.75 (1.250)*3	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Ah ADCCR.CCS = 1
		6.00 (2.500)*3	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 14h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*4	pF	High-precision channel
		—	—	10*4		Normal-precision channel
Analog input resistance	Rs	—	—	6*4	kΩ	High-precision channel
		—	—	14*4		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	High-precision channel
				±11.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.25	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. For 32-pin products, VREFH0 = AVCC0.

Note 2. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 3. The values in ( ) show the sampling times.

Note 4. The values are reference values.

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Table 2.64 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 5.5 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN021, AN024 to AN026		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 1.8 to 5.5 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 1.8 to 5.5 V	
CTSU input channels	AN008	AVCC0 = 1.8 to 5.5V	

Table 2.65 A/D Internal Reference Voltage Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*1	1.42	1.48	1.54	V	

Note 1. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

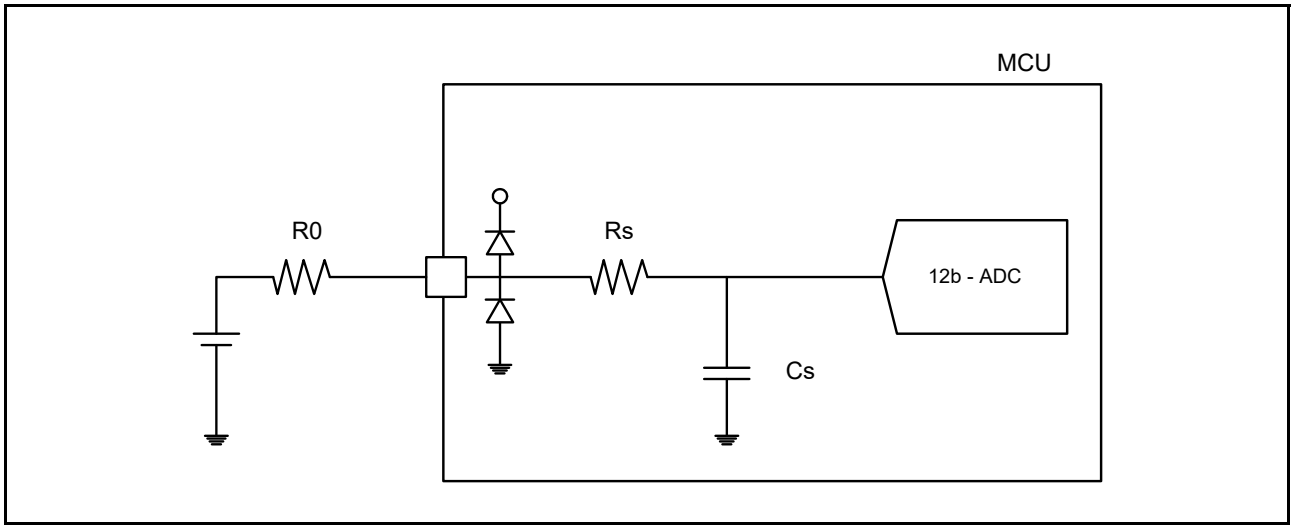

Figure 2.54 Equivalent Circuit

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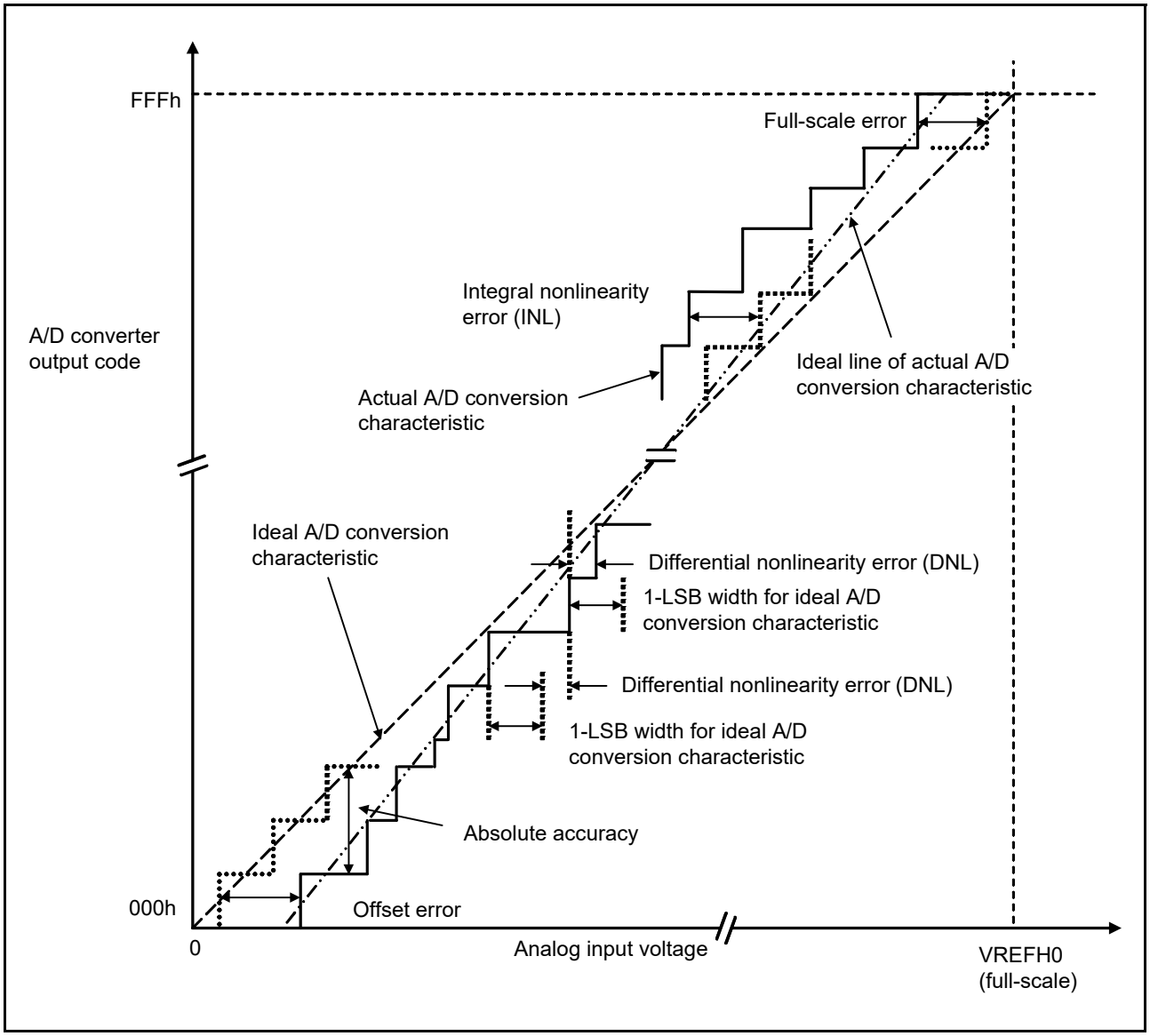

Figure 2.55 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, … are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

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Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

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2.7 D/A Conversion Characteristics

Table 2.66 D/A Conversion Characteristics (1)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	—	8	Bit	
Conversion time	VCC = 1.8 to 5.5 V	t_{DCONV}	—	—	3.0	μs	35-pF capacitive load
Absolute accuracy	VCC = 2.4 to 5.5 V	—	—	—	±3.0	LSB	2-MΩ resistive load
	VCC = 1.8 to 2.4 V	—	—	—	±3.5		
	VCC = 2.4 to 5.5 V	—	—	—	±2.0	LSB	4-MΩ resistive load
	VCC = 1.8 to 2.4 V	—	—	—	±2.5		
RO output resistance		—	—	9.0	—	kΩ	

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2.8 Temperature Sensor Characteristics

Table 2.67 Temperature Sensor Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.3	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	μs	
Sampling time*1	—	5	—	—	μs	

Note 1. Set the S12AD.ADSSTRT register so that the sampling time of the 12-bit A/D converter meets this specification.

2.9 Comparator Characteristics

Table 2.68 Comparator Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB1 input reference voltage		VREF	0	—	VCC – 1.4	V	
CMPB0 to CMPB1 input voltage		VI	0	—	VCC	V	
Internal reference voltage		—	1.34	1.44	1.54	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	μs	VCC = 3 V, input slew rate ≥ 50 mV/μs
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	μs	
	Comparator low-speed mode	Td	—	—	9.0	μs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 × VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 × VCC	—	V	
Operation stabilization wait time		Tcmp	100	—	—	μs	

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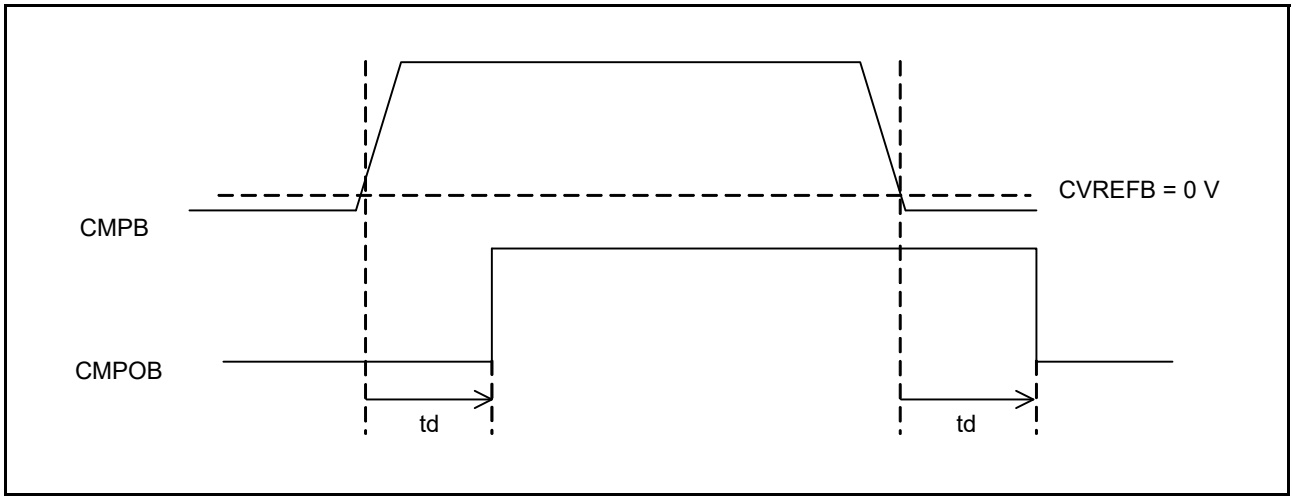

Figure 2.56 Comparator Output Delay Time in Comparator High-Speed Mode and Low-Speed Mode

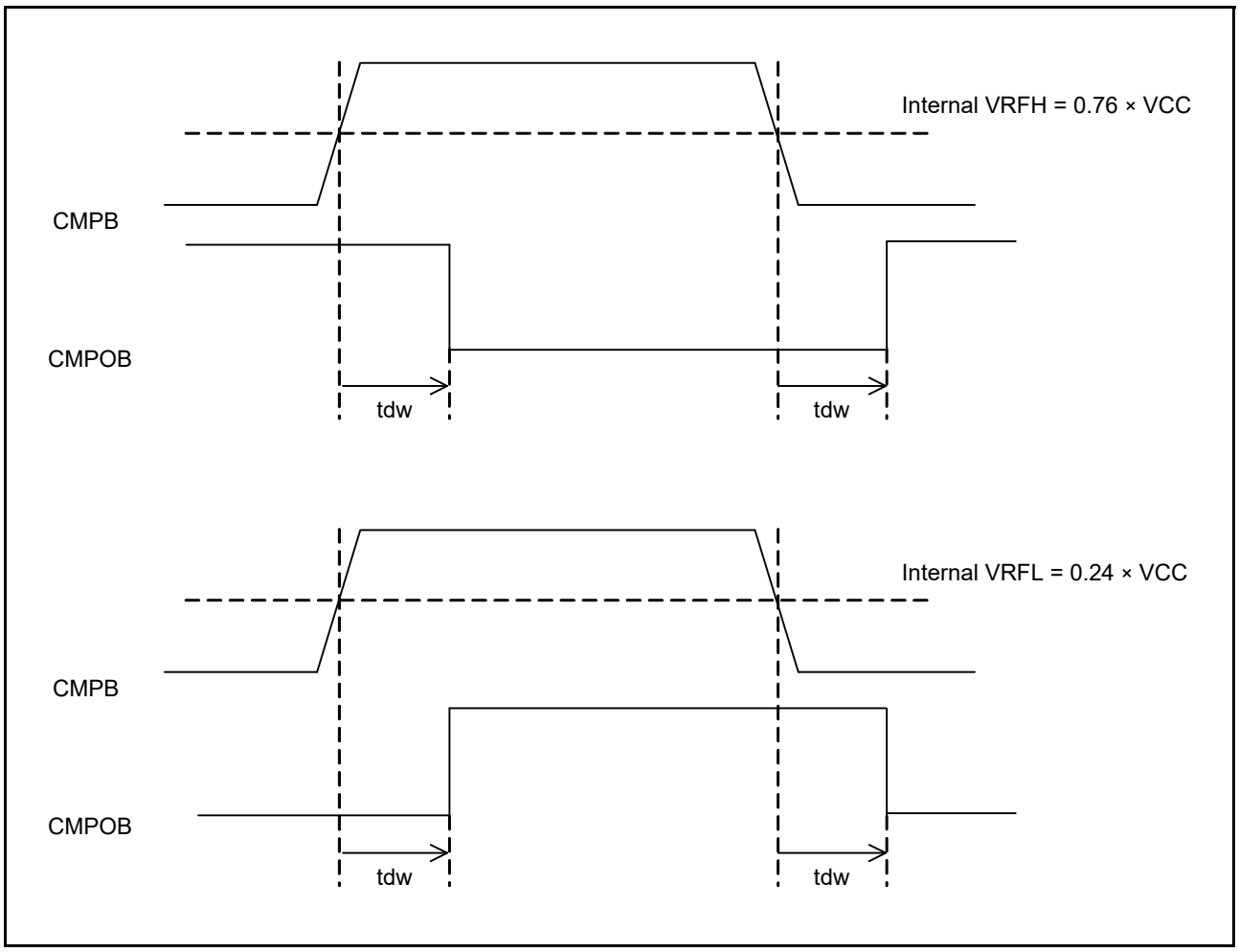

Figure 2.57 Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

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2.10 CTSU Characteristics

Table 2.69 CTSU Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin		C_{tscap}	9	10	11	nF	
Permissible output high/low current	P12 to P17, P20, P21, P26, P27, P30 to P32, P34, P35, P54, P55, PB1 to PB7, PC2 to PC7, PH0 to PH3	$\lvert \Sigma I_{OH} \rvert + \Sigma I_{OL}$	—	—	24	mA	When VXSEL = 0
	PA0, PA1, PA3, PA4, PA6, PB0, PE0 to PE5		—	—	16	mA	[Products with 64 Kbytes of flash memory or less] When VXSEL = 0
	PA0 to PA6, PB0, PD0 to PD2, PE0 to PE5		—	—	16	mA	[Products with at least 128 Kbytes of flash memory] When VXSEL = 0

2.11 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.70 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 2.58, Figure 2.59
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.85	3.97	V	Figure 2.60 At falling edge VCC
		V_{det0_1}	2.70	2.85	3.00		
		V_{det0_2}	2.37	2.53	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 2.61 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.28		
		V_{det1_2}	3.86	4.03	4.16		
		V_{det1_3}	3.68	3.86	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.80	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.59	2.67		
		V_{det1_A}	2.37	2.48	2.57		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.86	1.96	2.06		
		V_{det1_D}	1.80	1.86	1.96		
Voltage detection level	Voltage detection circuit (LVD2)*3	V_{det2_0}*4	4.08	4.32	4.48	V	Figure 2.62 At falling edge VCC
		V_{det2_1}	3.95	4.17	4.35		
		V_{det2_2}	3.82	4.03	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

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Note 1. n in the symbol Vdet0_n denotes the value of the LDSEL1[1:0] bits.
Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.
Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.
Note 4. Vdet2_0 selection can be used only when the CMPA2 pin input voltage is selected, and cannot be used when the power supply voltage (VCC) is selected.

Table 2.71 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup*1	t_{POR}	—	12.5	—	ms	Figure 2.59
	During fast startup time*2	t_{POR}	—	5.0	—		
Wait time after voltage monitoring 0 reset cancellation		t_{LVD0}	—	860	—	μs	Figure 2.60
Wait time after voltage monitoring 1 reset cancellation	LVD0 disabled*4	t_{LVD1}	—	160	—	μs	Figure 2.61
	LVD0 enabled*5		—	860	—	μs	
Wait time after voltage monitoring 2 reset cancellation	LVD0 disabled*4	t_{LVD2}	—	160	—	μs	Figure 2.62
	LVD0 enabled*5		—	860	—	μs	
PDR response delay time		t_{det}	—	—	500	μs	Figure 2.58
LVD0 response delay time			—	—	500	μs	Figure 2.58
LVD1 response delay time			—	—	360	μs	Figure 2.58
LVD2 response delay time			—	—	600	μs	Figure 2.58
POR/LVD0 minimum VCC down time*3		t_{VOFF}	500	—	—	μs	Figure 2.58, VCC = 1.0 V or above
LVD1 minimum VCC down time*3			300	—	—	μs	Figure 2.58, VCC = 1.0 V or above
LVD2 minimum VCC down time*3			600	—	—	μs	Figure 2.58, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 2.59, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	300	μs	Figure 2.61
LVD2 operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	1200	μs	Figure 2.62
Hysteresis width (power-on rest (POR))		V_{PORH}	—	110	—	mV	
Hysteresis width (LVD0, LVD1, and LVD2)		V_{LVH}	—	60	—	mV	Vdet0_0 to Vdet0_3 selected
			—	110	—		Vdet1_0 to Vdet1_2 selected
			—	70	—		Vdet1_3 to 9 selected
			—	60	—		Vdet1_A to B selected
			—	50	—		Vdet1_C to D selected
			—	90	—		LVD2 selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.
Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) ≠ 11b.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.
Note 4. When OFS1.LVDAS = 1b.
Note 5. When OFS1.LVDAS = 0b.

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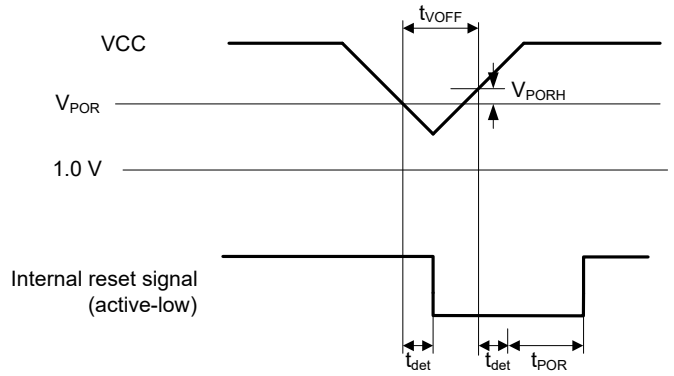
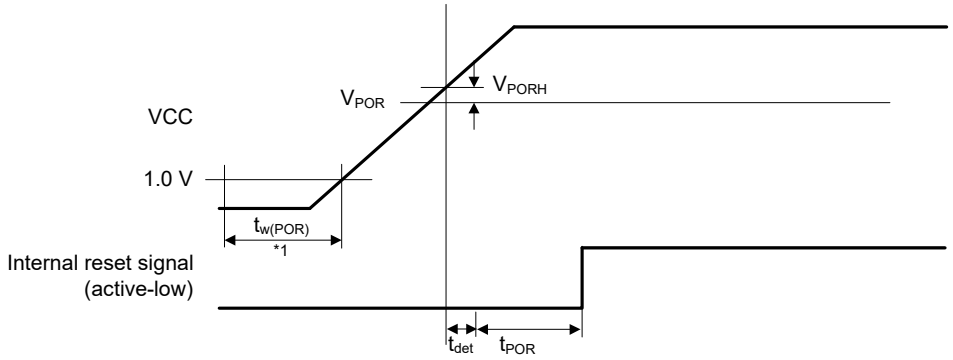


Figure 2.58 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.59 Power-On Reset Timing

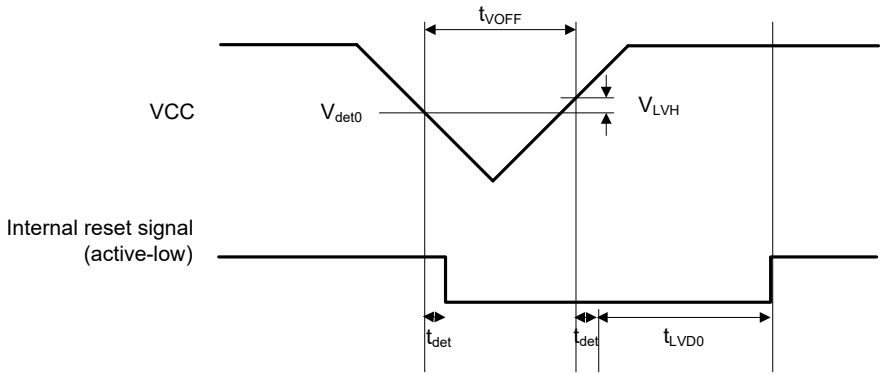


Figure 2.60 Voltage Detection Circuit Timing (V_{det0})

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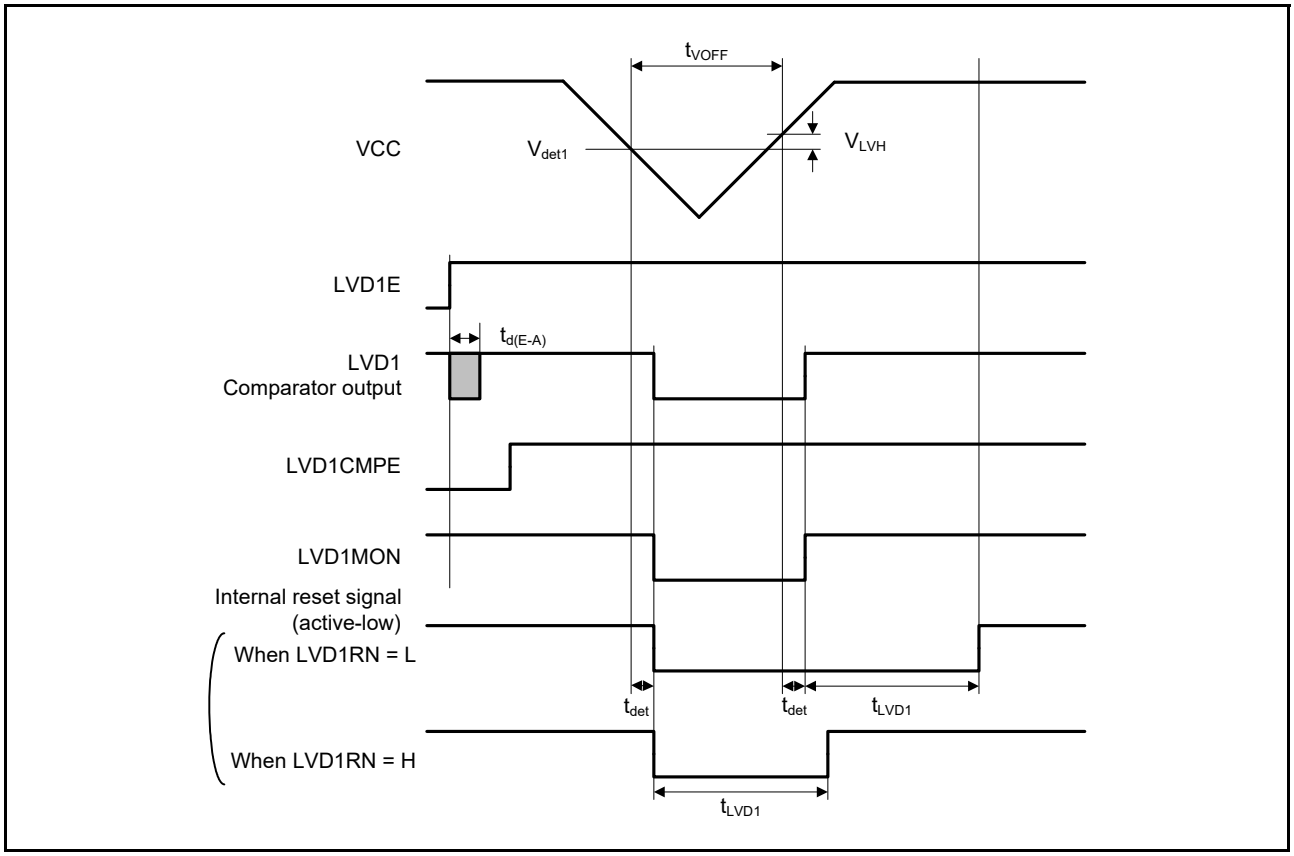

Figure 2.61 Voltage Detection Circuit Timing (V_{det1})

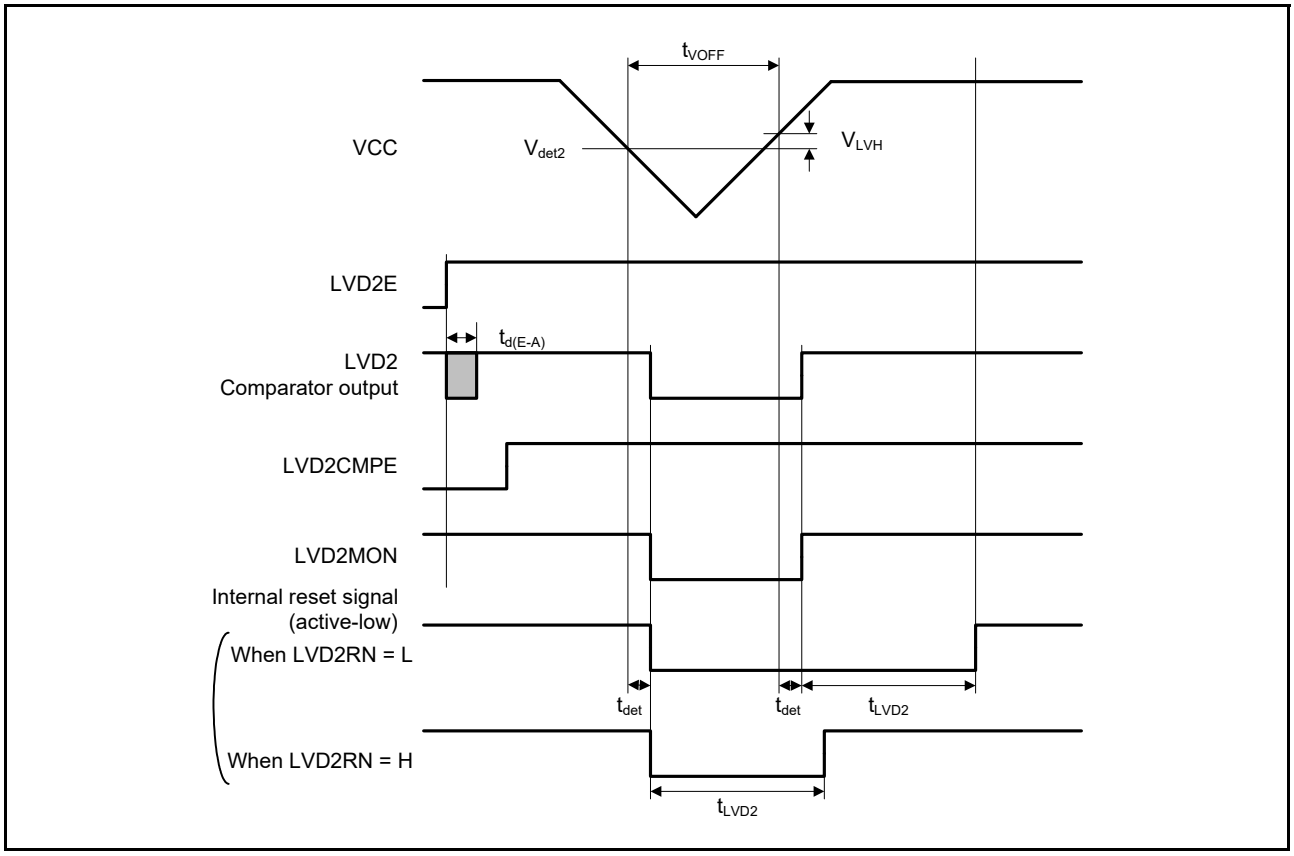

Figure 2.62 Voltage Detection Circuit Timing (V_{det2})

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2.12 Oscillation Stop Detection Timing

Table 2.72 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.63

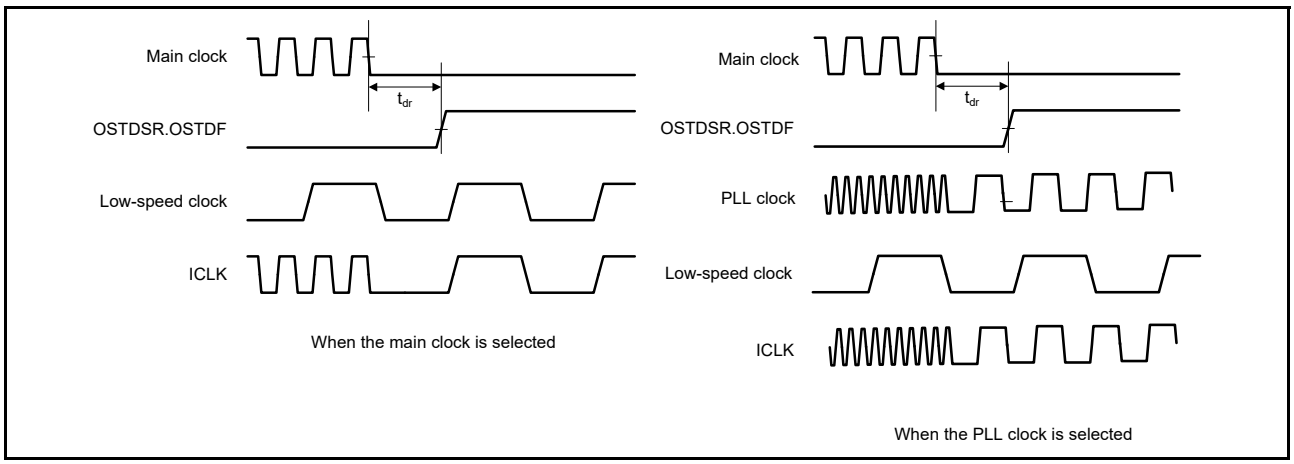

Figure 2.63 Oscillation Stop Detection Timing

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2.13 ROM (Flash Memory for Code Storage) Characteristics

Table 2.73 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{PEC}	1K	—	—	Times	
Data retention*2, *3	After 1K times of N_{PEC}	t_{DRP}	20	—	—	Year	T_a = +105°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 8-byte program is performed 256 times for different addresses in a 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.74 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	—	45.4	448.7	—	45.1	446.0	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	—	5.4	220.4	—	5.4	220.1	ms
	64-Kbyte	t_{E64K}	—	105	2331	—	12.7	375.4	—	12.4	368.0	ms
Blank check time	8-byte	t_{BC8}	—	—	45.0	—	—	8.9	—	—	8.7	μs
	2-Kbyte	t_{BC2K}	—	—	1573	—	—	120	—	—	115	μs
Erase operation forcible stop time		t_{SED}	—	—	22.8	—	—	11.1	—	—	11.0	μs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	—	5.6	438.0	—	5.6	437.7	ms
Access window setting time		t_{AWS}	—	8.2	503.3	—	5.6	438.0	—	5.6	437.7	ms
ROM mode transition wait time		t_{MS}	15	—	—	15	—	—	15	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

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Table 2.75 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 24 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	—	45.7	450.7	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	—	5.4	220.2	ms
	64-Kbyte	t_{E64K}	—	105	2331	—	17.0	500.5	ms
Blank check time	8-byte	t_{BC8}	—	—	45	—	—	9	μs
	2-Kbyte	t_{BC2K}	—	—	1573	—	—	115	μs
Erase operation forcible stop time		t_{SED}	—	—	22.8	—	—	11.2	μs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	—	5.6	437.7	ms
Access window setting time		t_{AWS}	—	8.2	503.3	—	5.6	437.7	ms
ROM mode transition wait time		t_{MS}	15	—	—	15	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 2.76 ROM (Flash Memory for Code Storage) Characteristics (4) Middle-Speed Operating Mode 2

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			Unit
			Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	ms
	64-Kbyte	t_{E64K}	—	105	2331	ms
Blank check time	8-byte	t_{BC8}	—	—	45	μs
	2-Kbyte	t_{BC2K}	—	—	1573	μs
Erase operation forcible stop time		t_{SED}	—	—	22.8	μs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	ms
Access window setting time		t_{AWS}	—	8.2	503.3	ms
ROM mode transition wait time		t_{MS}	15	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory.
Note: The frequency accuracy of FCLK should be ±3.5%.

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2.14 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 2.77 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycles*1		N_{DPEC}	100K	1000K	—	Times	
Data retention	After 10K times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +105°C
	After 100K times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000K times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycle is n, each block can be erased n times. For instance, when 1-byte program is performed 256 times for different addresses in a 256-byte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 2.78 E2 DataFlash Characteristics (2) High-speed operating mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	—	35.1	341.2	—	34.8	338.8	μs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	—	5.4	220.4	—	5.4	220.1	ms
	4-Kbyte	t_{DE4K}	—	55.0	1273.7	—	9.0	295.4	—	8.8	291.7	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	—	—	8.9	—	—	8.2	μs
	256-byte	t_{DBC256}	—	—	1573	—	—	120	—	—	115	μs
Erase operation forcible stop time		t_{DSED}	—	—	22.8	—	—	11.1	—	—	11.0	μs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 2.79 E2 DataFlash Characteristics (3) Middle-speed operating mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	—	35.3	343.2	μs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	—	5.4	220.2	ms
	4-Kbyte	t_{DE4K}	—	55.0	1273.7	—	8.8	291.8	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	—	—	9.0	μs
	256-byte	t_{DBC256}	—	—	1573	—	—	115	ms
Erase operation forcible stop time		t_{DSED}	—	—	22.8	—	—	11.2	μs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

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Table 2.80 E2 DataFlash Characteristics (4) Middle-speed operating mode 2

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			Unit
			Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	μs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	ms
	4-Kbyte	t_{DE4K}	—	55.0	1273.7	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	μs
	256-byte	t_{DBC256}	—	—	1573	ms
Erase operation forcible stop time		t_{DSED}	—	—	22.8	μs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory.
Note: The frequency accuracy of FCLK should be ±3.5%.

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2.15 Usage Notes

2.15.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 2.64 to Figure 2.66 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 35, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.

For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.

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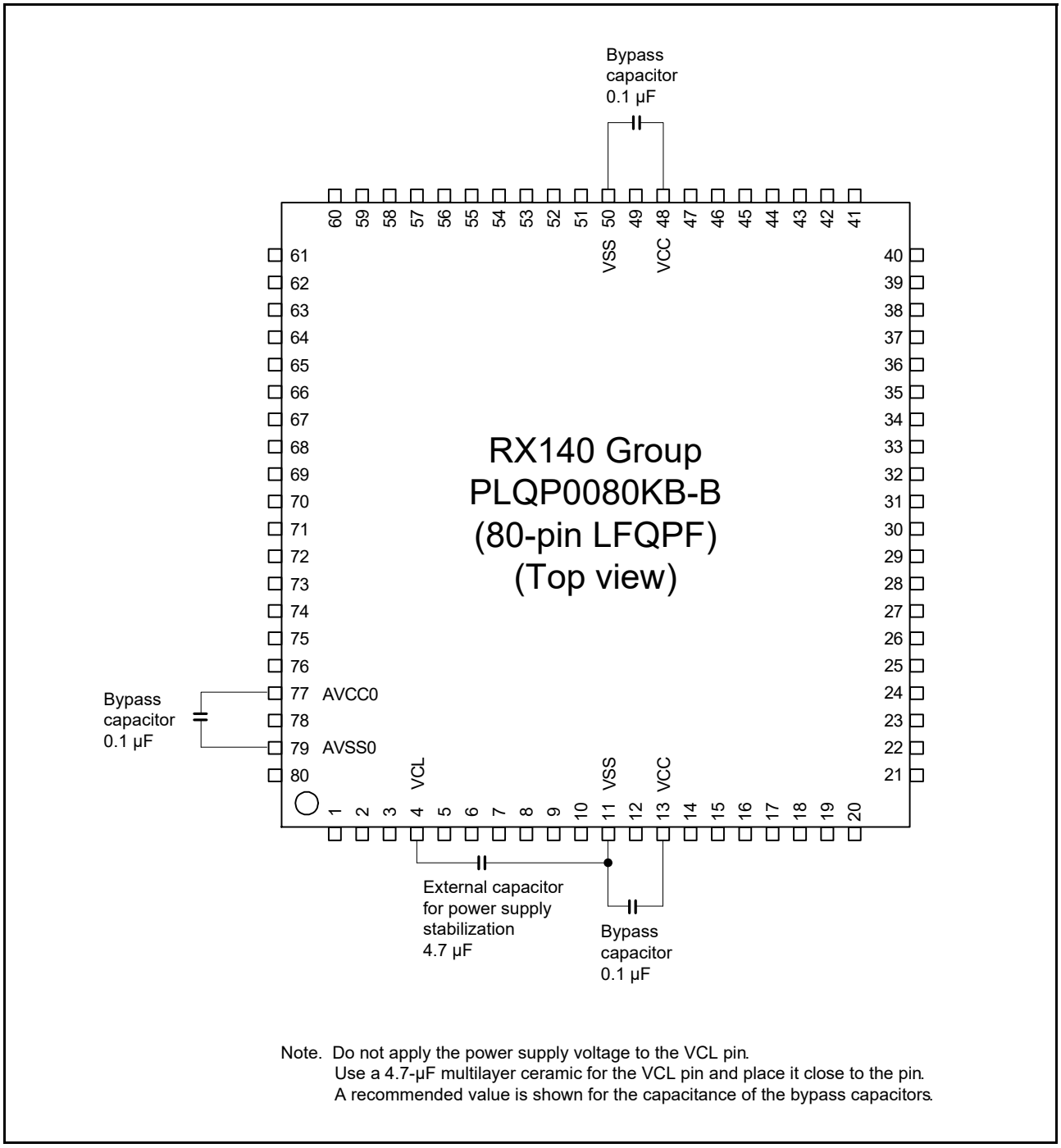

Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-μF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.64 Connecting Capacitors (80 Pins)

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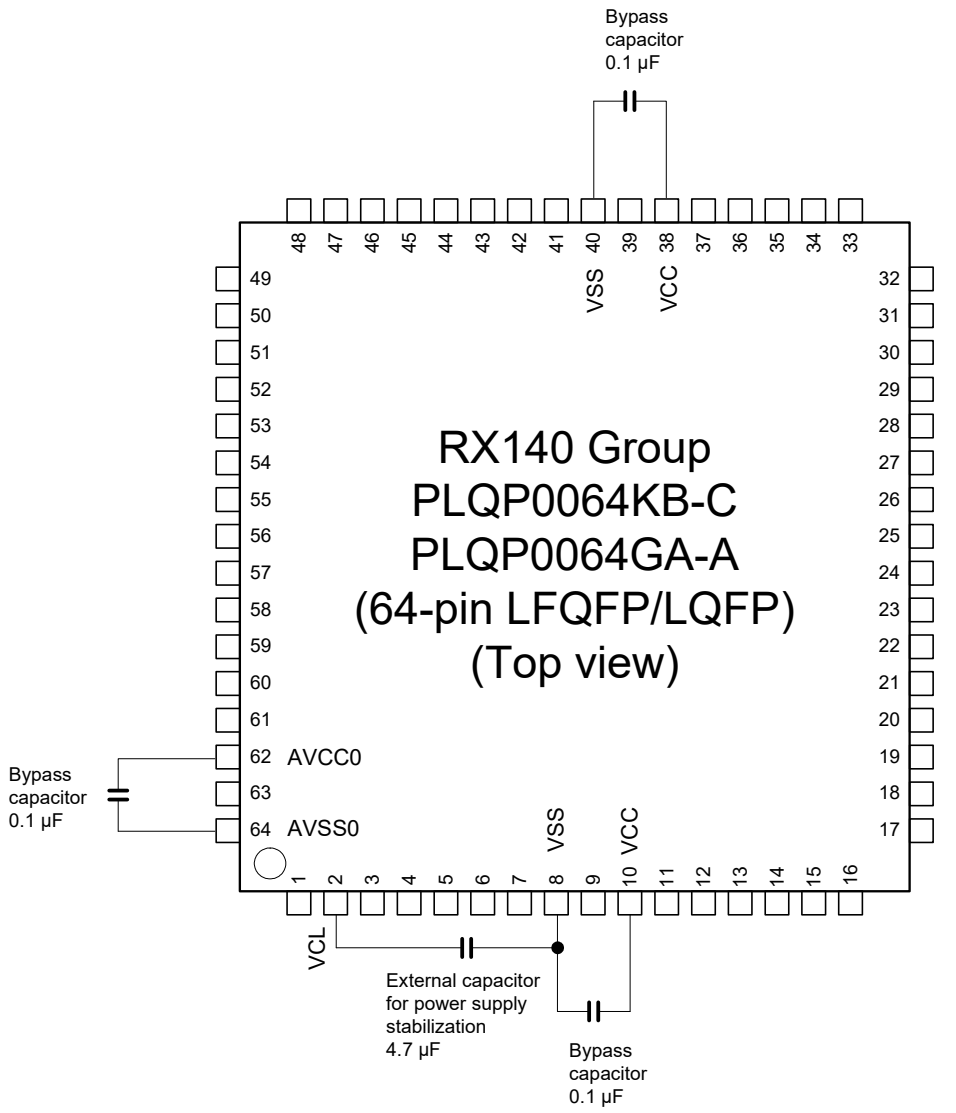

Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-μF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.65 Connecting Capacitors (64 Pins)

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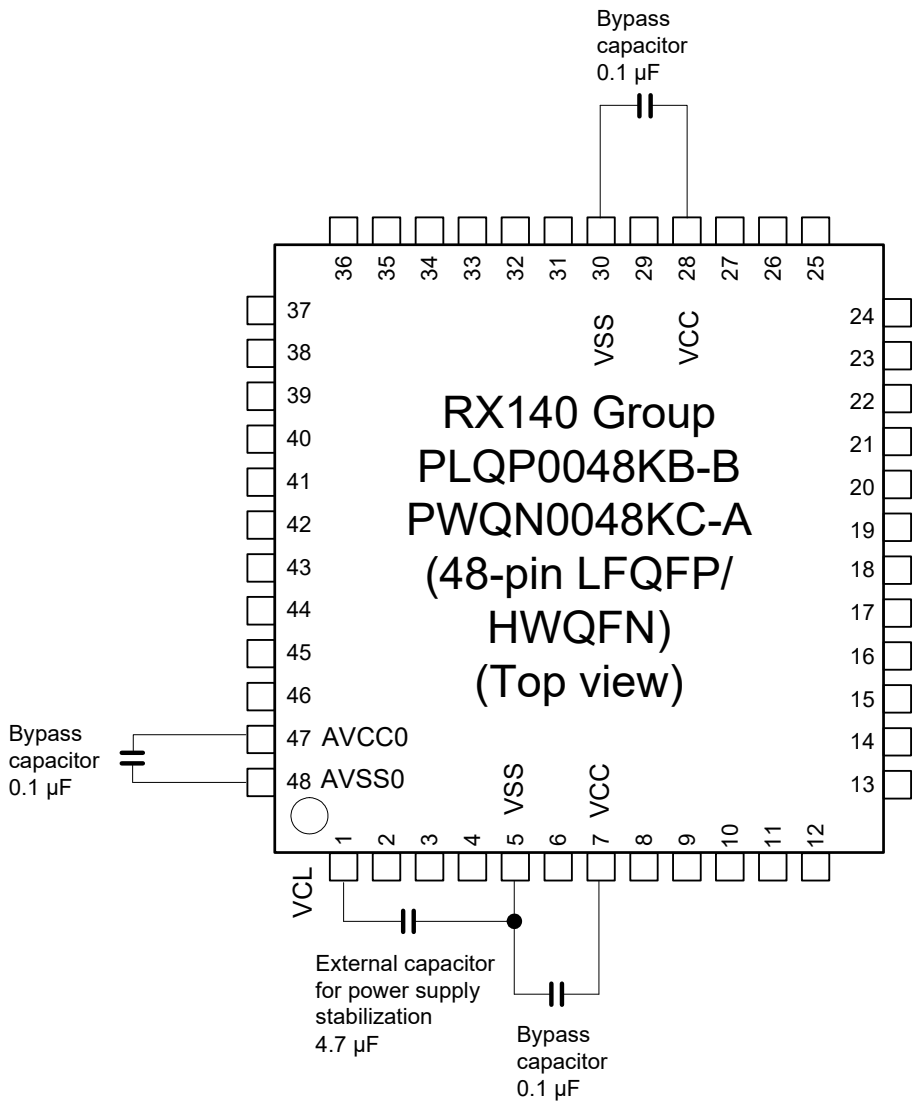

Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-μF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.66 Connecting Capacitors (48 Pins)

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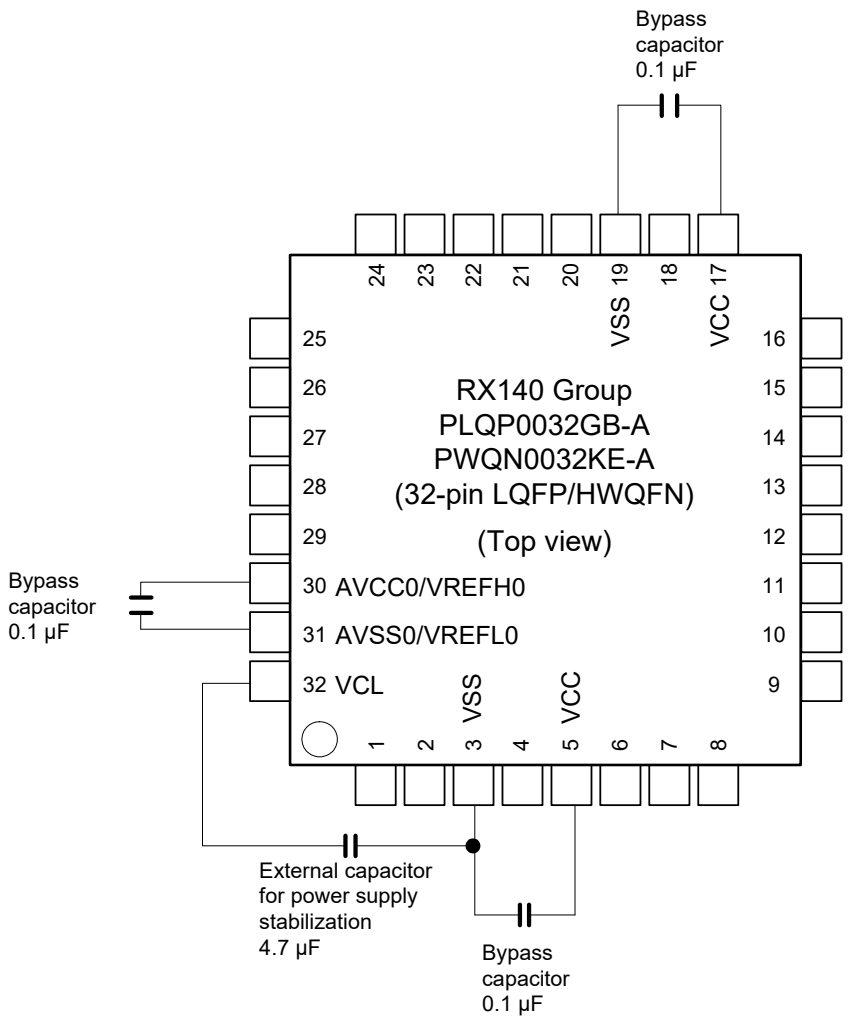

Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.67 Connecting Capacitors (32 Pins)

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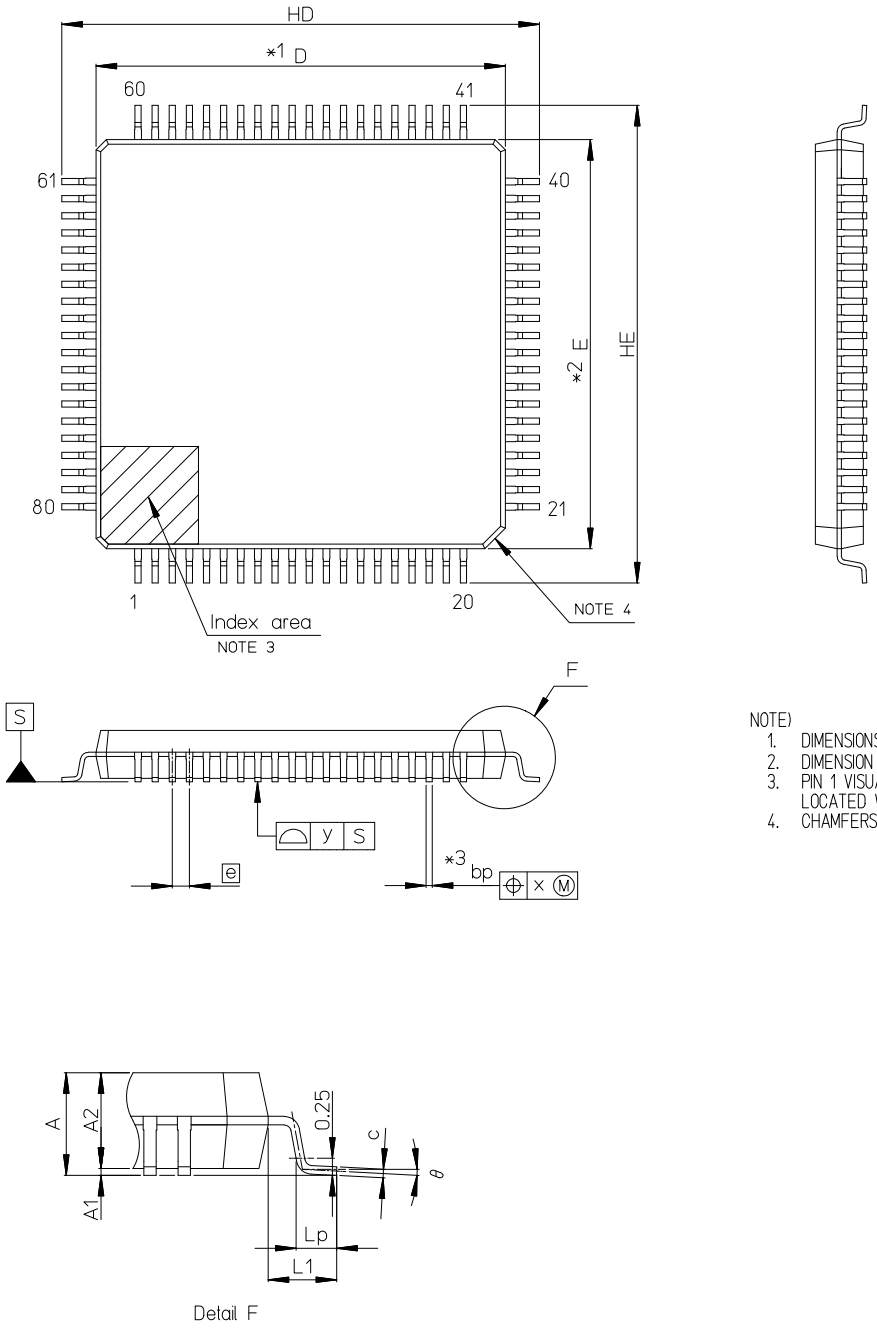
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	——	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A2	——	1.4	——
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure A 80-Pin LFQFP (PLQP0080KB-B)

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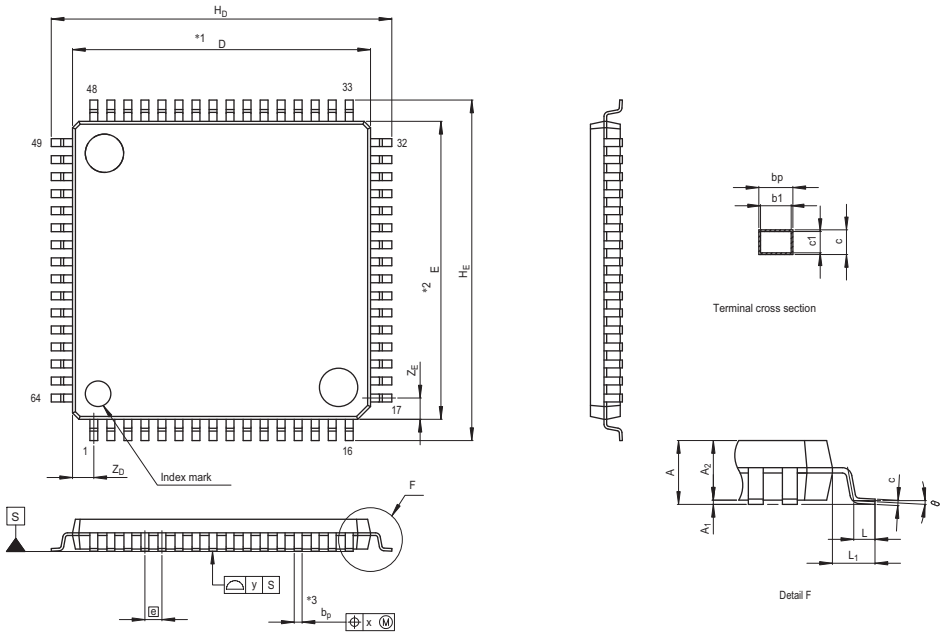
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure B 64-Pin LQFP (PLQP0064GA-A)

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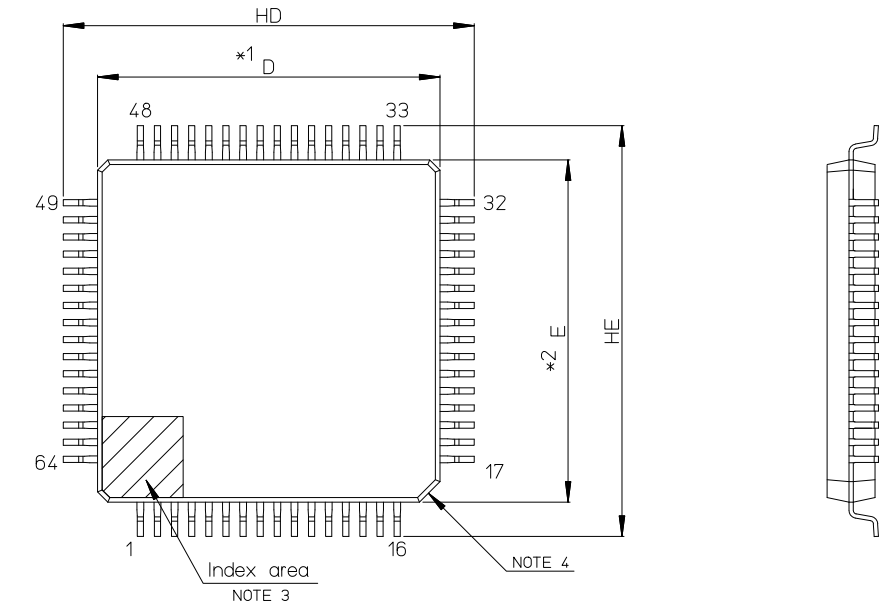
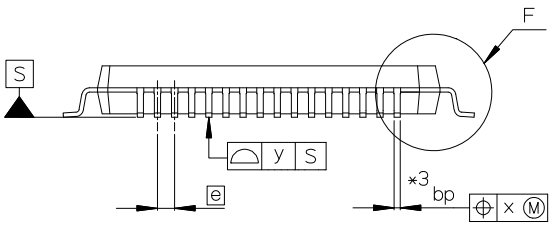
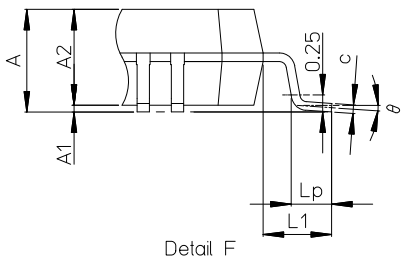
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure C 64-Pin LFQFP (PLQP0064KB-C)

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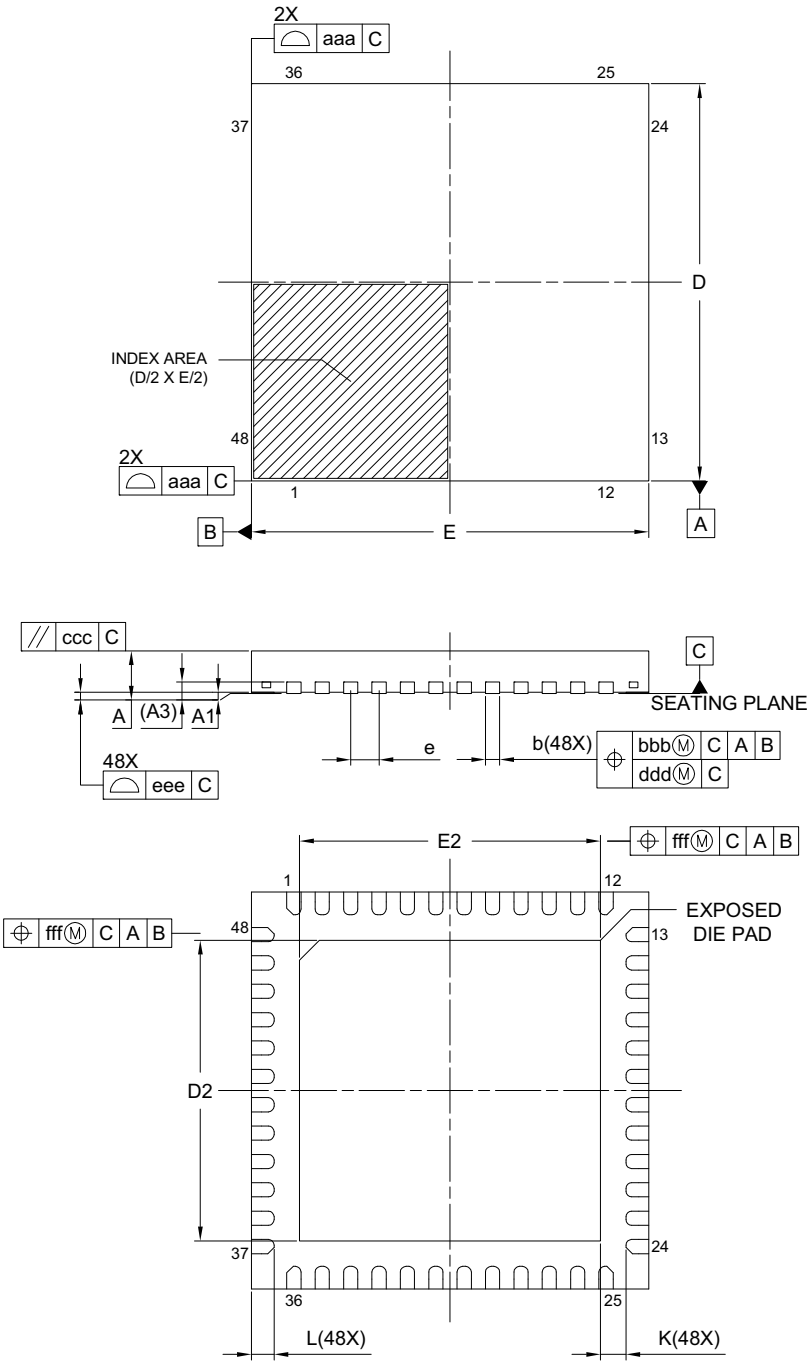
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure D 48-Pin HWQFN (PWQN0048KC-A)

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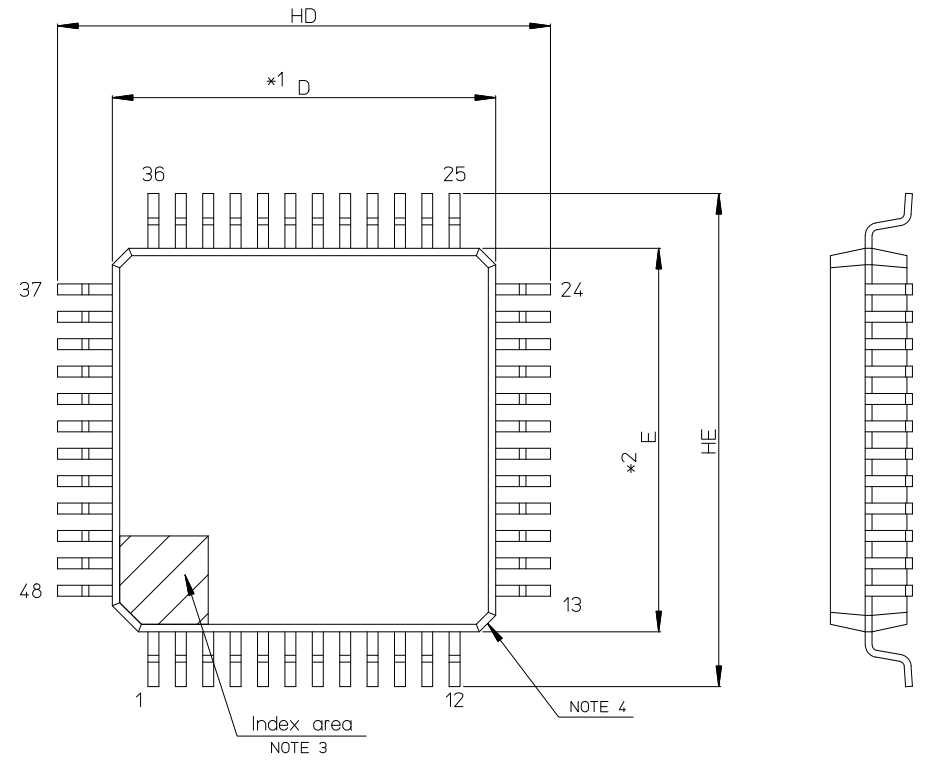
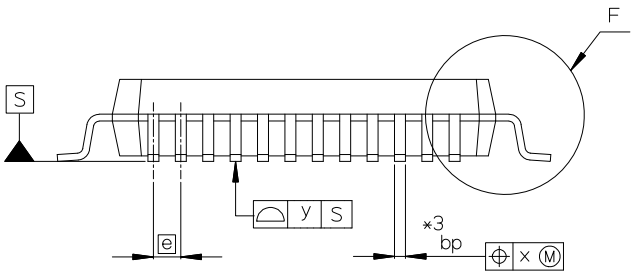
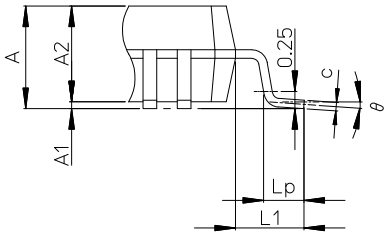
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure E 48-Pin LFQFP (PLQP0048KB-B)

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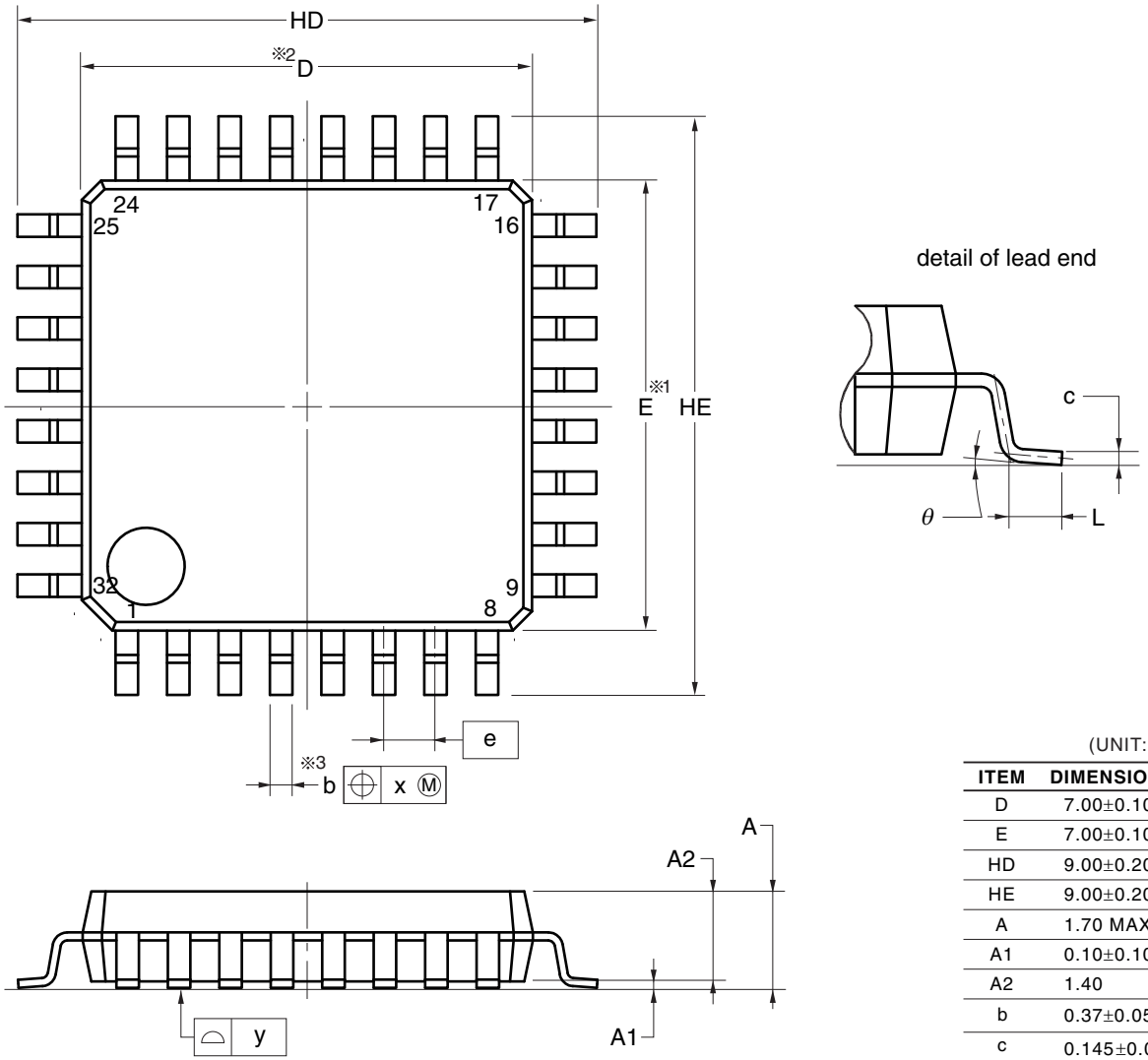
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

Figure F 32-Pin LQFP (PLQP0032GB-A)

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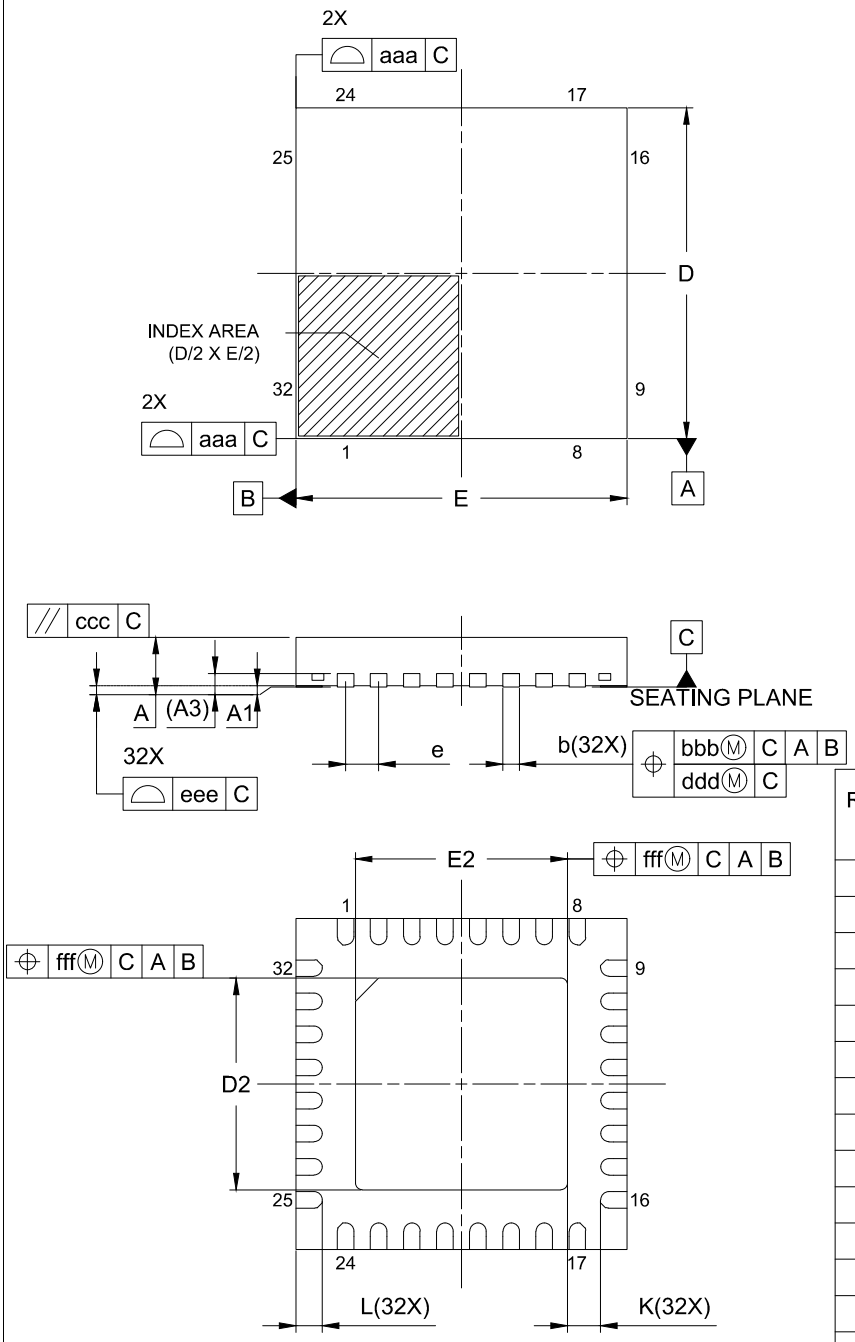
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure G 32-Pin HWQFN (PWQN0032KE-A)

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REVISION HISTORY	RX140 Group Datasheet

Classifications
- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Aug 05, 2021	—	First edition, issued	
1.10	Apr 20, 2022	Features		
		1	■ Low power design and architecture, changed	TN-RX*-A0258A/E
		1. Overview		
		3	Table 1.1 Outline of Specifications (2/4), changed	
		7, 8	Table 1.3 List of Products, changed	
		9	Figure 1.1 How to Read the Product Part Number, changed	
		13	Table 1.4 Pin Functions (3/3), changed	
		14	Figure 1.3 Pin Assignments of the 80-Pin LFQFP, changed	
		15	Figure 1.4 Pin Assignments of the 64-Pin LFQFP, 64-Pin LQFP, changed	
		16	Figure 1.5 Pin Assignments of the 48-Pin LQFP, changed	
		16	Figure 1.6 Pin Assignments of the 48-Pin HWQFN, changed	
		18	Table 1.5 List of Pins and Pin Functions (80-Pin LFQFP) (1/2), changed	
		20	Table 1.6 List of Pins and Pin Functions (64-Pin LFQFP, 64-Pin LQFP) (1/2), changed	
		24	Table 1.8 List of Pins and Pin Functions (32-Pin LQFP, 32-Pin HWQFN), changed	
		2. Electrical Characteristics		
		All	Characteristics of PH7 and PH6, added	
		All	Characteristics of products with ROM capacity of 128 Kbytes or more, added	
		46	Table 2.14 DC Characteristics (9), changed	TN-RX*-A0258A/E
		49	Table 2.17 Permissible Output Currents (2), changed	
		50	Table 2.21 Thermal Resistance Value (Reference Values), Note 1, added	
		56	Table 2.36 HOCO Clock Timing (ROM capacity: product with 64 Kbytes) Note 1, added	TN-RX*-A0258A/E
		85	Table 2.59 A/D Conversion Characteristics (2), changed	
		88	Table 2.62 A/D Conversion Characteristics (5), changed	TN-RX*-A0258A/E
		102	Table 2.77 E2 DataFlash Characteristics (2): high-speed operating mode, changed	
		Appendix 1. Package Dimensions		
		114	Figure F 32-Pin LQFP (PLQP0032GB-A), added	
1.20	Nov 22, 2024	2. Electrical Characteristics		
		26	Table 2.3 Recommended Operating Conditions (2), changed	TN-RX*-A0269A/E
		60	Table 2.40 Timing of Recovery from Low Power Consumption Modes (1), changed	TN-RX*-A0285A/E
		61	Table 2.41 Timing of Recovery from Low Power Consumption Modes (2), changed	
		62	Table 2.42 Timing of Recovery from Low Power Consumption Modes (3), added	
		63	Table 2.43 Timing of Recovery from Low Power Consumption Modes (4), changed	
		64	Table 2.44 Timing of Recovery from Low Power Consumption Modes (5), changed	
		71	Table 2.51 SCI Timing, changed	
		95	Table 2.67 Temperature Sensor Characteristics, Note 1 added	
		102	Table 2.73 ROM (Flash Memory for Code Storage) Characteristics (1), changed	
		102	Table 2.74 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode, changed	TN-RX*-A0285A/E
		103	Table 2.75 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode, changed	

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Rev.	Date	Description		Classification
		Page	Summary	
1.20	Nov 22, 2024	103	Table 2.76 ROM (Flash Memory for Code Storage) Characteristics (4) Middle-Speed Operating Mode 2, changed	
		104	Table 2.77 E2 DataFlash Characteristics (1), changed	

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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