DAC5682Z 16-Bit, 1.0 GSPS 2x-4x Interpolating Dual-Channel Digital-to-Analog Converter (DAC)

1 Features

- 16-Bit Digital-to-Analog Converter (DAC)
- 1.0 GSPS Update Rate
- 16-Bit Wideband Input LVDS Data Bus
  - 8 Sample Input FIFO
  - Interleaved I/Q Data for Dual-DAC Mode
- High Performance
  - 73-dBc ACLR WCDMA TM1 at 180 MHz
- 2x-32x Clock Multiplying PLL/VCO
- 2x or 4x Interpolation Filters
  - Stopband Transition 0.4 to 0.6 Fdata
  - Filters Configurable in Either Low-Pass or High-Pass Mode
    - Allows Selection of Higher Order Image
- Fs/4 Coarse Mixer
- On-Chip 1.2-V Reference
- Differential Scalable Output: 2 to 20 mA
- Package: 64-Pin 9-mm × 9-mm QFN

2 Applications

- Cellular Base Stations
- Broadband Wireless Access (BWA)
- WiMAX 802.16
- Fixed Wireless Backhaul
- Cable Modem Termination System (CMTS)

3 Description

The DAC5682Z is a dual-channel 16-bit 1.0 GSPS DAC with wideband LVDS data input, integrated 2x/4x interpolation filters, onboard clock multiplier, and internal voltage reference. The DAC5682Z offers superior linearity, noise, crosstalk, and PLL phase noise performance.

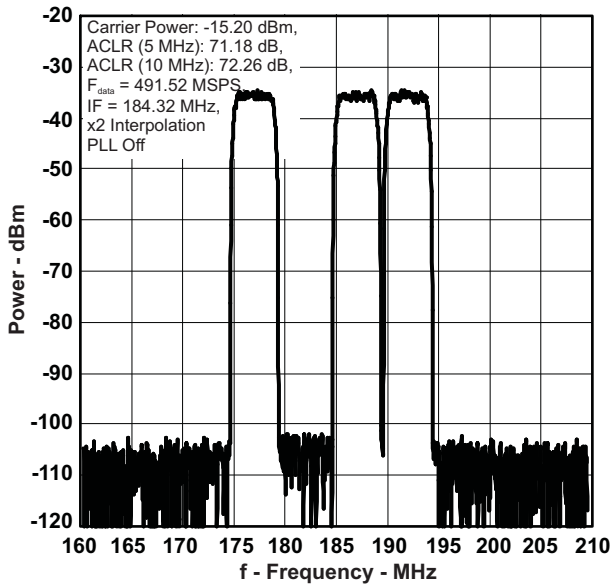
The DAC5682Z integrates a wideband LVDS port with on-chip termination. Full-rate input data can be transferred to a single DAC channel, or half-rate and 1/4-rate input data can be interpolated by onboard 2x or 4x FIR filters. Each interpolation FIR is configurable in either low-pass or high-pass mode, allowing selection of a higher order output spectral image. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC5682Z	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

3-Carrier WCDMA TM1 With a Gap



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4 Revision History

Changes from Revision E (August 2012) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (February 2011) to Revision E — **Page**

- Changed the Revision to E, August 2012 ... 1
- Changed the graphic entity of Figure 30 for clarification. ... 23
- Changed the first paragraph of ANALOG CURRENT OUTPUTS section for clarification. ... 29

Changes from Revision C (November 2008) to Revision D — **Page**

- Changed "defined by individual control bits in registers CONFIG1, CONFIG5 and CONFIG6." to "defined by individual control bits in registers CONFIG1 and CONFIG5." ... 26
- Changed wording in second sentence of RECOMMENED....PROCEDURE section from CONFIG5 **clkdiv_sync_dis** and **FIFO_sync_dis** bits as well to CONFIG5 **clkdiv_sync_dis** as well ... 35
- Deleted list items in first and second ordered list in RECOMMENED....PROCEDURE section ... 35
- Changed CONFIG5 Bit4 from "FIFO_ sync_dis" to "Reserved" in Register Map ... 39
- Changed CONFIG6 Bit 7 from "Hold_ sync_dis" to "Reserved" in Register Map ... 39
- Deleted - unless-----CONFIG5 register. in FIFO_offset(2:0): on page 21 ... 40
- Changed Bit 4 in CONFIG5 table from FIFO_sync_dis to Reserved ... 43
- Changed "FIFO_sync_sis: Disables the FIFO offset sync..... CONFIG1 register" to "Reserved (Bit 4): Set to 0 for proper operation." ... 43
- Changed Hold_sync _dis to Reserved ... 43
- Changed from Hold_sync_dis: When set, disables the sync to the FIFO .....control bit in CONFIG5." to " Reserved (Bit 7): Set to 0 for proper operation." ... 43

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Changes from Revision B (April 2008) to Revision C **Page**

- Changed Thermal Conductivity θ_{JA} (still air) from 22 to 20 8
- Changed θ_{JC} from 7 to 0.2 8
- Changed θ_{JP} from 0.2 to 3.5 8
- Changed DC Spec - Analog Output test condition from "without internal reference" 8
- Changed DC spec. REFERENCE INPUT, Small signal bandwidth conditions 9
- Changed Power Supply DVDD MIN from 1.71 to 1.7 and MAX from 2.15 to 1.9 9
- Changed Power Supply CLKVDD MIN from 1.71 to 1.7 and MAX from 2.15 to 1.9 9
- Added "DC tested" to PSRR spec. 10
- Added Digital latency spec. 10
- Added Power-up time spec 10
- Added D[15:0]P/N 11
- Changed V_{ITH+} spec 11
- Changed V_{ITH-} spec 11
- Changed I_{IH} and I_{IL} spec from –40 MIN and +40 MAX to ±20 TYP 12
- Changed $t_{(SCLK)}$ term to $t_{(SCLKL)}$ for Low time of SCLK 13
- Changed Clock Input Differential voltage from 0.5V to 0.4V MIN and added footnote 13
- Added explanatory paragraph for LVDS Inputs; prior to Figure 33 25
- Changed Figure 34 waveform label $V_{A,B}$ callout 26
- Added explanatory paragraph for Figure 35 26
- Changed calculation for C2 Designing the PLL Loop Filter 31
- Added URL link to calculator file. 32
- Changed last sentence of Dual-Channel Real Upconversion paragraph. 33
- Added modes to Dual-Channel Real Upconversion Options 33
- Added references to CDCE62005 (3 places) 33
- Added Multi-DAC Synchronization Procedure 35
- Changed Recommended DAC Startup Sequence 55

Changes from Revision A (September 2007) to Revision B **Page**

- Changed $t_{r(IOUT)}$ spec. output rise time 10% to 90% typical value from 2 ns to 220 ps 10
- Changed $t_{f(IOUT)}$ spec. output fall time 10% to 90% typical value from 2 ns to 220 ps 10
- Changed Z_T spec. internal termination from 100 Ω min, 120 Ω max; to 85 Ω min, 135 Ω max 12
- Deleted temperature deratings for f_{DATA} specifications 12
- Added DLL operating frequency range specifications 12
- Changed In-Band SFDR vs IF, Figure 6 15
- Changed C_{AC} values from 0.1 to 0.01μF, Figure 30 23
- Changed capacitor values from 0.1 to 0.01μF, Figure 35 26

Changes from Original (August 2007) to Revision A **Page**

- Changed from product preview to production data 1

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5 Description (continued)

The DAC5682Z allows both complex or real output. An optional Fs/4 coarse mixer in complex mode provides coarse frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. An external RF quadrature modulator then performs the final single sideband up-conversion. The interpolation filters and complex coarse mixers efficiently provide frequency plan flexibility while enabling higher output DAC rates to simplify image rejection filtering.

The DAC5682Z is characterized for operation over the industrial temperature range of –40°C to 85°C and is available in a 64-pin QFN package. Other single-channel members of the family include the interpolating DAC5681Z and the noninterpolating DAC5681.

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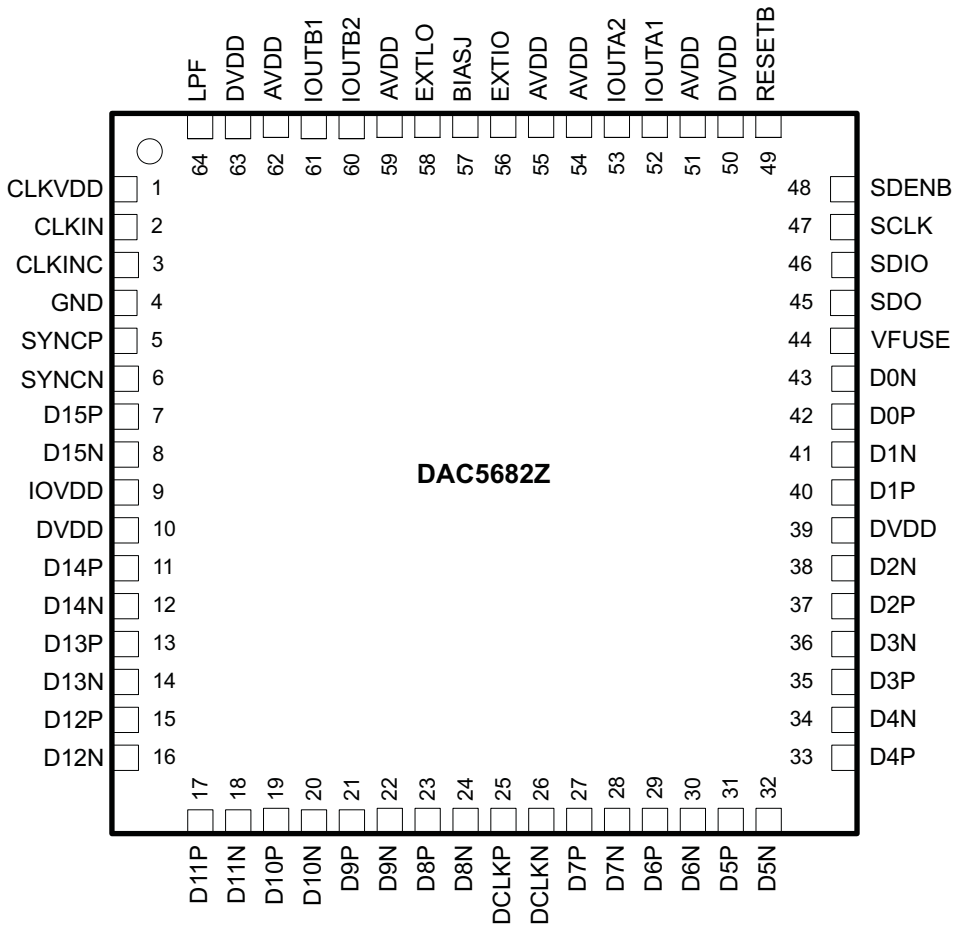
6 Pin Configuration and Functions

RGC Package
64 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	51, 54, 55, 59, 62	I	Analog supply voltage. (3.3 V)
BIASJ	57	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
CLKIN	2	I	Positive external clock input with a self-bias of approximately CLKVDD/2. With the clock multiplier PLL enabled, CLKIN provides lower frequency reference clock. If the PLL is disabled, CLKIN directly provides clock for DAC up to 1 GHz.
CLKINC	3	I	Complementary external clock input. (See the CLKIN description)
CLKVDD	1	I	Internal clock buffer supply voltage. (1.8 V)
D[15..0]P	7, 11, 13, 15, 17, 19, 21, 23, 27, 29, 31, 33, 35, 37, 40, 42	I	LVDS positive input data bits 0 through 15. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Order of bus can be reversed via **rev_bus** bit in CONFIG5 register. Data format relative to DCLKP/N clock is Double Data Rate (DDR) with two data samples input per DCLKP/N clock. In dual-channel mode, data for the A-channel is input while DCLKP is high. D15P is most significant data bit (MSB) – pin 7 D0P is least significant data bit (LSB) – pin 42

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
D[15..0]N	8, 12, 14, 16, 18, 20, 22, 24, 28, 30, 32, 34, 36, 38, 41, 43	I	LVDS negative input data bits 0 through 15. (See D[15:0]P description above) D15N is most significant data bit (MSB) – pin 8 D0N is least significant data bit (LSB) – pin 43
DCLKP	25	I	LVDS positive input clock. Unlike the other LVDS inputs, the DCLKP/N pair is self-biased to approximately DVDD/2 and does **not** have an internal termination resistor in order to optimize operation of the DLL circuit. See *DLL Operation*. For proper external termination, connect a 100 Ω resistor across LVDS clock source lines followed by series 0.01 µF capacitors connected to each of DCLKP and DCLKN pins (see). For best performance, the resistor and capacitors should be placed as close as possible to these pins.
DCLKN	26	I	LVDS negative input clock. (See the DCLKP description)
DVDD	10, 39, 50, 63	I	Digital supply voltage. (1.8 V)
EXTIO	56	I/O	Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as 1.2-V internal reference output when EXTLO = GND, requires a 0.1 µF decoupling capacitor to AGND when used as reference output.
EXTLO	58	O	Connect to GND for internal reference, or AVDD for external reference.
GND	4, Thermal Pad	I	Pin 4 and the Thermal Pad located on the bottom of the QFN package is ground for AVDD, DVDD and IOVDD supplies.
IOUTA1	52	O	A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current sink and the least positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current sink and the most positive voltage on the IOUTA1 pin. In single DAC mode, outputs appear on the IOUTA1/A2 pair only.
IOUTA2	53	O	A-Channel DAC complementary current output. The IOUTA2 has the opposite behavior of the IOUTA1 described above. An input data value of 0x0000 results in a 0-mA sink and the most positive voltage on the IOUTA2 pin.
IOUTB1	61	O	B-Channel DAC current output. See the IOUTA1 description above.
IOUTB2	60	O	B-Channel DAC complementary current output. See the IOUTA2 description above.
IOVDD	9	I	Digital I/O supply voltage (3.3 V) for pins RESETB, SCLK, SDENB, SDIO, SDO.
LPF	64	I	PLL loop filter connection. If not using the clock multiplying PLL, the LPF pin may be left open. Set both **PLL_bypass** and **PLL_sleep** control bits for reduced power dissipation.
RESETB	49	I	Resets the chip when low. Internal pullup.
SCLK	47	I	Serial interface clock. Internal pulldown.
SDENB	48	I	Active low serial data enable, always an input to the DAC5682Z. Internal pullup.
SDIO	46	I/O	Bi-directional serial interface data in 3-pin mode (default). In 4-pin interface mode (CONFIG5 **sif4**), the SDIO pin is an input only. Internal pulldown.
SDO	45	O	Uni-directional serial interface data in 4-pin mode (CONFIG5 **sif4**). The SDO pin is in high-impedance state in 3-pin interface mode (default), but can optionally be used as a status output pin via CONFIG14 **SDO_func_sel(2:0)**. Internal pulldown.
SYNCP	5	I	LVDS SYNC positive input data. The SYNCP/N LVDS pair has an internal 100 Ω termination resistor. By default, the **SYNCP/N input must be logic '1' to enable a DAC analog output**. See the *LVDS SYNCP/N Operation* paragraph for a detailed description.
SYNCN	6	I	LVDS SYNC negative input data.
VFUSE	44	I	Digital supply voltage. (1.8 V) **Connect to DVDD pins for normal operation**. This supply pin is also used for factory fuse programming.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	DVDD (2)	–0.5	2.3	V
	VFUSE (2)	–0.5	2.3	V
	CLKVDD (2)	–0.5	2.3	V
	AVDD (2)	–0.5	4	V
	IOVDD (2)	–0.5	4	V
Supply voltage	AVDD to DVDD	–2	2.6	V
	CLKVDD to DVDD	–0.5	0.5	V
	IOVDD to AVDD	–0.5	0.5	V
	D[15..0]P ,D[15..0]N, SYNCP, SYNCN (2)	–0.5	DVDD + 0.5	V
	DCLKP, DCLKN (2)	–0.3	2.1	V
	CLKIN, CLKINC (2)	–0.5	CLKVDD + 0.5	V
	SDO, SDIO, SCLK, SDENB, RESETB (2)	–0.5	IOVDD + 0.5	V
	IOUTA1/B1, IOUTA2/B2 (2)	–0.5	AVDD + 0.5	V
	LPF, EXTIO, EXTLO, BIASJ (2)	–0.5	AVDD + 0.5	V
Peak input current (any input)			20	mA
Peak total input current (all inputs)			–30	mA
Operating free-air temperature, T_A: DAC5682Z		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
SUPPLIES				
AVDD	3	3.3	3.6	V
DVDD	1.7	1.8	1.9	V
CLKVDD	1.7	1.8	1.9	V
IOVDD	3	3.3	3.6	V
ANALOG OUTPUT				
IOUTA1, IOUTA2, IOUTB1, IOUTB2	0	20	20	mA
V IOUTA1, IOUTA2, IOUTB1, IOUTB2 Compliance voltage	AVDD-0.5		AVDD+0.5	V

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
CLOCK INPUT				
CLKIN ECL/PECL Frequency			1000	MHz
CLKIN Amplitude Differential	0.4	1	CLKVDD	V
CLKIN Duty Cycle		50%		
CLKIN common mode voltage		CLKDVDD /2		V
DCLK LVDS Frequency			500	MHz
DIGITAL INPUTS				
SYNC LVDS	1	1.2	1.4	V
D15..D0 LVDS	1	1.2	1.4	V
LVDS Common mode		1.2		V
LVDS Differential Swing		0.4		V
SCLK, SDIO, SDENB, SDO CMOS SPI	GND		IOVDD	V

7.4 Thermal Information

THERMAL METRIC[1]		DAC5682Z QFN 64 PINS	UNIT
T_J	Maximum junction temperature [2]	125	°C
$R_{\theta JA}$	Theta junction-to-ambient (still air)	22	°C/W
	Theta junction-to-ambient (150 lfm)	16	
$R_{\theta JC}$	Theta junction-to-case	0.2	°C/W
$R_{\theta JP}$	Theta junction-to-pad	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Air flow or heat sinking reduces θ_{JA} and may be required for sustained operation at 85° under maximum operating conditions.

7.5 Electrical Characteristics — DC Specification

over operating free-air temperature range , AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, $Iout_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16			Bits
DC ACCURACY[1]						
INL	Integral nonlinearity	1 LSB = IOUTFS/2^{16}		±4		LSB
DNL	Differential nonlinearity			±2		
ANALOG OUTPUT						
	Course gain linearity			±0.04		LSB
	Offset error	Mid code offset		0.01		%FSR
	Gain error	With external reference		1		%FSR
	Gain error	With internal reference		0.7		%FSR
	Gain mismatch	With internal reference, dual DAC	–2		2	%FSR
	Minimum full scale output current[2]			2		mA
	Maximum full scale output current[2]			20		

(1) Measured differential across IOUTA1 and IOUTA2 or IOUTB1 and IOUTB2 with 25 Ω each to AVDD.
(2) Nominal full-scale current, IoutFS, equals 16 × IBIAS current.

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Electrical Characteristics — DC Specification (continued)

over operating free-air temperature range , AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, $Iout_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output Compliance range(3)	IOUTFS = 20 mA	AVDD –0.5V		AVDD + 0.5V	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
REFERENCE OUTPUT						
V_{ref}	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
REFERENCE INPUT						
V_{EXTIO}	Input voltage range		0.1		1.25	V
	Input resistance			1		MΩ
	Small signal bandwidth	CONFIG6: BiasLPF_A and BiasLPF_B = 0		95		kHz
		CONFIG6: BiasLPF_A and BiasLPF_B = 1		472		
	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift			±1		ppm of FSR/°C
	Gain drift	With external reference		±15		ppm of FSR/°C
		With internal reference		±30		
	Reference voltage drift			±8		ppm/°C
POWER SUPPLY						
	Analog supply voltage, AVDD		3.0	3.3	3.6	V
	Digital supply voltage, DVDD		1.7	1.8	1.9	V
	Clock supply voltage, CLKVDD		1.7	1.8	1.9	V
	I/O supply voltage, IOVDD		3.0	3.3	3.6	V
$I_{(AVDD)}$	Analog supply current	Mode 4 (below)		133		mA
$I_{(DVDD)}$	Digital supply current			455		mA
$I_{(CLKVDD)}$	Clock supply current			45		mA
$I_{(IOVDD)}$	IO supply current			12		mA
$I_{(AVDD)}$	Sleep mode, AVDD supply current	Mode 6 (below)		1.0		mA
$I_{(DVDD)}$	Sleep mode, DVDD supply current			1.5		mA
$I_{(CLKVDD)}$	Sleep mode, CLKVDD supply current			2.5		mA
$I_{(IOVDD)}$	Sleep mode, IOVDD supply current			2.0		mA

(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5682Z device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high impedance input to drive any external load.

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Electrical Characteristics — DC Specification (continued)

over operating free-air temperature range , AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, $Iout_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P	AVDD + IOVDD current, 3.3 V	Mode 1: 2X2, PLL = OFF, CLKIN = 983.04 MHz FDAC = 983.04 MHz, IF = 184.32 MHz DACA and DACB ON, 4 carrier WCDMA		135		mA
	DVDD + CLKVDD current, 1.8 V			450		mA
	Power Dissipation			1255		mW
	AVDD + IOVDD current, 3.3 V	Mode 2: 2X2, PLL = ON (8X), CLKIN = 122.88 MHz FDAC = 983.04 MHz, IF = 184.32 MHz DACA and DACB ON, 4 carrier WCDMA		145		mA
	DVDD + CLKVDD current, 1.8 V			485		mA
	Power Dissipation			1350		mW
	AVDD + IOVDD current, 3.3 V	Mode 3: 2X4, CMIX0 = Fs/4, PLL = OFF, CLKIN = 983.04 MHz FDAC = 983.04 MHz, IF = 215.04 MHz DACA and DACB ON, 4 carrier WCDMA		135		mA
	DVDD + CLKVDD current, 1.8 V			480		mA
	Power Dissipation			1310		mW
	AVDD + IOVDD current, 3.3 V	Mode 4: 2X4, CMIX0 = Fs/4, PLL = ON (8X), CLKIN = 122.88 MHz FDAC = 983.04 MHz, IF = 215.04 MHz DACA and DACB ON, 4 carrier WCDMA		145		mA
	DVDD + CLKVDD current, 1.8 V			505		mA
	Power Dissipation			1400	1600	mW
	AVDD + IOVDD current, 3.3 V	Mode 5: 2X2, CMIX0 = Fs/4, PLL = OFF, CLKIN = 983.04 MHz FDAC = 983.04 MHz, Digital Logic Disabled DACA and DACB SLEEP, Static Data Pattern		5		mA
	DVDD + CLKVDD current, 1.8 V			185		mA
	Power Dissipation			350		mW
	AVDD + IOVDD current, 3.3 V	Mode 6: 2X4, PLL = OFF, CLKIN = OFF FDAC = OFF, Digital Logic Disabled DACA and DACB = SLEEP, Static Data Pattern		3.0		mA
	DVDD + CLKVDD current, 1.8 V			4.0		mA
	Power Dissipation			17.0	30.0	mW
PSRR	Power supply rejection ratio	DC tested	–0.2		0.2	%FSR/V
T	Operating range		–40		85	°C

7.6 Electrical Characteristics — AC Specification(1)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA, 4:1 transformer output termination, 50Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
f_{CLK}	Maximum output update rate		1000			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10.4		ns
t_{pd}	Output propagation delay			2.5		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%			220		ps
$t_{f(IOUT)}$	Output fall time 90% to 10%			220		ps
	Digital latency	No interpolation, PLL Off		78		DAC clock cycles
		x2 interpolation, PLL Off		163		
		x4 interpolation, PLL Off		308		
Power-up time	DAC wake-up time	IOUT current settling to 1% of $IOUT_{FS}$. Measured from SDENB; Register 0x06, toggle Bit 4 from 1 to 0.		80		µs
	DAC sleep time	IOUT current settling to 1% of $IOUT_{FS}$. Measured from SDENB; Register 0x06, toggle Bit 4 from 0 to 1.		80		

(1) Measured single-ended into 50 Ω load.

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Electrical Characteristics — AC Specification(1) (continued)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA, 4:1 transformer output termination, 50Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SFDR	Spurious free dynamic range	1X1, PLL off, CLKIN = 500 MHz, DACA on, IF = 5.1 MHz, First Nyquist Zone < $f_{DATA}/2$		81		dBc
		2X2, PLL off, CLKIN = 1000 MHz, DACA and DACB on, IF = 5.1 MHz, First Nyquist Zone < $f_{DATA}/2$		80		
		2X2, PLL off, CLKIN = 1000 MHz, DACA and DACB on, IF = 20.1 MHz, First Nyquist Zone < $f_{DATA}/2$		77		
SNR	Signal-to-noise ratio	2X2, PLL off, CLKIN = 500 MHZ, DACA and DACB on, Single tone, 0 dBFS, IF = 20.1 MHz		75		dBc
		2X2, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, Single tone, 0 dBFS, IF = 20.1 MHz		70		
		2X2, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, Single tone, 0 dBFS, IF = 70.1 MHz		66		
		2X4, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, Single tone, 0 dBFS, IF = 180 MHz		60		
		2X2 CMIX, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, Single tone, 0 dBFS, IF = 300.2 MHz		60		
		2X2, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, Four tone, each -12 dBFS, IF = 24.7, 24.9, 25.1 and 25.3 MHz		73		
IMD3	Third-order two-tone intermodulation (each tone at –6 dBFS)	2X2, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, IF = 20.1 and 21.1 MHz		88		dBc
		2X2, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, IF = 70.1 and 71.1 MHz		75		
		2X2 CMIX, PLL off, CLKIN = 1000 MHZ, DACA and DACB on, IF = 150.1 and 151.1 MHz		67		
IMD	Four-tone intermodulation (each tone at –12 dBFS)	2X2 CMIX, PLL off, CLKIN = 1000 MHz, DACA and DACB on, fOUT = 298.4, 299.2, 300.8 and 301.6 MHz		64		dBc
ACLR(2)	Adjacent channel leakage ratio	Single carrier, baseband, 2X2, PLL off, CLKIN = 983.04 MHz, DACA and DACB on	80	83		dBc
		Single carrier, IF = 180 MHz, 2X2, PLL off, CLKIN = 983.04 MHz, DACA and DACB on		73		
		Four carrier, IF = 180 MHz, 2X2 CMIX, PLL off, CLKIN = 983.04 MHz, DACA and DACB on		68		
		Four carrier, IF = 275 MHz, 2X2 CMIX, PLL off, CLKIN = 983.04 MHz, DACA and DACB on		66		
	Noise floor(3)	50-MHz offset, 1-MHz BW, Single Carrier, baseband, 2X2, PLL off, CLKIN = 983.04		93		dBc
		50-MHz offset, 1-MHz BW, Four Carrier, baseband, 2X2, PLL off, CLKIN = 983.04.		85		

(2) W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF. TESTMODEL 1, 10 ms
(3) Carrier power measured in 3.84 MHz BW.

7.7 Electrical Characteristics (Digital Specifications)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS INTERFACE: D[15:0]P/N, SYNCP/N, DCLKP/N(1)						
$V_{A,B+}$	Logic high differential input voltage threshold		175			mV
$V_{A,B-}$	Logic low differential input voltage threshold		–175			mV
V_{COM1}	Input Common Mode	SYNCP/N, D[15:0]P/N only	1.0			V

(1) See *LVDS Inputs* for terminology.

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Electrical Characteristics (Digital Specifications) (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{COM2}	Input Common Mode	DCLKP/N only				DVDD ÷2		V
Z_T	Internal termination	SYNCP/N, D[15:0]P/N only			85	110	135	Ω
C_L	LVDS Input capacitance					2		pF
t_S, t_H	DCLK to Data	DCLKP/N: 0 to 125 MHz (see Figure 43) DLL Disabled, CONFIG5 **DLL_bypass** = 1, CONFIG10 = '00000000'		Setup_min		1100		ps
				Hold_min		–600		
$t_{SKEW(A)}$, $t_{SKEW(B)}$	DCLK to Data Skew(2)	DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format	DCLKP/N = 150 MHz	Positive		1000		ps
				Negative		–1800		
			DCLKP/N = 200 MHz	Positive		800		
				Negative		–1300		
			DCLKP/N = 250 MHz	Positive		600		
				Negative		–1000		
			DCLKP/N = 300 MHz	Positive		450		
				Negative		–800		
			DCLKP/N = 350 MHz	Positive		400		
				Negative		–700		
			DCLKP/N = 400 MHz	Positive		300		
				Negative		–600		
			DCLKP/N = 450 MHz	Positive		300		
				Negative		–500		
			DCLKP/N = 500 MHz	Positive		350		
				Negative		–300		
f_{DATA}	Input data rate supported	DLL Disabled, CONFIG5 **DLL_bypass** = 1, DDR format, DCLKP frequency: <125 MHz					250	MSPS
		DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format, DCLKP frequency: 125 to 500 MHz			250		1000	
	DLL Operating Frequency (DCLKP/N Frequency)	DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format	CONFIG10 = '11001101' = 0xCD		125		150	MHz
			CONFIG10 = '11001110' = 0xCE		150		175	
			CONFIG10 = '11001111' = 0xCF		175		200	
			CONFIG10 = '11001000' = 0xC8		200		325	
			CONFIG10 = '11000000' = 0xC0		325		500	
CMOS INTERFACE: SDO, SDIO, SCLK, SDENB, RESETB								
V_{IH}	High-level input voltage				2	3		V
V_{IL}	Low-level input voltage				0	0	0.8	V
I_{IH}	High-level input current					±20		μA
I_{IL}	Low-level input current					±20		μA
CI	CMOS Input capacitance					5		pF
V_{OH}	SDO, SDIO	I_{load} = –100 μA				IOVDD –0.2		V
		I_{load} = –2 mA				0.8 x IOVDD		V
V_{OL}	SDO, SDIO	I_{load} = 100 μA				0.2		V
		I_{load} = 2 mA				0.5		V
$t_{s(SDENB)}$	Setup time, SDENB to rising edge of SCLK				20			ns

(2) Positive skew: Clock ahead of data.
Negative skew: Data ahead of clock.

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Electrical Characteristics (Digital Specifications) (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{s(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK		10			ns
$t_{h(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK		5			ns
$t_{(SCLK)}$	Period of SCLK		100			ns
$t_{(SCLKH)}$	High time of SCLK		40			ns
$t_{(SCLKL)}$	Low time of SCLK		40			ns
$t_{d(Data)}$	Data output delay after falling edge of SCLK			10		ns
t_{RESET}	Minimum RESETB pulse width			25		ns
CLOCK INPUT (CLKIN/CLKINC)						
	Duty cycle			50%		
	Differential voltage(3)		0.4	1		V
	CLKIN/CLKINC input common mode			CLKVDD ÷2		V
PHASE LOCKED LOOP						
	Phase noise	DAC output at 600 kHz offset, 100 MHz, 0-dBFS tone, 2X4, f_{DATA} = 250 MSPS, CLKIN/C = 250 MHz, PLL_m = '00111', PLL_n = '001', VCO_div2 = 0, PLL_range = '1111', PLL_gain = '00'		–125		dBc/ Hz
		DAC output at 6 MHz offset, 100 MHz, 0-dBFS tone, 2X4, f_{DATA} = 250 MSPS, CLKIN/C = 250 MHz, PLL_m = '00111', PLL_n = '001', VCO_div2 = 0, PLL_range = '1111', PLL_gain = '00'		–146		

(3) Driving the clock input with a differential voltage lower than 1V will result in degraded performance.

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Electrical Characteristics (Digital Specifications) (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL/VCO Operating Frequency, Typical VCO Gain	**PLL_gain** = '00', **PLL_range** = '0000' (0)	160		290	MHz
			220		MHz/V
	PLL_gain = '01', **PLL_range** = '0001' (1)	290		460	MHz
			300		MHz/V
	PLL_gain = '01', **PLL_range** = '0010' (2)	400		520	MHz
			260		MHz/V
	PLL_gain = '01', **PLL_range** = '0011' (3)	480		570	MHz
			240		MHz/V
	PLL_gain = '01', **PLL_range** = '0100' (4)	560		620	MHz
			210		MHz/V
	PLL_gain = '10', **PLL_range** = '0101' (5)	620		740	MHz
			270		MHz/V
	PLL_gain = '10', **PLL_range** = '0110' (6)	690		780	MHz
			250		MHz/V
	PLL_gain = '10', **PLL_range** = '0111' (7)	740		820	MHz
			240		MHz/V
	PLL_gain = '10', **PLL_range** = '1000' (8)	790		850	MHz
			220		MHz/V
	PLL_gain = '10', **PLL_range** = '1001' (9)	840		880	MHz
			210		MHz/V
	PLL_gain = '11', **PLL_range** = '1010' (A)	880		940	MHz
			250		MHz/V
	PLL_gain = '11', **PLL_range** = '1011' (B)	920		990	MHz
			230		MHz/V
	PLL_gain = '11', **PLL_range** = '1100' (C)	960		1000	MHz
			220		MHz/V
PFD Maximum Frequency			160		MHz

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7.8 Typical Characteristics

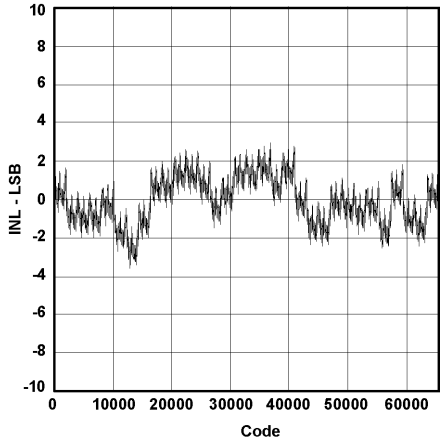

Figure 1. Integral Nonlinearity

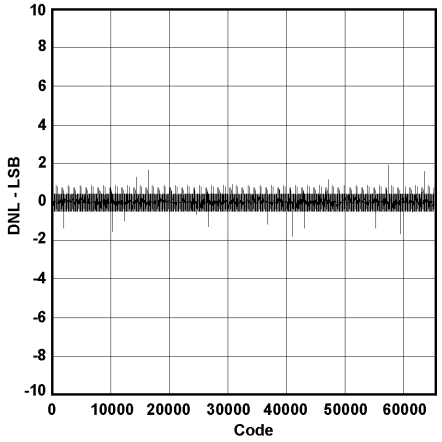

Figure 2. Differential Nonlinearity

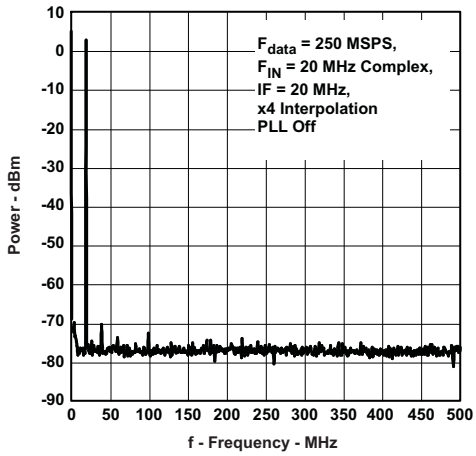

Figure 3. Single-Tone Spectral Plot

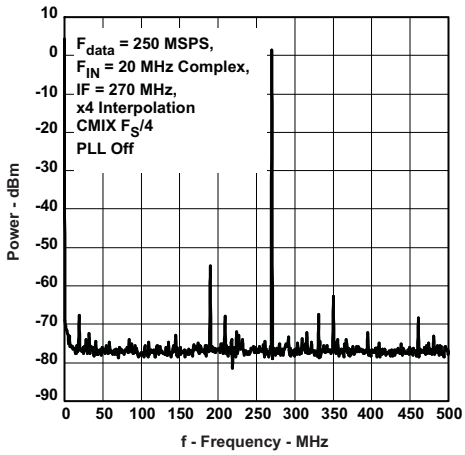

Figure 4. Single-Tone Spectral Plot

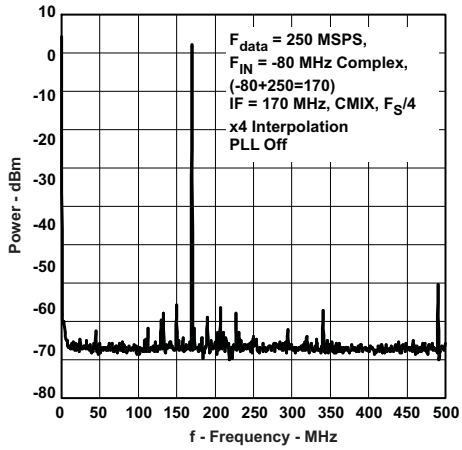

Figure 5. Single-Tone Spectral Plot

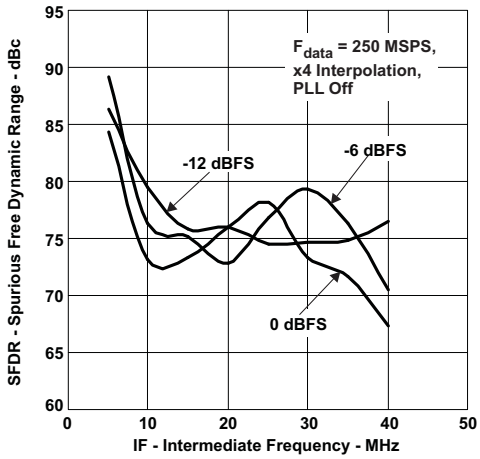

Figure 6. In-Band SFDR vs IF

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Typical Characteristics (continued)

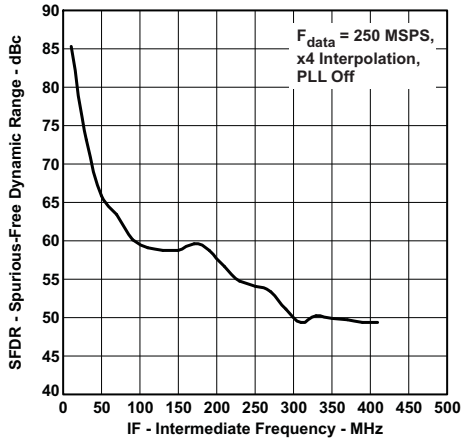

Figure 7. Out-Of-Band SFDR vs IF

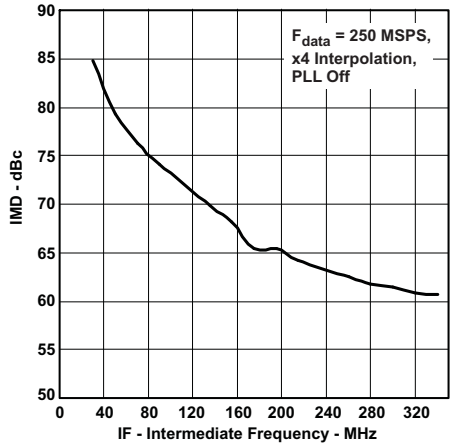

Figure 8. Two-Tone IMD vs Output Frequency

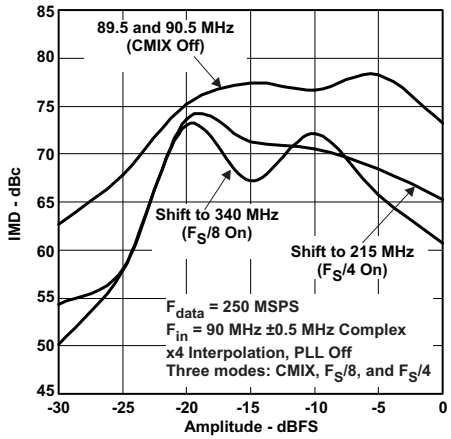

Figure 9. Two-Tone IMD vs Amplitude

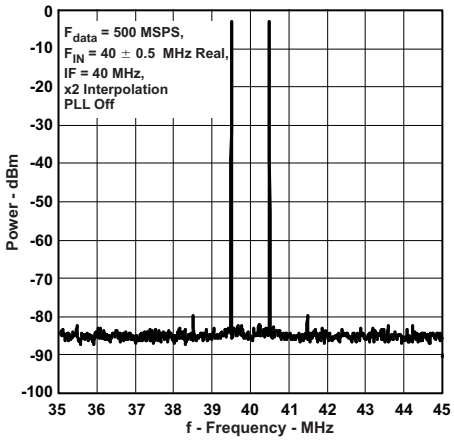

Figure 10. Two-Tone IMD Spectral Plot

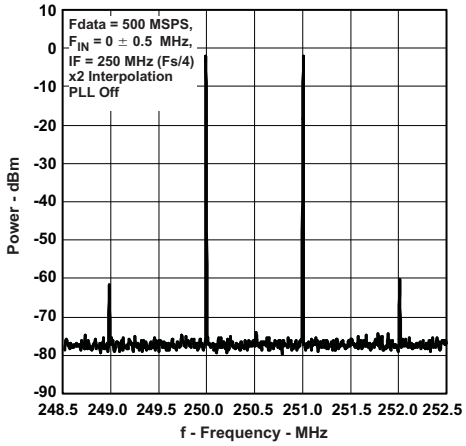

Figure 11. Two-Tone IMD Spectral Plot

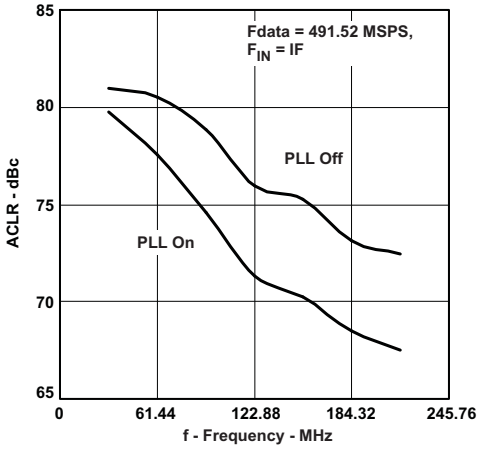

Figure 12. Single-Carrier W-CDMA Test Model 1

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Typical Characteristics (continued)

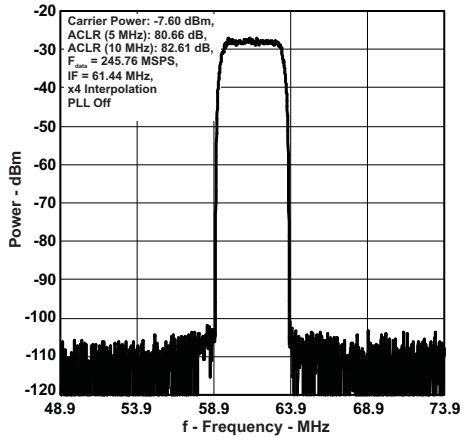

Figure 13. Single-Carrier W-CDMA Test Model 1

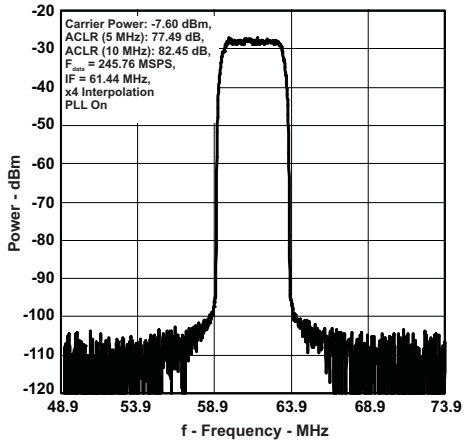

Figure 14. Single-Carrier W-CDMA Test Model 1

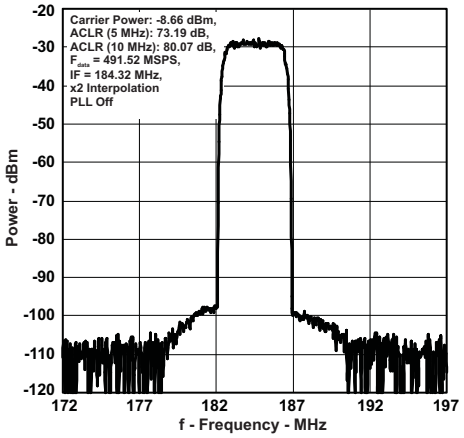

Figure 15. Single-Carrier W-CDMA Test Model 1

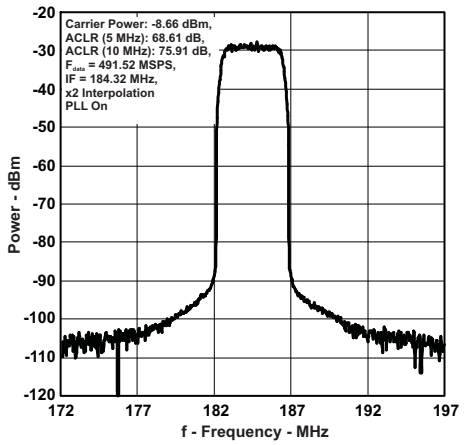

Figure 16. Single-Carrier W-CDMA Test Model 1

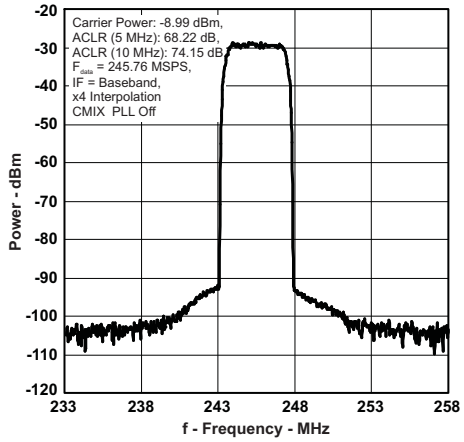

Figure 17. Single-Carrier W-CDMA Test Model 1

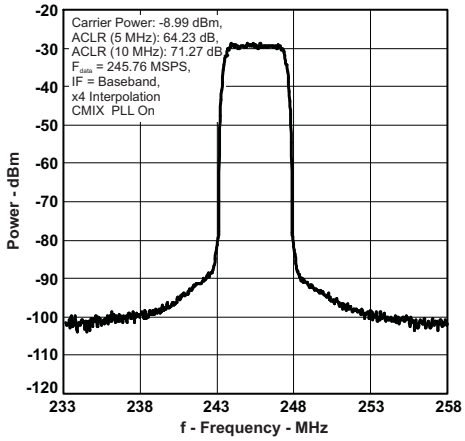

Figure 18. Single-Carrier W-CDMA Test Model 1

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Typical Characteristics (continued)

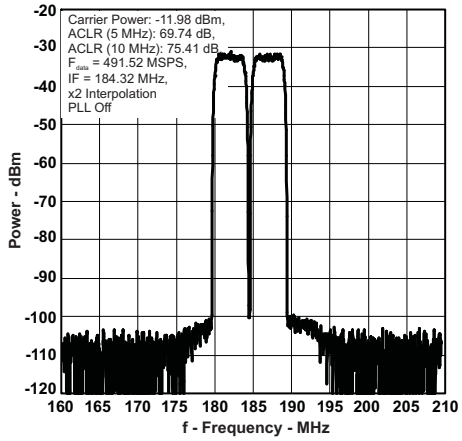

Figure 19. Two-Carrier W-CDMA Test Model 1

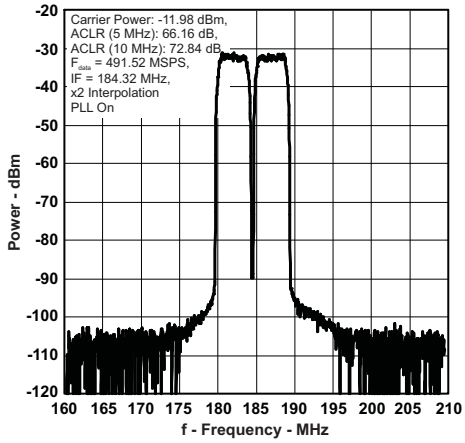

Figure 20. Two-Carrier W-CDMA Test Model 1

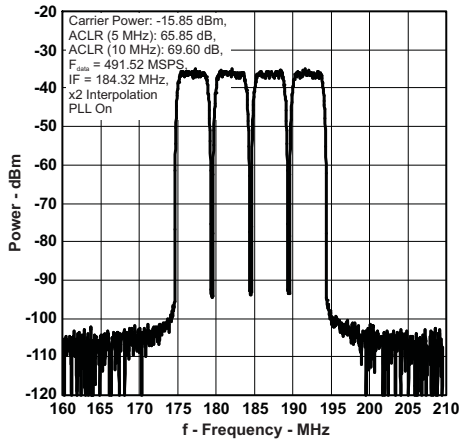

Figure 21. Four-Carrier W-CDMA Test Model 1

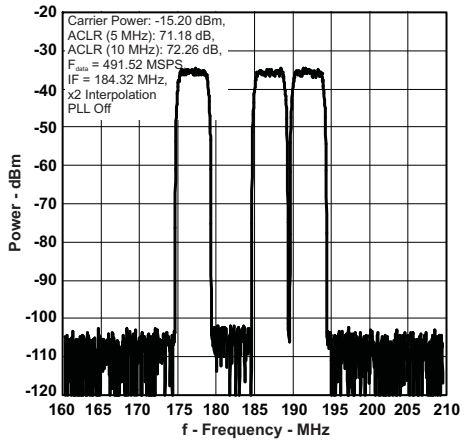

Figure 22. Three-Carrier W-CDMA Test Model 1 With Gap

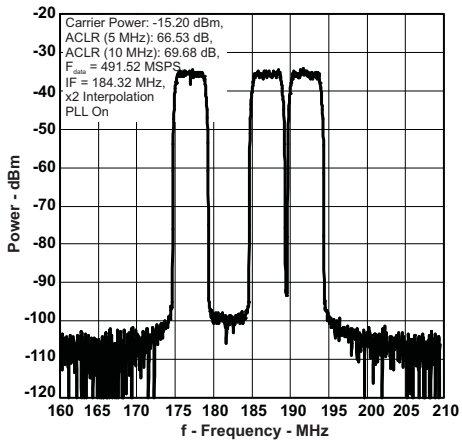

Figure 23. Three-Carrier W-CDMA Test Model 1 With Gap

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8 Detailed Description

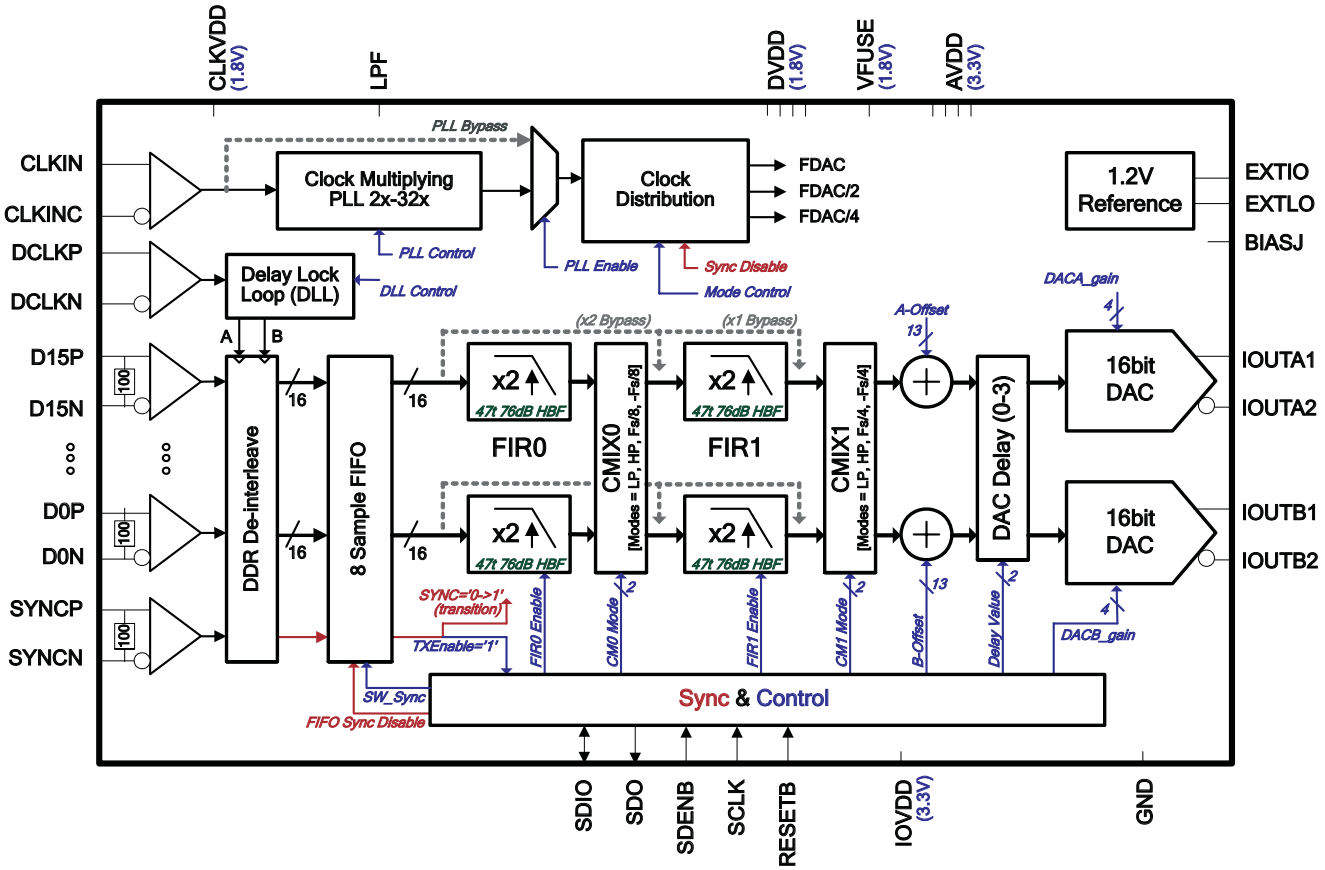
8.1 Overview

The DAC5682Z is a dual-channel 16-bit 1.0 GSPS DAC with wideband LVDS data input, integrated 2x/4x interpolation filters, onboard clock multiplier and internal voltage reference. The DAC5682Z offers superior linearity, noise, crosstalk, and PLL phase noise performance.

The DAC5682Z integrates a wideband LVDS port with on-chip termination. Full-rate input data can be transferred to a single DAC channel, or half-rate and 1/4-rate input data can be interpolated by onboard 2x or 4x FIR filters. Each interpolation FIR is configurable in either Low-Pass or High-Pass mode, allowing selection of a higher order output spectral image. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

The DAC5682Z allows both complex or real output. An optional Fs/4 coarse mixer in complex mode provides coarse frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. An external RF quadrature modulator then performs the final single sideband up-conversion. The interpolation filters and complex coarse mixers efficiently provide frequency plan flexibility while enabling higher output DAC rates to simplify image rejection filtering.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 FIR Filters

Figure 24 shows the magnitude spectrum response for the identical 47-tap FIR0 and FIR1 filters. The transition band is from 0.4 to 0.6 × F_{IN} (the input data rate for the FIR filter) with <0.002 dB of pass-band ripple and approximately 76 dB of stop-band attenuation. Figure 25 shows the region from 0.35 to 0.45 × F_{IN} – up to 0.44x FIN there is less than 0.4 dB attenuation. The composite spectrum for x4 interpolation mode, the cascaded response of FIR0 and FIR1, is shown in Figure 26. The filter taps for both FIR0 and FIR1 are listed in Table 1.

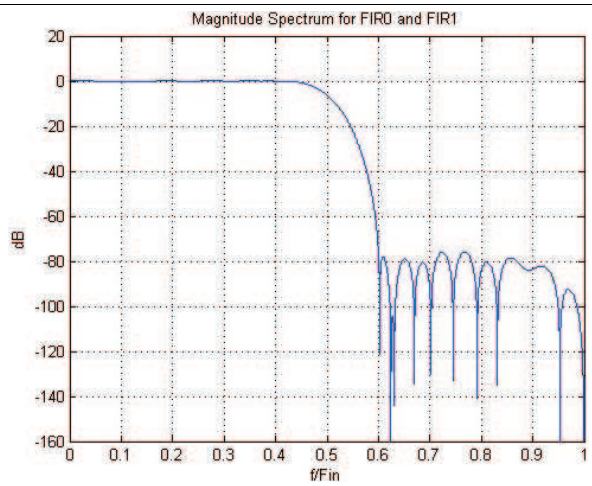

Figure 24. Magnitude Spectrum for FIR0 and FIR1

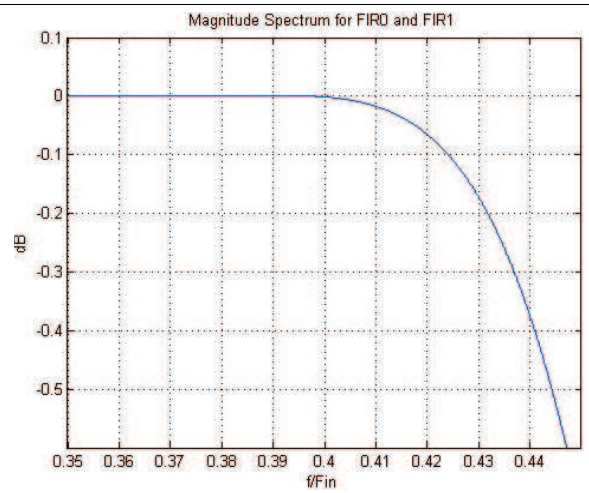

Figure 25. FIR0 and FIR1 Transition Band

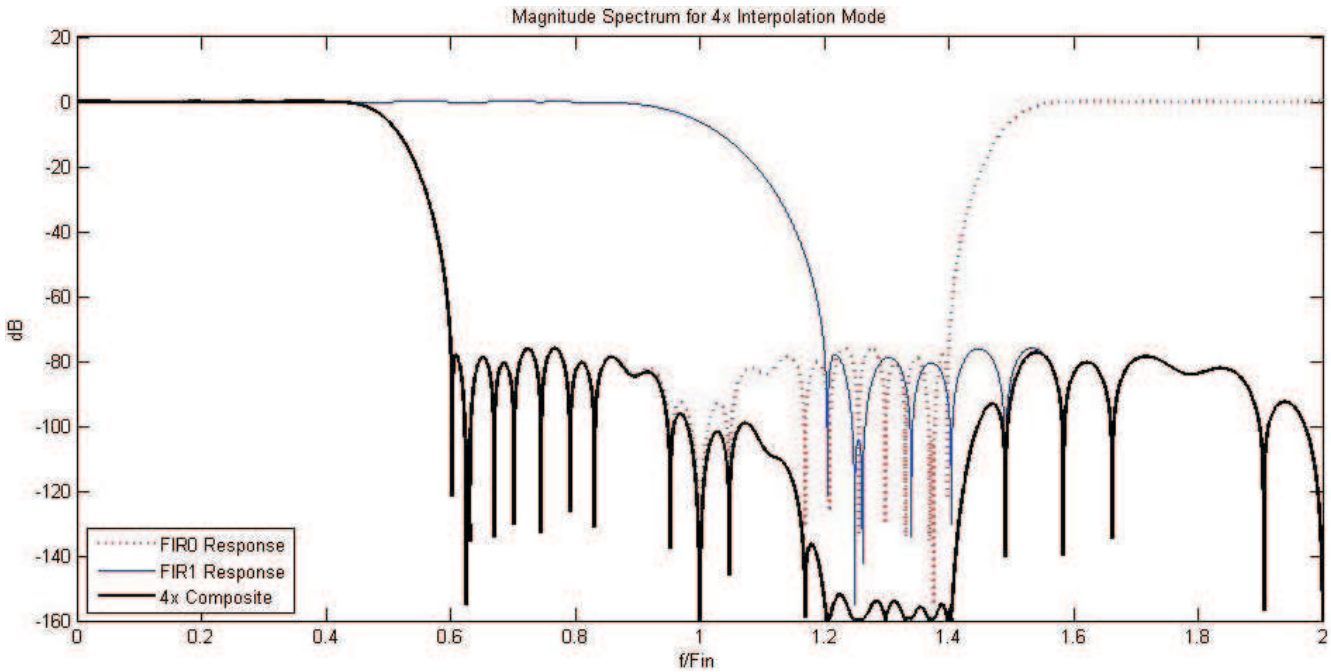

Figure 26. Magnitude Composite Spectrum for 4x Interpolation Mode

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Table 1. FIR0 and FIR1 Digital Filter Taps

TAP NO.	COEFF	TAP NO.	COEFF
1, 47	–5	2, 46	0
3, 45	18	4, 44	0
5, 43	–42	6, 42	0
7, 41	85	8, 40	0
9, 39	–158	10, 38	0
11, 37	272	12, 36	0
13, 35	–444	14, 34	0
15, 33	704	16, 32	0
17, 31	–1106	18, 30	0
19, 29	1795	20, 28	0
21, 27	–3295	22, 26	0
23, 25	10368	—	—
24	16384	—	—

8.3.2 Coarse Mixers: CMIX0 and CMIX1

The DAC5682Z has two coarse mixer (CMIX) blocks: CMIX0 follows FIR0 and CMIX1 follows FIR1. (See Figure 27) Each CMIX block provides mixing capability of fixed frequencies Fs/2 (real) or ±Fs/4 (complex) with respect to the output frequency of the preceding FIR block. Because FIR0 and CMIX0 are only used in x4 interpolation modes, the output is half-rate relative to the DAC output frequency. Therefore, an ±Fs/4 mixing sequence results in $\pm F_{DAC}/8$ frequency shift at the DAC output.

Table 2. CMIX0 Mixer Sequences

Mode	CMIX0_mode(1)	CMIX0_mode(0)	MIXING SEQUENCE
Normal (Low Pass, No Mixing)	0	0	FIR0A = { +A, +A , +A, +A } FIR0B = { +B, +B , +B, +B }
High Pass	0	1	FIR0A = { +A, –A , +A, –A } FIR0B = { +B, –B , +B, –B }
$+F_{DAC}$ /8 (+Fs/4)	1	0	FIR0A = { +A, –B , –A, +B } FIR0B = { +B, +A , –B, –A }
$–F_{DAC}$ /8 (–Fs/4)	1	1	FIR0A = { +A, +B , –A, –B } FIR0B = { +B, –A , –B, +A }

Table 3. CMIX1 Mixer Sequences

Mode	CMIX1_mode(1)	CMIX1_mode(0)	MIXING SEQUENCE
Normal (Low Pass, No Mixing)	0	0	DACA = { +A, +A , +A, +A } DACB = { +B, +B , +B, +B }
High Pass (Fs/2)	0	1	DACA = { +A, –A , +A, –A } DACB = { +B, –B , +B, –B }
$+F_{DAC}$ /4	1	0	DACA = { +A, –B , –A, +B } DACB = { +B, +A , –B, –A }
$–F_{DAC}$ /4	1	1	DACA = { +A, +B , –A, –B } DACB = { +B, –A , –B, +A }

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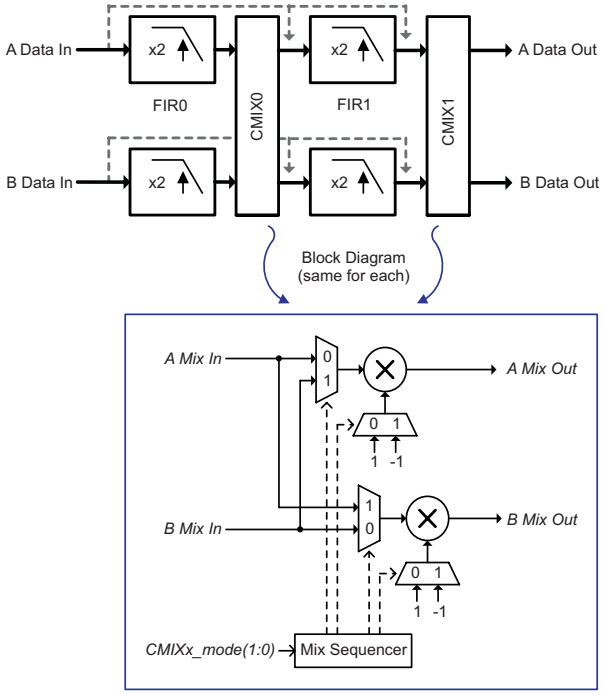

Figure 27. CMIX0 and CMIX1 Coarse Mixers Block Diagram

8.3.3 Clock Inputs

Figure 28 shows an equivalent circuit for the LVDS data input clock (DCLKP/N).

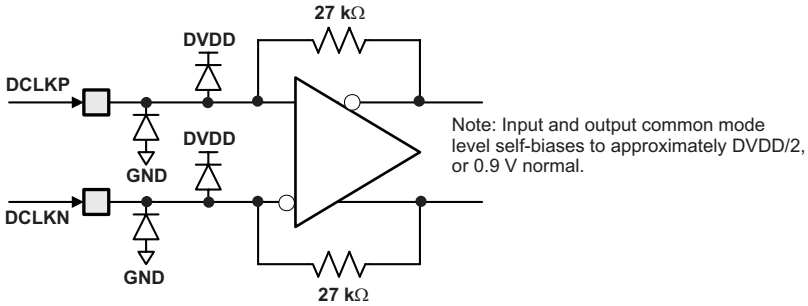

Figure 28. DCLKP/N Equivalent Input Circuit

Figure 29 shows an equivalent circuit for the DAC input clock (CLKIN/C).

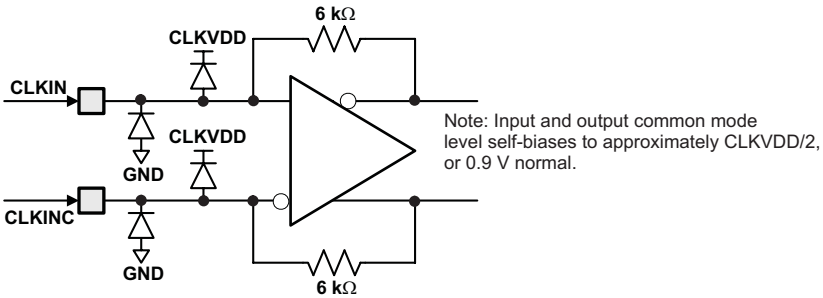

Figure 29. CLKIN/C Equivalent Input Circuit

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Figure 30 shows the preferred configuration for driving the CLKIN/CLKINC input clock with a differential ECL/PECL source.

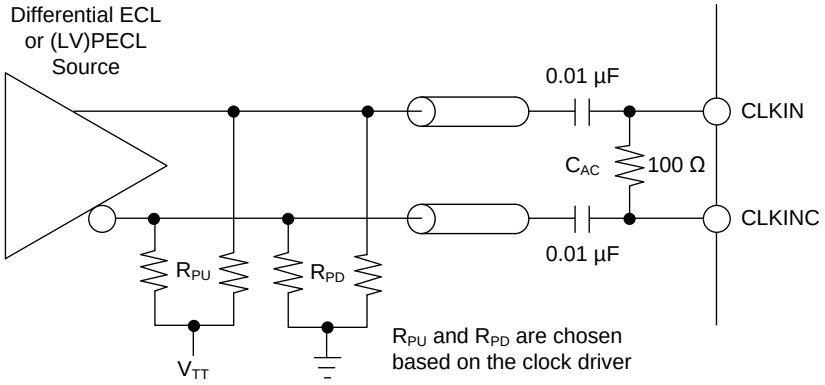

Figure 30. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source

8.3.4 LVDS Data Interfacing

Interfacing very high-speed LVDS data and clocks presents a big challenge to system designers as they have unique constraints and are often implemented with specialized circuits to increase bandwidth. One such specialized LVDS circuit used in many FPGAs and ASICs is a SERializer-DESerializer (SERDES) block. For interfacing to the DAC5682Z, only the SERializer functionality of the SERDES block is required. SERDES drivers accept lower rate parallel input data and output a serial stream using a shift register at a frequency multiple of the data bit width. For example, a 4-bit SERDES block can accept parallel 4-bit input data at 250 MSPS and output serial data 1000 MSPS.

External clock distribution for FPGA and ASIC SERDES drivers often have a chip-to-chip system constraint of a limited input clock frequency compared to the desired LVDS data rate. In this case, an internal clock multiplying PLL is often used in the FPGA or ASIC to drive the high-rate SERDES outputs. Due to this possible system clocking constraint, the DAC5682Z accommodates a scheme where a toggling LVDS SERDES data bit can provide a “data driven” half-rate clock (DCLK) from the data source. A DLL onboard the DAC is used to shift the DCLK edges relative to LVDS data to maintain internal setup and hold timing.

To increase bandwidth of a single 16-bit input bus, the DAC5682Z assumes Double Data Rate (DDR) style interfacing of data relative to the half-rate DCLK. Refer to Figure 31 and Figure 32 for an example implementation using FPGA-based LVDS data and clock interfaces to drive the DAC5682Z. In this example, an assumed system constraint is that the FPGA can only receive a 250 MHz maximum input clock while the desired DAC clock is 1000 MHz. A clock distribution chip such as the CDCM7005 or the CDCE62005 is useful in this case to provide frequency and phase locked clocks at 250 MHz and 1000 MHz.

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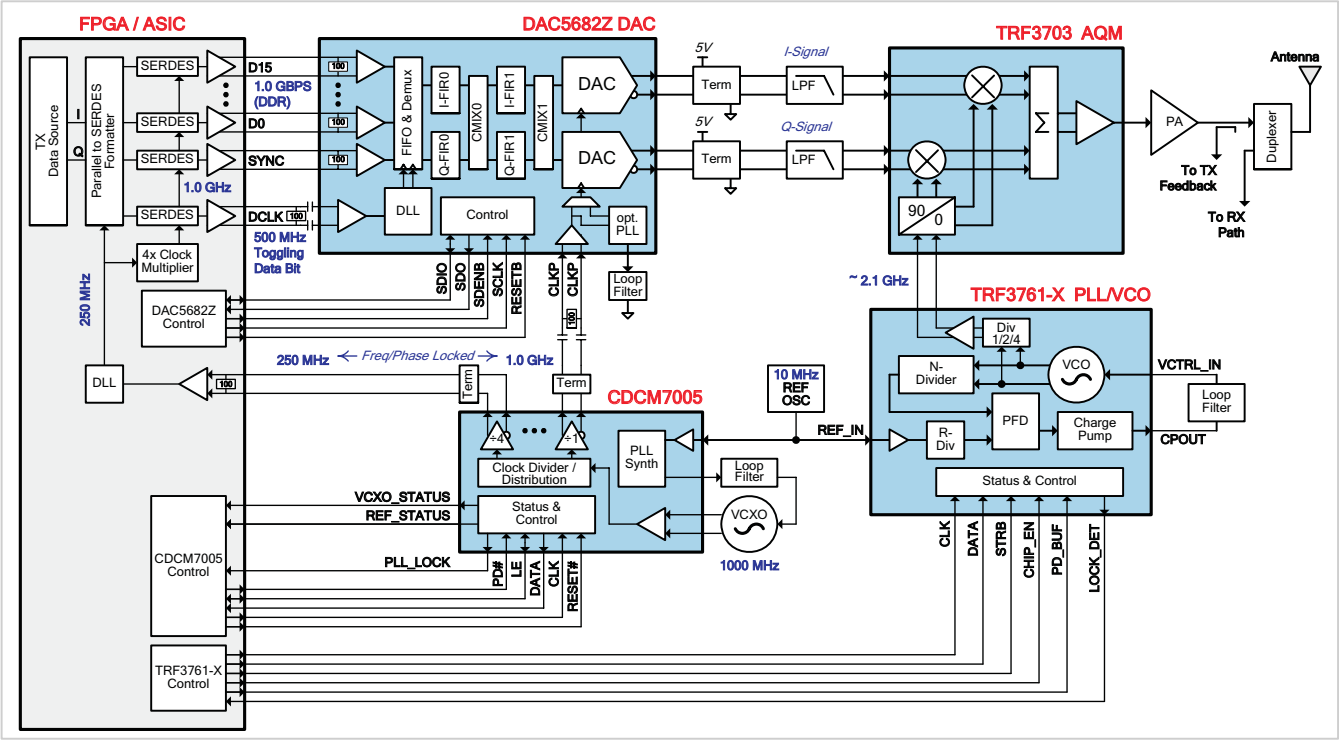

Figure 31. Example Direct Conversion System Diagram

From the example provided by Figure 32, driving LVDS data into the DAC using SERDES blocks requires a parallel load of 4 consecutive data samples to shift registers. Color is used in the figure to indicate how data and clocks flow from the FPGA to the DAC5682Z. The figure also shows the use of the SYNCP/N input, which along with DCLK, requires 18 individual SERDES data blocks to drive the input data FIFO of the DAC that provides an elastic buffer to the DAC5682Z digital processing chain.

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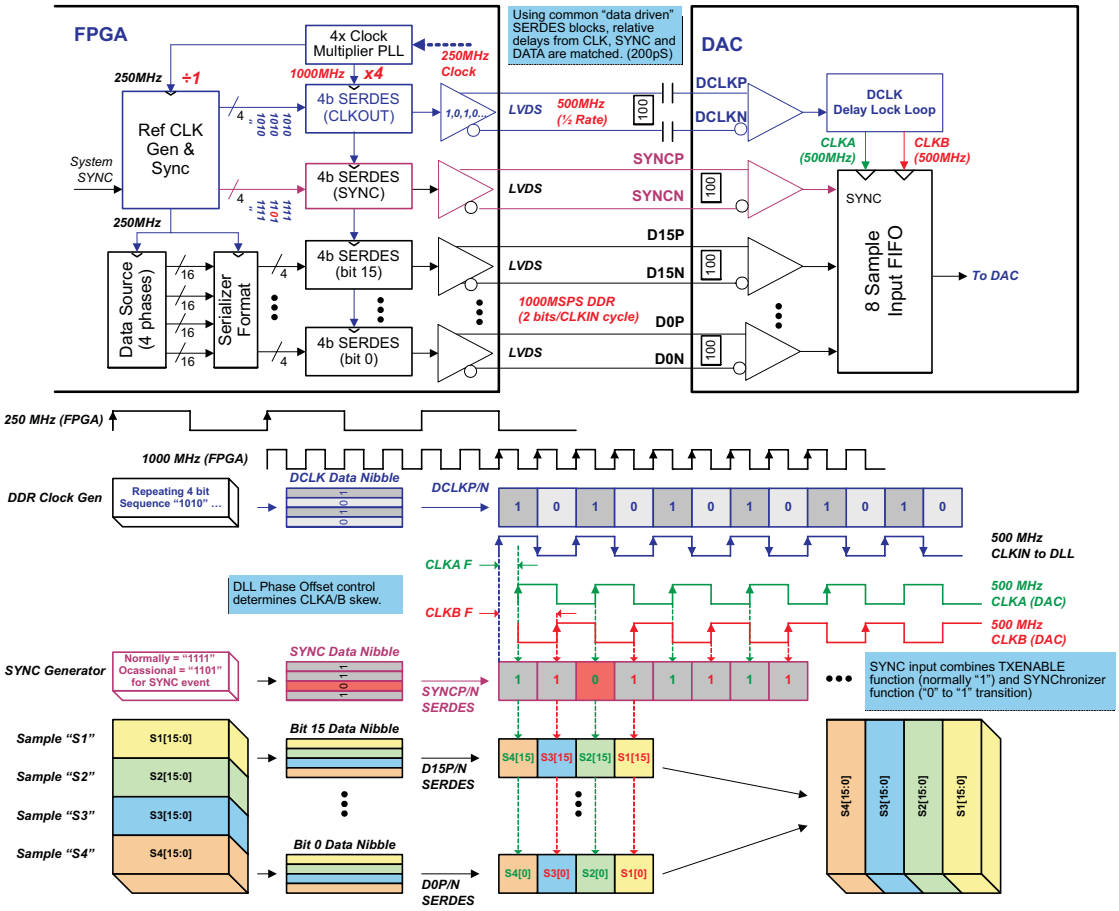

Figure 32. Example FPGA-Based LVDS Data Flow to DAC

8.3.5 LVDS Inputs

The D[15:0]P/N and SYNCP/N LVDS pairs have the input configuration shown in Figure 33. Figure 34 shows the typical input levels and common-mode voltage used to drive these inputs.

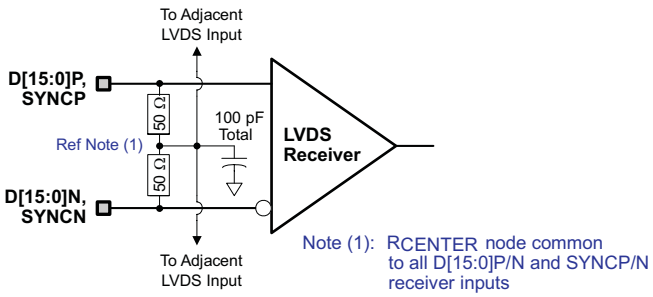

Figure 33. D[15:0]P/N and SYNCP/N LVDS Input Configuration

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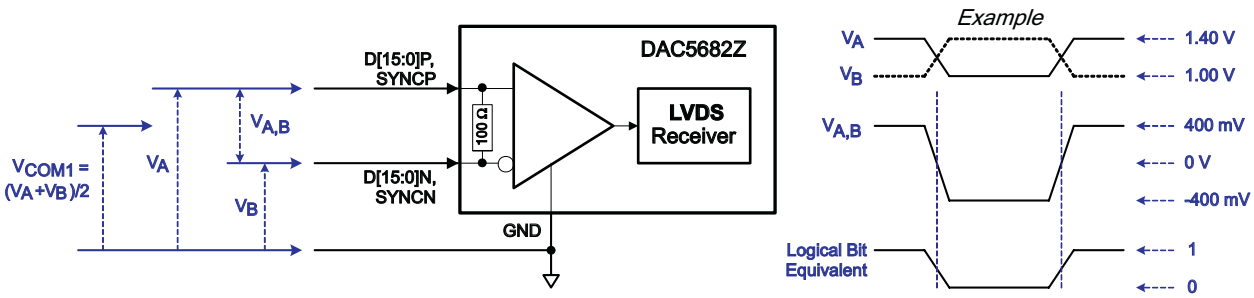

Figure 34. LVDS Data (DxP/N, D[15:0]P/N SYNCP/N Pairs) Input Levels

Table 4. Example LVDS Data Input Levels

APPLIED VOLTAGES		RESULTING DEFERENTIAL VOLTAGE	RESULTING COMMON-MODE VOLTAGE	LOGICAL BIT BINARY EQUIVALENT
V_A	V_B	$V_{A,B}$	V_{COM1}	
1.4 V	1.0 V	400 mV	1.2 V	1
1.0 V	1.4 V	–400 mV		0
1.2 V	0.8 V	400 mV	1.0 V	1
0.8 V	1.2 V	–400 mV		0

Figure 35 shows the DCLKP/N LVDS clock input levels. Unlike the D[15:0]P/N and SYNCP/N LVDS pairs, the DCLKP/N pair does not have an internal resistor and the common-mode voltage is self-biased to approximately DVDD/2 in order to optimize the operation of the DLL circuit. For proper external termination a 100-Ω resistor needs to be connected across the LVDS clock source lines followed by series 0.01-µF capacitors connected to each of the DCLKP and DCLKN pairs. For best performance, the resistor and capacitors should be placed as close as possible to these pins.

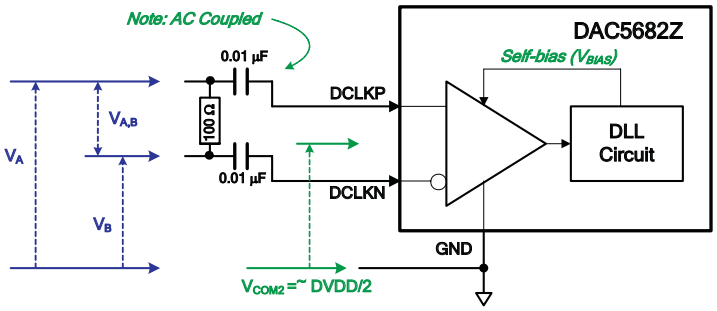

Figure 35. LVDS Clock (DCLKP/N) Input Levels

8.3.6 LVDS SYNCP/N Operation

The SYNCP/N LVDS input control functions as a combination of Transmit Enable (TXENABLE) and Synchronization trigger. If SYNCP is low, the transmit chain is disabled so input data from the FIFO is ignored while zero amplitude samples are inserted into the data path. If SYNCP is raised from low to high, a synchronization event occurs with behavior defined by individual control bits in registers CONFIG1 and CONFIG5. The SYNCP/N control is sampled and input into the FIFO along with the other LVDS data to maintain timing alignment with the data bus. Refer to Figure 32.

The software_sync_sel and software_sync controls in CONFIG3 provide a substitute for external SYNCP/N control; however, because the serial interface is used, no timing control is provided with respect to the DAC clock.

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8.3.7 DLL Operation

The DAC5682Z provides a digital delay lock loop (DLL) to skew the LVDS data clock (DCLK) relative to the data bits, D[15:0] and SYNC, in order to maintain proper setup and hold timing. Because the DLL operates closed-loop, it requires a stable DCLK to maintain delay lock. Refer to the description of DLL_ifixed(2:0) and DLL_delay(3:0) control bits in the CONFIG10 register. Prior to initializing the DLL, the DLL_ifixed value should be programmed to match the expected DCLK frequency range. To initialize the DLL, refer to the DLL_Restart programming bit in the CONFIG8 register. After initialization, the status of the DLL can be verified by reading the DLL_Lock bit from STATUS0. See *Recommended Start-up Sequence* below.

8.3.8 CMOS Digital Inputs

Figure 36 shows a schematic of the equivalent CMOS digital inputs of the DAC5682Z. SDIO and SCLK have pulldown resistors while RESETB and SDENB have pullup resistors internal the DAC5682Z. See the specification table for logic thresholds. The pullup and pulldown circuitry is approximately equivalent to 100kΩ.

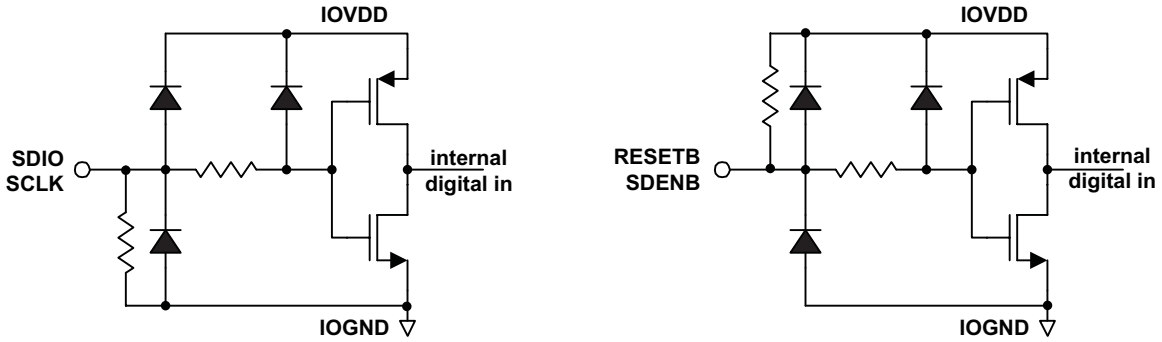

Figure 36. CMOS/TTL Digital Equivalent Input

8.3.9 Reference Operation

The DAC5682Z uses a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{EXTIO} / R_{BIAS} \quad (1)$$

Each DAC has a 4-bit independent coarse gain control via DACA_gain(3:0) and DACB_gain(3:0) in the CONFIG7 register. Using gain control, the IOUTFS can be expressed as:

$$IOUTA_{FS} = (DACA_gain + 1) \times I_{BIAS} = (DACA_gain + 1) \times V_{EXTIO} / R_{BIAS} \quad (2)$$

$$IOUTB_{FS} = (DACB_gain + 1) \times I_{BIAS} = (DACB_gain + 1) \times V_{EXTIO} / R_{BIAS} \quad (3)$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor C_{EXT} of 0.1 µF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor CEXT may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB.

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8.3.10 DAC Transfer Function

The CMOS DAC's consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUT1 or IOUT2. (DACA = IOUTA1 or IOUTA2 and DACB = IOUTB1 or IOUTB2.) Complementary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (+1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times I_{BIAS}.

The relation between IOUT1 and IOUT2 can be expressed as:

$$IOUT1 = – IOUT_{FS} – IOUT2 \quad (4)$$

We will denote current flowing into a node as – current and current flowing out of a node as + current. Because the output stage is a current sink the current can only flow from AVDD into the IOUT1 and IOUT2 pins. The output current flow in each pin driving a resistive load can be expressed as:

$$IOUT1 = IOUT_{FS} \times (65536 – CODE) / 65536 \quad (5)$$

$$IOUT2 = IOUT_{FS} \times CODE / 65536 \quad (6)$$

where CODE is the decimal representation of the DAC data input word.

For the case where IOUT1 and IOUT2 drive resistor loads R_L directly, this translates into single ended voltages at IOUT1 and IOUT2:

$$VOUT1 = AVDD – | IOUT1 | \times R_L \quad (7)$$

$$VOUT2 = AVDD – | IOUT2 | \times R_L \quad (8)$$

Assuming that the data is full scale (65536 in offset binary notation) and the R_L is 25 Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as:

$$VOUT1 = AVDD – | –0 \text{ mA} | \times 25\ \Omega = 3.3 \text{ V} \quad (9)$$

$$VOUT2 = AVDD – | –20 \text{ mA} | \times 25\ \Omega = 2.8 \text{ V} \quad (10)$$

$$VDIFF = VOUT1 – VOUT2 = 0.5 \text{ V} \quad (11)$$

Do not exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

8.3.11 DAC Output SINC Response

Due to sampled nature of a high-speed DAC, the well known sin(x)/x (or SINC) response can significantly attenuate higher frequency output signals. See the Figure 37 which shows the unitized SINC attenuation roll-off with respect to the final DAC sample rate in 4 Nyquist zones. For example, if the final DAC sample rate F_S = 1.0 GSPS, then a tone at 440MHz is attenuated by 3.0dB. Although the SINC response can create challenges in frequency planning, one side benefit is the natural attenuation of Nyquist images. The increased over-sampling ratio of the input data provided by the 2x and 4x digital interpolation modes of the DAC5682Z improve the SINC roll-off (droop) within the band of interest of the original signal.

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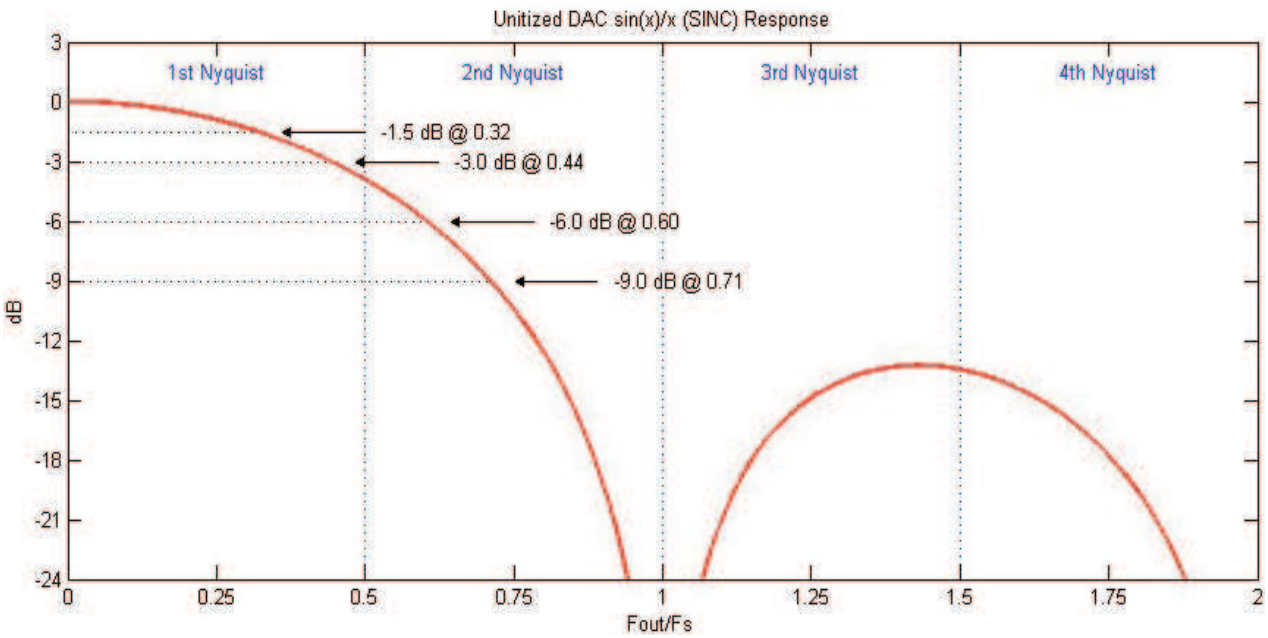

Figure 37. Unitized DAC sin(x)/x (SINC) Response

8.3.12 Analog Current Outputs

Figure 38 shows a simplified schematic of the current source array output with corresponding switches in a current sink configuration. Differential switches direct the current into either the positive output node, IOUT1, or its complement, IOUT2, then through the individual NMOS current sources. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referred to an external ground. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to AVDD – 0.5 V, determined by the CMOS process. Beyond this value, transistor breakdown may occur resulting in reduced reliability of the DAC5682Z device. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals AVDD + 0.5 V. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral non-linearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V.

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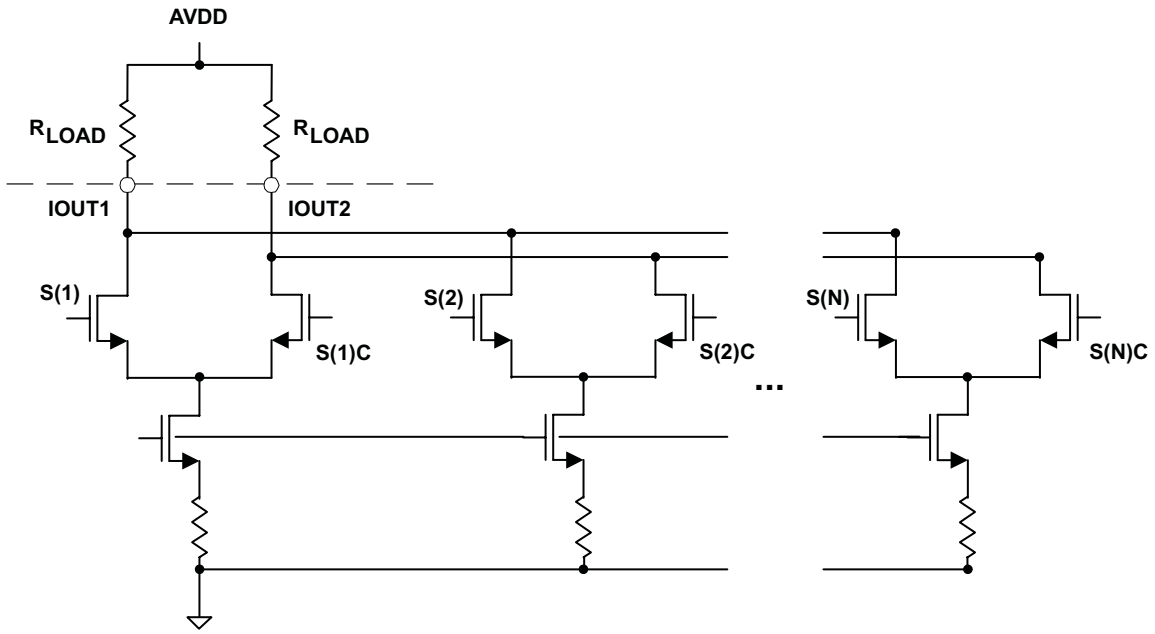

Figure 38. Equivalent Analog Current Output

The DAC5682Z can be easily configured to drive a doubly terminated 50Ω cable using a properly selected RF transformer. Figure 39 and Figure 40 show the 50Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. The center tap of the primary input of the transformer must be connected to AVDD to enable a dc current flow. Applying a 20-mA full-scale output current would lead to a 0.5 V_{PP} for a 1:1 transformer and a 1 V_{PP} output for a 4:1 transformer. The low dc-impedance between IOUT1 or IOUT2 and the transformer center tap sets the center of the ac-signal at AVDD, so the 1 V_{PP} output for the 4:1 transformer results in an output between AVDD + 0.5 V and AVDD – 0.5 V.

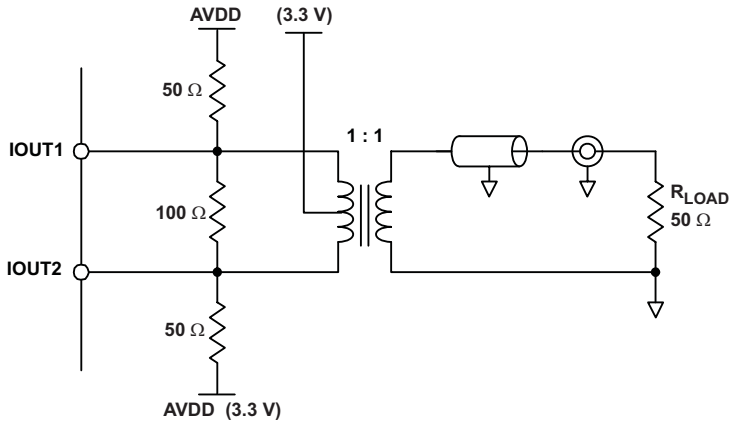

Figure 39. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

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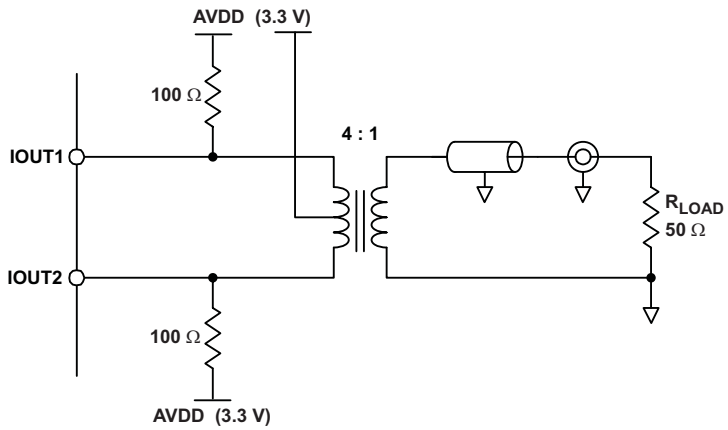

Figure 40. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

8.3.13 Designing the PLL Loop Filter

To minimize phase noise given for a given fDAC and M/N, the values of PLL_gain and PLL_range are selected so that G_{VCO} is minimized and within the MIN and MAX frequency for a given setting.

The external loop filter components C1, C2, and R1 are set by the G_{VCO}, M/N, the loop phase margin φ_d and the loop bandwidth ω_d. Except for applications where abrupt clock frequency changes require a fast PLL lock time, it is suggested that φ_d be set to at least 80 degrees for stable locking and suppression of the phase noise side lobes. Phase margins of 60 degrees or less can be sensitive to board layout and decoupling details.

See Figure 41, the recommend external loop filter topology. C1, C2, and R1 are calculated by the following equations:

$$C1 = \tau 1\left(1 - \frac{\tau 2}{\tau 3}\right) \qquad C2 = \frac{\tau 1 \times \tau 2}{\tau 3} \qquad R1 = \frac{\tau 3^2}{\tau 1(\tau 3 - \tau 2)} \tag{12}$$

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where,

$$\tau 1 = \frac{K_d K_{VCO}}{\omega_d^2}\left(\tan \Phi_d + \sec \Phi_d\right) \quad \tau 2 = \frac{1}{\omega_d\left(\tan \Phi_d + \sec \Phi_d\right)} \quad \tau 3 = \frac{\tan \Phi_d + \sec \Phi_d}{\omega_d} \tag{13}$$

charge pump current: iqp = 1 mA
vco gain: $K_{VCO} = 2\pi \times G_{VCO}$ rad/V
PFD Frequency: $\omega_d \leq 160$ MHz
phase detector gain: $K_d = iqp \div (2 \times \pi \times M)$ A/rad

An Excel spreadsheet is available from Texas Instruments for automatically calculating the values for C1, R1 and C2 in the *DAC5682 LPF Caluclator* (SLAC169).

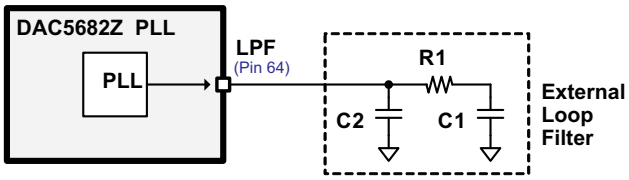

Figure 41. Recommended External Loop Filter Topology

8.3.14 Test Methodology

Typical AC specifications were characterized with the DAC5682ZEVM using the test configuration shown in Figure 42. A sinusoidal master clock frequency is generated by an HP8665B signal generator and into a splitter. One output drives an Agilent 8133A pulse generator, and the other drives the CDCM7005 clock driver. The 8133A converts the sinusoidal frequency into a square wave output clock and drives an Agilent ParBERT 81250A pattern-generator clock. On the EVM, the DAC5682Z CLKIN/C input clock is driven by an CDCM7005 clock distribution chip that is configured to simply buffer the external 8665B clock or divide it down for PLL test configurations.

The DAC5682Z output is characterized with a Rohde and Schwarz FSU spectrum analyzer. For WCDMA signal characterization, it is important to use a spectrum analyzer with high IP3 and noise subtraction capability so that the spectrum analyzer does not limit the ACPR measurement. For all specifications, both DACA and DACB are measured and the lowest value used as the specification.

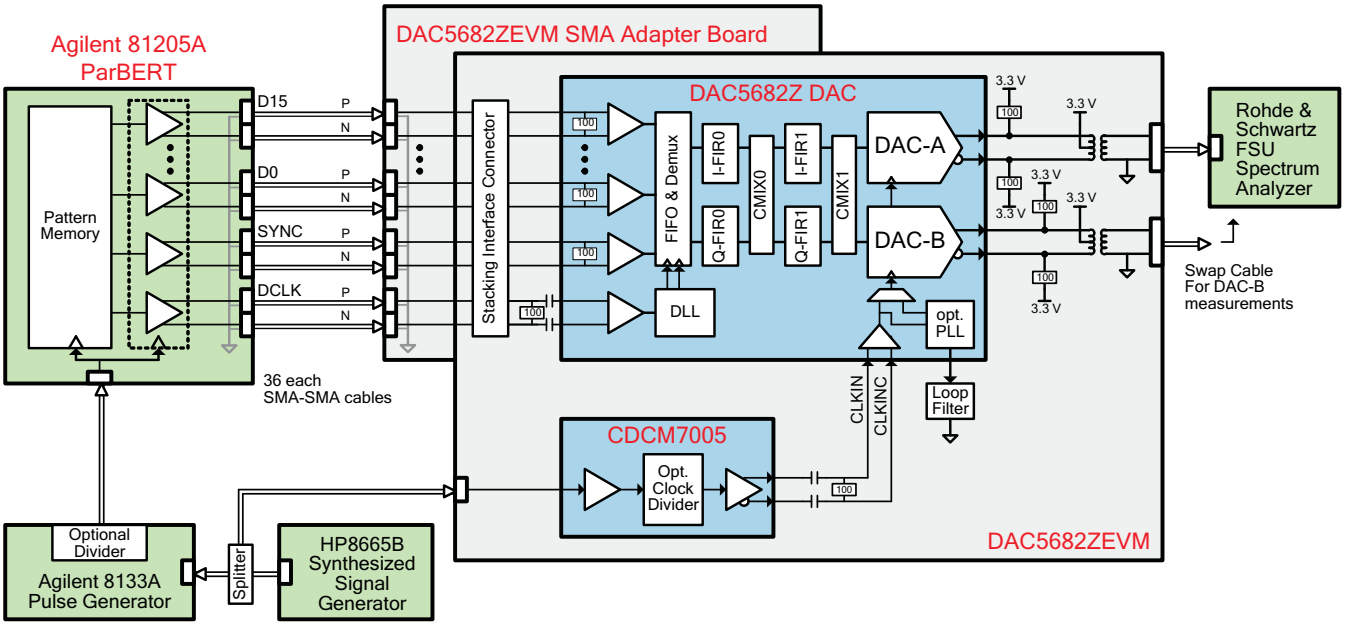

Figure 42. DAC5682Z Test Configuration for Normal Clock Mode

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8.4 Device Functional Modes

8.4.1 Dual-Channel Real Upconversion

The DAC5682Z can be used in a dual channel mode with real upconversion by mixing with a 1, –1, … sequence in the signal chain to invert the spectrum. This mixing mode maintains isolation of the A and B channels. The two points of mixing, CMIX0 and CMIX1, follow each FIR filter. The mixing modes for each CMIX block are controlled by CMIX0_mode(1:0) and CMIX1(1:0) in register CONFIG2. The wide bandwidths of both FIR0 and FIR1 (40% passband) provide options for setting the frequency ranges listed in Table 5. With the High Pass (2x2 HP mode), High Pass/Low Pass (2X4 HP/LP mode) and Low Pass/High Pass (2X4 LP/HP mode) settings, the upconverted signal is spectrally inverted.

Table 5. Dual-Channel Real Upconversion Options

MODE NAME	INTERP. FACTOR	FIR0, CMIX0 MODE	FIR1, CMIX1 MODE	INPUT FREQUENCY (1)	OUTPUT FREQUENCY (1)	SIGNAL BANDWIDTH (1)	SPECTRUM INVERTED?
2X2	X2	--	LP	0.0 to 0.4 × f_{DATA}	0.0 to 0.4 × f_{DATA}	0.4 × f_{DATA}	No
2X2 HP	X2	--	HP	0.0 to 0.4 × f_{DATA}	0.6 to 1.0 × f_{DATA}	0.4 × f_{DATA}	Yes
1X4	X4	LP	LP	0.0 to 0.4 × f_{DATA}	0.0 to 0.4 × f_{DATA}	0.4 × f_{DATA}	No
2X4	X4	LP	LP	0.0 to 0.4 × f_{DATA}	0.0 to 0.4 × f_{DATA}	0.4 × f_{DATA}	No
2X4 HP/LP	X4	HP	LP	0.2 to 0.4 × f_{DATA}	0.6 to 0.8 × f_{DATA}	0.2 × f_{DATA}	Yes
2X4 HP/HP	X4	HP	HP	0.2 to 0.4 × f_{DATA}	1.2 to 1.4 × f_{DATA}	0.2 × f_{DATA}	No
2X4 LP/HP	X4	LP	HP	0.0 to 0.4 × f_{DATA}	1.6 to 2.0 × f_{DATA}	0.4 × f_{DATA}	Yes

(1) f_{DATA} is the input data rate of each channel after de-interleaving.

8.4.2 Clock and Data Modes

There are two modes of operation to drive the internal clocks on the DAC5682Z. Timing diagrams for both modes are shown in Figure 43. EXTERNAL CLOCK MODE accepts an external full-rate clock input on the CLKIN/CLKINC pins to drive the DACs and final logic stages while distributing an internally divided down clock for lower speed logic such as the interpolating FIRs. PLL CLOCK MODE uses an internal clock multiplying PLL to derive the full-rate clock from an external lower rate reference frequency on the CLKIN/CLKINC pins. In both modes, an LVDS half-rate data clock (DCLKP/DCLKN) is provided by the user and is typically generated by a *toggling data bit* to maintain LVDS data to DCLK timing alignment. LVDS data relative to DCLK is input using Double Data Rate (DDR) switching using both rising and falling edges as shown in the both figures below. The CONFIG10 register contains user controlled settings for the DLL to adjust for the DCLK input frequency and various $\mathbf{t_{SKEW}}$ timing offsets between the LVDS data and DCLK. The CDCM7005 and CDCE62005 from Texas Instruments are recommended for providing phase aligned clocks at different frequencies for device-to-device clock distribution and multiple DAC synchronization.

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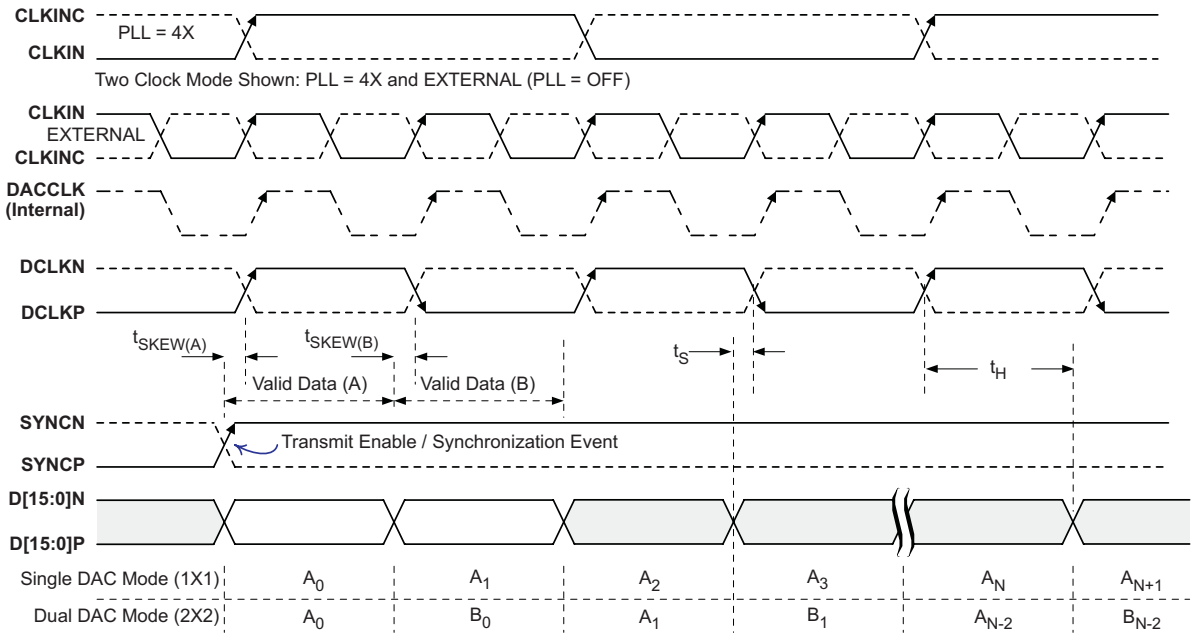

Figure 43. Clock and Data Timing Diagram

8.4.3 PLL Clock Mode

In PLL Clock Mode, the user provides an external reference clock to the CLKIN/C input pins. Refer to Figure 44. An internal clock multiplying PLL uses the lower-rate reference clock to generate a high-rate clock for the DAC. This function is very useful when a high-rate clock is not already available at the system level; however, the internal VCO phase noise in PLL Clock Mode may degrade the quality of the DAC output signal when compared to an external low jitter clock source.

The internal PLL has a type four phase-frequency detector (PFD) comparing the CLKIN/C reference clock with a feedback clock to drive a charge pump controlling the VCO operating voltage and maintaining synchronization between the two clocks. An external low-pass filter is required to control the loop response of the PLL. See *Designing the PLL Loop Filter* for the filter setting calculations. This is the only mode where the LPF filter applies.

The input reference clock N-Divider is selected by CONFIG9 **PLL_n(2:0)** for values of ÷1, ÷2, ÷4 or ÷8. The VCO feedback clock M-Divider is selected by CONFIG9 **PLL_m(4:0)** for values of ÷1, ÷2, ÷4, ÷8, ÷16 or ÷32. The combination of M-Divider and N-Divider form the clock multiplying ratio of M/N. If the reference clock frequency is greater than 160 MHz, use a N-Divider of ÷2, ÷4 or ÷8 to avoid exceeding the maximum PFD operating frequency.

For DAC sample rates less than 500MHz, the phase noise of DAC clock signal can be improved by programming the PLL for twice the desired DAC clock frequency, and setting the CONFIG11 **VCO_div2** bit. If not using the PLL, set CONFIG5 **PLL_bypass** and CONFIG6 **PLL_sleep** to reduce power consumption. In some cases, it may be useful to reset the VCO control voltage by toggling CONFIG11 **PLL_LPF_reset**.

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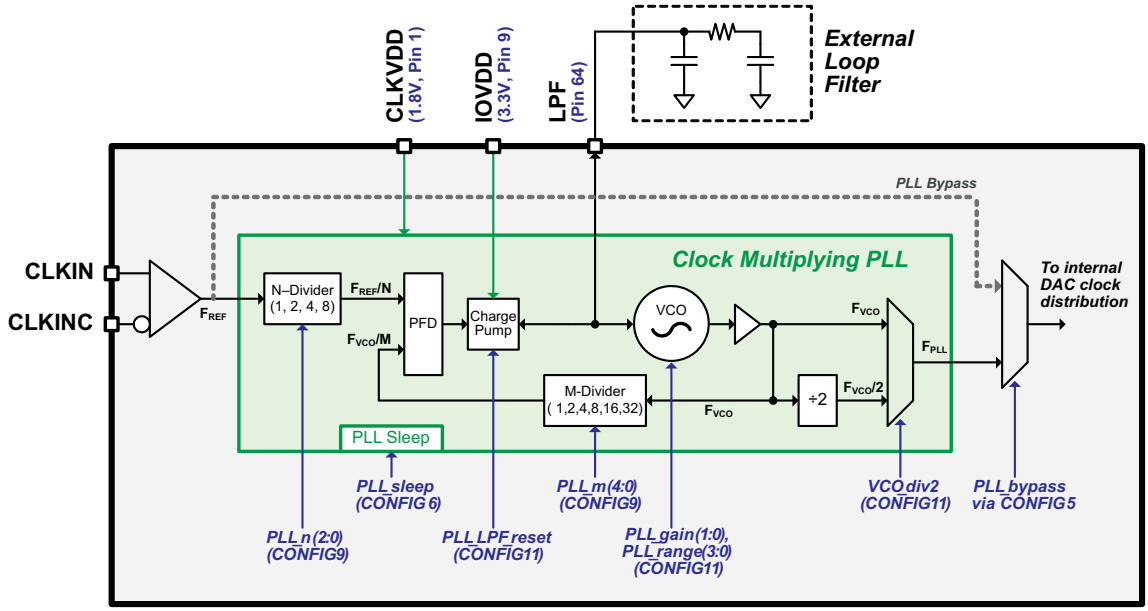

Figure 44. Functional Block Diagram for PLL

8.4.4 Recommended Multi-DAC Synchronization Procedure

The DAC5682Z provides a mechanism to synchronize multiple DAC devices in a system. The procedure has two steps involving control of the CONFIG5 **clkdiv_sync_dis** as well as external control of the LVDS SYNCP/N input. (All DACs involved need to be configured to accept the external SYNCP/N input and not "software" sync mode).

1. Synchronize Clock Dividers (for each DAC):
   (a) Set CONFIG5 **clkdiv_sync_dis** = 0.
   (b) Toggle SYNCP/N input to all DACs simultaneously (same input to all DACs).
2. Synchronize FIFO pointers (for each DAC):
   (a) Set CONFIG5 **clkdiv_sync_dis** = 1 (Disable clock divider re-sync).
   (b) Wait a minimum of 50 CLKIN cycles from previous SYNCP/N toggle. In practice, the time required to write the above register value will typically occupy more than 50 cycles.
   (c) Assert SYNCP/N input and hold at 1 to all DACs simultaneously. Holding this at 1 is effectively the TXENABLE for the chip so data will be output on the analog pins.
3. After the normal pipeline delay of the device, the outputs of all DACs will be synchronized to within ±1 DAC clock cycle.

8.4.5 Digital Self Test Mode

The DAC5682Z has a Digital Self Test (SLFTST) mode to designed to enable board level testing without requiring specific input data test patterns. The SLFTST mode is enabled via the CONFIG1 **SLFTST_ena** bit and results are only valid when CONFIG3 **SLFTST_err_mask** bit is cleared. An internal Linear Feedback Shift Register (LFSR) is used to generate the input test patterns for the full test cycle while a checksum result is computed on the digital signal chain outputs. The LVDS input data bus is ignored in SLFTST mode. After the test cycle completes, if the checksum result does not match a hardwired comparison value, the STATUS4 **SLFTST_err** bit is set and will remain set until cleared by writing a ‘0’ to the **SLFTST_err** bit. A full self test cycle requires no more than 400,000 CLKIN/C clock cycles to complete and will automatically repeat until the **SLFTEST_ena** bit is cleared.

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To initiate a the Digital Self Test:

1. Provide a normal CLKIN/C input clock. (The PLL is not used in SLFTST mode)
2. Provide a RESETB pulse to perform a hardware reset on device.
3. Program the registers with the values shown in Table 6. These register values contain the settings to properly configure the SLFTST including **SLFTST_ena** and **SLFTST_err_mask** bits
4. Provide a '1' on the SYNCP/N input to initiate TXENABLE.
5. Wait at a minimum of 400,000 CLKIN/C cycles for the SLFTST to complete. Example: If CLKIN = 1GHz, then the wait period is 400,000 × 1 / 1GHz = 400 µSec.
6. Read STATUS4 **SLFTST_err** bit. If set, a self test error has occurred. The **SLFTST_err** status may optionally be programmed to output on the SDO pin if using the 3-bit SIF interface. See Table 6 Note (1).
7. (Optional) The SLFTST function automatically repeats until **SLFTST_ena** bit is cleared. To the loop the test, write a '0' to STATUS4 **SLFTST_err** to clear previous errors and continue at step 5 above.
8. To continue normal operating mode, provide another RESETB pulse and reprogram registers to the desired normal settings.

Table 6. Digital Self Test (SLFTST) Register Values

REGISTER	ADDRESS (hex)	VALUE (Binary)	VALUE (Hex)
CONFIG1	01	00011000	18
CONFIG2	02	11101010	EA
CONFIG3	03	10110000	B0
STATUS4	04	00000000	00
CONFIG5	05	00000110	06
CONFIG6	06	00001111	0F
CONFIG12	0C	00001010	0A
CONFIG13	0D	01010101	55
CONFIG14 (1)	0E	00001010	0A
CONFIG15	0F	10101010	AA
All others	–	Default	Default

(1) If using a 3-bit SIF interface, the SDO pin can be programmed to report **SLFTST_err** status via the **SDO_fun_sel(2:0)** bits. In this case, set CONFIG14 = '10101010' or AA hex.

8.5 Programming

8.5.1 Serial Interface

The serial port of the DAC5682Z is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC5682Z. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by **SIF4** in register **CONFIG5**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For 3 pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For 4 pin configuration, **SDIO** is data in only and **SDO** is data out only. Data is input into the device with the rising edge of **SCLK**. Data is output from the device on the falling edge of **SCLK.**

Each read/write operation is framed by signal **SDENB** (Serial Data Enable Bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data. indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 to 5 comprise the data transfer cycle.

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

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R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC5682Z and a low indicates a write operation to DAC5682Z.

[N1 : N0] Identifies the number of data bytes to be transferred per Table 5 below. Data is transferred MSB first.

Table 7. Number of Transferred Bytes Within One Communication Frame

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

[A4 : A0] Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the DAC5682Z MSB first and counts down for each byte.

Figure 45 shows the serial interface timing diagram for a DAC5682Z write operation. **SCLK** is the serial interface clock input to DAC5682Z. Serial data enable **SDENB** is an active low input to DAC5682Z. **SDIO** is serial data in. Input data to DAC5682Z is clocked on the rising edges of **SCLK**.

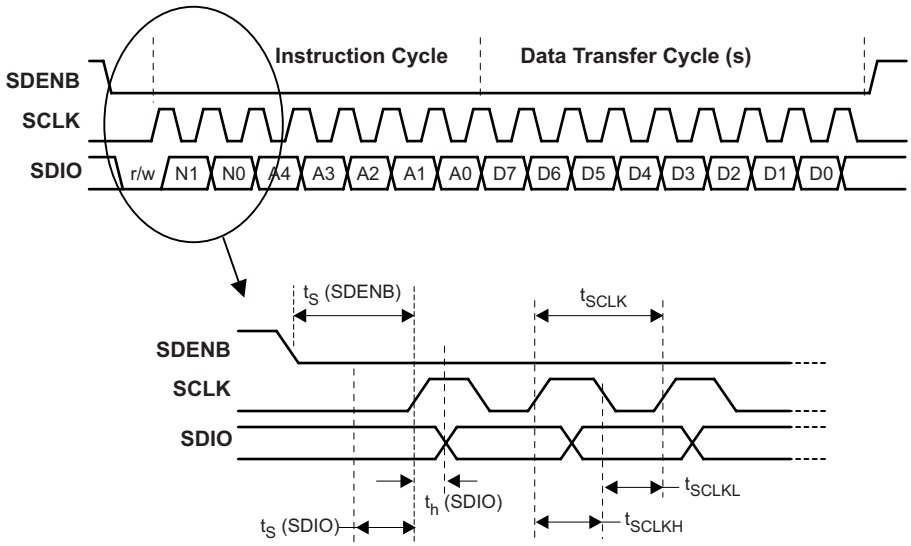

Figure 45. Serial Interface Write Timing Diagram

Figure 46 shows the serial interface timing diagram for a DAC5682Z read operation. **SCLK** is the serial interface clock input to DAC5682Z. Serial data enable **SDENB** is an active low input to DAC5682Z. **SDIO** is serial data in during the instruction cycle. In 3 pin configuration, **SDIO** is data out from DAC5682Z during the data transfer cycle(s), while **SDO** is in a high-impedance state. In 4 pin configuration, **SDO** is data out from DAC5682Z during the data transfer cycle(s). At the end of the data transfer, SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when it will 3-state.

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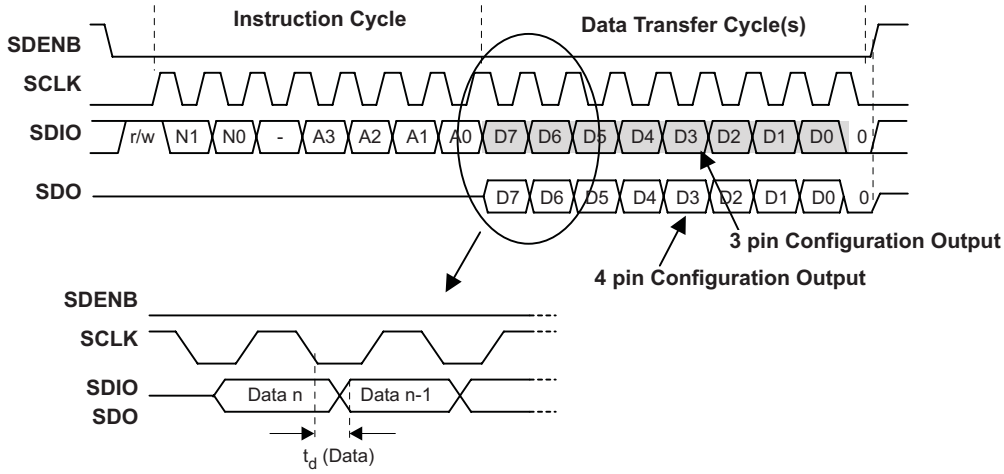

Figure 46. Serial Interface Read Timing Diagram

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8.6 Register Maps

The primary modes of operation, listed in Table 8, are selected by registers CONFIG1, CONFIG2, and CONFIG3.

Table 8. DAC5682Z Modes of Operation

Mode Name	No. of DACs Out	Interp. Factor	FIR0, CMIX0 Mode	FIR1, CMIX1 Mode	Device Config.	LVDS Input Data Mode	Max CLKIN Freq (MHz)(1)	Max DCLK Freq [DDR] (MHz)	Max Total Input Bus Rate (MSPS)	Max Input Data Rate Per Chan (#Ch @ MSPS)	Max Signal BW Per DAC (MHz) (2)
1X1 (Bypass)	1	X1	–	–	Single Real	A	1000	500	1000	1 at 1000	500
1X2	1	X2	–	LP	Single Real	A	1000	250	500	1 at 500	200
1X2 HP	1	X2	–	HP	Single Real	A	1000	250	500	1 at 500	200
1X4	1	X4	LP	LP	Single Real	A	1000	125	250	1 at 250	100
1X4 LP/HP	1	X4	LP	HP	Single Real	A	1000	125	250	1 at 250	100
1X4 HP/LP	1	X4	HP	LP	Single Real	A	1000	125	250	1 at 250	50
1X4 HP/HP	1	X4	HP	HP	Single Real	A	1000	125	250	1 at 250	50
2X1	2	X1	–	–	Dual Real	A/B	500	500	1000	2 at 500	250
2X2	2	X2	–	LP	Dual Real	A/B	1000	500	1000	2 at 500	200
2X2 HP	2	X2	–	HP	Dual Real	A/B	1000	500	1000	2 at 500	200
2X2 CMIX	2	X2	–	LP, Fs/4	Complex	A/B	1000	500	1000	2 at 500	200
2X4	2	X4	LP	LP	Dual Real	A/B	1000	250	500	2 at 250	100
2X4 LP/HP	2	X4	LP	HP	Dual Real	A/B	1000	250	500	2 at 250	100
2X4 CMIX	2	X4	LP	LP, Fs/4	Complex	A/B	1000	250	500	2 at 250	100
2X4 HP/LP	2	X4	HP	LP	Dual Real	A/B	1000	250	500	2 at 250	50
2X4 HP/HP	2	X4	HP	HP	Dual Real	A/B	1000	250	500	2 at 250	50

(1) Also the final DAC sample rate in MSPS.
(2) Assumes a 40% passband for FIR0 and/or FIR1 filters in all modes except 1X1 and 2X1 where simple Nyquist frequency is listed. Slightly wider bandwidths may be achievable depending on filtering requirements. Refer to *FIR Filters* section for more detail on filter characteristics. Also refer to Table 5 for IF placement and upconversion considerations.

Table 9. Register Map

Name	Address	Default	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0
STATUS0	0x00	0x03	PLL_lock	DLL_lock	Unused	device_ID(2:0)			version(1:0)	
CONFIG1	0x01	0x10	DAC_delay(1:0)		Unused	fir_ena	SLFTST _ena	FIFO_offset(2:0)		
CONFIG2	0x02	0xC0	Twos_ comp	dual_DAC	FIR2x4x	Unused	CMIX1_mode(1:0)		CMIX0_mode(1:0)	
CONFIG3	0x03	0x70	DAC_offset _ena	SLFTST_err _mask	FIFO_err_ mask	Pattern_err _mask	SwapAB_ out	B_equals _A	SW_sync	SW_sync _sel
STATUS4	0x04	0x00	Unused	SLFTST_err	FIFO_err	Pattern_ err	Unused	Unused	Unused	Unused
CONFIG5	0x05	0x00	SIF4	rev_bus	clkdiv_ sync_dis	Reserved	Reserved	DLL_ bypass	PLL_ bypass	Reserved
CONFIG6	0x06	0x0C	Reserved	Unused	Sleep_B	Sleep_A	BiasLPF_A	BiasLPF_B	PLL_ sleep	DLL_ sleep
CONFIG7	0x07	0xFF	DACA_gain(3:0)				DACB_gain(3:0)			
CONFIG8	0x08	0x00	Reserved					DLL_ restart	Reserved	
CONFIG9	0x09	0x00	PLL_m(4:0)					PLL_n(2:0)		
CONFIG10	0x0A	0x00	DLL_delay(3:0)				DLL_invclk	DLL_ifixed(2:0)		
CONFIG11	0x0B	0x00	PLL_LPF _reset	VCO_div2	PLL_gain(1:0)		PLL_range(3:0)			
CONFIG12	0x0C	0x00	Reserved(1:0)		Offset_sync	OffsetA(12:8)				
CONFIG13	0x0D	0x00	OffsetA(7:0)							
CONFIG14	0x0E	0x00	SDO_func_sel(2:0)			OffsetB(12:8)				
CONFIG15	0x0F	0x00	OffsetB(7:0)							

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8.6.1 Register Name: STATUS0 – Address: 0x00, Default = 0x03

7	6	5	4	3	2	1	0
PLL_lock	DLL_lock	Unused	device_ID(2:0)			version(1:0)	
0	0	0	0	0	0	1	1

PLL_lock: Asserted when the internal PLL is locked. (**Read Only**)

DLL_lock: Asserted when the internal DLL is locked. Once the DLL is locked, this bit should remain a '1' unless the DCLK input clock is removed or abruptly changes frequency causing the DLL to fall out of lock. (**Read Only**)

device_ID(2:0): Returns '000' for DAC5682Z Device_ID code. (**ReadOnly**)

version(1:0): A hardwired register that contains the register set version of the chip. (**ReadOnly**)

version (1:0)	Identification
'01'	PG1.0 Initial Register Set
'10'	PG1.1 Register Set
'11'	Production Register Set

8.6.2 Register Name: CONFIG1 – Address: 0x01, Default = 0x10

7	6	5	4	3	2	1	0
DAC_delay(1:0)		Unused	FIR_ena	SLFTST_ena	FIFO_offset(2:0)		
0	0	0	1	0	0	0	0

DAC_delay(1:0): DAC data delay adjustment. (0–3 periods of the DAC clock) This can be used to adjust system level output timing. The same delay is applied to both DACA and DACB data paths.

FIR_ena: When set, the interpolation filters are enabled.

SLFTST_ena: When set, a Digital Self Test (SLFTST) of the core logic is enabled. Refer to *Digital Self Test Mode* for details on SLFTST operation.

FIFO_offset(2:0): Programs the output pointer location of the FIFO, allowing the input pointer to be shifted –4 to +3 positions upon SYNC. Default offset is 0 and is updated upon each sync event.

FIFO_offset(2:0)	Offset
011	+3
010	+2
001	+1
000	0
111	–1
110	–2
101	–3
100	–4

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8.6.3 Register Name: CONFIG2 – Address: 0x02, Default = 0xC0

7	6	5	4	3	2	1	0
Twos_comp	dual_DAC	FIR2x4x	Unused	CMIX1_mode(1:0)		CMIX0_mode(1:0)	
1	1	0	0	0	0	0	0

Twos_comp: When set (default) the input data format is expected to be 2's complement, otherwise offset binary format is expected.

dual_DAC: Selects between dual DAC mode (default) and single DAC mode. This bit is also used to select input interleaved data.

FIR2x4x: When set, 4X interpolation of the input data is performed, otherwise 2X interpolation.

CMIX1_mode(1:0): Determines the mode of FIR1 and final CMIX1 blocks. Settings apply to both A and B channels. Refer to Table 3 for a detailed description of CMIX1 modes.

Mode	CMIX1_mode(1)	CMIX1_mode(0)
Normal (Low Pass)	0	0
High Pass	0	1
$+F_{DAC}$ /4	1	0
$–F_{DAC}$/4	1	1

CMIX0_mode(1:0): Determines the mode of FIR0 and CMIX0 blocks. Because CMIX0 is located between FIR0 and FIR1, its output is half-rate. Refer to Table 2 for a detailed description of CMIX0 modes. The table below shows the effective Fs/4 or ±Fs/8 mixing with respect to the final DAC sample rate. Settings apply to both A and B channels.

Mode	CMIX1_mode(1)	CMIX1_mode(0)
Normal (Low Pass)	0	0
High Pass	0	1
$+F_{DAC}$ /8	1	0
$–F_{DAC}$/8	1	1

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8.6.4 Register Name: CONFIG3 – Address: 0x03, Default = 0x70

7	6	5	4	3	2	1	0
DAC_offset _ena	SLFTST_err _mask	FIFO_err_ mask	Pattern_err_ mask	SwapAB_out	B_equals_A	SW_sync	SW_sync_sel
0	1	1	1	0	0	0	0

DAC_offset_ena: When set, the values of **OffsetA(12:0)** and **OffsetB(12:0)** in CONFIG12 through CONFIG15 registers are summed into the DAC-A and DAC-B data paths. This provides a system-level offset adjustment capability that is independent of the input data.

SLFTST_err_mask: When set, masks out the **SLFTST_err** bit in STATUS4 register. Refer to *Digital Self Test Mode* for details on SLFTST operation.

FIFO_err_mask: When set, masks out the **FIFO_err** bit in STATUS4 register.

Pattern_err_mask: When set, masks out the **Pattern err** bit in STATUS4 register.

SwapAB_out: When set, the A/B data paths are swapped prior to routing to the DAC-A and DAC-B outputs.

B_equals_A: When set, the data routed to DAC-A is also routed to DAC-B. This allows wire OR'ing of the two DAC outputs together at the board level to create a 2X drive strength single DAC output.

SW_sync: This bit can be used as a substitute for the LVDS external SYNC input pins for both synchronization and transmit enable control.

SW_sync_sel: When set, the SW_sync bit is used as the only synchronization input and the LVDS external SYNC input pins are ignored.

8.6.5 Register Name: STATUS4 – Address: 0x04, Default = 0x00

7	6	5	4	3	2	1	0
Unused	SLFTST_err	FIFO_err	Pattern_err	Unused	Unused	Unused	Unused
0	0	0	0	0	0	0	0

SLFTST_err: Asserted when the Digital Self Test (SLFTST) fails. To clear the error, write a '0' to this register bit. This bit is also output on the SDO pin when the Self Test is enabled via **SLFTST_ena** control bit in CONFIG1. Refer to *Digital Self Test Mode* for details on SLFTST operation.

FIFO_err: Asserted when the FIFO pointers over run each other causing a sample to be missed. To clear the error, write a '0' to this register bit.

Pattern_err: A digital checkerboard pattern compare function is provided for board level confidence testing and DLL limit checks. If the **Pattern_err_mask** bit via CONFIG3 is cleared, logic is enabled to continuously monitor input FIFO data. Any received data pattern other than 0xAAAA or 0x5555 causes this bit to be set. To clear the error, flush out the previous pattern error by inputting at least 8 samples of the 0xAAAA and/or 0x5555, then write a '0' to this register bit.

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8.6.6 Register Name: CONFIG5 – Address: 0x05, Default = 0x00

7	6	5	4	3	2	1	0
SIF4	rev_bus	clkdiv_sync _dis	Reserved	Reserved	DLL_bypass	PLL_bypass	Reserved
0	0	0	0	0	0	0	0

SIF4: When set, the serial interface is in 4 pin mode, otherwise it is in 3 pin mode. Refer to **SDO_func_sel (2:0)** bits in CONFIG14 register for options available to output status indicator data on the SDO pin.

rev_bus: Reverses the LVDS input data bus so that the MSB to LSB order is swapped. This function is provided to ease board level layout and avoid wire crossovers in case the LVDS data source output bus is mirrored with respect to the input data bus of the DAC.

clkdiv_sync_dis: Disables the clock divider sync when this bit is set.

Reserved (Bit 4): Set to 0 for proper operation.

Reserved (Bit 3): Set to 0 for proper operation.

DLL_bypass: When set, the DLL is bypassed and the LVDS data source is responsible for providing correct setup and hold timing.

PLL_bypass: When set, the PLL is bypassed.

Reserved (Bit 0): Set to 0 for proper operation.

8.6.7 Register Name: CONFIG6 – Address: 0x06, Default = 0x0C

7	6	5	4	3	2	1	0
Reserved	Unused	Sleep_B	Sleep_A	BiasLPF_A	BiasLPF_B	PLL_sleep	DLL_sleep
0	0	0	0	1	1	0	0

Reserved (Bit 7): Set to 0 for proper operation.

Sleep_B: When set, DACB is put into sleep mode. DACB is not automatically set into sleep mode when configured for single DAC mode through **dual_DAC** bit in CONFIG2. Set this **Sleep_B** bit for the lowest power configuration in single DAC mode because output is on DACA only.

Sleep_A: When set, DACA is put into sleep mode.

BiasLPF_A: Enables a 95 kHz low pass filter corner on the DACA current source bias when cleared. If this bit is set, a 472 kHz filter corner is used.

BiasLPF_B: Enables a 95 kHz low pass filter corner on the DACB current source bias when cleared. If this bit is set, a 472 kHz filter corner is used.

PLL_sleep: When set, the PLL is put into sleep mode.

DLL_sleep: When set, the DLL is put into sleep mode.

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8.6.8 Register Name: CONFIG7 – Address: 0x07, Default = 0xFF

7	6	5	4	3	2	1	0
DACA_gain(3:0)				DACB_gain(3:0)			
1	1	1	1	1	1	1	1

DACA_gain(3:0): Scales DACA output current in 16 equal steps.

$$\frac{VEXTIO}{R_{bias}} \times (DACA_gain + 1)$$

DACB_gain(3:0): Same as above except for DACB.

8.6.9 Register Name: CONFIG8 – Address: 0x08, Default = 0x00

7	6	5	4	3	2	1	0
Reserved					DLL_restart	Reserved	
0	0	0	0	0	0	0	0

Reserved (7:3): Set to ‘00000’ for proper operation.

DLL_restart: This bit is used to restart the DLL. When this bit is set, the internal DLL loop filter is reset to zero volts, and the DLL delay line is held at the center of its bias range. When cleared, the DLL will acquire lock to the DCLK signal. A DLL restart is accomplished by setting this bit with a serial interface write, and then clearing this bit with another serial interface write. Any interruption in the DCLK signal or changes to the DLL programming in the CONFIG10 register must be followed by this DLL restart sequence. Also, when this bit is set, the **DLL_lock** indicator in the STATUS0 register is cleared.

Reserved (1:0): Set to ‘00’ for proper operation

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8.6.10 Register Name: CONFIG9 – Address: 0x09, Default = 0x00

7	6	5	4	3	2	1	0
PLL_m(4:0)					PLL_n(2:0)		
0	0	0	0	0	0	0	0

PLL_m: M portion of the M/N divider of the PLL thermometer encoded:

PLL_m(4:0)	M value
00000	1
00001	2
00011	4
00111	8
01111	16
11111	32
All other values	Invalid

PLL_n: N portion of the M/N divider of the PLL thermometer encoded. If supplying a high rate CLKIN frequency, the PLL_n value should be used to divide down the input CLKIN to maintain a maximum PFD operating of 160 MHz.

PLL_n(2:0)	N value
000	1
001	2
011	4
111	8
All other values	Invalid

PLL Function:

$$f_{vco} = \left[\frac{(M)}{(N)}\right] \times f_{ref}$$

where f_{ref} is the frequency of the external DAC clock input on the CLKIN/CLKINC pins.

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8.6.11 Register Name: CONFIG10 – Address: 0x0A, Default = 0x00

7	6	5	4	3	2	1	0
DLL_delay(3:0)				DLL_invclk	DLL_ifixed(2:0)		
0	0	0	0	0	0	0	0

DLL_delay(3:0): The DCLKP/N LVDS input data clock has a DLL to automatically skew the clock to LVDS data timing relationship, providing proper setup and hold times. **DLL_delay(3:0)** is used to manually adjust the DLL delay ± from the fixed delay set by **DLL_ifixed(2:0)**. Adjustment amounts are approximate.

DLL_delay(3:0)	Delay Adjust (degrees)
1000	50°
1001	55°
1010	60°
1011	65°
1100	70°
1101	75°
1110	80°
1111	85°
0000	90° (Default)
0001	95°
0010	100°
0011	105°
0100	110°
0101	115°
0110	120°
0111	125°

DLL_invclk: When set, used to invert an internal DLL clock to force convergence to a different solution. This can be used in the case where the DLL delay adjustment has exceeded the limits of its range.

DLL_ifixed(2:0): Adjusts the DLL delay line bias current. Refer to the Electrical Characteristics table. Used in conjunction with the DLL_invclk bit to select appropriate delay range for a given DCLK frequency:
'011' – maximum bias current and minimum delay range
'000' – mid scale bias current
'101' – minimum bias current and maximum delay range
'100' – do not use.

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8.6.12 Register Name: CONFIG11 – Address: 0x0B, Default = 0x00

7	6	5	4	3	2	1	0
PLL_LPF_ reset	VCO_div2	PLL_gain(1:0)		PLL_range(3:0)			
0	0	0	0	0	0	0	0

PLL_LPF_reset: When a logic high, the PLL loop filter (LPF) is pulled down to 0V. Toggle from ‘1’ to ‘0’ to restart the PLL if an over-speed lock-up occurs. Over-speed can happen when the process is fast, the supplies are higher than nominal, etc., resulting in the feedback dividers missing a clock.

VCO_div2: When set, the PLL CLOCK output is 1/2 the PLL VCO frequency. Used to run the VCO at 2X the needed clock frequency to reduce phase noise for lower input clock rates.

PLL_gain(1:0): Used to adjust the PLL Voltage Controlled Oscillator (VCO) gain, K_{VCO}. Refer to the Electrical Characteristics table. By increasing the **PLL_gain**, the VCO can cover a broader range of frequencies; however, the higher gain also increases the phase noise of the PLL. In general, lower **PLL_gain** settings result in lower phase noise. The K_{VCO} of the VCO can also affect the PLL stability and is used to determine the loop filter components. See section on determining the PLL filter components for more detail.

PLL_range(3:0): Programs the PLL VCO fixed bias current. Refer to the Electrical Characteristics table. This setting, in conjunction with the PLL_gain(1:0), sets the achievable frequency range of the PLL VCO:
'000' – minimum bias current and lowest VCO frequency range
'111' – maximum bias current and highest VCO frequency range

8.6.13 Register Name: CONFIG12 – Address: 0x0C, Default = 0x00

7	6	5	4	3	2	1	0
Reserved(1:0)		Offset_sync	OffsetA(12:8)				
0	0	0	0	0	0	0	0

Reserved(1:0): Set to ‘00’ for proper operation.

Offset_sync: On a change from ‘0’ to ‘1’ the values of the OffsetA(12:0) and OffsetB(12:0) control registers are transferred to the registers used in the DAC-A and DAC-B offset calculations. This double buffering allows complete control by the user as to when the change in the offset value occurs. This bit does not auto-clear. Prior to updating new offset values, it is recommended that the user clear this bit.

OffsetA(12:8): Upper 5 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

8.6.14 Register Name: CONFIG13 – Address: 0x0D, Default = 0x00

7	6	5	4	3	2	1	0
OffsetA(7:0)							
0	0	0	0	0	0	0	0

OffsetA(7:0): Lower 8 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

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8.6.15 Register Name: CONFIG14 – Address: 0x0E, Default = 0x00

7	6	5	4	3	2	1	0
SDO_func_sel(2:0)			OffsetB(12:8)				
0	0	0	0	0	0	0	0

SDO_func_sel(2:0): Selects the signal for output on the SDO pin. When using the 3 pin serial interface mode, this allows the user to multiplex several status indicators onto the SDO pin. In 4 pin serial interface mode, programming this register to view one of the 5 available status indicators will override normal SDO serial interface operation.

SDO_func_sel (2:0)	Output to SDO
000, 110, 111	Normal SDO function
001	PLL_lock
010	DLL_lock
011	Pattern_err
100	FIFO_err
101	SLFTST_err

OffsetB(12:8): Upper 5 bits of the offset adjustment value for the B data path. (**SYNCED via Offset_sync**)

8.6.16 Register Name: CONFIG15 – Address: 0x0F, Default = 0x00

7	6	5	4	3	2	1	0
OffsetB(7:0)							
0	0	0	0	0	0	0	0

OffsetB(7:0): Lower 8 bits of the offset adjustment value for the B data path. (**SYNCED via Offset_sync**)

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DAC5682z is a high-speed, wide bandwidth Digital-to-Analog converter. The dual DAC outputs can sample at 1Gsps allowing synthesis of complex IQ signals from -400 to 400 MHz with a complex bandwidth of up to 400 MHz. When the DAC is operated in single channel bypass mode, the maximum data rate is 1Gsps and can sustain a signal bandwidth of 500 MHz. The interpolation modes of the DAC allow the input baseband rates to be 2-4 times slower than the DAC output rate reducing the processing requirements of the digital baseband processor and simplifies the DAC image filtering requirements. The coarse mixing blocks within the DAC allow power efficient placement of the final carrier at the DAC output. Typically this dual DAC with its digital features is very well equipped for complex quadrature communications applications, however it is also suitable for use in applications that require arbitrary waveform generation.

9.2 Typical Application

A typical application for the DAC5682z is a wideband transmitter. The DAC is provided with some input digital baseband signal and it outputs an analog carrier. A typical configuration is described below.

- Dual DAC mode
- Datarate = 491.52 Msps (DCLK LVPECL or LVDS)
- 2x Interpolation
- External clock mode = 983.04 MHz (CLKIN LVPECL or LVDS)
- Input data = 4C WCDMA with IF frequency at 184.32 MHz
- AVDD/IOVDD = 3.3 V
- DVDD/CLKVDD=1.8 V
- SYNCP/N = LVDS "1"
- IOUTAP/N and IOUTBP/N to transformers

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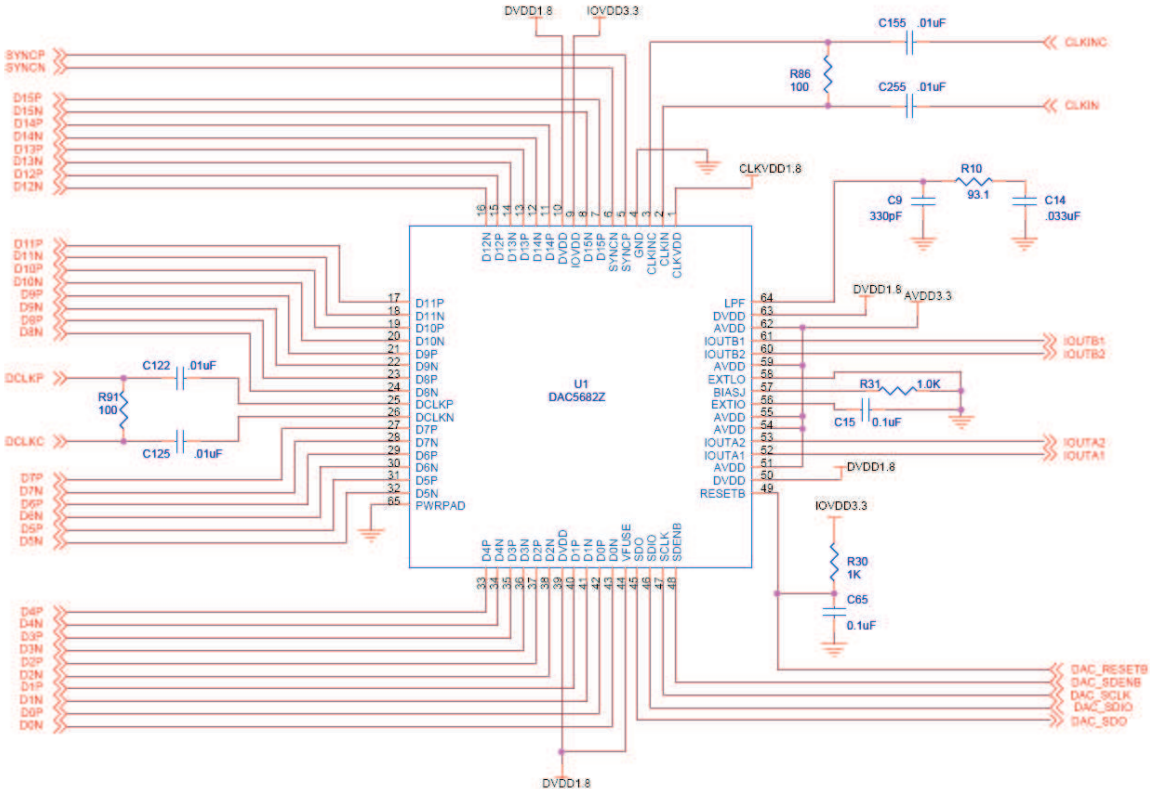
Typical Application (continued)



(1) Power supply decoupling capacitors not shown.

(2) Internal Reference configuration shown.

Figure 47. Typical Application Schematic

9.2.1 Design Requirements

The requirements for this design were to generate a 4-carrier WCDMA signal at an intermediate frequency of 184.32 MHz. The ACPR needs to be better than 65 dBc.

9.2.2 Detailed Design Procedure

The 4-carrier signal with an intermediate frequency of 184.32 MHz must be created in the digital processor at a sample rate of 491.52 Msps for channels A and B. These 16 bit samples must be interleaved into ABAB... format and placed on the 16b LVDS input port of the DAC.

A differential DAC clock must be generated from a clock source at 983.04 MHz and a data clock at 491.52 MHz. This must be provided to the CLKIN and DCLK pins of the DAC respectively.

The DAC register map must be reset, then programmed for 2x interpolation and external clock mode as per the data sheet. The digital sample format (2s complement or offset binary) must match the incoming data from the processor. The SYNC signal must he held high for the DAC to have an analog output.

The IOUOTA and IOUTB differential connections must be connected to a transformer to provide a single ended output. A typical 2:1 impedance transformer is used on the device EVM. The DAC5682zEVM provides a good reference for this design example.

9.2.3 Application Curves

This spectrum analyzer plot shows the ACPR for the transformer output using x2 interpolation, PLL Off mode. The results meet the system requirements for a minimum of 65 dBc ACPR.

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Typical Application (continued)

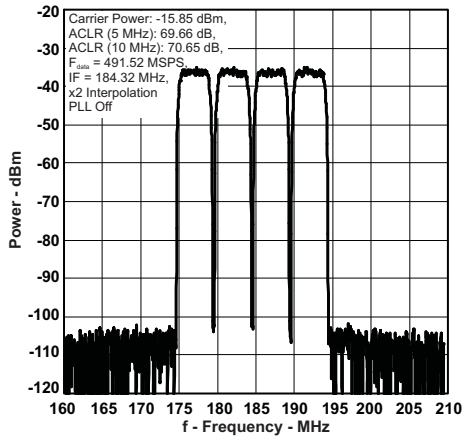

Figure 48. Four Carrier W-CDMA Test Model 1

9.3 System Examples

9.3.1 Digital Interface and Clocking Considerations for Application Examples

The DAC5682Z's LVDS digital input bus can be driven by an FPGA or digital ASIC. This input signal can be generated directly by the FPGA, or fed by a Texas Instruments Digital Up Converter (DUC) such as the GC5016 or GC5316. Optionally, a GC1115 Crest Factor Reduction (CFR) or Digital Pre-Distortion (DPD) processor may be inserted in the digital signal chain for improving the efficiency of high-power RF amplifiers. For the details on the high-rate digital interface of the DAC, refer to *LVDS Data Interfacing*.

A low phase noise clock for the DAC at the final sample rate can be generated by a VCXO and a Clock Synchronizer/PLL such as the Texas Instruments CDCM7005 or CDCE62005, which can also provide other system clocks. An optional system clocking solution can use the DAC in clock multiplying PLL mode in order to avoid distributing a high-frequency clock at the DAC sample rate; however, the internal VCO phase noise of the DAC in PLL mode may degrade the quality of the DAC output signal.

9.3.2 Single Complex Input, Real IF Output Radio

Refer to Figure 49 for an example Single Complex Input, Real IF Output Radio. The DAC5682Z receives an interleaved complex I/Q baseband input data stream and increases the sample rate through interpolation by a factor of 2 or 4. By performing digital interpolation on the input data, undesired images of the original signal can be push out of the band of interest and more easily suppressed with analog filters. Complex mixing is available at each stage of interpolation using the CMIX0 and CMIX1 blocks to up-convert the signal to a frequency placement at a multiples ±Fdac/8 or ±Fdac/4. Only the real portion of the digital signal is converted by DAC-A while DAC-B can be programmed to sleep mode for reduced power consumption. The DAC output signal would typically be terminated with a transformer (see *Analog Current Outputs*). An IF filter, either LC or SAW, is used to suppress the DAC Nyquist zone images and other spurious signals before being mixed to RF with a mixer. The TRF3671 Frequency Synthesizer, with integrated VCO, may be used to drive the LO input of the mixer for frequencies between 375 and 2380 MHz.

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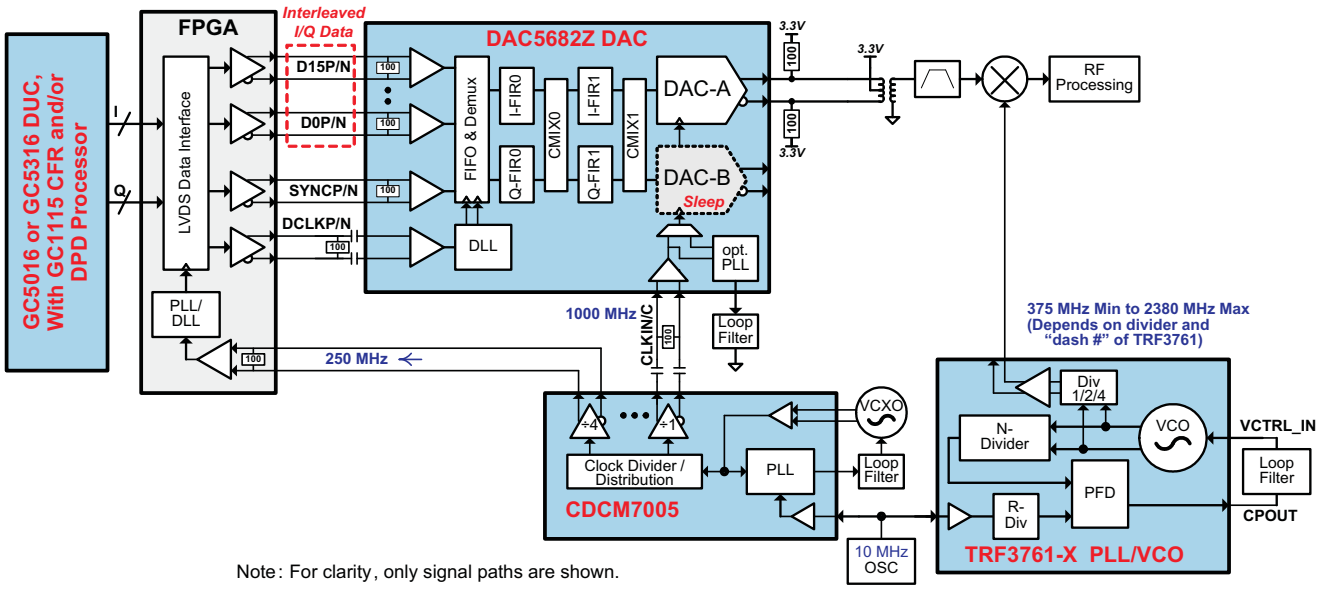
System Examples (continued)

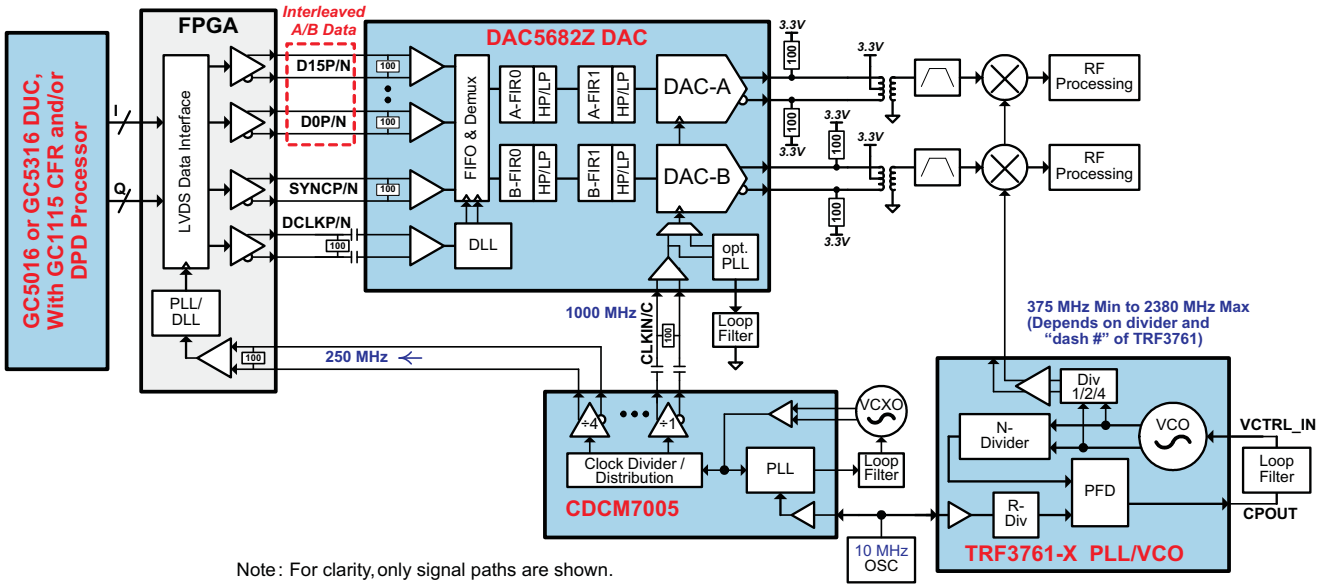


Note: For clarity, only signal paths are shown.

Figure 49. System Diagram of a Complex Input, Real IF Output Radio

9.3.3 Dual Channel Real IF Output Radio

Refer to Figure 50 for an example Dual-Channel Real IF Output Radio. The DAC5682Z receives an interleaved A/B input data stream and increases the sample rate through interpolation by a factor of 2 or 4. By performing digital interpolation on the input data, undesired images of the original signal can be push out of the band of interest and more easily suppressed with analog filters. Real mixing is available at each stage of interpolation using the CMIX0 and CMIX1 blocks to up-convert the signal (see *Dual-Channel Real Upconversion*). Both DAC output signals would typically be terminated with a transformer (see *Analog Current Outputs*). An IF filter, either LC or SAW, is used to suppress the DAC Nyquist zone images and other spurious signals before being mixed to RF with a mixer. The TRF3671 Frequency Synthesizer, with integrated VCO, may be used to drive a common LO input of the mixers for frequencies between 375 and 2380 MHz. Alternatively, two separate TRF3761 synthesizers could be used for independent final RF frequency placement.



Note: For clarity, only signal paths are shown.

Figure 50. System Diagram of a Dual-Channel Real IF Output Radio

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System Examples (continued)

9.3.4 Direct Conversion Radio

Refer to Figure 51 for an example Direct Conversion Radio. The DAC5682Z receives an interleaved complex I/Q baseband input data stream and increases the sample rate through interpolation by a factor of 2 or 4. By performing digital interpolation on the input data, undesired images of the original signal can be push out of the band of interest and more easily suppressed with analog filters.

For a Zero IF (ZIF) frequency plan, complex mixing of the baseband signal is not required. Alternatively, for a Complex IF frequency plan the input data can be placed at an pre-placed at an IF within the bandwidth limitations of the interpolation filters. In addition, complex mixing is available at each stage of interpolation using the CMIX0 and CMIX1 blocks to up-convert the signal to a frequency placement at a multiples ±Fdac/8 or ±Fdac/4. The output of both DAC channels is used to produce a Hilbert transform pair and can be expressed as:

$$A(t) = I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t)\ m(t) \quad (14)$$

$$A(t) = I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t)\ m_h(t) \quad (15)$$

where m(t) and mh(t) connote a Hilbert transform pair and ωc is the sum of the CMIX0 and CMIX1 frequencies. The complex output is input to an analog quadrature modulator (AQM) such as the Texas Instruments TRF3703-33 for a single side-band (SSB) up conversion to RF. A passive (resistor only) interface to the AQM is recommended, with an optional LC filter network. The TRF3671 Frequency Synthesizer with integrated VCO may be used to drive the LO input of the TRF3703-33 for frequencies between 375 and 2380 MHz. Upper single-sideband upconversion is achieved at the output of the analog quadrature modulator, whose output is expressed as:

$$RF(t) = I(t)\cos(\omega_c + \omega_{LO})t - Q(t)\sin(\omega_c + \omega_{LO})t \quad (16)$$

Flexibility is provided to the user by allowing for the selection of negative CMIX mixing sequences to produce a lower-sideband upconversion. Note that the process of complex mixing translates the signal frequency from 0 Hz means that the analog quadrature modulator IQ imbalance produces a sideband that falls outside the signal of interest. DC offset error in DAC and AQM signal path may produce LO feed-through at the RF output which may fall in the band of interest. To suppress the LO feed-through, the DAC5682Z provides a digital offset correction capability for both DAC-A and DAC-B paths. (See DAC_offset_ena bit in CONFIG3.)

The complex IF architecture has several advantages over the real IF architecture:

- Uncalibrated side-band suppression ~ 35 dBc compared to 0 dBc for real IF architecture.
- Direct DAC to AQM interface – no amplifiers required
- Nonharmonic clock-related spurious signals fall out-of-band
- DAC 2nd Nyquist zone image is offset f_{DAC} compared with f_{DAC}– 2 × IF for a real IF architecture, reducing the need for filtering at the DAC output.
- Uncalibrated LO feed through for AQM is ~ 35 dBc and calibration can reduce or completely remove the LO feed through.

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System Examples (continued)

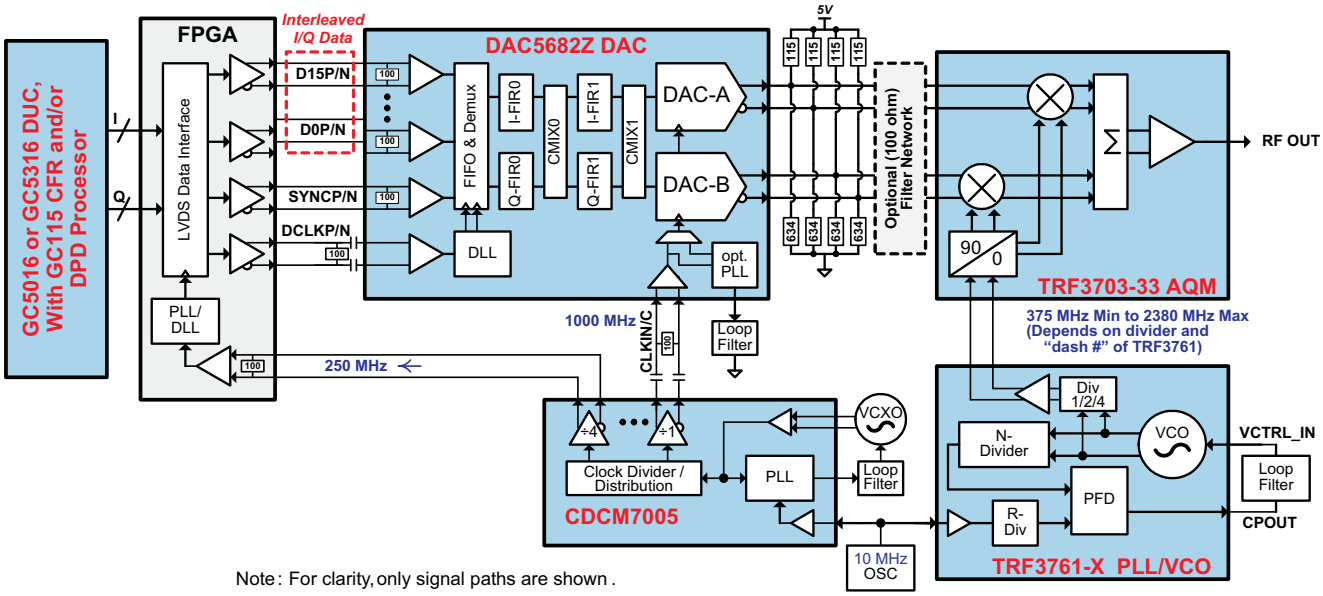

Figure 51. System Diagram of Direct Conversion Radio

9.3.5 CMTS/VOD Transmitter

The exceptional SNR of the DAC5682Z enables a dual-cable modem termination system (CMTS) or video on demand (VOD) QAM transmitter in excess of the stringent DOCSIS specification, with >74 dBc and 75 dBc in the adjacent and alternate channels.

Refer to Figure 50 for an example Dual Channel Real IF Output Radio – this signal chain is nearly identical to a typical system using the DAC5682Z for a cost optimized dual channel two QAM transmitter. A GC5016 would take four separate symbol rate inputs and provide pulse shaping and interpolation to ~ 128 MSPS. The four QAM carriers would be combined into two groups of two QAM carriers with intermediate frequencies of approximately 30 MHz to 40 MHz. The GC5016 would output two real data streams to one DAC5682Z through an FPGA for CMOS to LVDS translation. The DAC5682Z would function as a dual-channel device and provide 2x or 4x interpolation to increase the frequency of the 2nd Nyquist zone image. The two signals are then output through the two DAC outputs, through a transformer and to an RF upconverter.

9.3.6 High-Speed Arbitrary Waveform Generator

The 1GSPS bandwidth input data bus combined with the 16-bit DAC resolution of the DAC5682Z allows wideband signal generation for test and measurement applications. In this case, interpolation is not desired by the FPGA-based waveform generator as it can make use of the full Nyquist bandwidth of up to 500MHz.

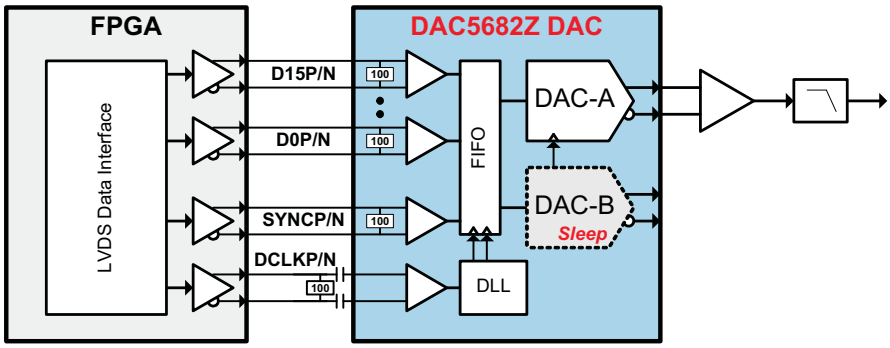

Figure 52. System Diagram of Arbitrary Waveform Generator

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9.4 Initialization Set Up

9.4.1 Recommended Start-up Sequence

The following start-up sequence is recommended to initialize the DAC5682Z:

1. Supply all 1.8 V (CLKVDD, DVDD, VFUSE) voltages simultaneously followed by all 3.3 V (AVDD and IOVDD) voltages.
2. Provide stable CLKIN/C clock.
3. Toggle RESETB pin for a minimum 25 nSec active low pulse width.
4. Program all desired SIF registers. Set **DLL_Restart** bit during this write cycle. The CONFIG10 register value should match the corresponding DCLKP/N frequency range in the Electrical Characteristics table.
5. Provide stable DCLKP/N clock. (This can also be provided earlier in the sequence)
6. Clear the **DLL_Restart** bit when the DCLKP/N clock is expected to be stable.
7. Verify the status of **DLL_Lock** and repeat until set to ‘1’. **DLL_Lock** can be monitored by reading the STATUS0 register or by monitoring the SDO pin in 3-wire SIF mode. (See description for CONFIG14 **SDO_func_sel**.)
8. Enable transmit of data by asserting the LVDS SYNCP/N input or setting CONFIG3 **SW_sync** bit. (See description for CONFIG3 **SW_sync** and **SW_sync_sel**) The SYNC source must be held at a logic ‘1’ to enable data flow through the DAC. If multiple DAC devices require synchronization, refer to the "Recommended Multi-DAC Synchronization Procedure" below.
9. Provide data flow to LVDS D[15:0]P/N pins. If using the LVDS SYNCP/N input, data can be input simultaneous with the logic ‘1’ transition of SYNCP/N.

10 Power Supply Recommendations

It is recommended that the device be powered with the nominal supply voltages as indicated in the *Recommended Operating Conditions*.

In most instances the best performance is achieved with LDO supplies. However the supplies may be driven with direct outputs from a DC-DC switcher as long as the noise performance of the switcher is acceptable.

For an LDO power supply reference, it is best to refer to the DAC5682zEVM.

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11 Layout

11.1 Layout Guidelines

The DAC5682Z EVM layout should be used as a reference for the layout to obtain the best performance. A sample layout is shown in Figure 53. Some important layout recommendations are:

1. Use a single ground plane. Keep the digital and analog signals on distinct separate sections of the board. This may be virtually divided down the middle of the device package when doing placement and layout.
2. Keep the analog outputs as far away from the switching clocks and digital signals as possible. This will keep coupling from the digital circuits to the analog outputs to a minimum.
3. Decoupling caps should be kept close to the power pins of the device.

11.2 Layout Example

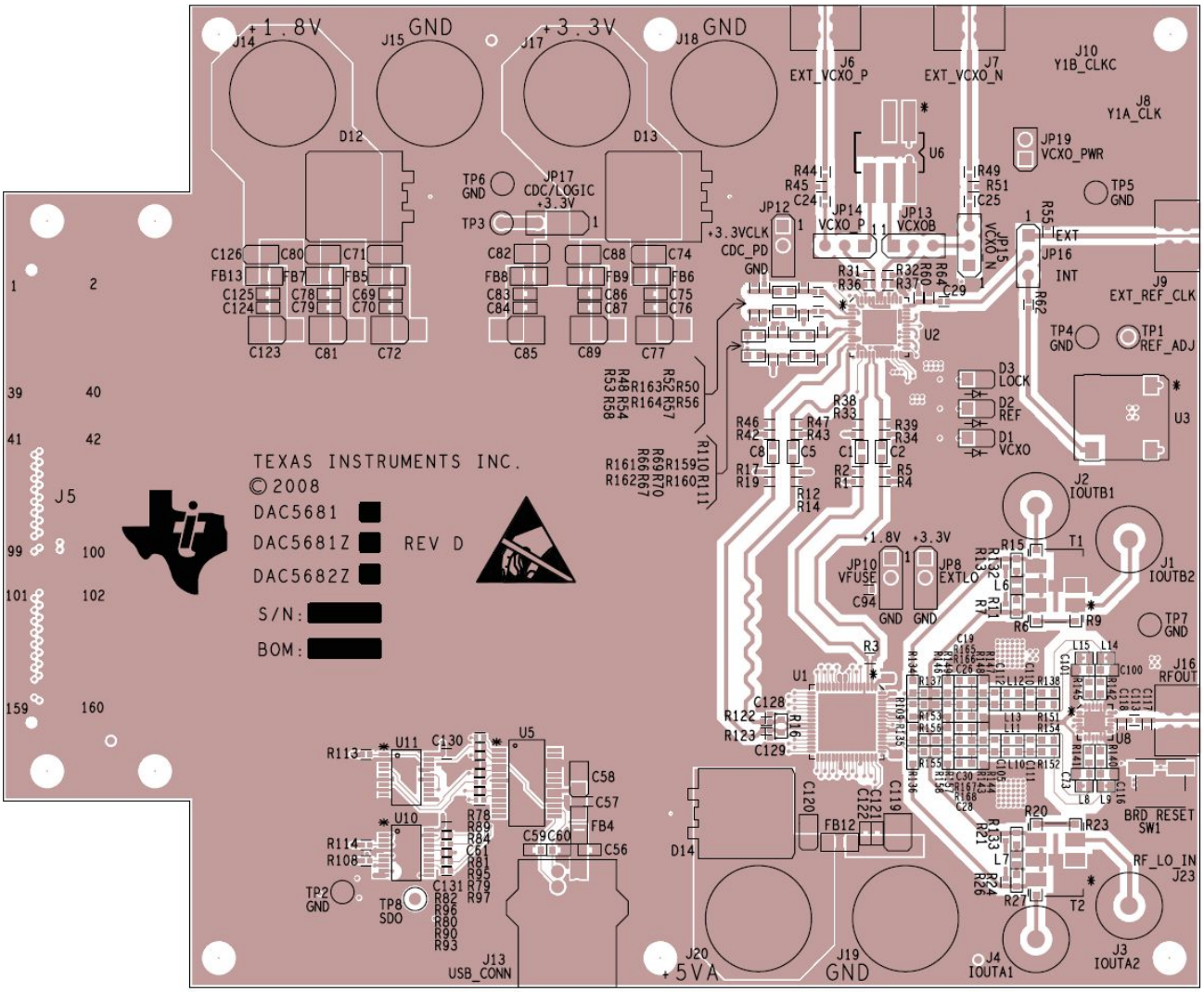

Figure 53. Top Layer of DAC5682zEVM Layout

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Device Nomenclature

Adjacent Carrier Leakage Ratio (ACLR): Defined for a 3.84Mcps 3GPP W-CDMA input signal measured in a 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio.

Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3, IMD): The two-tone IMD3 or four-tone IMD is defined as the ratio (in dBc) of the worst 3rd-order (or higher) intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio of the differential output current (IOUT1–IOUT2) and the mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

Signal to Noise Ratio (SNR): Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC5682ZIRGC	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5682ZI	Samples
DAC5682ZIRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5682ZI	Samples
DAC5682ZIRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC5682ZI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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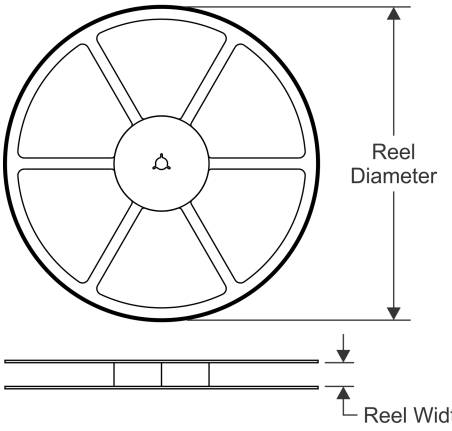
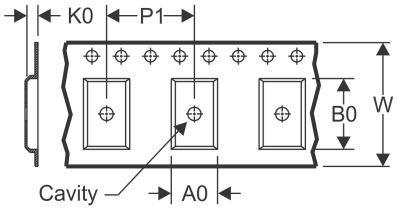
TAPE AND REEL INFORMATION

REEL DIMENSIONS

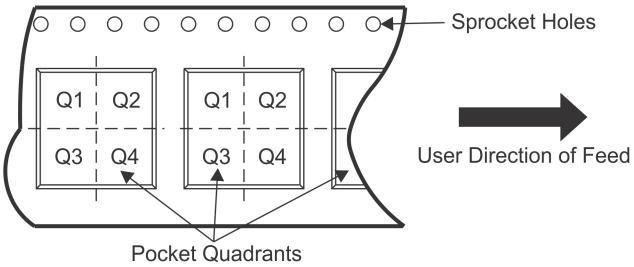


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5682ZIRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC5682ZIRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

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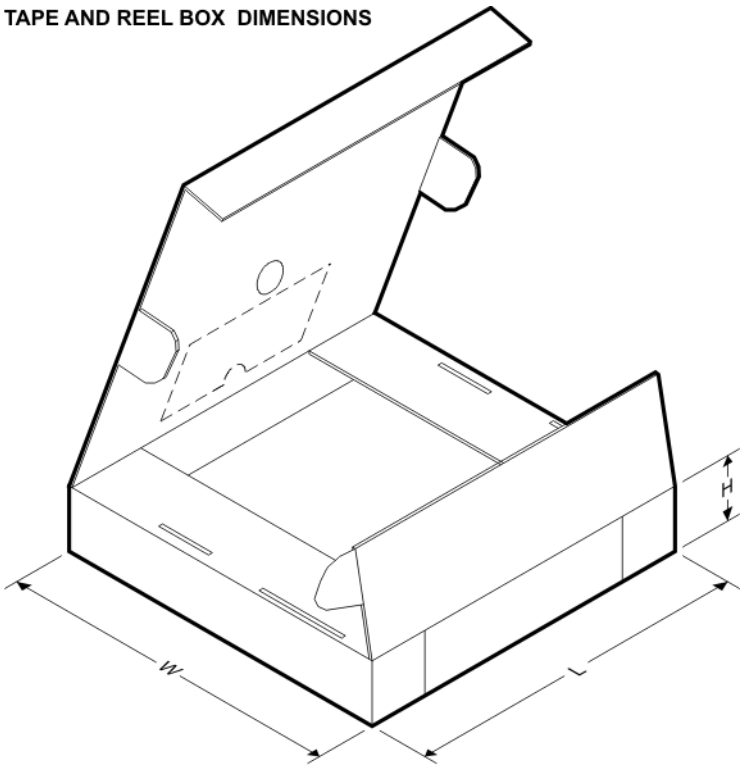
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5682ZIRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
DAC5682ZIRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

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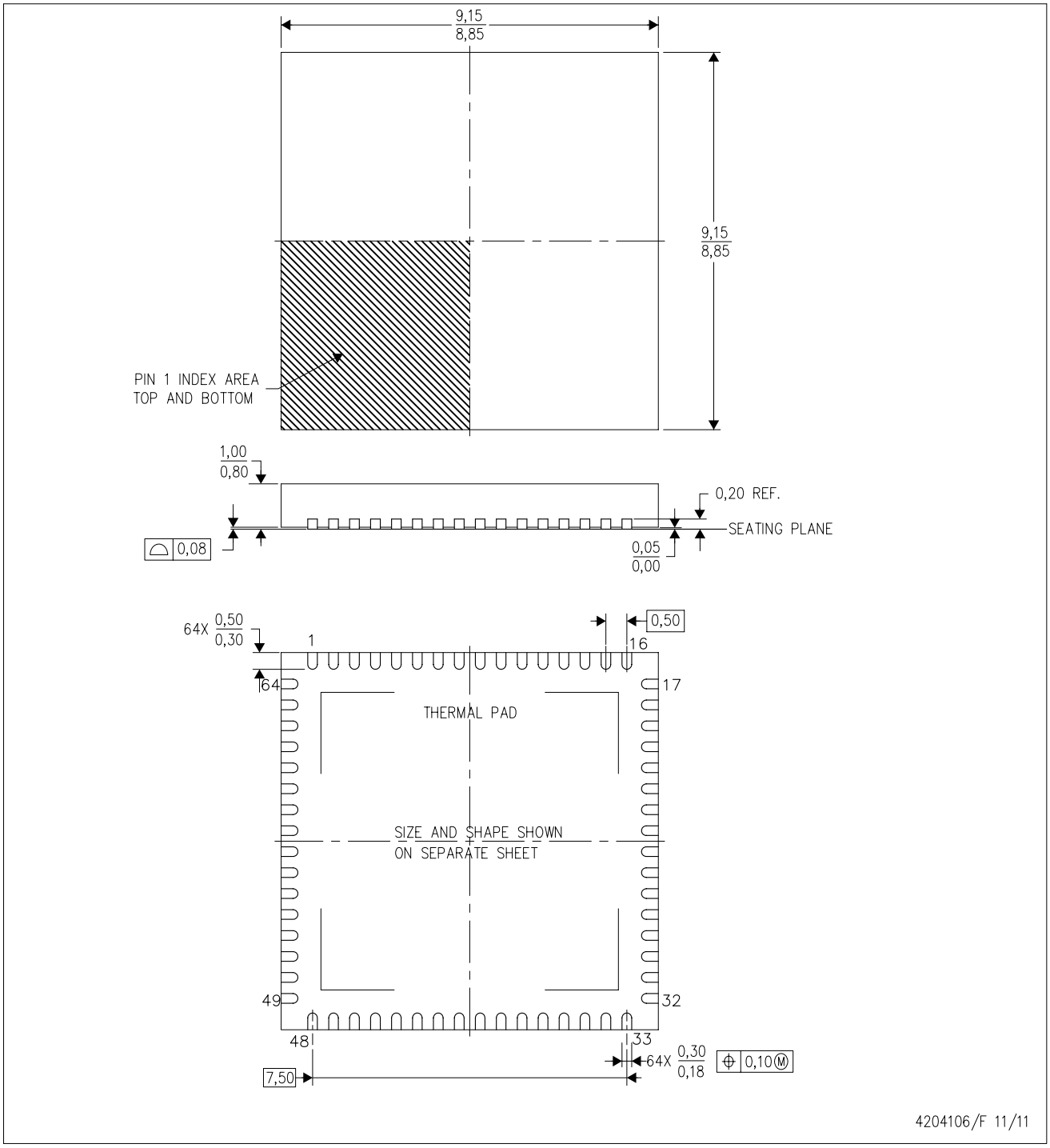
RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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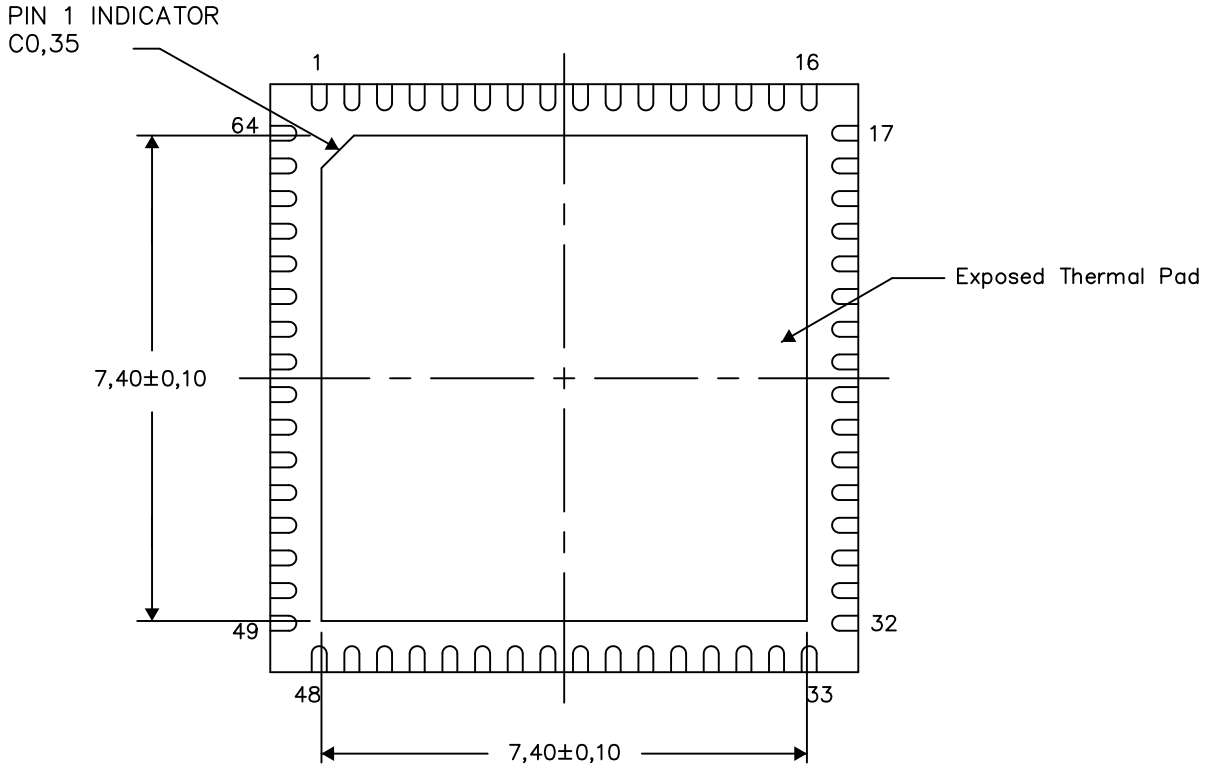
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206192–4/AE 03/15

NOTE: A. All linear dimensions are in millimeters

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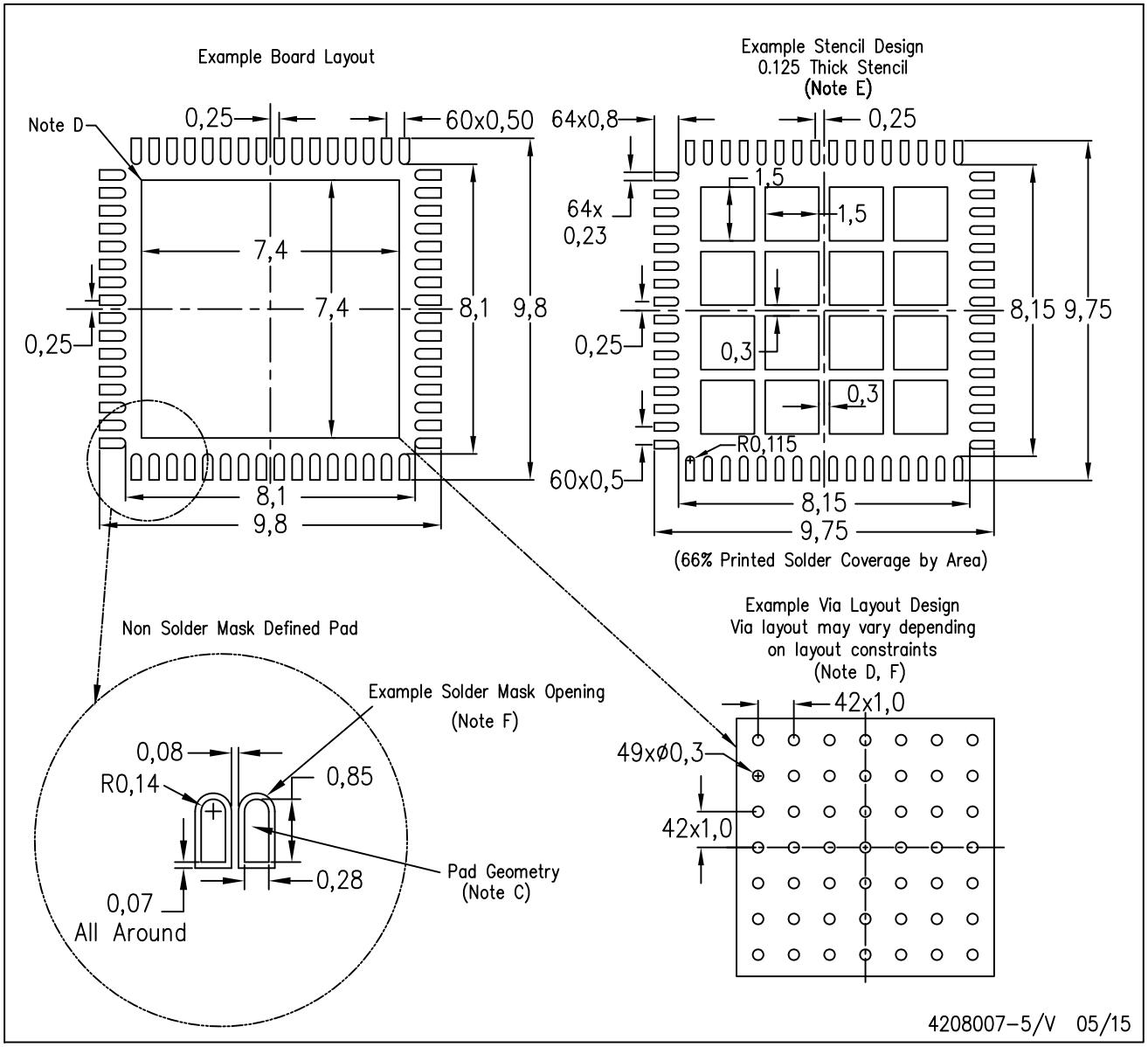
RGC (S-PVQFN-N64) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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