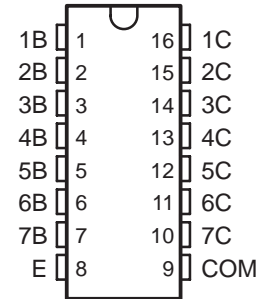


# ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SLRS055 – APRIL 2004

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

D, N, OR NS PACKAGE  
(TOP VIEW)



## description/ordering information

The ULN2004AI is a high-voltage, high-current Darlington transistor array. This device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher-current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULN2004AI has a 10.5-k $\Omega$  series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	PDIP (N)	Tube of 25	ULN2004AIN	ULN2004AIN
	SOIC (D)	Tube of 40	ULN2004AID	ULN2004AI
		Reel of 2500	ULN2004AIDR	
	SOP (NS)	Reel of 2000	ULN2004AINSR	ULN2004AI

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

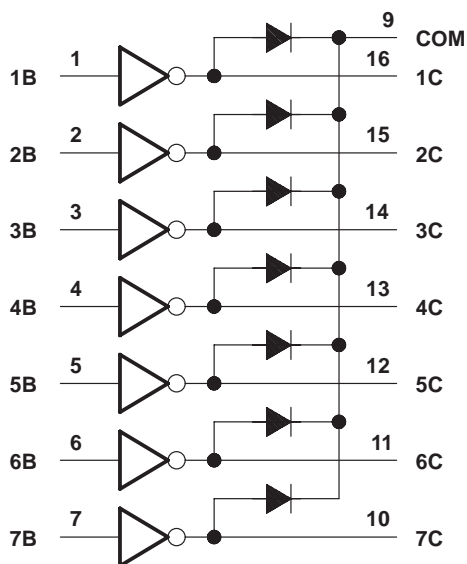
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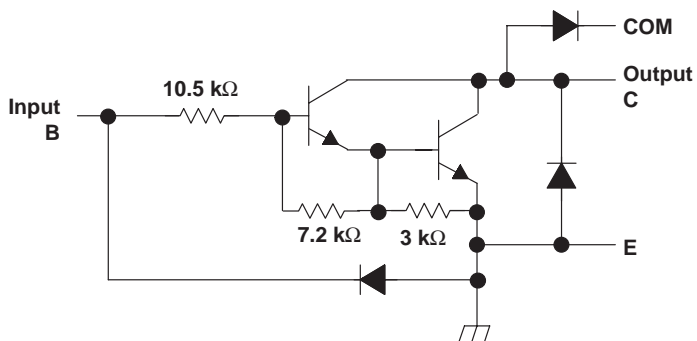
# ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

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## logic diagram



## schematics (each Darlington pair)



All resistor values shown are nominal.

**absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†**

Collector-emitter voltage	50 V
Clamp diode reverse voltage (see Note 1)	50 V
Input voltage, $V_I$ (see Note 1)	30 V
Peak collector current (see Notes 2 and 4)	500 mA
Output clamp current, $I_{OK}$	500 mA
Total emitter-terminal current	–2.5 A
Operating free-air temperature range, $T_A$	–40°C to 105°C
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Operating virtual junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.  
 2. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

**electrical characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(\text{on})}$ On-state input voltage	6	$V_{CE} = 2\text{ V}$			5	V
					6	
					7	
					8	
$V_{CE(\text{sat})}$ Collector-emitter saturation voltage	5	$I_I = 250\text{ }\mu\text{A}$ , $I_C = 100\text{ mA}$		0.9	1.1	V
		$I_I = 350\text{ }\mu\text{A}$ , $I_C = 200\text{ mA}$		1	1.3	
		$I_I = 500\text{ }\mu\text{A}$ , $I_C = 350\text{ mA}$		1.2	1.6	
$I_{CEX}$ Collector cutoff current	1	$V_{CE} = 50\text{ V}$ , $I_I = 0$			50	$\mu\text{A}$
$V_F$ Clamp forward voltage	8	$I_F = 350\text{ mA}$		1.7	2	V
$I_I$ Input current	4	$V_I = 5\text{ V}$		0.35	0.5	mA
		$V_I = 12\text{ V}$		1	1.45	
$I_R$ Clamp reverse current	7	$V_R = 50\text{ V}$			50	$\mu\text{A}$
$C_i$ Input capacitance		$V_I = 0$ , $f = 1\text{ MHz}$		15	25	pF

# ULN2004AI

## HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

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### electrical characteristics, $T_A = -40^{\circ}\text{C}$ to $105^{\circ}\text{C}$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>I(on)</sub>	On-state input voltage	6	V <sub>CE</sub> = 2 V	I <sub>C</sub> = 125 mA			5	V
				I <sub>C</sub> = 200 mA			6	
				I <sub>C</sub> = 275 mA			7	
				I <sub>C</sub> = 350 mA			8	
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	5	I <sub>I</sub> = 250 μA, I <sub>C</sub> = 100 mA		0.9	1.1	V	
			I <sub>I</sub> = 350 μA, I <sub>C</sub> = 200 mA		1	1.3		
			I <sub>I</sub> = 500 μA, I <sub>C</sub> = 350 mA		1.2	1.6		
I <sub>CEX</sub>	Collector cutoff current	1	V <sub>CE</sub> = 50 V, I <sub>I</sub> = 0			50	μA	
		2	V <sub>CE</sub> = 50 V	I <sub>I</sub> = 0		100		
				V <sub>I</sub> = 1 V		500		
V <sub>F</sub>	Clamp forward voltage	8	I <sub>F</sub> = 350 mA			1.7	2	V
I <sub>I(off)</sub>	Off-state input current	3	V <sub>CE</sub> = 50 V, I <sub>C</sub> = 500 μA		50	65		μA
I <sub>I</sub>	Input current	4	V <sub>I</sub> = 5 V			0.35	0.5	mA
			V <sub>I</sub> = 12 V			1	1.45	
I <sub>R</sub>	Clamp reverse current	7	V <sub>R</sub> = 50 V				100	μA
C <sub>i</sub>	Input capacitance		V <sub>I</sub> = 0, f = 1 MHz			15	25	pF

### switching characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	See Figure 8		0.25	1	μs
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	See Figure 8		0.25	1	μs
V <sub>OH</sub>	High-level output voltage after switching	V <sub>S</sub> = 50 V, I <sub>O</sub> ≈ 300 mA, See Figure 9	V <sub>S</sub> – 20			mV

### switching characteristics, $T_A = -40^{\circ}\text{C}$ to $105^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level output	See Figure 8			1	10	μs
tPHL	Propagation delay time, high- to low-level output	See Figure 8			1	10	μs
VOH	High-level output voltage after switching	VS = 50 V, See Figure 9	IO ≈ 300 mA,	VS – 500			mV



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## PARAMETER MEASUREMENT INFORMATION

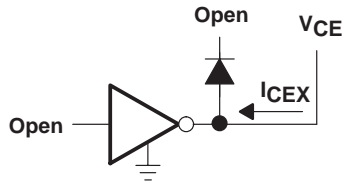


Figure 1.  $I_{CEX}$  Test Circuit

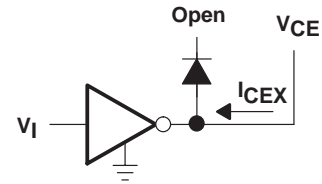


Figure 2.  $I_{CEX}$  Test Circuit

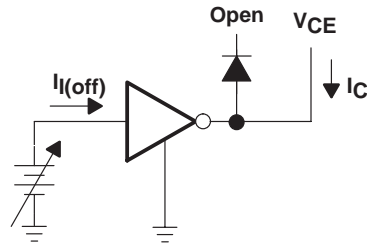


Figure 3.  $I_{I(off)}$  Test Circuit

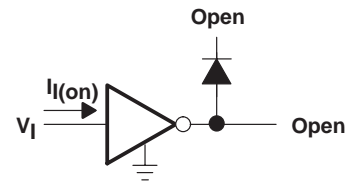
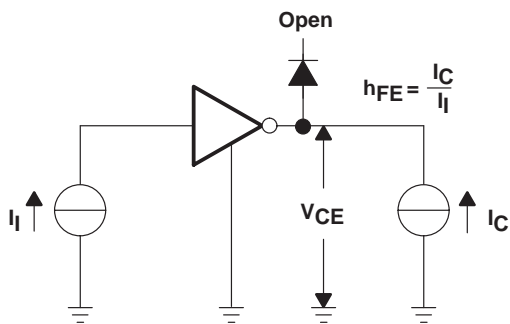


Figure 4.  $I_I$  Test Circuit



NOTE:  $I_I$  is fixed for measuring  $V_{CE(sat)}$ , variable for measuring  $h_{FE}$ .

Figure 5.  $h_{FE}$ ,  $V_{CE(sat)}$  Test Circuit

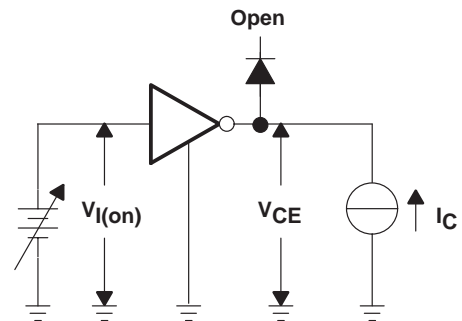


Figure 6.  $V_{I(on)}$  Test Circuit

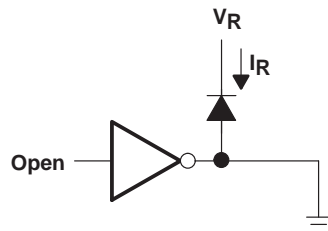


Figure 7.  $I_R$  Test Circuit

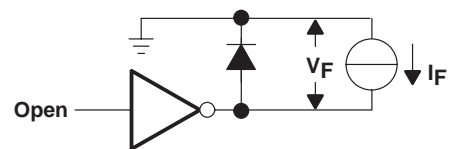


Figure 8.  $V_F$  Test Circuit

# ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

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## PARAMETER MEASUREMENT INFORMATION

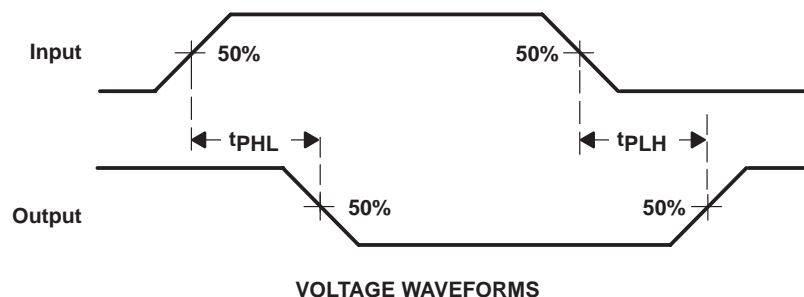
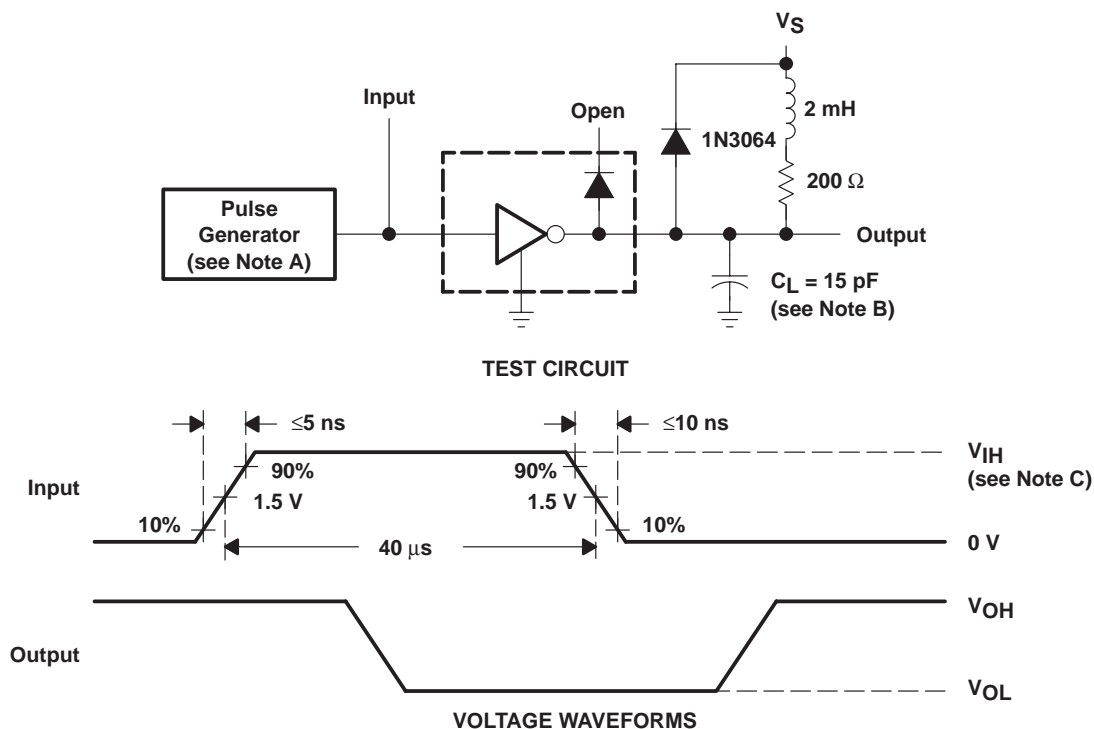


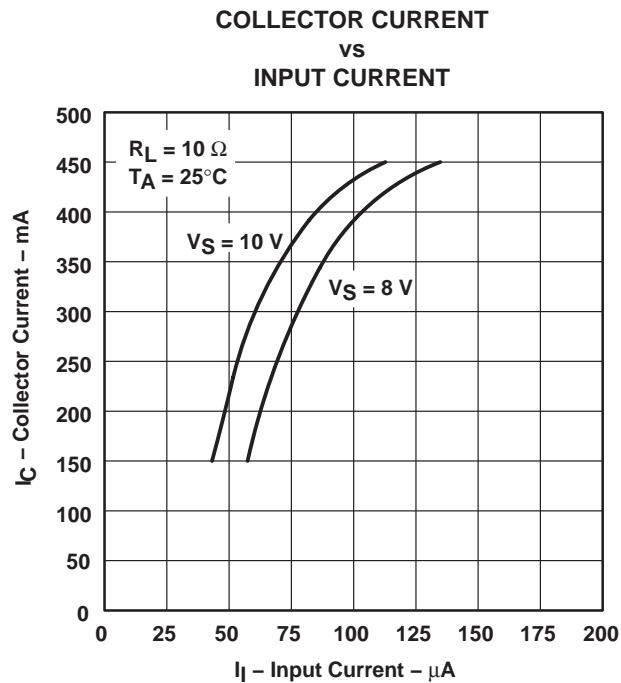
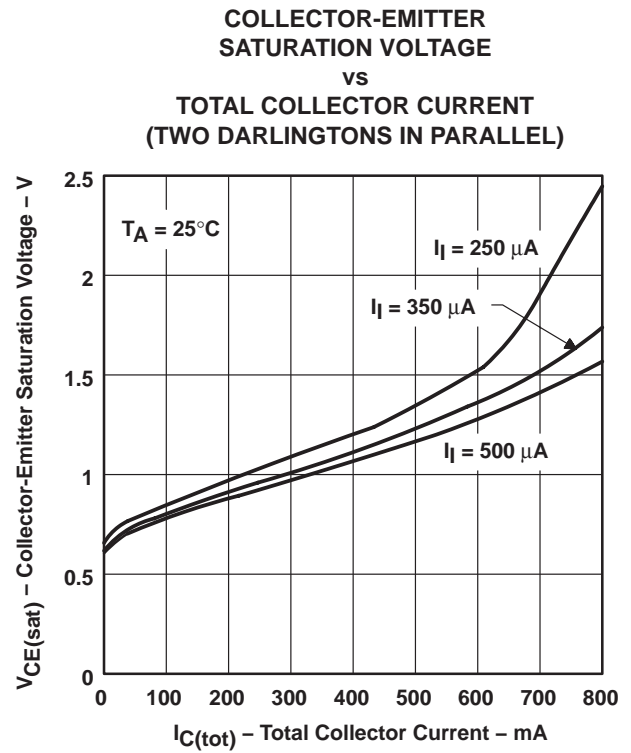
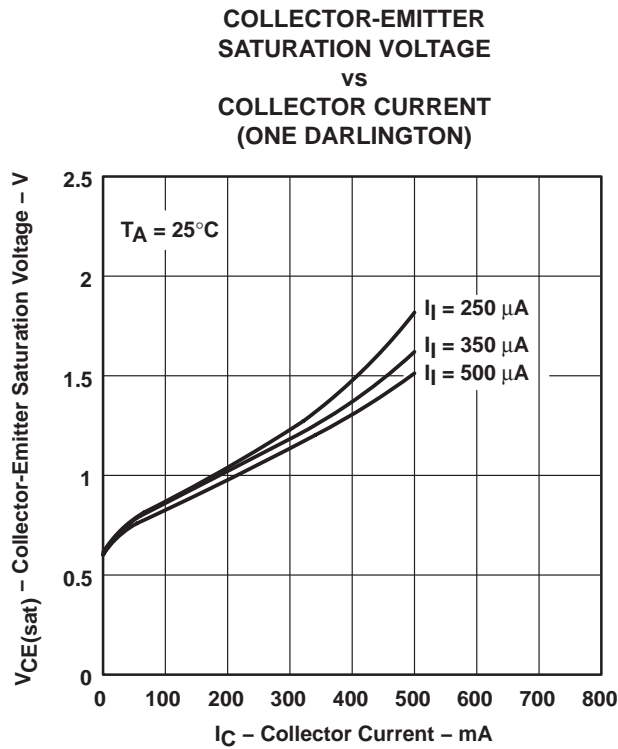
Figure 9. Propagation Delay-Time Waveforms



- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.  
C. For testing,  $V_{IH} = 3 \text{ V}$

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

### TYPICAL CHARACTERISTICS



# ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

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## APPLICATION INFORMATION

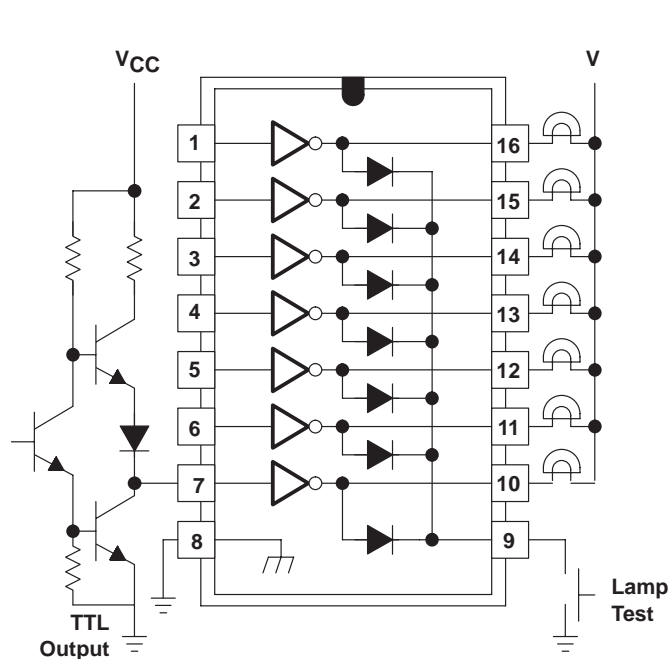


Figure 14. TTL to Load

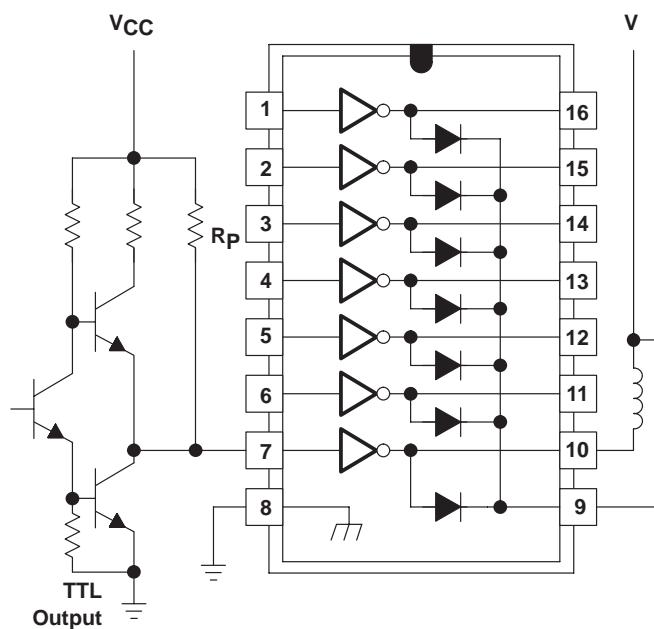


Figure 15. Use of Pullup Resistors to Increase Drive Current



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2004AID	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2004AI	
ULN2004AIDR	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2004AI	
ULN2004AIN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	ULN2004AIN	
ULN2004AINSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULN2004AI	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2004AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2004AINSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

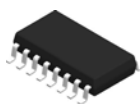
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2004AIDR	SOIC	D	16	2500	340.5	336.1	32.0
ULN2004AINSR	SO	NS	16	2000	356.0	356.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ULN2004AID	D	SOIC	16	40	507	8	3940	4.32
ULN2004AIN	N	PDIP	16	25	506	13.97	11230	4.32
ULN2004AIN	N	PDIP	16	25	506	13.97	11230	4.32



# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

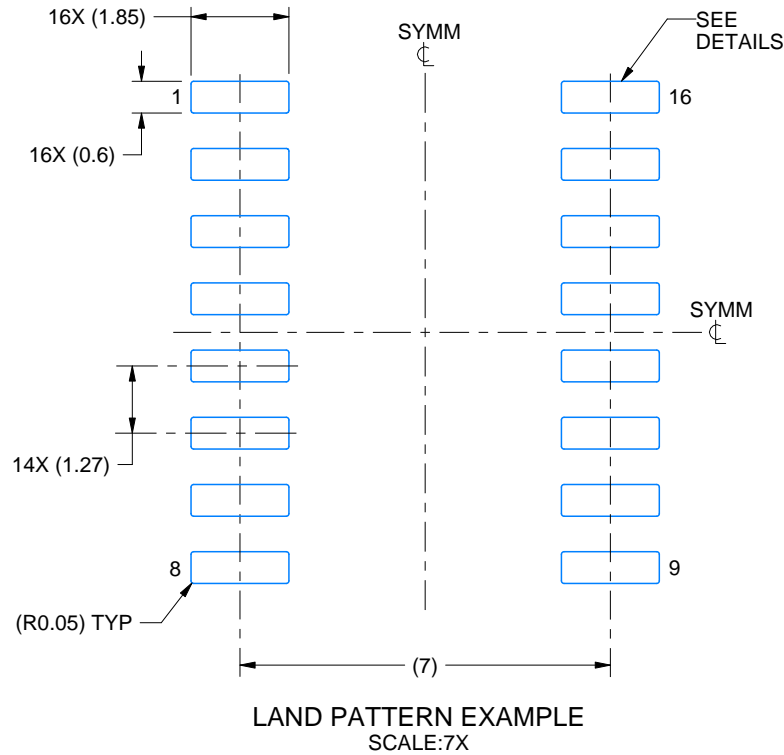
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



## NOTES:

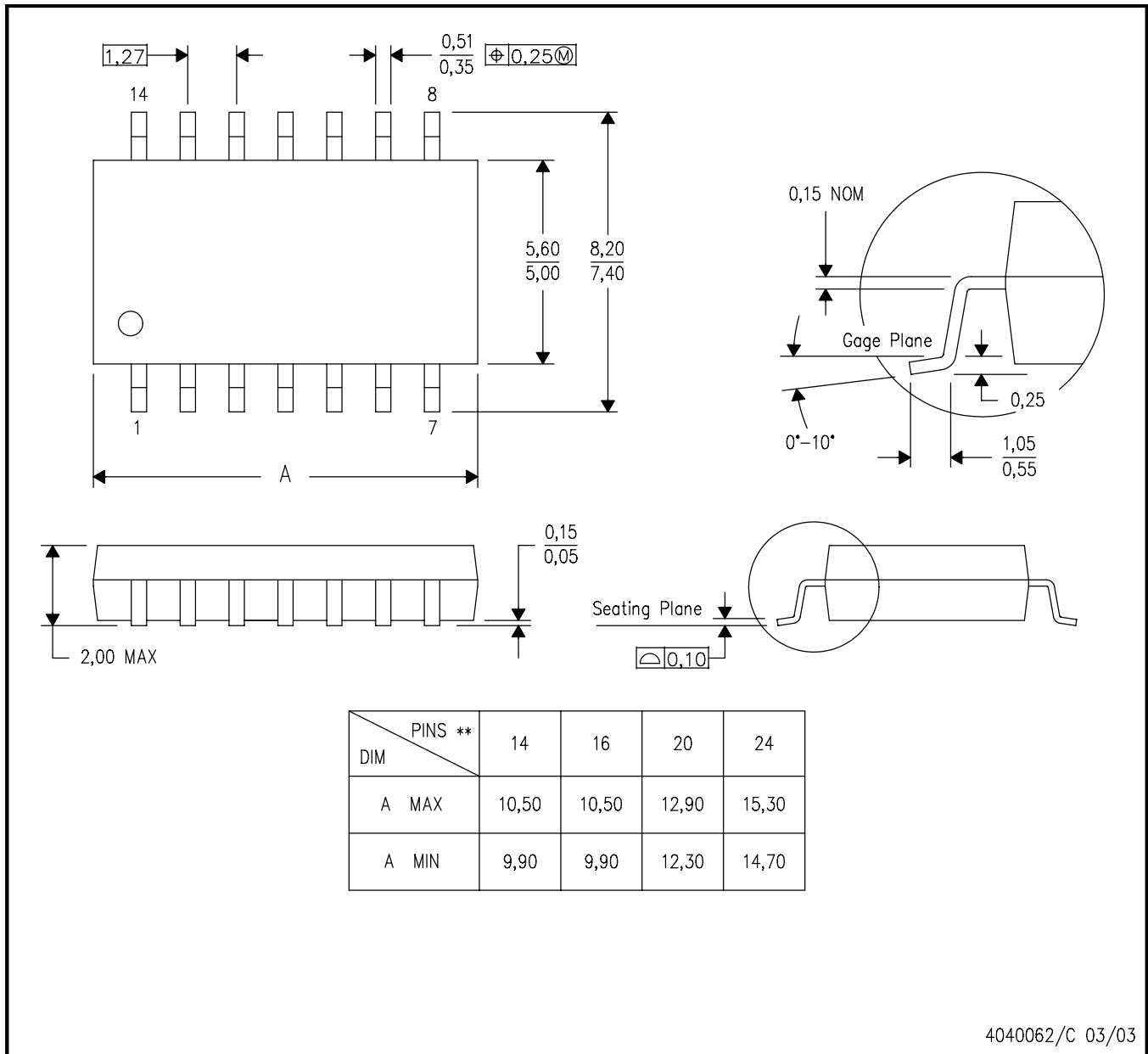
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

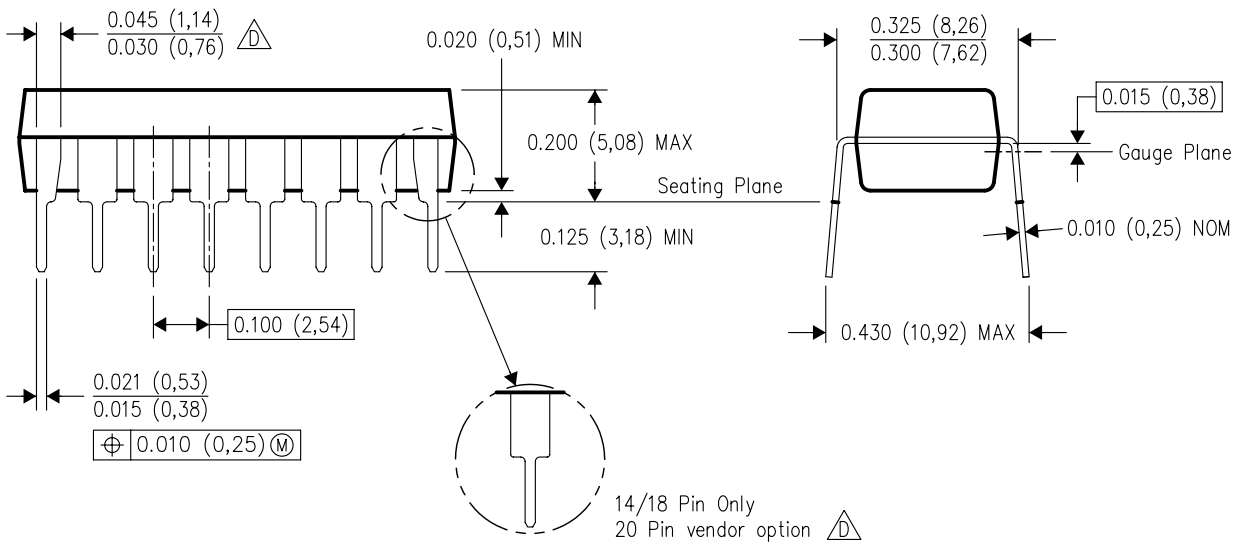
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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