ASM330LHHG1

Datasheet

High-accuracy 6-axis automotive inertial measurement unit (IMU) with dual operating modes

LGA-14L
Typ: 2.5 x 3.0 x 0.83 mm³

Product status link
ASM330LHHG1

Product summary	
Order code	ASM330LHHG1TR
Temp. range [°C]	-40 to +125
Package	LGA-14L (2.5 x 3.0 x 0.83 mm³)
Packing	Tape and reel

Product resources
AN6352 (device application note)
TN0018 (handling, mounting, and soldering guidelines)

Product label
LONGEVITY 15 YEARS COMMITMENT

Features

- AEC-Q100 qualified
- Android Auto™ compliant and CarPlay® compliant
- Extended temperature range from -40 to +125°C
- Embedded compensation for high stability over temperature
- Accelerometer user-selectable full scale up to ±16 *g*
- Extended gyroscope range from ±125 to ±4000 dps
- Dual operating modes: high-performance and low-power mode
- I²C, MIPI I3C®, and SPI serial interfaces
- Six-channel synchronized output to enhance the accuracy of dead-reckoning algorithms
- Smart programmable interrupts
- Embedded 3 KB FIFO available to underload host processor
- ECOPACK and RoHS compliant

Applications

- Dead reckoning (DR)
- Vehicle-to-everything (V2X)
- Telematics, e-tolling
- Antitheft systems
- Impact detection and crash reconstruction
- Motion-activated functions
- Driving comfort
- Vibration monitoring and compensation

Description

The ASM330LHHG1 is a 6-axis IMU featuring a 3-axis digital accelerometer and a 3-axis digital gyroscope with an extended temperature range up to +125°C, designed to address automotive nonsafety applications.

ST's family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes to serve both the automotive and consumer markets. The ASM330LHHG1 is AEC-Q100 compliant and industrialized through a dedicated MEMS production flow to meet automotive reliability standards. All the parts are fully tested with respect to temperature to ensure the highest quality level.

The sensing elements are manufactured using ST's proprietary micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHHG1 has a full-scale acceleration range of ±2/±4/±8/±16 g and a wide angular rate range of ±125/±250/±500/±1000/±2000/±4000 dps that enables its usage in a broad range of automotive applications.

The device supports dual operating modes: high-performance mode and low-power mode.

All the design aspects of the ASM330LHHG1 have been optimized to reach superior output stability, extremely low noise, and full data synchronization to the benefit of sensor-assisted applications like dead reckoning and sensor fusion.

The ASM330LHHG1 is available in an overmolded 14-lead plastic, land grid array (LGA) package.

1 Overview

The ASM330LHHG1 is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

This device is suitable for telematics and dead-reckoning applications as well as vehicle-to-vehicle (V2X) and impact detection as a result of its high stability over temperature and time, combined with superior sensing precision.

Supporting dual operating modes, the device has enhanced flexibility versus application requirements, leveraging on multiple voltage and multiple ODR selections.

The event-detection interrupts enable efficient and reliable motion-activated functions, implementing hardware recognition of free-fall events, 6D orientation, activity or inactivity, and wake-up events.

Like the entire portfolio of MEMS sensor modules, the ASM330LHHG1 leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHHG1 is available in a small plastic, land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultracompact solutions.

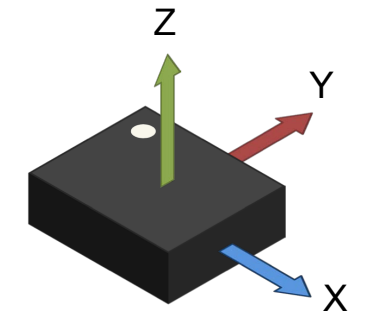
2 Embedded low-power features

The ASM330LHHG1 has been designed to feature the following on-chip functions:

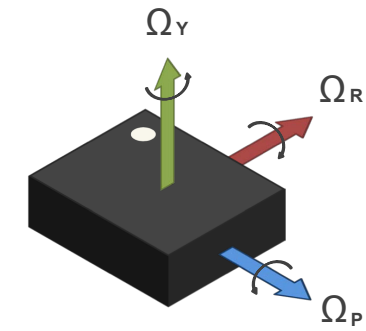
- 3 KB data buffering
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wake-up
  - 6D orientation
  - Activity/inactivity recognition
  - Stationary/motion detection
- Sensor hub
  - Up to six total sensors: two internal (accelerometer and gyroscope) and four external sensors

3 Pin description

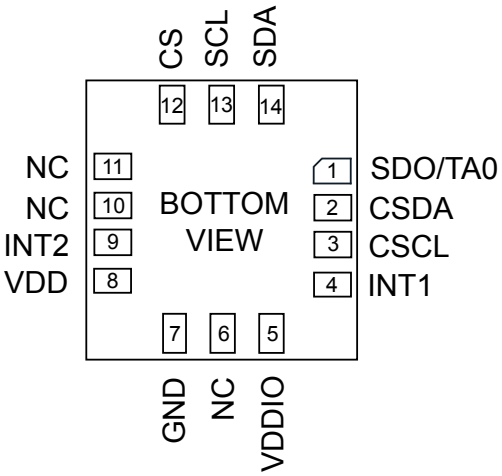
Figure 1. **Pin connections**



Direction of detectable accelerations (top view)



Direction of detectable angular rates (top view)

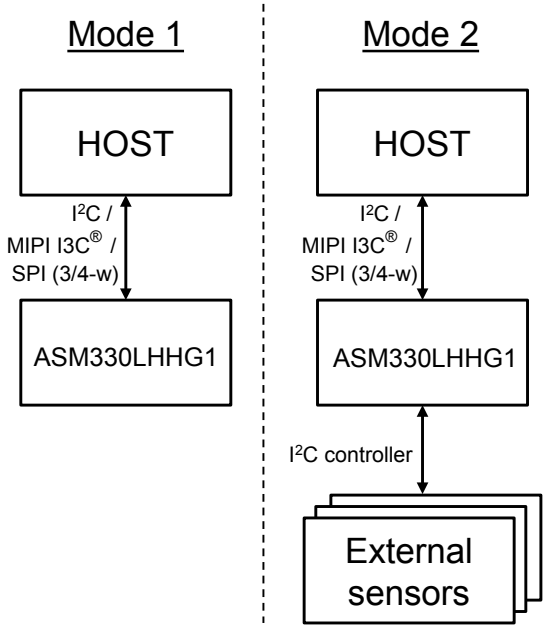


3.1 Pin connections

The ASM330LHHG1 offers flexibility to connect the pins in order to have two different mode connections and functionalities. In detail:

- **Mode 1:** I²C / MIPI I3C® target interface or SPI (3- and 4-wire) serial interface is available
- **Mode 2:** I²C / MIPI I3C® target interface or SPI (3- and 4-wire) serial interface and I²C controller interface for external sensor connections are available

Figure 2. ASM330LHHG1 connection modes



In the following table, each mode is described for the pin connections and function.

Table 1. Pin description

Pin#	Name	Mode 1 function	Mode 2 function
1	SDO/TA0	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)
2	CSDA	Connect to VDDIO or GND	I²C controller serial data (CSDA)
3	CSCL	Connect to VDDIO or GND	I²C controller serial clock (CSCL)
4	INT1	Programmable interrupt in I²C and SPI	
5	VDDIO(1)	Power supply for I/O pins	
6	NC	Connect to VDDIO or GND or leave unconnected	
7	GND	0 V supply	
8	VDD(1)	Power supply	
9	INT2	Programmable interrupt 2 (INT2) / Data enabled (DEN)	Programmable interrupt 2 (INT2) / Data enabled (DEN) / I²C controller external synchronization signal (CDRDY)
10	NC	Leave unconnected(2)	Leave unconnected(2)
11	NC	Leave unconnected(2)	Leave unconnected(2)
12	CS	I²C/MIPI I3C®/SPI mode selection (1: SPI idle mode / I²C/MIPI I3C® communication enabled; 0: SPI communication mode / I²C/MIPI I3C® disabled)	I²C/MIPI I3C®/SPI mode selection (1: SPI idle mode / I²C/MIPI I3C® communication enabled; 0: SPI communication mode / I²C/MIPI I3C® disabled)
13	SCL	I²C/MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)	I²C/MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)
14	SDA	I²C/MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	I²C/MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

1. *VDDIO: Recommended 100 nF filter capacitor. VDD: Recommended 100 nF plus 10 µF capacitors.*
2. *Leave pin electrically unconnected and soldered to PCB.*

4 Module specifications

4.1 Mechanical characteristics

@VDD = 3.0 V, T = -40°C to +125°C, up to gyroscope FS = ±2000 dps unless otherwise noted.
The product is factory calibrated at 3.0 V. The operational power supply range is from 1.71 V to 3.6 V.

Table 2. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±125		dps
				±250		
				±500		
				±1000		
				±2000		
				±4000		
LA_So	Linear acceleration sensitivity	@LA_FS = ±2 *g*		0.061		mg/LSB
		@LA_FS = ±4 *g*		0.122		
		@LA_FS = ±8 *g*		0.244		
		@LA_FS = ±16 *g*		0.488		
G_So	Angular rate sensitivity	@G_FS = ±125 dps		4.37		mdps/LSB
		@G_FS = ±250 dps		8.75		
		@G_FS = ±500 dps		17.5		
		@G_FS = ±1000 dps		35.0		
		@G_FS = ±2000 dps		70.0		
		@G_FS = ±4000 dps		140.0		
LA_TySo%	Linear acceleration sensitivity tolerance(2)	@25°C		±2		%
G_TySo%	Angular rate sensitivity tolerance(2)	@25°C		±2		%
LA_So%	Linear acceleration sensitivity tolerance - long term(3)		-6		+6	%
G_So%	Angular rate sensitivity tolerance - long term(3)		-10		+10	%
LA_SoDr	Linear acceleration sensitivity change vs. temperature			±100		ppm/°C
G_SoDr	Angular rate sensitivity change vs. temperature			±70		ppm/°C
LA_TyOff	Linear acceleration zero-*g* level offset accuracy(2)	@25°C		±20		mg
LA_Off	Linear acceleration offset accuracy - long term(3)		-210		+210	mg
G_TyOff	Angular rate zero-rate level accuracy(2)	@25°C		±2		dps
G_Off	Angular rate offset accuracy - long term(3)		-10		+10	dps
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature			±0.10		mg/°C
G_TCOff	Angular rate typical zero-rate level change vs. temperature			±0.005		dps/°C
LA_Cx	Linear acceleration cross-axis sensitivity	@25°C		±1		%

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
G_Cx	Angular rate cross-axis sensitivity	@25°C		±1		%
An	Acceleration noise density(4)(6)	@LA_FS = ±2 *g* @25°C		60	200	µg/√Hz
AnRMS	Acceleration RMS noise in low-power mode(5)			1.8		mg(RMS)
Rn	Rate noise density(4)(6)	@25°C		5	12	mdps/√Hz
RnRMS	Gyroscope RMS noise in low-power mode(5)			90		mdps(RMS)
XL_NL	Accelerometer nonlinearity(7)	Best-fit straight line		0.5		%FS
G_NL	Gyroscope nonlinearity(7)	Best-fit straight line		0.01		% FS
VRW	Velocity random walk(7)	@25°C		0.03		m/sec/√h
XL_BI	Accelerometer bias instability(7)	@25°C		40		µ*g*
ARW	Angular random walk(7)	@25°C		0.21		°/√h
G_BI	Gyroscope bias instability(7)	@25°C		3		°/h
LA_ODR	Linear acceleration output data rate			1.6(8) 12.5 26 52 104 208 416 833 1667 3333 6667		Hz
G_ODR	Angular rate output data rate			12.5 26 52 104 208 416 833 1667 3333 6667		Hz
Vst	Linear acceleration self-test output change(9)(10)(11)		40		1700	mg
	Angular rate self-test output change(12)(13)	FS = ±250 dps	20		80	dps
		FS = ±2000 dps	150		700	dps
Top	Operating temperature range		-40		+125	°C

1. *Typical specifications are not guaranteed.*
2. *Values after factory calibration test and trimming at T = 25°C.*
3. *Long term includes the following conditions: post solder, drift in temperature in the range [-40°C to +125°C] and over life.*
4. *Max. values from design and characterization at ambient temperature (T = 25°C).*
5. *RMS noise is the same for all ODRs.*
6. *Noise density is the same for all ODRs.*
7. *Based on characterization data on a limited number of samples. Not measured during final test for production.*

8. *This ODR is available when the accelerometer is in low-power mode.*
9. *Accelerometer self-test limits are full-scale independent.*
10. *The sign of the linear acceleration self-test output change is defined by the STx_XL bits in a dedicated register for all axes.*
11. *The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 0.061 mg at ±2 g full scale.*
12. *The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 70 mdps at ±2000 dps full scale.*
13. *The sign of the angular rate self-test output change is defined by the STx_G bits in a dedicated register for all axes.*

4.2 Electrical characteristics

@VDD = 3.0 V, T = -40°C to +125°C, up to gyroscope FS = ±2000 dps unless otherwise noted.

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
VDD	Supply voltage		1.71		3.6	V
VDDIO	Power supply for I/O		1.62		3.6	V
GA_Idd	Gyroscope and accelerometer supply current	ODR = 1.6 kHz		1.3	1.7	mA
LA_IddHP	Accelerometer supply current in high-performance mode	ODR = 1.6 kHz		360	750	µA
LA_IddLM	Accelerometer supply current in low-power mode	ODR = 52 Hz @25°C		50	500	µA
		ODR = 12.5 Hz @25°C(3)		14		µA
		ODR = 1.6 Hz @25°C(3)		7		µA
		VDD = 1.71 V, ODR = 52 Hz @25°C		40	500	µA
		VDD = 1.71 V, ODR = 12.5 Hz @25°C(3)		11		µA
		VDD = 1.71 V, ODR = 1.6 Hz @25°C(3)		5.5		µA
LC_IddLM	Supply current in low-power mode, combo	ODR = 52 Hz		530	1000	µA
		ODR = 12.5 Hz @25°C(3)		475		µA
		VDD = 1.71 V, ODR = 52 Hz		520	1000	µA
		VDD = 1.71 V, ODR = 12.5 Hz @25°C(3)		470		µA
IddPD	Gyroscope and accelerometer supply current during power-down	@25°C		5	13	µA
Ton	Turn-on time(2)			35		ms
V_{IH}(3)	Digital high-level input voltage		0.7 * VDDIO			V
V_{IL}(3)	Digital low-level input voltage				0.3 * VDDIO	V
V_{OH}(3)	High-level output voltage	I_{OH} = 4 mA(4)	VDDIO - 0.2			V
V_{OL}(3)	Low-level output voltage	I_{OL} = 4 mA(4)			0.2	V
Top	Operating temperature range		-40		+125	°C

1. *Typical specifications are not guaranteed.*
2. *Time to obtain stable sensitivity (within ±5% of final value) switching from power-down to normal operation*
3. *Evaluated by characterization - not tested in production*
4. *4 mA is the minimum driving capability, that is, the minimum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.*

4.3 Temperature sensor characteristics

@VDD = 3.0 V, T = 25°C unless otherwise noted. The product is factory calibrated at 3.0 V.

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TODR(2)	Temperature refresh rate			52		Hz
Toff	Temperature offset(3)		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
TST	Temperature stabilization time(4)				500	µs
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+125	°C

1. *Typical specifications are not guaranteed.*
2. *When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.*
3. *The output of the temperature sensor is 0 LSB (typ.) at 25°C.*
4. *Time from power ON to valid output data. Based on characterization.*

4.4 Communication interface characteristics

4.4.1 SPI - serial peripheral interface

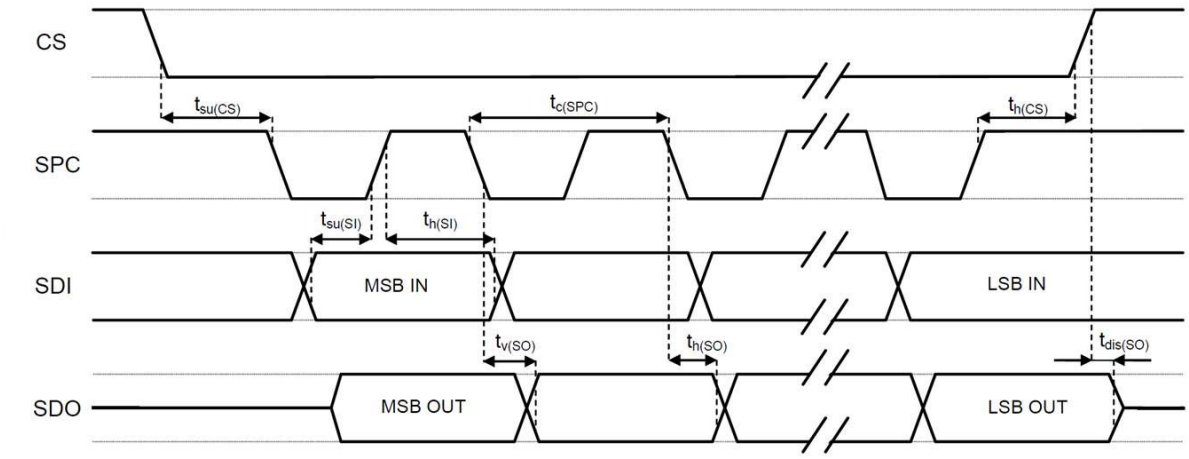
Subject to general operating conditions for VDD and Top.

Table 5. SPI target timing values (in mode 3)

Symbol	Parameter	Value[1]		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

Figure 3. SPI target timing diagram (in mode 3)



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both input and output ports.

4.4.2 I²C - inter-IC control interface

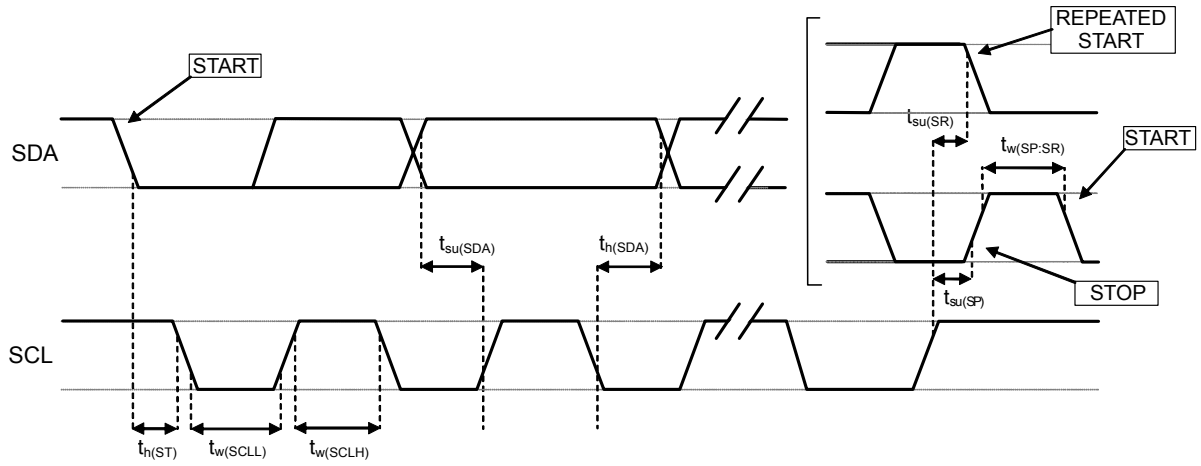
Subject to general operating conditions for VDD and Top.

Table 6. I²C target timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. *Data based on standard I²C protocol requirement, not tested in production.*

Figure 4. I²C target timing diagram



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both ports.

Table 7. I²C high-speed mode specifications at 1 MHz

	Symbol	Parameter	Min.	Max.	Unit
Fast mode plus[1]	f_{SCL}	SCL clock frequency	0	1	MHz
	$t_{HD;STA}$	Hold time (repeated) START condition	260	-	ns
	t_{LOW}	Low period of the SCL clock	500	-	
	t_{HIGH}	High period of the SCL clock	260	-	
	$t_{SU;STA}$	Setup time for a repeated START condition	260	-	
	$t_{HD;DAT}$	Data hold time	0	-	
	$t_{SU;DAT}$	Data setup time	50	-	
	t_{rDA}	Rise time of SDA signal	-	120	
	t_{fDA}	Fall time of SDA signal	-	120	
	t_{rCL}	Rise time of SCL signal	20*VDD/5.5	120	
	t_{fCL}	Fall time of SCL signal	20*VDD/5.5	120	
	$t_{SU;STO}$	Setup time for STOP condition	260	-	
	C_b	Capacitive load for each bus line	-	550	pF
	$t_{VD;DAT}$	Data valid time	-	450	ns
	$t_{VD;ACK}$	Data valid acknowledge time	-	450	
	V_{nL}	Noise margin at low level	0.1VDD	-	V
	V_{nH}	Noise margin at high level	0.2VDD	-	
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	ns

1. *Data based on characterization, not tested in production*

4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
VDD	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.3 ms	3000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/TA0)	-0.3 to VDDIO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4.6 Terminology

4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky), and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see Table 2).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see Table 2).

4.6.2 Zero-*g* and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0*g* on both the X-axis and Y-axis, whereas the Z-axis measures 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Linear acceleration zero-*g* level change vs. temperature” in Table 2. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see Table 2).

5 Digital interfaces

5.1 I²C/SPI interface

The registers embedded inside the ASM330LHHG1 may be accessed through both the I²C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped to the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to VDDIO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	Enable SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/TA0	SPI serial data output (SDO) I²C less significant bit of the device address

5.1.1 I²C serial interface

The ASM330LHHG1 I²C is a bus target. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

Table 10. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Controller	The device that initiates a transfer, generates clock signals, and terminates a transfer
Target	The device addressed by the controller

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to VDDIO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with the standard mode.

In order to disable the I²C block, (I2C_disable) = 1 must be written in CTRL4_C (13h).

5.1.1.1 *I²C operation*

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the controller, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the target in the first 7 bits and the eighth bit tells whether the controller is receiving data from the target or transmitting data to the target. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the controller.

The target address (TAD) associated to the ASM330LHHG1 is 110101xb. The SDO/TA0 pin can be used to modify the less significant bit of the device address. If the SDO/TA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b); else if the SDO/TA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ASM330LHHG1 behaves like a target device and the following protocol must be adhered to. After the start condition (ST) a target address is sent, once a target acknowledge (TAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by CTRL3_C (12h) (IF_INC).

The target address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the controller transmits to the target with direction unchanged. Table 11 explains how the TAD+read/write bit pattern is composed, listing all the possible configurations.

Table 11. TAD + read/write patterns

Command	TAD[6:1]	TAD[0] = TA0	R/W	TAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 12. Transfer when controller is writing one byte to target

Controller	ST	TAD + W		SUB		DATA		SP
Target			TAK		TAK		TAK	

Table 13. Transfer when controller is writing multiple bytes to target

Controller	ST	TAD + W		SUB		DATA		DATA		SP
Target			TAK		TAK		TAK		TAK	

Table 14. Transfer when controller is receiving (reading) one byte of data from target

Controller	ST	TAD + W		SUB		SR	TAD + R			NCAK	SP
Target			TAK		TAK			TAK	DATA		

Table 15. Transfer when controller is receiving (reading) multiple bytes of data from target

Controller	ST	TAD+W		SUB		SR	TAD+R			CAK		CAK		NCAK	SP
Target			TAK		TAK			TAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a target receiver does not acknowledge the target address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the target. The controller can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

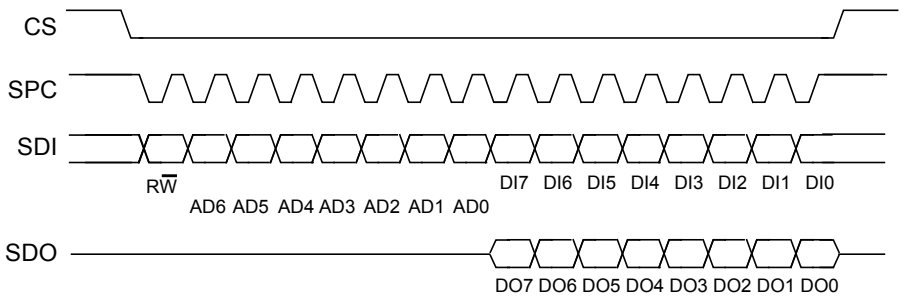
In the presented communication format CAK is controller acknowledge and NCAK is no controller acknowledge.

5.1.2 SPI bus interface

The ASM330LHHG1 SPI is a bus target. The SPI allows writing to and reading from the registers of the device.

The serial interface communicates to the application using four wires: **CS**, **SPC**, **SDI**, and **SDO**.

Figure 5. Read and write protocol (in mode 3)



CS enables the serial port and it is controlled by the SPI controller. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI controller. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip drives **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

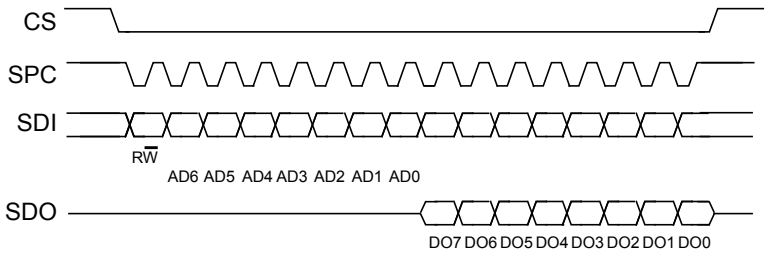
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of eight clock periods are added. When the CTRL3_C (12h) (IF_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3_C (12h) (IF_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.1.2.1 SPI read

Figure 6. SPI read protocol (in mode 3)



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

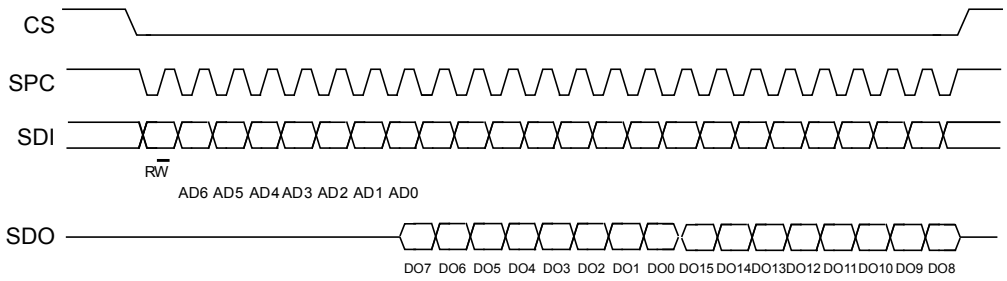
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

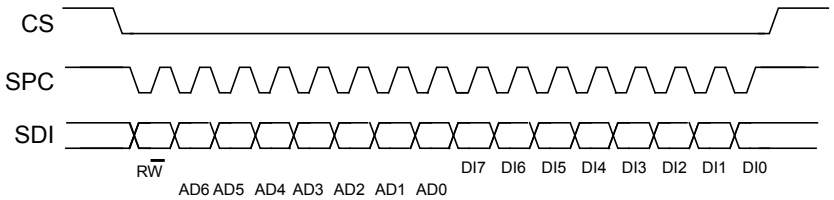
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 7. Multiple byte SPI read protocol (2-byte example) (in mode 3)



5.1.2.2 *SPI write*

Figure 8. SPI write protocol (in mode 3)



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

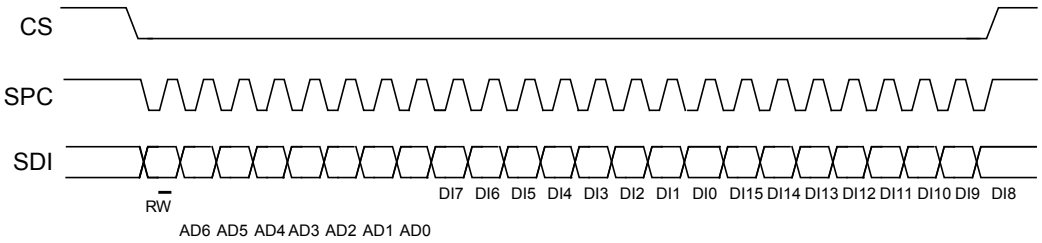
bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

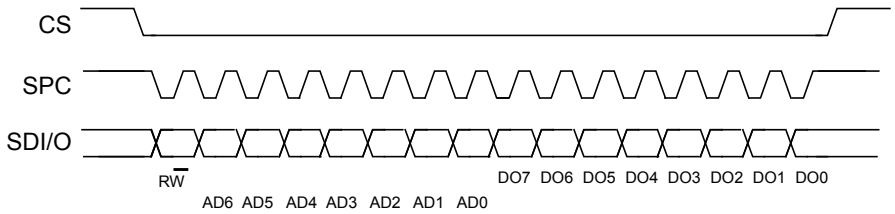
Figure 9. Multiple byte SPI write protocol (2-byte example) (in mode 3)



5.1.2.3 *SPI read in 3-wire mode*

A 3-wire mode is entered by setting the CTRL3_C (12h) (SIM) bit equal to 1 (SPI serial interface mode selection).

Figure 10. SPI read protocol in 3-wire mode (in mode 3)



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

5.2 MIPI I3C® interface

5.2.1 MIPI I3C® target interface

The ASM330LHHG1 interface includes a MIPI I3C® SDR only target interface with MIPI I3C® SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- Error detection and recovery methods

Refer to Section 5.3: I²C/I3C coexistence in ASM330LHHG1 for details concerning the choice of the interface when powering up the device.

5.2.2 MIPI I3C® CCC supported commands

The list of MIPI I3C® CCC commands supported by the device is detailed in the following table.

Table 16. MIPI I3C® CCC commands

Command	Command code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address 0x6B/0x6A depending on SDO pin
ENEC	0x80 / 0x00		Target activity control (direct and broadcast)
DISEC	0x81/ 0x01		Target activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
ENTAS1	0x83 / 0x03		Enter activity state (direct and broadcast)
ENTAS2	0x84 / 0x04		Enter activity state (direct and broadcast)
ENTAS3	0x85 / 0x05		Enter activity state (direct and broadcast)
RSTDAA	0x86 / 0x06		Reset the assigned dynamic address (direct and broadcast)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x09 (3 byte)	Get maximum read length during private read
GETPID	0x8D	0x02 0x08 0x00 0x6B 0x10 0x0B	Device ID register
GETBCR	0x8E	0x07 (1 byte)	Bus characteristics register
GETDCR	0x8F	0x00	MIPI I3C® device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register
GETMXDS	0x94	0x00 0x38 (2 byte)	Return max data speed(1)

1. *Bits[5:3] are set to "111" which indicates that Tsco is greater than 12 nsec. To calculate the effective bus frequency, Tsco should be used together with line capacitance, number of targets and stubs (if present).*

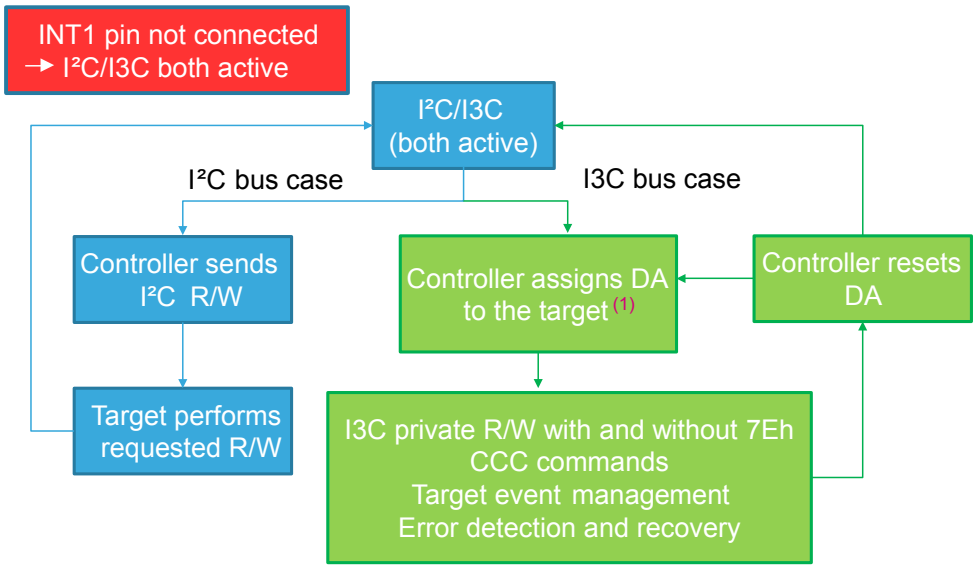
5.3 I²C/I3C coexistence in ASM330LHHG1

In the ASM330LHHG1, the SDA and SCL lines are common to both I²C and I3C. The I²C bus requires antispike filters on the SDA and SCL pins that are not compatible with I3C timing.

The device can be connected to both I²C and I3C or only to the I3C bus depending on the connection of the INT1 pin when the device is powered up:

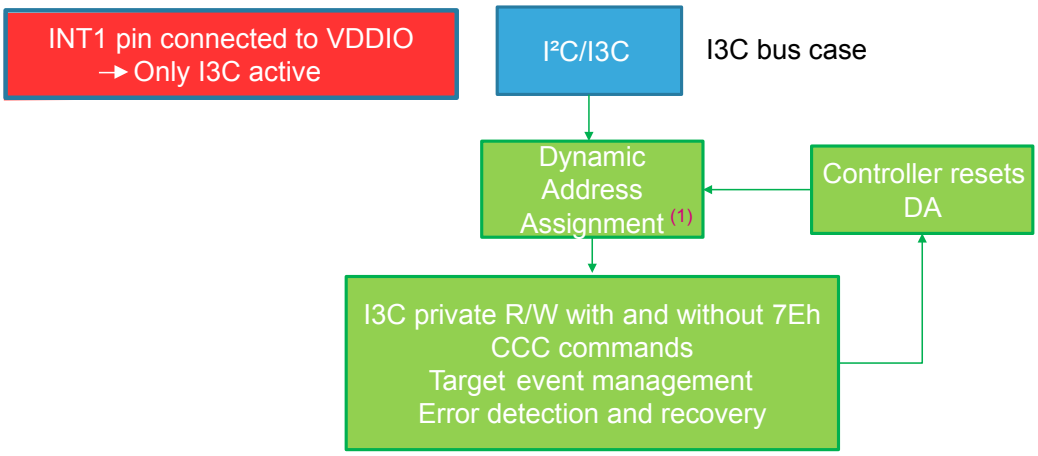
- INT1 pin floating (internal pull-down): I²C/I3C both active, see Figure 11
- INT1 pin connected to VDDIO: only I3C active, see Figure 12

Figure 11. I²C and I3C both active (INT1 pin not connected)



1. *Address assignment (DAA or ENTDA) must be performed with I²C fast mode plus timing. When the target is addressed, the I²C target is disabled and the timing is compatible with I3C specifications.*

Figure 12. Only I3C active (INT1 pin connected to VDDIO)



1. *When the target is I3C only, the I²C target is always disabled. The address can be assigned using I3C SDR timing.*

5.4 I²C controller interface

If the ASM330LHHG1 is configured in mode 2, an I²C controller line is available. The controller serial interface is mapped to the following dedicated pins.

Table 17. I²C controller pin details

Pin name	Pin description
CSCL	I²C controller serial clock
CSDA	I²C controller serial data
CDRDY	I²C controller external synchronization signal

6 Functionality

6.1 Operating modes

In the ASM330LHHG1, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The ASM330LHHG1 has three operating modes available:

- Only accelerometer active and gyroscope in power-down or sleep mode
- Only gyroscope active and accelerometer in power-down
- Both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR_XL[3:0] in CTRL1_XL (10h) while the gyroscope is activated from power-down by writing ODR_G[3:0] in CTRL2_G (11h). For combo mode the ODRs are totally independent.

Note: *If the accelerometer is to be activated in high-performance operating mode while the gyroscope is already running (that is, the gyroscope is not in power-down mode), proceed as follows:*

1. *Disable the accelerometer high-performance operating mode (set the XL_HM_MODE bit to 1 in the CTRL6_C (15h) register).*
2. *Write the CTRL1_XL (10h) register to 50h.*
3. *Read the OUTZ_H_A (2Dh) register to clear the XLDA bit in the STATUS_REG (1Eh) register.*
4. *Wait the duration of 1/ODR_XL or wait until the XLDA bit in the STATUS_REG (1Eh) register becomes equal to 1.*
5. *Enable the accelerometer high-performance operating mode (set the XL_HM_MODE bit to 0 in the CTRL6_C (15h) register).*
6. *Write the CTRL1_XL (10h) register to the desired value.*

6.2 Gyroscope power modes

In the ASM330LHHG1, the gyroscope can be configured in two different operating modes: low-power and high-performance mode. The operating mode selected depends on the value of the G_HM_MODE bit in CTRL7_G (16h). If G_HM_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 6667 Hz).

To enable low-power mode, the G_HM_MODE bit has to be set to 1. Low-power mode is available for ODRs equal to 12.5 Hz, 26 Hz, 52 Hz, 104 Hz and 208 Hz.

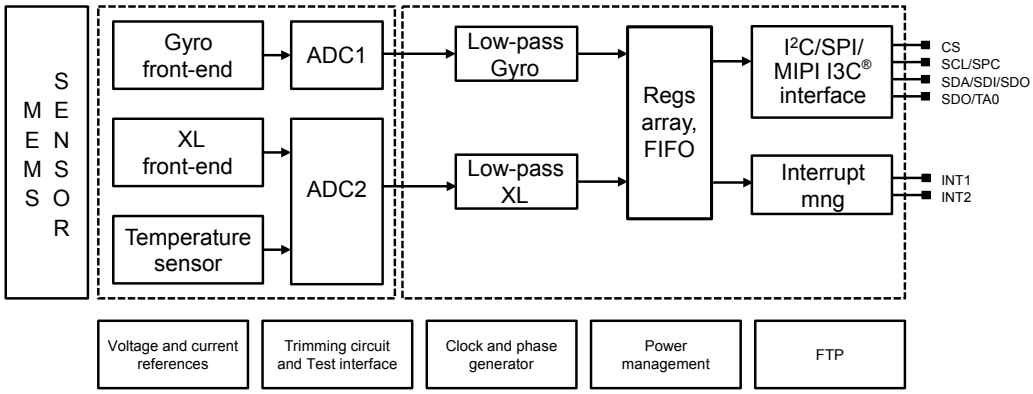
6.3 Accelerometer power modes

In the ASM330LHHG1, the accelerometer can be configured in two different operating modes: low-power and high-performance mode. The operating mode selected depends on the value of the XL_HM_MODE bit in CTRL6_C (15h). If XL_HM_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 6667 Hz).

To enable low-power mode, the XL_HM_MODE bit has to be set to 1. Low-power mode is available for ODRs equal to 1.6 Hz, 12.5 Hz, 26 Hz, 52 Hz, 104 Hz and 208 Hz.

6.4 Block diagram of filters

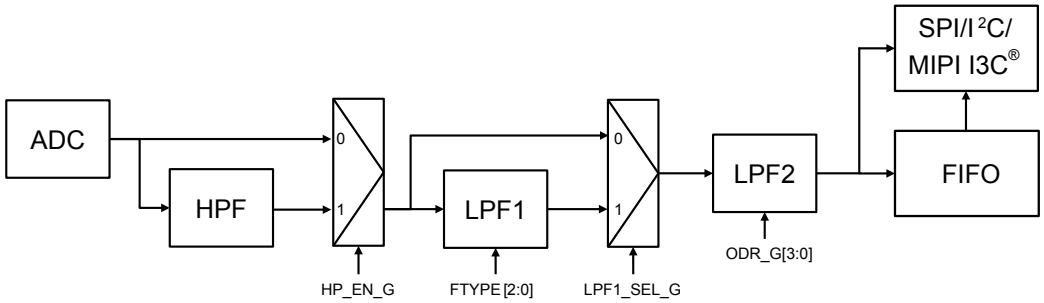
Figure 13. **Block diagram of filters**



6.4.1 Block diagram of the gyroscope filter

The gyroscope filtering chain appears below.

Figure 14. Gyroscope filtering chain



The gyroscope ODR is selectable from 12.5 Hz up to 6667 Hz. A low-pass filter (LPF1) is available, for more details about the filter characteristics see Table 59. Gyroscope LPF1 bandwidth selection. The digital LPF2 filter cannot be configured by the user and its cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

Data can be acquired from the output registers and FIFO.

Table 18. Gyroscope LPF2 bandwidth selection

Gyroscope ODR [Hz]	LPF2 cutoff [Hz]
12.5	4.3
26	8.3
52	16.7
104	33
208	67
417	133
833	267
1667	539
3333	1137
6667	3333

6.4.2 Block diagrams of the accelerometer filters

In the ASM330LHHG1, the filtering chain for the accelerometer part is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

Figure 15. Accelerometer chain

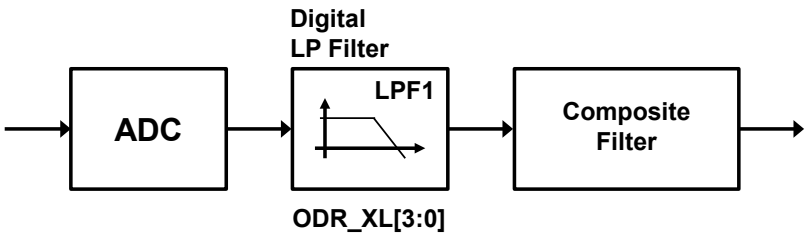
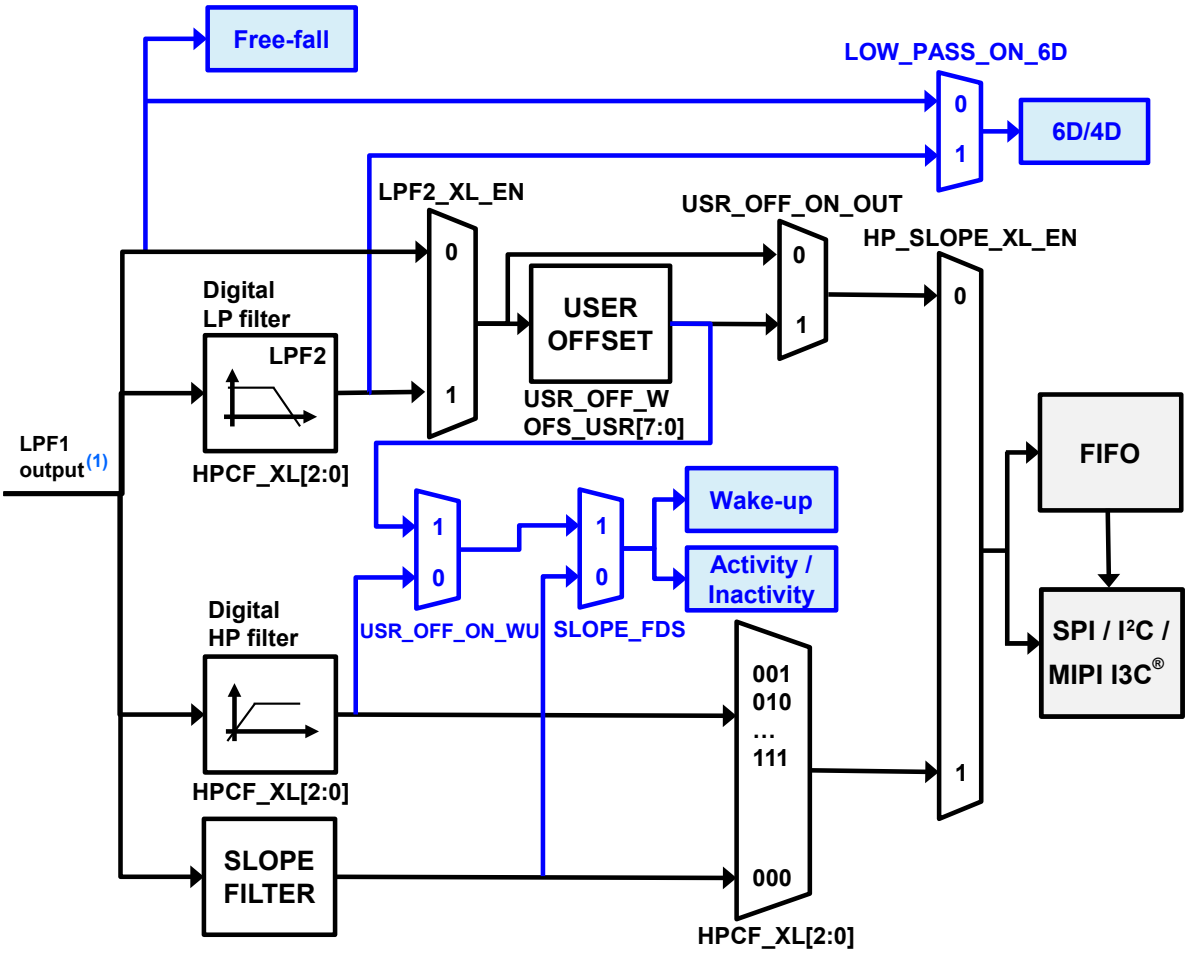


Figure 16. Accelerometer composite filter



1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode and ODR up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power mode.*

6.5 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The ASM330LHHG1 embeds 3 KB of data in FIFO to store the following data:

- Gyroscope
- Accelerometer
- External sensors (up to four)
- Timestamp
- Temperature

Writing data in the FIFO can be configured to be triggered by the:

- Accelerometer / gyroscope data-ready signal
- Sensor hub data-ready signal

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batch rates can be selected by the user. Writing external sensor data in FIFO can be triggered by the accelerometer data-ready signal or by an external sensor interrupt. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

The programmable FIFO watermark threshold can be set in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h) using the WTM[8:0] bits. To monitor the FIFO status, dedicated registers (FIFO_STATUS1 (3Ah), FIFO_STATUS2 (3Bh)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1_CTRL (0Dh) and INT2_CTRL (0Eh).

The FIFO buffer can be configured according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the FIFO_CTRL4 (0Ah) register.

6.5.1 Bypass mode

In bypass mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

6.5.2 FIFO mode

In FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0]) to 000. After this reset command, it is possible to restart FIFO mode by writing FIFO_CTRL4 (0Ah) (FIFO_MODE_[2:0]) to 001.

The FIFO buffer memorizes up to 3 KB of data but the depth of the FIFO can be resized by setting the WTM[8:0] bits in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h). If the STOP_ON_WTM bit in FIFO_CTRL2 (08h) is set to 1, FIFO depth is limited up to the WTM[8:0] bits in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h).

6.5.3 Continuous mode

Continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag FIFO_STATUS2 (3Bh)(FIFO_WTM_IA) is asserted when the number of unread samples in FIFO is greater than or equal to FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h) (WTM[8:0]).

It is possible to route the FIFO_WTM_IA flag to the INT1 pin by writing in register INT1_CTRL (0Dh) (INT1_FIFO_TH) = 1 or to the INT2 pin by writing in register INT2_CTRL (0Eh)(INT2_FIFO_TH) = 1.

A full-flag interrupt can be enabled, INT1_CTRL (0Dh)(INT1_FIFO_FULL) = 1 or INT2_CTRL (0Eh) (INT2_FIFO_FULL) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO_OVR_IA flag in FIFO_STATUS2 (3Bh) is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in FIFO_STATUS1 (3Ah) and FIFO_STATUS2 (3Bh)(DIFF_FIFO_[9:0]).

6.5.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

6.5.5 Bypass-to-continuous mode

In bypass-to-continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 100), data measurement storage inside FIFO operates in continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

6.5.6 Bypass-to-FIFO mode

n bypass-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

6.5.7 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (FIFO_DATA_OUT_TAG (78h), in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (79h) to (7Eh)).

The DIFF_FIFO_[9:0] field in the FIFO_STATUS1 (3Ah) and FIFO_STATUS2 (3Bh) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

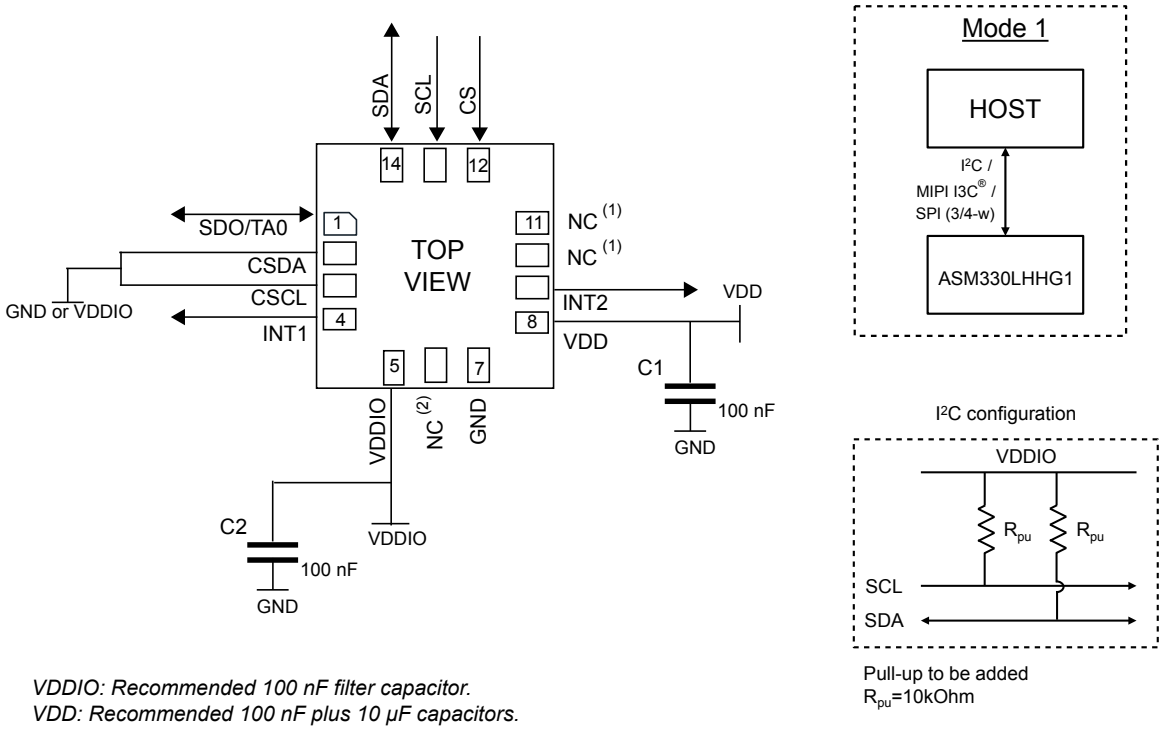
In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag COUNTER_BDR_IA in FIFO_STATUS2 (3Bh) alerts that the counter reaches a selectable threshold (CNT_BDR_TH_[10:0] field in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG_COUNTER_BDR bit in COUNTER_BDR_REG1 (0Bh). As for the other FIFO status events, the flag COUNTER_BDR_IA can be routed to the INT1 or INT2 pins by asserting the corresponding bits (INT1_CNT_BDR of INT1_CTRL (0Dh) and INT2_CNT_BDR of INT2_CTRL (0Eh)).

Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the ODR_CHG_EN bit in FIFO_CTRL2 (08h).

7 Application hints

7.1 ASM330LHHG1 electrical connections in mode 1

Figure 17. ASM330LHHG1 electrical connections in mode 1



VDDIO: Recommended 100 nF filter capacitor.
VDD: Recommended 100 nF plus 10 µF capacitors.

1. *Leave pin electrically unconnected and soldered to PCB.*
2. *Connect to VDDIO or GND or leave unconnected and soldered to PCB.*

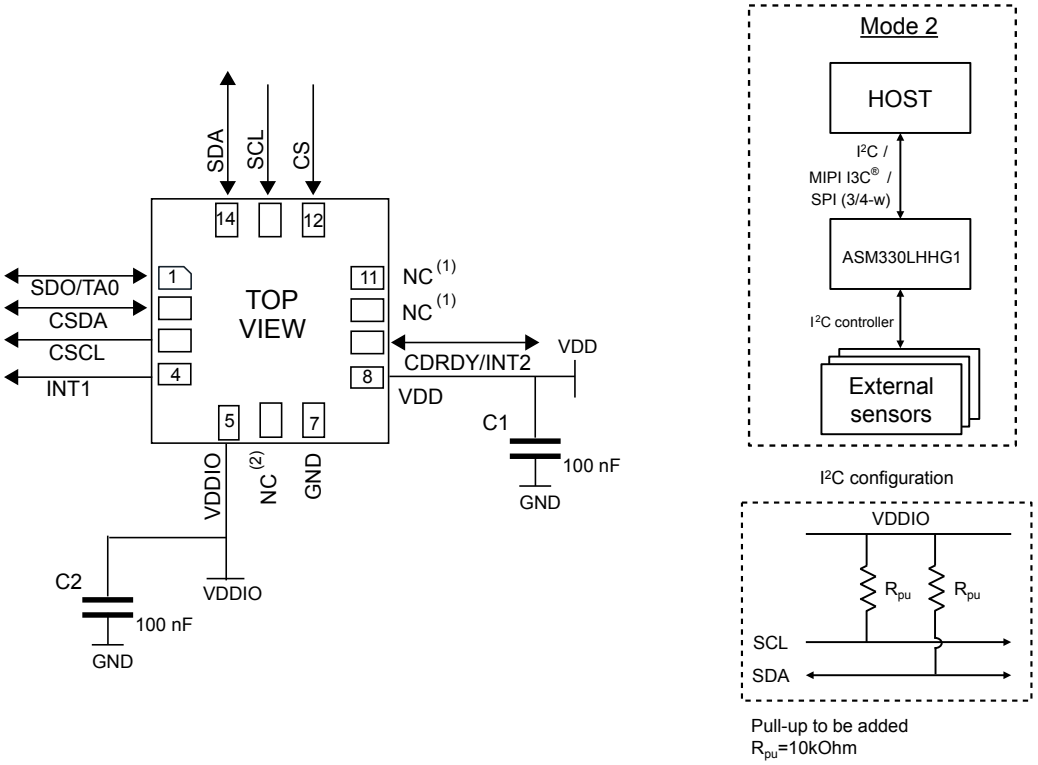
The device core is supplied through the VDD line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® primary interface.

7.2 ASM330LHHG1 electrical connections in mode 2

Figure 18. **ASM330LHHG1 electrical connections in mode 2**



1. *Leave pin electrically unconnected and soldered to PCB.*
2. *Connect to VDDIO or GND or leave unconnected and soldered to PCB.*

The device core is supplied through the VDD line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C/MIPI I3C® primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C/MIPI I3C® primary interface.

Table 19. Internal pin status

Pin #	Name	Mode 1 function	Mode 2 function	Pin status mode 1	Pin status mode 2
1	SDO	SPI 4-wire interface serial data output (SDO)	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h).	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h).
	TA0	I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)	I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)		
2	CSDA	Connect to VDDIO or GND	I²C controller serial data (CSDA)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register CONTROLLER_CONFIG (14h). (see Note to enable pull-up)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register CONTROLLER_CONFIG (14h). (see Note to enable pull-up)
3	CSCL	Connect to VDDIO or GND	I²C controller serial clock (CSCL)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register CONTROLLER_CONFIG (14h). (see Note to enable pull-up)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in register CONTROLLER_CONFIG (14h). (see Note to enable pull-up)
4	INT1	Programmable interrupt 1. If device is used as MIPI I3C® pure target, this pin must be set to 1.	Programmable interrupt 1. If device is used as MIPI I3C® pure target, this pin must be set to 1.	Default: input with pull-down(1) Pull-down is disabled if bit PD_DIS_INT1 = 1 in register I3C_BUS_AVB (62h).	Default: input with pull-down(1) Pull-down is disabled if bit PD_DIS_INT1 = 1 in register I3C_BUS_AVB (62h).
5	VDDIO	Power supply for I/O pins	Power supply for I/O pins		
6	NC	Connect to VDDIO or GND or leave unconnected	Connect to VDDIO or GND or leave unconnected		
7	GND	0 V supply	0 V supply		
8	VDD	Power supply	Power supply		
9	INT2	Programmable interrupt 2 (INT2) / Data enabled (DEN)	Programmable interrupt 2 (INT2) / Data enabled (DEN)/ I²C controller external synchronization signal (CDRDY)	Default: output forced to ground	Default: output forced to ground
10	NC	Leave unconnected	Leave unconnected		
11	NC	Leave unconnected	Leave unconnected		
12	CS	I²C and MIPI I3C®/SPI mode selection (1:SPI idle mode / I²C and MIPI I3C® communication enabled; 0: SPI communication mode / I²C and MIPI I3C® disabled)	I²C and MIPI I3C®/SPI mode selection (1:SPI idle mode / I²C and MIPI I3C® communication enabled; 0: SPI communication mode / I²C and MIPI I3C® disabled)	Default: input with pull-up Pull-up is disabled if bit I2C_disable = 1 in register CTRL4_C (13h) and I3C_disable = 1 in register CTRL9_XL (18h).	Default: input with pull-up Pull-up is disabled if bit I2C_disable = 1 in register CTRL4_C (13h) and I3C_disable = 1 in register CTRL9_XL (18h).
13	SCL	I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC)	I²C/MIPI I3C® serial clock (SCL) / SPI serial port clock (SPC)	Default: input without pull-up	Default: input without pull-up
14	SDA	I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	I²C/MIPI I3C® serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up	Default: input without pull-up

1. *INT1 must be set to 0 or left unconnected during power-on if the I²C/SPI interfaces are used.*

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on VDDIO.

Note: The procedure to enable the pull-up on pins 2 and 3 is as follows:

1. From the primary I²C/I3C/SPI interface: write 40h in register at address 01h (enable access to the sensor hub registers)

2. From the primary I²C/I3C/SPI interface: write 08h in register at address 14h (enable the pull-up on pins 2 and 3)

3. From the primary I²C/I3C/SPI interface: write 00h in register at address 01h (disable access to the sensor hub registers)

8 Register map

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 20. Registers address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
FUNC_CFG_ACCESS	R/W	01	00000001	00000000	
PIN_CTRL	R/W	02	00000010	00111111	
RESERVED	-	03-06			Reserved
FIFO_CTRL1	R/W	07	00000111	00000000	
FIFO_CTRL2	R/W	08	00001000	00000000	
FIFO_CTRL3	R/W	09	00001001	00000000	
FIFO_CTRL4	R/W	0A	00001010	00000000	
COUNTER_BDR_REG1	R/W	0B	00001011	00000000	
COUNTER_BDR_REG2	R/W	0C	00001100	00000000	
INT1_CTRL	R/W	0D	00001101	00000000	
INT2_CTRL	R/W	0E	00001110	00000000	
WHO_AM_I	R	0F	00001111	01101011	
CTRL1_XL	R/W	10	00010000	00000000	
CTRL2_G	R/W	11	00010001	00000000	
CTRL3_C	R/W	12	00010010	00000100	
CTRL4_C	R/W	13	00010011	00000000	
CTRL5_C	R/W	14	00010100	00000000	
CTRL6_C	R/W	15	00010101	00000000	
CTRL7_G	R/W	16	00010110	00000000	
CTRL8_XL	R/W	17	00010111	00000000	
CTRL9_XL	R/W	18	00011000	11100000	
CTRL10_C	R/W	19	00011001	00000000	
ALL_INT_SRC	R	1A	00011010	output	
WAKE_UP_SRC	R	1B	00011011	output	
RESERVED	-	1C			Reserved
D6D_SRC	R	1D	00011101	output	
STATUS_REG	R	1E	00011110	output	
RESERVED	-	1F			Reserved
OUT_TEMP_L	R	20	00100000	output	
OUT_TEMP_H	R	21	00100001	output	
OUTX_L_G	R	22	00100010	output	
OUTX_H_G	R	23	00100011	output	
OUTY_L_G	R	24	00100100	output	
OUTY_H_G	R	25	00100101	output	
OUTZ_L_G	R	26	00100110	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUTZ_H_G	R	27	00100111	output	
OUTX_L_A	R	28	00101000	output	
OUTX_H_A	R	29	00101001	output	
OUTY_L_A	R	2A	00101010	output	
OUTY_H_A	R	2B	00101011	output	
OUTZ_L_A	R	2C	00101100	output	
OUTZ_H_A	R	2D	00101101	output	
RESERVED	-	2E-38			Reserved
STATUS_CONTROLLER_MAINPAGE	R	39	00111001	output	
FIFO_STATUS1	R	3A	00111010	output	
FIFO_STATUS2	R	3B	00111011	output	
RESERVED	-	3C-3F			Reserved
TIMESTAMP0_REG	R	40	01000000	output	
TIMESTAMP1_REG	R	41	01000001	output	
TIMESTAMP2_REG	R	42	01000010	output	
TIMESTAMP3_REG	R	43	01000011	output	
RESERVED	-	44-55			Reserved
INT_CFG0	R/W	56	01010110	00000000	
RESERVED	-	57			Reserved
INT_CFG1	R/W	58	01011000	00000000	
THS_6D	R/W	59	01011001	00000000	
RESERVED	-	5A			Reserved
WAKE_UP_THS	R/W	5B	01011011	00000000	
WAKE_UP_DUR	R/W	5C	01011100	00000000	
FREE_FALL	R/W	5D	01011101	00000000	
MD1_CFG	R/W	5E	01011110	00000000	
MD2_CFG	R/W	5F	01011111	00000000	
RESERVED	-	60-61		00000000	Reserved
I3C_BUS_AVB	R/W	62	01100010	00000000	
INTERNAL_FREQ_FINE	R	63	01100011	output	
RESERVED	-	64-72			Reserved
X_OFS_USR	R/W	73	01110011	00000000	
Y_OFS_USR	R/W	74	01110100	00000000	
Z_OFS_USR	R/W	75	01110101	00000000	
RESERVED	-	76-77			Reserved
FIFO_DATA_OUT_TAG	R	78	01111000	output	
FIFO_DATA_OUT_X_L	R	79	01111001	output	
FIFO_DATA_OUT_X_H	R	7A	01111010	output	
FIFO_DATA_OUT_Y_L	R	7B	01111011	output	
FIFO_DATA_OUT_Y_H	R	7C	01111100	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
FIFO_DATA_OUT_Z_L	R	7D	01111101	output	
FIFO_DATA_OUT_Z_H	R	7E	01111110	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write data through the serial interface.

9.1 FUNC_CFG_ACCESS (01h)

Enable access to sensor hub registers (R/W)

Table 21. FUNC_CFG_ACCESS register

0(1)	SHUB_REG_ ACCESS	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 22. FUNC_CFG_ACCESS register description

SHUB_REG_ACCESS	Enables access to the sensor hub (I²C controller) registers. Default value: 0(1)

1. *Details concerning the sensor hub registers are available in Section 10: Sensor hub register mapping and Section 11: Sensor hub register description.*

9.2 PIN_CTRL (02h)

Enable SDO pin pull-up register (R/W)

Table 23. PIN_CTRL register

0(1)	SDO_ PU_EN	1(2)	1(2)	1(2)	1(2)	1(2)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 24. PIN_CTRL register description

SDO_PU_EN	Enables pull-up on SDO pin. Default value: 0 (0: SDO pin pull-up disconnected (default); 1: SDO pin with pull-up)

9.3 FIFO_CTRL1 (07h)

FIFO control register 1 (R/W)

Table 25. FIFO_CTRL1 register

WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

Table 26. FIFO_CTRL1 register description

WTM[7:0]	FIFO watermark threshold, in conjunction with WTM8 in FIFO_CTRL2 (08h) 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of samples written in the FIFO is greater than or equal to the threshold level.

9.4 FIFO_CTRL2 (08h)

FIFO control register 2 (R/W)

Table 27. FIFO_CTRL2 register

STOP_ON_WTM	0(1)	0(1)	ODRCHG_EN	0(1)	0(1)	0(1)	WTM8

1. *This bit must be set to 0 for the correct operation of the device.*

Table 28. FIFO_CTRL2 register

STOP_ON_WTM	Sensing chain FIFO stop values memorization at threshold level (0: FIFO depth is not limited (default); 1: FIFO depth is limited to the threshold level, defined in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h)
ODRCHG_EN	Enables ODR CHANGE virtual sensor to be batched in FIFO
WTM8	FIFO watermark threshold, in conjunction with WTM[7:0] in FIFO_CTRL1 (07h) 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of samples written in FIFO is greater than or equal to the threshold level.

9.5 FIFO_CTRL3 (09h)

FIFO control register 3 (R/W)

Table 29. FIFO_CTRL3 register

BDR_GY_3	BDR_GY_2	BDR_GY_1	BDR_GY_0	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0

Table 30. FIFO_CTRL3 register description

BDR_GY_[3:0]	Selects batch data rate (write frequency in FIFO) for gyroscope data. (0000: gyroscope not batched in FIFO (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011: 6.5 Hz; 1100-1111: reserved)
BDR_XL_[3:0]	Selects batch data rate (write frequency in FIFO) for accelerometer data. (0000: accelerometer not batched in FIFO (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 417 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011: 1.6 Hz; 1100-1111: reserved)

9.6 FIFO_CTRL4 (0Ah)

FIFO control register 4 (R/W)

Table 31. FIFO_CTRL4 register

DEC_TS_ BATCH_1	DEC_TS_ BATCH_0	ODR_T_ BATCH_1	ODR_T_ BATCH_0	0(1)	FIFO_ MODE2	FIFO_ MODE1	FIFO_ MODE0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 32. FIFO_CTRL4 register description

DEC_TS_BATCH_[1:0]	Selects decimation for timestamp batching in FIFO. The write rate is the maximum rate between accelerometer and gyroscope BDR divided by decimation decoder. (00: timestamp not batched in FIFO (default); 01: decimation 1: max(BDR_XL[Hz],BDR_GY[Hz]) [Hz]; 10: decimation 8: max(BDR_XL[Hz],BDR_GY[Hz])/8 [Hz]; 11: decimation 32: max(BDR_XL[Hz],BDR_GY[Hz])/32 [Hz])
ODR_T_BATCH_[1:0]	Selects batch data rate (write frequency in FIFO) for temperature data (00: temperature not batched in FIFO (default); 01: 1.6 Hz; 10: 12.5 Hz; 11: 52 Hz)
FIFO_MODE[2:0]	FIFO mode selection (000: bypass mode: FIFO disabled; 001: FIFO mode: stops collecting data when FIFO is full; 010: reserved; 011: continuous-to-FIFO mode: continuous mode until trigger is deasserted, then FIFO mode; 100: bypass-to-continuous mode: bypass mode until trigger is deasserted, then continuous mode; 101: reserved; 110: continuous mode: if the FIFO is full, the new sample overwrites the older one; 111: bypass-to-FIFO mode: bypass mode until trigger is deasserted, then FIFO mode.)

9.7 COUNTER_BDR_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

Table 33. COUNTER_BDR_REG1 register

dataready_ pulsed	RST_COUNTER _BDR	TRIG_COUNTER _BDR	0(1)	0(1)	CNT_BDR_ TH_10	CNT_BDR_ TH_9	CNT_BDR_ TH_8

1. *This bit must be set to 0 for the correct operation of the device.*

Table 34. COUNTER_BDR_REG1 register description

dataready_pulsed	Enables pulsed data-ready mode (0: data-ready latched mode (returns to 0 only after an interface reading) (default); 1: data-ready pulsed mode (the data ready pulses are 75 µs long)
RST_COUNTER_BDR	Resets the internal counter of batch events for a single sensor. This bit is automatically reset to zero if it was set to 1.
TRIG_COUNTER_BDR	Selects the trigger for the internal counter of batch events between the accelerometer and gyroscope. (0: accelerometer batch event; 1: gyroscope batch event)
CNT_BDR_TH_[10:8]	In conjunction with CNT_BDR_TH_[7:0] in COUNTER_BDR_REG2 (0Ch), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (3Bh) is set to 1.

9.8 COUNTER_BDR_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

Table 35. COUNTER_BDR_REG2 register

CNT_BDR_ TH_7	CNT_BDR_ TH_6	CNT_BDR_ TH_5	CNT_BDR_ TH_4	CNT_BDR_ TH_3	CNT_BDR_ TH_2	CNT_BDR_ TH_1	CNT_BDR_ TH_0

Table 36. COUNTER_BDR_REG2 register description

CNT_BDR_TH_[7:0]	In conjunction with CNT_BDR_TH_[10:8] in COUNTER_BDR_REG1 (0Bh), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (3Bh) is set to 1.

9.9 INT1_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1 when the MIPI I3C® dynamic address is not assigned (I²C or SPI is used). Some bits can also be used to trigger an IBI (in-band interrupt) when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in register MD1_CFG (5Eh).

Table 37. INT1_CTRL register

DEN_DRDY _flag	INT1_ CNT_BDR	INT1_ FIFO_FULL	INT1_ FIFO_OVR	INT1_ FIFO_TH	INT1_ BOOT	INT1_ DRDY_G	INT1_ DRDY_XL

Table 38. INT1_CTRL register description

DEN_DRDY_flag	Sends DEN_DRDY (DEN stamped on sensor data flag) to the INT1 pin.
INT1_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT1.
INT1_FIFO_FULL	Enables FIFO full flag interrupt on the INT1 pin. It can also be used to trigger an IBI when the MIPI I3C® interface is used.
INT1_FIFO_OVR	Enables FIFO overrun interrupt on the INT1 pin. It can also be used to trigger an IBI when the MIPI I3C® interface is used.
INT1_FIFO_TH	Enables FIFO threshold interrupt on the INT1 pin. It can also be used to trigger an IBI when the MIPI I3C® interface is used.
INT1_BOOT	Enables boot status on the INT1 pin.
INT1_DRDY_G	Enables gyroscope data-ready interrupt on the INT1 pin. It can also be used to trigger an IBI when the MIPI I3C® interface is used.
INT1_DRDY_XL	Enables accelerometer data-ready interrupt on the INT1 pin. It can also be used to trigger an IBI when the MIPI I3C® interface is used.

9.10 INT2_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2 when the MIPI I3C dynamic address is not assigned (I²C or SPI is used). Some bits can also be used to trigger an IBI when the MIPI I3C® interface is used. The output of the pin is the OR combination of the signals selected here and in register MD2_CFG (5Fh).

Table 39. INT2_CTRL register

0(1)	INT2_ CNT_BDR	INT2_ FIFO_FULL	INT2_ FIFO_OVR	INT2_ FIFO_TH	INT2_ DRDY_TEMP	INT2_ DRDY_G	INT2_ DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 40. INT2_CTRL register description

INT2_CNT_BDR	Enables COUNTER_BDR_IA interrupt on the INT2 pin.
INT2_FIFO_FULL	Enables FIFO full flag interrupt on the INT2 pin.
INT2_FIFO_OVR	Enables FIFO overrun interrupt on the INT2 pin.
INT2_FIFO_TH	Enables FIFO threshold interrupt on the INT2 pin.
INT2_DRDY_TEMP	Enables temperature sensor data-ready interrupt on the INT2 pin. It can be also used to trigger an IBI when the MIPI I3C® interface is used and INT2_ON_INT1 = 1 in CTRL4_C (13h).
INT2_DRDY_G	Enables gyroscope data-ready interrupt on the INT2 pin.
INT2_DRDY_XL	Enables accelerometer data-ready interrupt on the INT2 pin.

9.11 WHO_AM_I (0Fh)

WHO_AM_I register (R). This is a read-only register. Its value is fixed at 6Bh.

Table 41. Who_Am_I register

0	1	1	0	1	0	1	1

9.12 CTRL1_XL (10h)

Accelerometer control register 1 (R/W)

Table 42. CTRL1_XL register

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	LPF2_XL_EN	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 43. CTRL1_XL register description

ODR_XL[3:0]	Accelerometer ODR selection (see Table 44)
FS[1:0]_XL	Accelerometer full-scale selection. Default value: 00 (00: ±2 *g*; 01: ±16 *g*; 10: ±4 *g*; 11: ±8 *g*)
LPF2_XL_EN	Accelerometer high-resolution selection (0: output from first stage digital filtering selected (default); 1: output from LPF2 second filtering stage selected)

Table 44. Accelerometer ODR register setting

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz] when XL_HM_MODE = 1 in CTRL6_C (15h)	ODR selection [Hz] when XL_HM_MODE = 0 in CTRL6_C (15h)
0	0	0	0	Power-down	Power-down
1	0	1	1	1.6 Hz (low power only)	N.A.
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (low power)	104 Hz (high performance)
0	1	0	1	208 Hz (low power)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1667 Hz (high performance)	1667 Hz (high performance)
1	0	0	1	3333 Hz (high performance)	3333 Hz (high performance)
1	0	1	0	6667 Hz (high performance)	6667 Hz (high performance)
1	1	x	x	Reserved	Reserved

9.13 CTRL2_G (11h)

Gyroscope control register 2 (R/W)

Table 45. CTRL2_G register

ODR_G3	ODR_G2	ODR_G1	ODR_G0	FS1_G	FS0_G	FS_125	FS_4000

Table 46. CTRL2_G register description

ODR_G[3:0]	Gyroscope output data rate selection. Default value: 0000 (Refer to Table 47)
FS[1:0]_G	Gyroscope chain full-scale selection (00: ±250 dps; 01: ±500 dps; 10: ±1000 dps; 11: ±2000 dps)
FS_125	Selects gyroscope chain full-scale ±125 dps (0: FS selected through bits FS[1:0]_G; 1: FS set to ±125 dps)
FS_4000	Selects gyroscope chain full-scale ±4000 dps (0: FS selected through bits FS[1:0]_G or FS_125; 1: FS set to ±4000 dps)

Table 47. Gyroscope ODR configuration setting

ODR_G3	ODR_G2	ODR_G1	ODR_G0	ODR selection [Hz] when G_HM_MODE = 1 in CTRL7_G (16h)	ODR selection [Hz] when G_HM_MODE = 0 in CTRL7_G (16h)
0	0	0	0	Power-down	Power-down
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (low power)	104 Hz (high performance)
0	1	0	1	208 Hz (low power)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1667 Hz (high performance)	1667 Hz (high performance)
1	0	0	1	3333 Hz (high performance)	3333 Hz (high performance)
1	0	1	0	6667 Hz (high performance)	6667 Hz (high performance)
1	0	1	1	Reserved	Reserved

9.14 CTRL3_C (12h)

Control register 3 (R/W)

Table 48. CTRL3_C register

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	0(1)	SW_RESET

1. *This bit must be set to 0 for the correct operation of the device.*

Table 49. CTRL3_C register description

BOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content) Note: the accelerometer must be ON. This bit is automatically cleared.
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers are not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pins. This bit must be set to 0 when H_LACTIVE is set to 1. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared.

9.15 CTRL4_C (13h)

Control register 4 (R/W)

Table 50. CTRL4_C register

0(1)	SLEEP_G	INT2_on_INT1	0(1)	DRDY_MASK	I2C_disable	LPF1_SEL_G	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 51. CTRL4_C register description

SLEEP_G	Enables gyroscope sleep mode. Default value:0 (0: disabled; 1: enabled)
INT2_on_INT1	Enables all interrupt signals available on the INT1 pin. Default value: 0 (0: interrupt signals divided between the INT1 and INT2 pins; 1: all interrupt signals in logic or on the INT1 pin)
DRDY_MASK	Enables data available (0: disabled; 1: mask DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked).
I2C_disable	Disables I²C interface. Default value: 0 (0: SPI, I²C, and MIPI I3C® interfaces enabled (default); 1: I²C interface disabled)
LPF1_SEL_G	Enables gyroscope digital LPF1; the bandwidth can be selected through FTYPE[2:0] in CTRL6_C (15h). (0: disabled; 1: enabled)

9.16 CTRL5_C (14h)

Control register 5 (R/W)

Table 52. CTRL5_C register

0(1)	ROUNDING1	ROUNDING0	0(1)	ST1_G	ST0_G	ST1_XL	ST0_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 53. CTRL5_C register description

ROUNDING[1:0]	Circular burst mode (wraparound) read of the output registers. Default value: 00 (00: no wraparound; 01: accelerometer only; 10: gyroscope only; 11: gyroscope + accelerometer)
ST[1:0]_G	Enables angular rate sensor self-test. Default value: 00 (00: self-test disabled; other: refer to Table 54)
ST[1:0]_XL	Enables linear acceleration sensor self-test. Default value: 00 (00: self-test disabled; other: refer to Table 55)

Table 54. Angular rate sensor self-test mode selection

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Not allowed
1	1	Negative sign self-test

Table 55. Linear acceleration sensor self-test mode selection

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

9.17 CTRL6_C (15h)

Control register 6 (R/W)

Table 56. CTRL6_C register

TRIG_EN	LVL1_EN	LVL2_EN	XL_HM_ MODE	USR_ OFF_W	FTYPE_2	FTYPE_1	FTYPE_0

Table 57. CTRL6_C register description

TRIG_EN	Enables DEN data edge-sensitive trigger mode. Refer to Table 58.
LVL1_EN	Enables DEN data level-sensitive trigger mode. Refer to Table 58.
LVL2_EN	Enables DEN level-sensitive latched mode. Refer toTable 58.
XL_HM_MODE	Disables high-performance operating mode for accelerometer. Default value: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)
USR_OFF_W	Weight of XL user offset bits of registers X_OFS_USR (73h), Y_OFS_USR (74h), Z_OFS_USR (75h) (0: 2^{-10} *g*/LSB; 1: 2^{-6} *g*/LSB)
FTYPE[2:0]	Gyroscope low-pass filter (LPF1) bandwidth selection. Table 59 shows the selectable bandwidth values.

Table 58. Trigger mode selection

TRIG_EN, LVL1_EN, LVL2_EN	Trigger mode
100	Edge-sensitive trigger mode is selected
010	Level-sensitive trigger mode is selected
011	Level-sensitive latched mode is selected
110	Level-sensitive FIFO mode is selected

Table 59. Gyroscope LPF1 bandwidth selection

FTYPE[2:0]	12.5 Hz	26 Hz	52 Hz	104 Hz	208 Hz	416 Hz	833 Hz	1667 Hz	3333 Hz	6667 Hz
000	4.3	8.3	16.7	33	67	133	222	274	292	297
001	4.3	8.3	16.7	33	67	128	186	212	220	223
010	4.3	8.3	16.7	33	67	112	140	150	153	154
011	4.3	8.3	16.7	33	67	134	260	390	451	470
100	4.3	8.3	16.7	34	62	86	96	99	NA	
101	4.3	8.3	16.9	31	43	48	49	50	NA	
110	4.3	8.3	13.4	19	23	24.6	25	25	NA	
111	4.3	8.3	9.8	11.6	12.2	12.4	12.6	12.6	NA	

9.18 CTRL7_G (16h)

Control register 7 (R/W)

Table 60. CTRL7_G register

G_HM_MODE	HP_EN_G	HPM1_G	HPM0_G	0(1)	0(1)	USR_OFF_ON_OUT	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

G_HM_MODE	Disables high-performance operating mode for gyroscope. Default: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)
HP_EN_G	Enables gyroscope digital high-pass filter. The filter is enabled only if the gyroscope is in HP mode. Default value: 0 (0: HPF disabled; 1: HPF enabled)
HPM_G[1:0]	Gyroscope digital HP filter cutoff selection. Default: 00 (00: 16 mHz; 01: 65 mHz; 10: 260 mHz; 11: 1.04 Hz)
USR_OFF_ON_OUT	Enables accelerometer user offset correction block; it's valid for the low-pass path - see Figure 16 . Default value: 0 (0: accelerometer user offset correction block bypassed; 1: accelerometer user offset correction block enabled)

9.19 CTRL8_XL (17h)

Control register 8 (R/W)

Table 61. CTRL8_XL register

HPCF_XL_2	HPCF_XL_1	HPCF_XL_0	HP_REF_MODE_XL	FASTSETTL_MODE_XL	HP_SLOPE_XL_EN	0(1)	LOW_PASS_ON_6D

1. *This bit must be set to 0 for the correct operation of the device.*

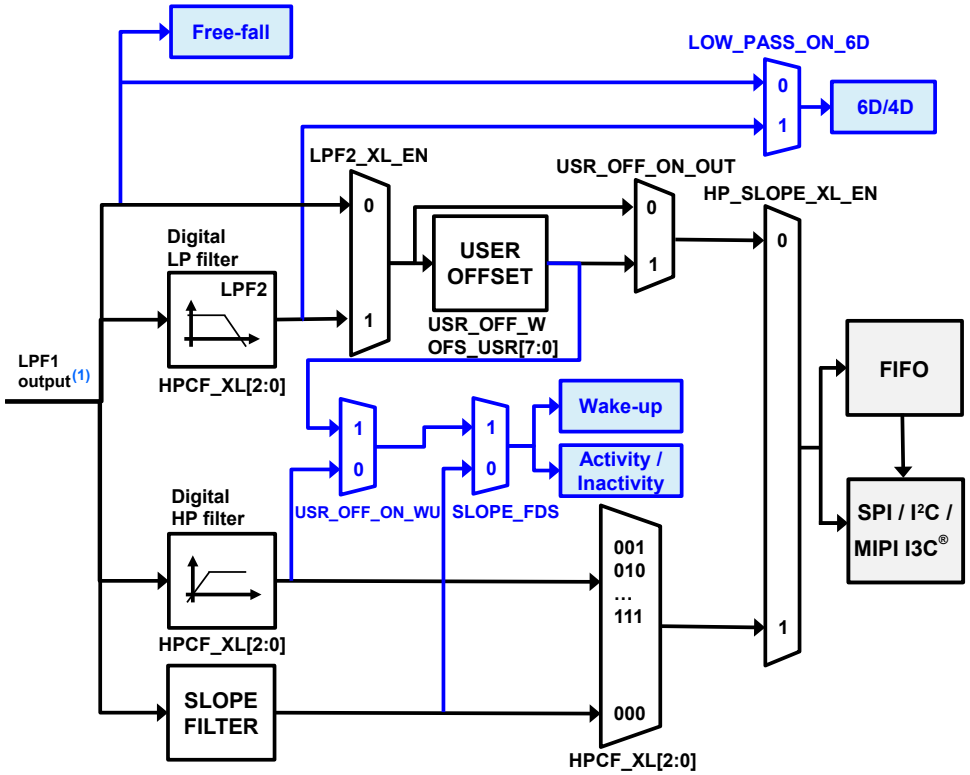
HPCF_XL_[2:0]	Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to Table 62.
HP_REF_MODE_XL	Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be 1). Default value: 0(1) (0: disabled, 1: enabled)
FASTSETTL_MODE_XL	Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the second samples after writing this bit. Active only during device exit from power- down mode. Default value: 0 (0: disabled, 1: enabled)
HP_SLOPE_XL_EN	Accelerometer slope filter / high-pass filter selection. Refer to Figure 19.
LOW_PASS_ON_6D	LPF2 on 6D function selection. Refer to Figure 19. Default value: 0 (0: ODR/2 low-pass filtered data sent to 6D interrupt function; 1: LPF2 output data sent to 6D interrupt function)

1. *When enabled, the first output data have to be discarded.*

Table 62. **Accelerometer bandwidth configurations**

Filter type	HP_SLOPE_ XL_EN	LPF2_XL_EN	HPCF_XL_[2:0]	Bandwidth
Low pass	0	0	-	ODR/2
		1	000	ODR/4
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800
High pass	1	-	000	SLOPE (ODR/4)
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800

Figure 19. **Accelerometer block diagram**



1. *The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode and ODR up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power mode.*

9.20 CTRL9_XL (18h)

Control register 9 (R/W)

Table 63. CTRL9_XL register

DEN_X	DEN_Y	DEN_Z	DEN_XL_G	DEN_XL_EN	DEN_LH	I3C_disable	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 64. CTRL9_XL register description

DEN_X	DEN value stored in LSB of X-axis. Default value: 1 (0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB)
DEN_Y	DEN value stored in LSB of Y-axis. Default value: 1 (0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB)
DEN_Z	DEN value stored in LSB of Z-axis. Default value: 1 (0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB)
DEN_XL_G	DEN stamping sensor selection. Default value: 0 (0: DEN pin info stamped in the gyroscope axis selected by bits [7:5]; 1: DEN pin info stamped in the accelerometer axis selected by bits [7:5])
DEN_XL_EN	Extends DEN functionality to accelerometer sensor. Default value: 0 (0: disabled; 1: enabled)
DEN_LH	DEN active level configuration. Default value: 0 (0: active low; 1: active high)
I3C_disable	Disables MIPI I3C® communication protocol(1) (0: SPI, I²C, MIPI I3C® interfaces enabled (default); 1: MIPI I3C® interface disabled)

1. *It is recommended to set this bit to 1 during the initial device configuration phase, when the I3C interface is not used.*

9.21 CTRL10_C (19h)

Control register 10 (R/W)

Table 65. CTRL10_C register

0(1)	0(1)	TIMESTAMP_EN	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 66. CTRL10_C register description

TIMESTAMP_EN	Enables timestamp counter. Default value: 0 (0: disabled; 1: enabled) The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h).

9.22 ALL_INT_SRC (1Ah)

Source register for all interrupts (R)

Table 67. ALL_INT_SRC register

TIMESTAMP_ENDCOUNT	0	SLEEP_CHANGE_IA	D6D_IA	0	0	WU_IA	FF_IA

Table 68. ALL_INT_SRC register description

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 6.4 ms
SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
D6D_IA	Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0 (0: change in position not detected; 1: change in position detected)
WU_IA	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)
FF_IA	Free-fall event status. Default value: 0 (0: event not detected, 1: event detected)

9.23 WAKE_UP_SRC (1Bh)

Wake-up interrupt source register (R)

Table 69. WAKE_UP_SRC register

0	SLEEP_CHANGE_IA	FF_IA	SLEEP_STATE	WU_IA	X_WU	Y_WU	Z_WU

Table 70. WAKE_UP_SRC register description

SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
FF_IA	Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE	Sleep event status. Default value: 0 (0: sleep event not detected; 1: sleep event detected)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected.)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)

9.24 DRD_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (R)

Table 71. D6D_SRC register

DEN_DRDY	D6D_IA	ZH	ZL	YH	YL	XH	XL

Table 72. D6D_SRC register description

DEN_DRDY	DEN data-ready signal. It is set high when data output is related to the data coming from a DEN active condition. (1)
D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

1. *The DEN data-ready signal can be latched or pulsed depending on the value of the dataready_pulsed bit of the COUNTER_BDR_REG1 (0Bh) register.*

9.25 STATUS_REG (1Eh)

Status register (R)

Table 73. **STATUS_REG register**

0	0	0	0	0	TDA	GDA	XLDA

Table 74. **STATUS_REG register description**

TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

9.26 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two’s complement.

Table 75. **OUT_TEMP_L register**

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 76. **OUT_TEMP_H register**

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8

Table 77. **OUT_TEMP register description**

Temp[15:0]	Temperature sensor output data The value is expressed as two’s complement sign extended on the MSB.

9.27 OUTX_H_G (23h), OUTX_L_G (22h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Table 78. OUTX_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 79. OUTX_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 80. OUTX_H_G, OUTX_L_G register description

D[15:0]	Gyroscope pitch axis output expressed in two's complement

9.28 OUTY_H_G (25h), OUTY_L_G (24h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Table 81. OUTY_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 82. OUTY_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 83. OUTY_H_G, OUTY_L_G register description

D[15:0]	Gyroscope roll axis output expressed in two's complement

9.29 OUTZ_H_G (27h), OUTZ_L_G (26h)

Angular rate sensor pitch yaw (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Table 84. OUTZ_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 85. OUTZ_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 86. OUTZ_H_G, OUTZ_L_G register description

D[15:0]	Gyroscope yaw axis output expressed in two's complement

9.30 OUTX_H_A (29h), OUTX_L_A (28h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Table 87. OUTX_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 88. OUTX_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 89. OUTX_H_A, OUTX_L_A register description

D[15:0]	Accelerometer X-axis output expressed as two's complement

9.31 OUTY_H_A (2Bh), OUTY_L_A (2Ah)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Table 90. OUTY_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 91. OUTY_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 92. OUTY_H_A, OUTY_L_A register description

D[15:0]	Accelerometer Y-axis output expressed as two's complement

9.32 OUTZ_H_A (2Dh), OUTZ_L_A (2Ch)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Table 93. OUTZ_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 94. OUTZ_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 95. OUTZ_H_A, OUTZ_L_A register description

D[15:0]	Accelerometer Z-axis output expressed as two's complement

9.33 STATUS_CONTROLLER_MAINPAGE (39h)

Sensor hub source register (R)

Table 96. STATUS_CONTROLLER_MAINPAGE register

WR_ONCE_DONE	TARGET3_NACK	TARGET2_NACK	TARGET1_NACK	TARGET0_NACK	0	0	SENS_HUB_ENDOP

Table 97. STATUS_CONTROLLER_MAINPAGE register description

WR_ONCE_DONE	When the bit WRITE_ONCE in CONTROLLER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on target 0 has been performed and completed. Default value: 0
TARGET3_NACK	This bit is set to 1 if not acknowledge occurs on target 3 communication. Default value: 0
TARGET2_NACK	This bit is set to 1 if not acknowledge occurs on target 2 communication. Default value: 0
TARGET1_NACK	This bit is set to 1 if not acknowledge occurs on target 1 communication. Default value: 0
TARGET0_NACK	This bit is set to 1 if not acknowledge occurs on target 0 communication. Default value: 0
SENS_HUB_ENDOP	Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded)

9.34 FIFO_STATUS1 (3Ah)

FIFO status register 1 (R)

Table 98. FIFO_STATUS1 register

DIFF_FIFO_7	DIFF_FIFO_6	DIFF_FIFO_5	DIFF_FIFO_4	DIFF_FIFO_3	DIFF_FIFO_2	DIFF_FIFO_1	DIFF_FIFO_0

Table 99. FIFO_STATUS1 register description

DIFF_FIFO_[7:0]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO In conjunction with DIFF_FIFO[9:8] in FIFO_STATUS2 (3Bh).

9.35 FIFO_STATUS2 (3Bh)

FIFO status register 2 (R)

Table 100. FIFO_STATUS2 register

FIFO_ WTM_IA	FIFO_ OVR_IA	FIFO_ FULL_IA	COUNTER_ BDR_IA	FIFO_OVR_ LATCHED	0	DIFF_FIFO_9	DIFF_FIFO_8

Table 101. FIFO_STATUS2 register description

FIFO_WTM_IA	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or greater than WTM) Watermark is set through bits WTM[8:0] in FIFO_CTRL2 (08h) and FIFO_CTRL1 (07h).
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL_IA	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
COUNTER_BDR_IA	Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0 This bit is reset when these registers are read.
FIFO_OVR_LATCHED	Latched FIFO overrun status. Default value: 0 This bit is reset when this register is read.
DIFF_FIFO_[9:8]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00 In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (3Ah)

9.36 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 25 µs.

Table 102. TIMESTAMP3 register

D31	D30	D29	D28	D27	D26	D25	D24

Table 103. TIMESTAMP2 register

D23	D22	D21	D20	D19	D18	D17	D16

Table 104. TIMESTAMP1 register

D15	D14	D13	D12	D11	D10	D9	D8

Table 105. TIMESTAMP0 register

D7	D6	D5	D4	D3	D2	D1	D0

D[31:0]	Timestamp output registers: 1LSB = 25 µs

The formula below can be used to calculate a better estimation of the actual timestamp resolution:
TS_Res = 1 / (40000 + (0.0015 * INTERNAL_FREQ_FINE * 40000))
where INTERNAL_FREQ_FINE is the content of INTERNAL_FREQ_FINE (63h).

9.37 INT_CFG0 (56h)

Activity/inactivity functions, configuration of filtering, and interrupt latch mode configuration (R/W)

Table 106. INT_CFG0 register

0(1)	INT_CLR_ ON_READ	SLEEP_ STATUS_ON _INT	SLOPE_ FDS	0(1)	0(1)	0(1)	LIR

1. *This bit must be set to 0 for the correct operation of the device.*

Table 107. INT_CFG0 register description

INT_CLR_ON_READ	This bit allows immediately clearing the latched interrupts of an event detection upon the read of the corresponding status register. It must be set to 1 together with LIR. Default value: 0 (0: latched interrupt signal cleared at the end of the ODR period; 1: latched interrupt signal immediately cleared)
SLEEP_STATUS_ON_INT	Activity/inactivity interrupt mode configuration. If INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bits are enabled, drives the sleep status or sleep change on INT pins. Default value: 0 (0: sleep change notification on INT pins; 1: sleep status reported on INT pins)
SLOPE_FDS	HPF or slope filter selection on wake-up and activity/inactivity functions. Default value: 0 (0: SLOPE filter applied; 1: HPF applied)
LIR	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

9.38 INT_CFG1 (58h)

Enable interrupt function register (R/W)

Table 108. INT_CFG1 register

INTERRUPTS_ ENABLE	INACT_EN1	INACT_EN0	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 109. INT_CFG1 register description

INTERRUPTS_ENABLE	Enables hardcoded functions
INACT_EN[1:0]	Enables activity/inactivity (sleep) function. Default value: 00 (00: stationary/motion-only interrupts generated, XL and gyro do not change; 01: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro does not change; 10: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to sleep mode; 11: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to power-down mode)

9.39 THS_6D (59h)

Portrait/landscape position register (R/W)

Table 110. THS_6D register

D4D_EN	SIXD_THS1	SIXD_THS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 111. THS_6D register description

D4D_EN	Enables detection of 4D orientation. Z-axis position detection is disabled. Default value: 0 (0: disabled; 1: enabled)
SIXD_THS[1:0]	Threshold for 4D/6D function (00: 80 degrees (default); 01: 70 degrees; 10: 60 degrees; 11: 50 degrees)

9.40 WAKE_UP_THS (5Bh)

Wake-up configuration register (R/W)

Table 112. WAKE_UP_THS register

0(1)	USR_OFF_ON_WU	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 113. WAKE_UP_THS register description

USR_OFF_ON_WU	Sends the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up and the activity/inactivity functions. Default value: 0
WK_THS[5:0]	Threshold for wake-up: 1 LSB weight depends on WAKE_THS_W in WAKE_UP_DUR (5Ch). Default value: 000000

9.41 WAKE_UP_DUR (5Ch)

Free-fall, wake-up and sleep mode functions duration setting register (R/W)

Table 114. WAKE_UP_DUR register

FF_DUR5	WAKE_DUR1	WAKE_DUR0	WAKE_ THS_W	SLEEP_ DUR3	SLEEP_ DUR2	SLEEP_ DUR1	SLEEP_ DUR0

Table 115. WAKE_UP_DUR register description

FF_DUR5	Free-fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in FREE_FALL (5Dh) configuration. 1 LSB = 1 ODR_time
WAKE_DUR[1:0]	Wake-up duration event. Default: 00 1LSB = 1 ODR_time
WAKE_THS_W	Weight of 1 LSB of wake-up threshold. Default: 0 (0: 1 LSB =FS_XL / (2^6); 1: 1 LSB = FS_XL / (2^8))
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512 ODR

9.42 FREE_FALL (5Dh)

Free-fall function duration setting register (R/W)

Table 116. FREE_FALL register

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0

Table 117. FREE_FALL register description

FF_DUR[4:0]	Free-fall duration event. Default: 0 For the complete configuration of the free fall duration, refer to FF_DUR5 in WAKE_UP_DUR (5Ch) configuration
FF_THS[2:0]	Free-fall threshold setting (000: 156 mg (default); 001: 219 mg; 010: 250 mg; 011: 312 mg; 100: 344 mg; 101: 406 mg; 110: 469 mg; 111: 500 mg)

9.43 MD1_CFG (5Eh)

Functions routing to INT1 pin register (R/W)

Table 118. MD1_CFG register

INT1_SLEEP_CHANGE	0(1)	INT1_WU	INT1_FF	0(1)	INT1_6D	0(1)	INT1_SHUB

1. *This bit must be set to 0 for the correct operation of the device.*

Table 119. MD1_CFG register description

INT1_SLEEP_CHANGE(1)	Routing activity/inactivity recognition event to INT1. Default: 0 (0: routing activity/inactivity event to INT1 disabled; 1: routing activity/inactivity event to INT1 enabled)
INT1_WU	Routing wake-up event to INT1. Default value: 0 (0: routing wake-up event to INT1 disabled; 1: routing wake-up event to INT1 enabled)
INT1_FF	Routing free-fall event to INT1. Default value: 0 (0: routing free-fall event to INT1 disabled; 1: routing free-fall event to INT1 enabled)
INT1_6D	Routing 6D event to INT1. Default value: 0 (0: routing 6D event to INT1 disabled; 1: routing 6D event to INT1 enabled)
INT1_SHUB	Routing sensor hub communication concluded event to INT1. Default value: 0 (0: routing sensor hub communication concluded event to INT1 disabled; 1: routing sensor hub communication concluded event to INT1 enabled)

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INT_CFG0 (56h) register.*

9.44 MD2_CFG (5Fh)

Functions routing to INT2 pin register (R/W)

Table 120. MD2_CFG register

INT2_SLEEP_CHANGE	0(1)	INT2_WU	INT2_FF	0(1)	INT2_6D	0(1)	INT2_TIMESTAMP

1. *This bit must be set to 0 for the correct operation of the device.*

Table 121. MD2_CFG register description

INT2_SLEEP_CHANGE(1)	Routing activity/inactivity recognition event to INT2. Default: 0 (0: routing activity/inactivity event to INT2 disabled; 1: routing activity/inactivity event to INT2 enabled)
INT2_WU	Routing wake-up event to INT2. Default value: 0 (0: routing wake-up event to INT2 disabled; 1: routing wake-up event to INT2 enabled)
INT2_FF	Routing free-fall event to INT2. Default value: 0 (0: routing free-fall event to INT2 disabled; 1: routing free-fall event to INT2 enabled)
INT2_6D	Routing 6D event to INT2. Default value: 0 (0: routing 6D event to INT2 disabled; 1: routing 6D event to INT2 enabled)
INT2_TIMESTAMP	Enables routing the alert for timestamp overflow within 6.4 ms to the INT2 pin.

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the INT_CFG0 (56h) register.*

9.45 I3C_BUS_AVB (62h)

I3C_BUS_AVB register (R/W)

Table 122. I3C_BUS_AVB register

0(1)	0(1)	0(1)	I3C_Bus_ Avb_Sel1	I3C_Bus_ Avb_Sel0	0(1)	0(1)	PD_DIS_ INT1

1. *This bit must be set to 0 for the correct operation of the device.*

Table 123. I3C_BUS_AVB register description

I3C_Bus_Avb_Sel[1:0]	These bits are used to select the bus available time when I3C IBI is used. Default value: 00 (00: bus available time equal to 50 µs (default); 01: bus available time equal to 2 µs; 10: bus available time equal to 1 ms; 11: bus available time equal to 25 ms)
PD_DIS_INT1	This bit allows disabling the INT1 pull-down. (0: pull-down on INT1 enabled (pull-down is effectively connected only when no interrupts are routed to the INT1 pin or when the I3C dynamic address is assigned); 1: pull-down on INT1 disabled (pull-down not connected))

Note: The IBI (in-band interrupt) is continuously generated (each time a bus available condition is satisfied) until an interrupt is served. The controller should execute the interrupt service routine (ISR) at a time lower than the configured bus available time, otherwise the controller should disable the interrupt (I3C DISEC in order to disable the interrupt request) at a time lower than the bus available time.

If the controller needs more time to analyze and start the correct ISR, then the controller can change the bus available time from 50 µs (default) to a higher time.

9.46 INTERNAL_FREQ_FINE (63h)

Internal frequency register (R)

Table 124. INTERNAL_FREQ_FINE register

FREQ_FINE7	FREQ_FINE6	FREQ_FINE5	FREQ_FINE4	FREQ_FINE3	FREQ_FINE2	FREQ_FINE1	FREQ_FINE0

Table 125. INTERNAL_FREQ_FINE register description

FREQ_FINE[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, two's complement.

The formula below can be used to calculate a better estimation of the actual ODR:
ODR_Actual = (6667 + ((0.0015 * INTERNAL_FREQ_FINE) * 6667)) / ODR_Coeff

Selected_ODR	ODR_Coeff
12.5	512
26	256
52	128
104	64
208	32
416	16
833	8
1667	4
3333	2
6667	1

The Selected_ODR parameter has to be derived from the ODR_XL selection (Table 43. CTRL1_XL register description) in order to estimate the accelerometer ODR and from the ODR_G selection (Table 46. CTRL2_G register description) in order to estimate the gyroscope ODR.

9.47 X_OFS_USR (73h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X_OFS_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

Table 126. X_OFS_USR register

X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0

Table 127. X_OFS_USR register description

X_OFS_USR_[7:0]	Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127 127].

9.48 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y_OFS_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

Table 128. Y_OFS_USR register

Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0

Y_OFS_USR_[7:0]	Accelerometer Y-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].

9.49 Z_OFS_USR (75h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z_OFS_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

Table 129. Z_OFS_USR register

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0

Table 130. Z_OFS_USR register description

Z_OFS_USR_[7:0]	Accelerometer Z-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].

9.50 FIFO_DATA_OUT_TAG (78h)

FIFO tag register (R)

Table 131. FIFO_DATA_OUT_TAG register

TAG_ SENSOR_4	TAG_ SENSOR_3	TAG_ SENSOR_2	TAG_ SENSOR_1	TAG_ SENSOR_0	TAG_CNT_1	TAG_CNT_0	TAG_ PARITY

Table 132. FIFO_DATA_OUT_TAG register description

TAG_SENSOR_[4:0]	Identifies the sensor in: FIFO_DATA_OUT_X_H (7Ah) and FIFO_DATA_OUT_X_L (79h), FIFO_DATA_OUT_Y_H (7Ch) and FIFO_DATA_OUT_Y_L (7Bh), and FIFO_DATA_OUT_Z_H (7Eh) and FIFO_DATA_OUT_Z_L (7Dh)
TAG_CNT_[1:0]	2-bit counter which identifies sensor time slot
TAG_PARITY	Parity check of TAG content

Table 133. FIFO tag

TAG_SENSOR_[4:0]	Sensor name
0x01	Gyroscope
0x02	Accelerometer
0x03	Temperature
0x04	Timestamp
0x05	CFG_Change
0x0E	Sensor hub target 0
0x0F	Sensor hub target 1
0x10	Sensor hub target 2
0x11	Sensor hub target 3
0x19	Sensor hub nack

9.51 FIFO_DATA_OUT_X_H (7Ah) and FIFO_DATA_OUT_X_L (79h)

FIFO data output X (R)

Table 134. FIFO_DATA_OUT_X_H register

D15	D14	D13	D12	D11	D10	D9	D8

Table 135. FIFO_DATA_OUT_X_L register

D7	D6	D5	D4	D3	D2	D1	D0

Table 136. FIFO_DATA_OUT_X_H, FIFO_DATA_OUT_X_L register description

D[15:0]	FIFO X-axis output

9.52 FIFO_DATA_OUT_Y_H (7Ch) and FIFO_DATA_OUT_Y_L (7Bh)

FIFO data output Y (R)

Table 137. FIFO_DATA_OUT_Y_H register

D15	D14	D13	D12	D11	D10	D9	D8

Table 138. FIFO_DATA_OUT_Y_L register

D7	D6	D5	D4	D3	D2	D1	D0

Table 139. FIFO_DATA_OUT_Y_H, FIFO_DATA_OUT_Y_L register description

D[15:0]	FIFO Y-axis output

9.53 FIFO_DATA_OUT_Z_H (7Eh) and FIFO_DATA_OUT_Z_L (7Dh)

FIFO data output Z (R)

Table 140. FIFO_DATA_OUT_Z_H register

D15	D14	D13	D12	D11	D10	D9	D8

Table 141. FIFO_DATA_OUT_Z_L register

D7	D6	D5	D4	D3	D2	D1	D0

Table 142. FIFO_DATA_OUT_Z_H, FIFO_DATA_OUT_Z_L register description

D[15:0]	FIFO Z-axis output

10 Sensor hub register mapping

The table given below provides a list of the registers for the sensor hub functions available in the device and the corresponding addresses. The sensor hub registers are accessible when bit SHUB_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

Table 143. Registers address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
SENSOR_HUB_1	R	02	00000010	output	
SENSOR_HUB_2	R	03	00000011	output	
SENSOR_HUB_3	R	04	00000100	output	
SENSOR_HUB_4	R	05	00000101	output	
SENSOR_HUB_5	R	06	00000110	output	
SENSOR_HUB_6	R	07	00000111	output	
SENSOR_HUB_7	R	08	00001000	output	
SENSOR_HUB_8	R	09	00001001	output	
SENSOR_HUB_9	R	0A	00001010	output	
SENSOR_HUB_10	R	0B	00001011	output	
SENSOR_HUB_11	R	0C	00001100	output	
SENSOR_HUB_12	R	0D	00001101	output	
SENSOR_HUB_13	R	0E	00001110	output	
SENSOR_HUB_14	R	0F	00001111	output	
SENSOR_HUB_15	R	10	00010000	output	
SENSOR_HUB_16	R	11	00010001	output	
SENSOR_HUB_17	R	12	00010010	output	
SENSOR_HUB_18	R	13	00010011	output	
CONTROLLER_CONFIG	R/W	14	00010100	00000000	
TGT0_ADD	R/W	15	00010101	00000000	
TGT0_SUBADD	R/W	16	00010110	00000000	
TGT0_CONFIG	R/W	17	00010111	00000000	
TGT1_ADD	R/W	18	00011000	00000000	
TGT1_SUBADD	R/W	19	00011001	00000000	
TGT1_CONFIG	R/W	1A	00011010	00000000	
TGT2_ADD	R/W	1B	00011011	00000000	
TGT2_SUBADD	R/W	1C	00011100	00000000	
TGT2_CONFIG	R/W	1D	00011101	00000000	
TGT3_ADD	R/W	1E	00011110	00000000	
TGT3_SUBADD	R/W	1F	00011111	00000000	
TGT3_CONFIG	R/W	20	00100000	00000000	
DATAWRITE_TGT0	R/W	21	00100001	00000000	
STATUS_CONTROLLER	R	22	00100010	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

11 Sensor hub register description

11.1 SENSOR_HUB_1 (02h)

Sensor hub output register (R)

First byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 144. SENSOR_HUB_1 register

Sensor Hub1_7	Sensor Hub1_6	Sensor Hub1_5	Sensor Hub1_4	Sensor Hub1_3	Sensor Hub1_2	Sensor Hub1_1	Sensor Hub1_0

Table 145. SENSOR_HUB_1 register description

SensorHub1_[7:0]	First byte associated to external sensors

11.2 SENSOR_HUB_2 (03h)

Sensor hub output register (R)

Second byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 146. SENSOR_HUB_2 register

Sensor Hub2_7	Sensor Hub2_6	Sensor Hub2_5	Sensor Hub2_4	Sensor Hub2_3	Sensor Hub2_2	Sensor Hub2_1	Sensor Hub2_0

Table 147. SENSOR_HUB_2 register description

SensorHub2_[7:0]	Second byte associated to external sensors

11.3 SENSOR_HUB_3 (04h)

Sensor hub output register (R)

Third byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 148. SENSOR_HUB_3 register

Sensor Hub3_7	Sensor Hub3_6	Sensor Hub3_5	Sensor Hub3_4	Sensor Hub3_3	Sensor Hub3_2	Sensor Hub3_1	Sensor Hub3_0

Table 149. SENSOR_HUB_3 register description

SensorHub3_[7:0]	Third byte associated to external sensors

11.4 SENSOR_HUB_4 (05h)

Sensor hub output register (R)

Fourth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 150. SENSOR_HUB_4 register

Sensor Hub4_7	Sensor Hub4_6	Sensor Hub4_5	Sensor Hub4_4	Sensor Hub4_3	Sensor Hub4_2	Sensor Hub4_1	Sensor Hub4_0

Table 151. SENSOR_HUB_4 register description

SensorHub4_[7:0]	Fourth byte associated to external sensors

11.5 SENSOR_HUB_5 (06h)

Sensor hub output register (R)

Fifth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 152. SENSOR_HUB_5 register

Sensor Hub5_7	Sensor Hub5_6	Sensor Hub5_5	Sensor Hub5_4	Sensor Hub5_3	Sensor Hub5_2	Sensor Hub5_1	Sensor Hub5_0

Table 153. SENSOR_HUB_5 register description

SensorHub5_[7:0]	Fifth byte associated to external sensors

11.6 SENSOR_HUB_6 (07h)

Sensor hub output register (R)

Sixth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 154. SENSOR_HUB_6 register

Sensor Hub6_7	Sensor Hub6_6	Sensor Hub6_5	Sensor Hub6_4	Sensor Hub6_3	Sensor Hub6_2	Sensor Hub6_1	Sensor Hub6_0

Table 155. SENSOR_HUB_6 register description

SensorHub6_[7:0]	Sixth byte associated to external sensors

11.7 SENSOR_HUB_7 (08h)

Sensor hub output register (R)

Seventh byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 156. SENSOR_HUB_7 register

Sensor Hub7_7	Sensor Hub7_6	Sensor Hub7_5	Sensor Hub7_4	Sensor Hub7_3	Sensor Hub7_2	Sensor Hub7_1	Sensor Hub7_0

Table 157. SENSOR_HUB_7 register description

SensorHub7_[7:0]	Seventh byte associated to external sensors

11.8 SENSOR_HUB_8 (09h)

Sensor hub output register (R)

Eighth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 158. SENSOR_HUB_8 register

Sensor Hub8_7	Sensor Hub8_6	Sensor Hub8_5	Sensor Hub8_4	Sensor Hub8_3	Sensor Hub8_2	Sensor Hub8_1	Sensor Hub8_0

Table 159. SENSOR_HUB_8 register description

SensorHub8_[7:0]	Eighth byte associated to external sensors

11.9 SENSOR_HUB_9 (0Ah)

Sensor hub output register (R)

Ninth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 160. SENSOR_HUB_9 register

Sensor Hub9_7	Sensor Hub9_6	Sensor Hub9_5	Sensor Hub9_4	Sensor Hub9_3	Sensor Hub9_2	Sensor Hub9_1	Sensor Hub9_0

Table 161. SENSOR_HUB_9 register description

SensorHub9_[7:0]	Ninth byte associated to external sensors

11.10 SENSOR_HUB_10 (0Bh)

Sensor hub output register (R)

Tenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 162. SENSOR_HUB_10 register

Sensor Hub10_7	Sensor Hub10_6	Sensor Hub10_5	Sensor Hub10_4	Sensor Hub10_3	Sensor Hub10_2	Sensor Hub10_1	Sensor Hub10_0

Table 163. SENSOR_HUB_10 register description

SensorHub10_[7:0]	Tenth byte associated to external sensors

11.11 SENSOR_HUB_11 (0Ch)

Sensor hub output register (R)

Eleventh byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 164. SENSOR_HUB_11 register

Sensor Hub11_7	Sensor Hub11_6	Sensor Hub11_5	Sensor Hub11_4	Sensor Hub11_3	Sensor Hub11_2	Sensor Hub11_1	Sensor Hub11_0

Table 165. SENSOR_HUB_11 register description

SensorHub11_[7:0]	Eleventh byte associated to external sensors

11.12 SENSOR_HUB_12 (0Dh)

Sensor hub output register (R)

Twelfth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 166. SENSOR_HUB_12 register

Sensor Hub12_7	Sensor Hub12_6	Sensor Hub12_5	Sensor Hub12_4	Sensor Hub12_3	Sensor Hub12_2	Sensor Hub12_1	Sensor Hub12_0

Table 167. SENSOR_HUB_12 register description

SensorHub12_[7:0]	Twelfth byte associated to external sensors

11.13 SENSOR_HUB_13 (0Eh)

Sensor hub output register (R)

Thirteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 168. SENSOR_HUB_13 register

Sensor Hub13_7	Sensor Hub13_6	Sensor Hub13_5	Sensor Hub13_4	Sensor Hub13_3	Sensor Hub13_2	Sensor Hub13_1	Sensor Hub13_0

Table 169. SENSOR_HUB_13 register description

SensorHub13_[7:0]	Thirteenth byte associated to external sensors

11.14 SENSOR_HUB_14 (0Fh)

Sensor hub output register (R)

Fourteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 170. SENSOR_HUB_14 register

Sensor Hub14_7	Sensor Hub14_6	Sensor Hub14_5	Sensor Hub14_4	Sensor Hub14_3	Sensor Hub14_2	Sensor Hub14_1	Sensor Hub14_0

Table 171. SENSOR_HUB_14 register description

SensorHub14_[7:0]	Fourteenth byte associated to external sensors

11.15 SENSOR_HUB_15 (10h)

Sensor hub output register (R)

Fifteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 172. SENSOR_HUB_15 register

Sensor Hub15_7	Sensor Hub15_6	Sensor Hub15_5	Sensor Hub15_4	Sensor Hub15_3	Sensor Hub15_2	Sensor Hub15_1	Sensor Hub15_0

Table 173. SENSOR_HUB_15 register description

SensorHub15_[7:0]	Fifteenth byte associated to external sensors

11.16 SENSOR_HUB_16 (11h)

Sensor hub output register (R)

Sixteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 174. SENSOR_HUB_16 register

Sensor Hub16_7	Sensor Hub16_6	Sensor Hub16_5	Sensor Hub16_4	Sensor Hub16_3	Sensor Hub16_2	Sensor Hub16_1	Sensor Hub16_0

Table 175. SENSOR_HUB_16 register description

SensorHub16_[7:0]	Sixteenth byte associated to external sensors

11.17 SENSOR_HUB_17 (12h)

Sensor hub output register (R)

Seventeenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 176. SENSOR_HUB_17 register

Sensor Hub17_7	Sensor Hub17_6	Sensor Hub17_5	Sensor Hub17_4	Sensor Hub17_3	Sensor Hub17_2	Sensor Hub17_1	Sensor Hub17_0

Table 177. SENSOR_HUB_17 register description

SensorHub17_[7:0]	Seventeenth byte associated to external sensors

11.18 SENSOR_HUB_18 (13h)

Sensor hub output register (R)

Eighteenth byte associated to external sensors. The content of the register is consistent with the TGTx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 178. SENSOR_HUB_18 register

Sensor Hub18_7	Sensor Hub18_6	Sensor Hub18_5	Sensor Hub18_4	Sensor Hub18_3	Sensor Hub18_2	Sensor Hub18_1	Sensor Hub18_0

Table 179. SENSOR_HUB_18 register description

SensorHub18_[7:0]	Eighteenth byte associated to external sensors

11.19 CONTROLLER_CONFIG (14h)

Controller configuration register (R/W)

Table 180. CONTROLLER_CONFIG register

RST_CONTROLLER_REGS	WRITE_ONCE	START_CONFIG	PASS_THROUGH_MODE	SHUB_PU_EN	CONTROLLER_ON	AUX_SENS_ON1	AUX_SENS_ON0

Table 181. CONTROLLER_CONFIG register description

RST_CONTROLLER_REGS	Reset controller logic and output registers. Must be set to 1 and then set it to 0. Default value: 0
WRITE_ONCE	Target 0 write operation is performed only at the first sensor hub cycle. Default value: 0 (0: write operation for each sensor hub cycle; 1: write operation only for the first sensor hub cycle)
START_CONFIG	Sensor hub trigger signal selection. Default value: 0 (0: sensor hub trigger signal is the accelerometer/gyro data-ready; 1: sensor hub trigger signal external from INT2 pin)
PASS_THROUGH_MODE	I²C interface pass-through. Default value: 0 (0: pass-through disabled; 1: pass-through enabled, main I²C line is short-circuited with the auxiliary line)
SHUB_PU_EN	Enables I²C controller pull-up. Default value: 0 (0: internal pull-up on auxiliary I²C line disabled; 1: internal pull-up on auxiliary I²C line enabled)
CONTROLLER_ON	Enables sensor hub I²C controller. Default: 0 (0: I²C controller of sensor hub disabled; 1: I²C controller of sensor hub enabled)
AUX_SENS_ON[1:0]	Number of external sensors to be read by the sensor hub. (00: one sensor (default); 01: two sensors; 10: three sensors; 11: four sensors)

11.20 TGT0_ADD (15h)

I²C target address of the first external sensor (sensor 1) register (R/W)

Table 182. TGT0_ADD register

target0_ add6	target0_ add5	target0_ add4	target0_ add3	target0_ add2	target0_ add1	target0_ add0	rw_0

Table 183. TGT0_ADD register description

target0_add[6:0]	I²C target address of sensor 1 that can be read by the sensor hub. Default value: 0000000
rw_0	Read/write operation on sensor 1. Default value: 0 (0: write operation; 1: read operation)

11.21 TGT0_SUBADD (16h)

Address of register on the first external sensor (sensor 1) register (R/W)

Table 184. TGT0_SUBADD register

target0_ reg7	target0_ reg6	target0_ reg5	target0_ reg4	target0_ reg3	target0_ reg2	target0_ reg1	target0_ reg0

Table 185. TGT0_SUBADD register description

target0_reg[7:0]	Address of register on sensor 1 that has to be read/written according to the rw_0 bit value in TGT0_ADD (15h). Default value: 00000000

11.22 TGT0_CONFIG (17h)

First external sensor (sensor 1) configuration and sensor hub settings register (R/W)

Table 186. TGT0_CONFIG register

SHUB_ ODR_1	SHUB_ ODR_0	0(1)	0(1)	BATCH_EXT_ SENS_0_EN	Target0_ numop2	Target0_ numop1	Target0_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 187. TGT0_CONFIG register description

SHUB_ODR_[1:0]	Rate at which the controller communicates. Default value: 00 (00: 104 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 104 Hz); 01: 52 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 52 Hz); 10: 26 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 26 Hz); 11: 12.5 Hz (or at the maximum ODR between the accelerometer and gyroscope if it is less than 12.5 Hz)
BATCH_EXT_SENS_0_EN	Enables FIFO data batching of first target. Default value: 0
Target0_numop[2:0]	Number of read operations on sensor 1. Default value: 000

11.23 TGT1_ADD (18h)

I²C target address of the second external sensor (sensor 2) register (R/W)

Table 188. TGT1_ADD register

Target1_ add6	Target1_ add5	Target1_ add4	Target1_ add3	Target1_ add2	Target1_ add1	Target1_ add0	r_1

Table 189. TGT1_ADD register description

Target1_add[6:0]	I²C target address of sensor 2 that can be read by the sensor hub. Default value: 0000000
r_1	Enables read operation on sensor 2. Default value: 0 (0: read operation disabled; 1: read operation enabled)

11.24 TGT1_SUBADD (19h)

Address of register on the second external sensor (sensor 2) register (R/W)

Table 190. TGT1_SUBADD register

Target1_ reg7	Target1_ reg6	Target1_ reg5	Target1_ reg4	Target1_ reg3	Target1_ reg2	Target1_ reg1	Target1_ reg0

Table 191. TGT1_SUBADD register description

Target1_reg[7:0]	Address of register on sensor 2 that has to be read/written according to the r_1 bit value in TGT1_ADD (18h).

11.25 TGT1_CONFIG (1Ah)

Second external sensor (sensor 2) configuration register (R/W)

Table 192. TGT1_CONFIG register

0(1)	0(1)	0(1)	0(1)	BATCH_EXT_ SENS_1_EN	Target1_ numop2	Target1_ numop1	Target1_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 193. TGT1_CONFIG register description

BATCH_EXT_SENS_1_EN	Enables FIFO data batching of second target. Default value: 0
Target1_numop[2:0]	Number of read operations on sensor 2. Default value: 000

11.26 TGT2_ADD (1Bh)

I²C target address of the third external sensor (sensor 3) register (R/W)

Table 194. TGT2_ADD register

Target2_ add6	Target2_ add5	Target2_ add4	Target2_ add3	Target2_ add2	Target2_ add1	Target2_ add0	r_2

Table 195. TGT2_ADD register description

Target2_add[6:0]	I²C target address of sensor 3 that can be read by the sensor hub.
r_2	Enables read operation on sensor 3. Default value: 0 (0: read operation disabled; 1: read operation enabled)

11.27 TGT2_SUBADD (1Ch)

Address of register on the third external sensor (sensor 3) register (R/W)

Table 196. TGT2_SUBADD register

Target2_ reg7	Target2_ reg6	Target2_ reg5	Target2_ reg4	Target2_ reg3	Target2_ reg2	Target2_ reg1	Target2_ reg0

Table 197. TGT2_SUBADD register description

Target2_reg[7:0]	Address of register on sensor 3 that has to be read/written according to the r_2 bit value in TGT2_ADD (1Bh).

11.28 TGT2_CONFIG (1Dh)

Third external sensor (sensor 3) configuration register (R/W)

Table 198. TGT2_CONFIG register

0(1)	0(1)	0(1)	0(1)	BATCH_EXT_ SENS_2_EN	Target2_ numop2	Target2_ numop1	Target2_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 199. TGT2_CONFIG register description

BATCH_EXT_SENS_2_EN	Enables FIFO data batching of third target. Default value: 0
Target2_numop[2:0]	Number of read operations on sensor 3. Default value: 000

11.29 TGT3_ADD (1Eh)

I²C target address of the fourth external sensor (sensor 4) register (R/W)

Table 200. TGT3_ADD register

Target3_ add6	Target3_ add5	Target3_ add4	Target3_ add3	Target3_ add2	Target3_ add1	Target3_ add0	r_3

Table 201. TGT3_ADD register description

Target3_add[6:0]	I²C target address of sensor 4 that can be read by the sensor hub.
r_3	Enables read operation on sensor 4. Default value: 0 (0: read operation disabled; 1: read operation enabled)

11.30 TGT3_SUBADD (1Fh)

Address of register on the fourth external sensor (sensor 4) register (R/W)

Table 202. TGT3_SUBADD register

Target3_ reg7	Target3_ reg6	Target3_ reg5	Target3_ reg4	Target3_ reg3	Target3_ reg2	Target3_ reg1	Target3_ reg0

Table 203. TGT3_SUBADD register description

Target3_reg[7:0]	Address of register on sensor 4 that has to be read according to the r_3 bit value in TGT3_ADD (1Eh).

11.31 TGT3_CONFIG (20h)

Fourth external sensor (sensor 4) configuration register (R/W)

Table 204. TGT3_CONFIG register

0(1)	0(1)	0(1)	0(1)	BATCH_EXT_ SENS_3_EN	Target3_ numop2	Target3_ numop1	Target3_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 205. TGT3_CONFIG register description

BATCH_EXT_SENS_3_EN	Enables FIFO data batching of fourth target. Default value: 0
Target3_numop[2:0]	Number of read operations on sensor 4. Default value: 000

11.32 DATAWRITE_TGT0 (21h)

Data to be written into the target device register (R/W)

Table 206. DATAWRITE_TGT0 register

Target0_ dataw7	Target0_ dataw6	Target0_ dataw5	Target0_ dataw4	Target0_ dataw3	Target0_ dataw2	Target0_ dataw1	Target0_ dataw0

Table 207. DATAWRITE_TGT0 register description

Target0_dataw[7:0]	Data to be written into the target 0 device according to the rw_0 bit in register TGT0_ADD (15h). Default value: 00000000

11.33 STATUS_CONTROLLER (22h)

Sensor hub source register (R)

Table 208. STATUS_CONTROLLER register

WR_ONCE _DONE	TARGET3_ NACK	TARGET2_ NACK	TARGET1_ NACK	TARGET0_ NACK	0	0	SENS_HUB _ENDOP

Table 209. STATUS_CONTROLLER register description

WR_ONCE_DONE	When the bit WRITE_ONCE in CONTROLLER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on target 0 has been performed and completed. Default value: 0
TARGET3_NACK	This bit is set to 1 if not acknowledge occurs on target 3 communication. Default value: 0
TARGET2_NACK	This bit is set to 1 if not acknowledge occurs on target 2 communication. Default value: 0
TARGET1_NACK	This bit is set to 1 if not acknowledge occurs on target 1 communication. Default value: 0
TARGET0_NACK	This bit is set to 1 if not acknowledge occurs on target 0 communication. Default value: 0
SENS_HUB_ENDOP	Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded)

12 Soldering information

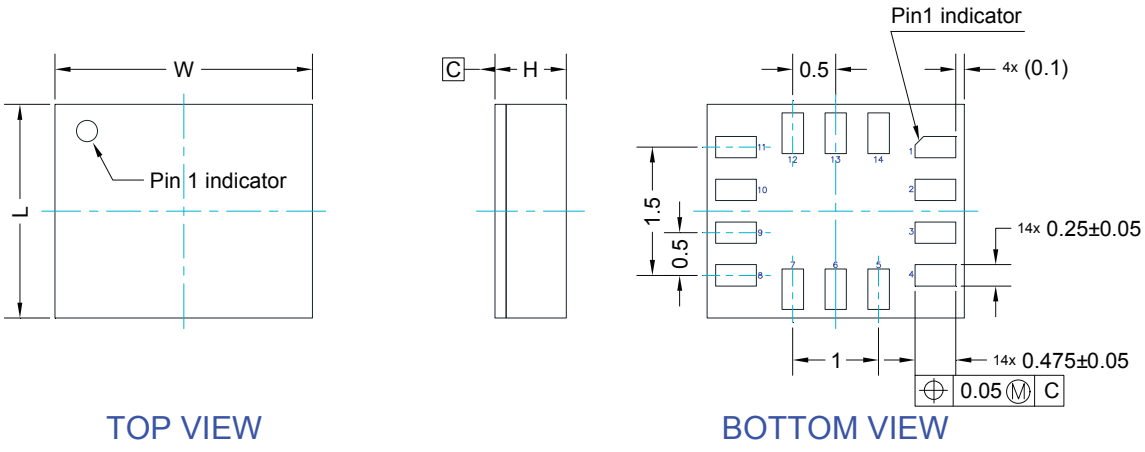
The LGA package is compliant with the ECOPACK and RoHS standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.
For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

13 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

13.1 LGA-14L package information

Figure 20. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

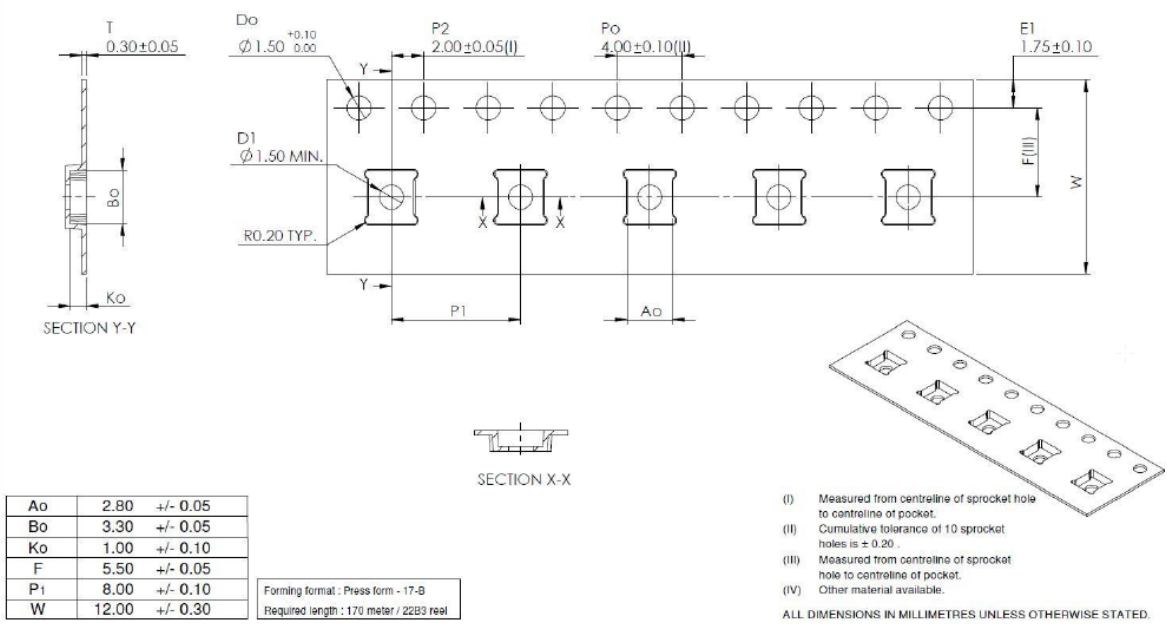
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	3.00	±0.1
Height [H]	0.86	MAX

DM00249496_5

13.2 LGA-14L packing information

Figure 21. **Carrier tape information for LGA-14L package**



Ao	2.80	+/- 0.05
Bo	3.30	+/- 0.05
Ko	1.00	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press form - 17-B
Required length : 170 meter / 22B3 reel

Figure 22. **LGA-14L package orientation in carrier tape**

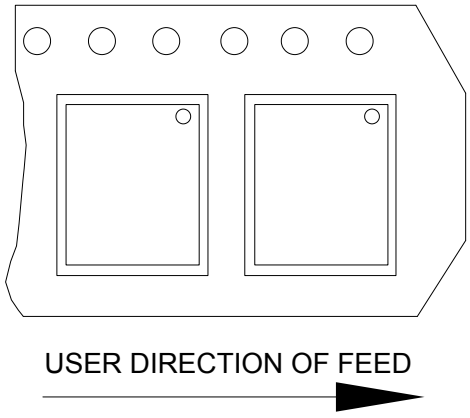


Figure 23. **Reel information for carrier tape of LGA-14L package**

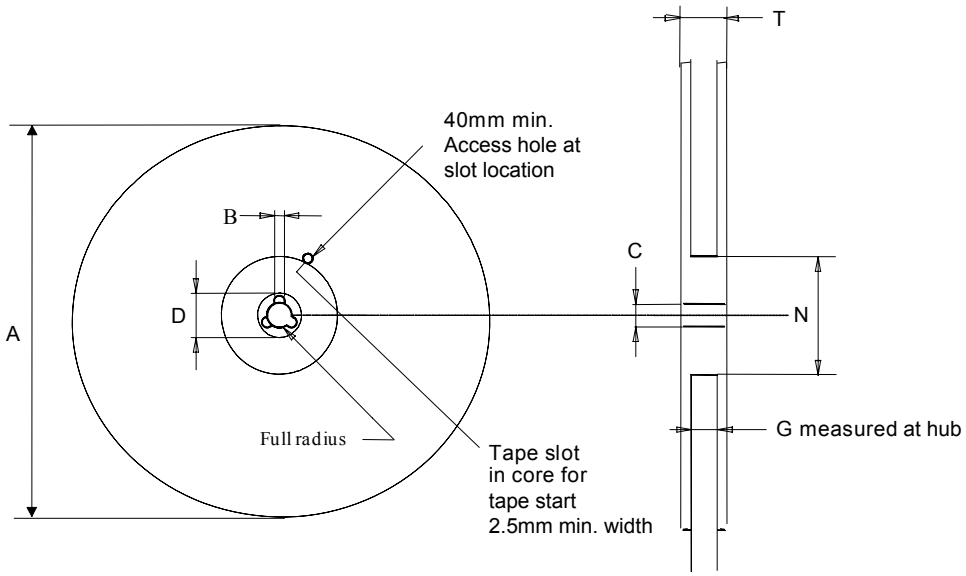


Table 210. **Reel dimensions for carrier tape of LGA-14L package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

Revision history

Table 211. **Document revision history**

Date	Version	Changes
12-Jan-2026	2	First public release

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