

ON Semiconductor

Is Now



To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that onsemi was negligent regarding the design or manufacture of the part. onsemi is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

NDD60N900U1

N-Channel Power MOSFET 600 V, 900 mΩ

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|--|--------------|------------------------|-----------------------------------|-------------|------|
| Drain-to-Source Voltage | | | V _{DSS} | 600 | V |
| Gate-to-Source Voltage | | | V _{GS} | ±25 | V |
| Continuous Drain Current R _{θJC} | Steady State | T _C = 25°C | I _D | 5.7 | A |
| | | T _C = 100°C | | 3.6 | |
| Power Dissipation – R _{θJC} | Steady State | T _C = 25°C | P _D | 74 | W |
| Pulsed Drain Current | | t _p = 10 µs | I _{DM} | 20 | A |
| Operating Junction and Storage Temperature | | | T _J , T _{STG} | -55 to +150 | °C |
| Source Current (Body Diode) | | | I _S | 5.7 | A |
| Single Pulse Drain-to-Source Avalanche Energy (I _D = 2 A) | | | EAS | 33 | mJ |
| Peak Diode Recovery (Note 1) | | | dv/dt | 15 | V/ns |
| Lead Temperature for Soldering Leads | | | T _L | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{SD} < 5.7 A, di/dt ≤ 400 A/µs, V_{peak} < V_{(BR)DSS}

THERMAL RESISTANCE

| Parameter | | Symbol | Value | Unit |
|---|----------------|------------------|-------|------|
| Junction-to-Case (Drain) | NDD60N900U1 | R _{θJC} | 1.7 | °C/W |
| Junction-to-Ambient Steady State (Note 3) | NDD60N900U1 | R _{θJA} | 47 | °C/W |
| (Note 2) | NDD60N900U1-1 | | 99 | |
| (Note 2) | NDD60N900U1-35 | | 95 | |

2. Insertion mounted

3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

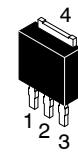
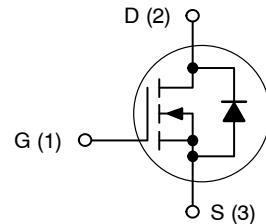


ON Semiconductor®

<http://onsemi.com>

| V _{(BR)DSS} | R _{DS(ON) MAX} |
|----------------------|-------------------------|
| 600 V | 900 mΩ @ 10 V |

N-Channel MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NDD60N900U1

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------|--------|-----------------|-----|-----|-----|------|
|----------------|--------|-----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|---------------------------------|--|---------------------------|-----|-----------|----------------------------|
| Drain-to-Source Breakdown Voltage | $V_{(\text{BR})\text{DSS}}$ | $V_{\text{GS}} = 0 \text{ V}, I_D = 1 \text{ mA}$ | 600 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(\text{BR})\text{DSS}}/T_J$ | | | 550 | | $\text{mV}/^\circ\text{C}$ |
| Drain-to-Source Leakage Current | I_{DSS} | $V_{\text{DS}} = 600 \text{ V}, V_{\text{GS}} = 0 \text{ V}$ | $T_J = 25^\circ\text{C}$ | | 1 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 100 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{\text{GS}} = \pm 20 \text{ V}$ | | | ± 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|--|--------------------------------|---|---|-----|-----|----------------------------|
| Gate Threshold Voltage | $V_{\text{GS}(\text{TH})}$ | $V_{\text{DS}} = V_{\text{GS}}, I_D = 250 \mu\text{A}$ | 2 | 3.2 | 4 | V |
| Negative Threshold Temperature Coefficient | $V_{\text{GS}(\text{TH})}/T_J$ | Reference to 25°C , $I_D = 250 \mu\text{A}$ | | 7.2 | | $\text{mV}/^\circ\text{C}$ |
| Static Drain-to-Source On Resistance | $R_{\text{DS}(\text{on})}$ | $V_{\text{GS}} = 10 \text{ V}, I_D = 2.5 \text{ A}$ | | 820 | 900 | $\text{m}\Omega$ |
| Forward Transconductance | g_{FS} | $V_{\text{DS}} = 15 \text{ V}, I_D = 2.5 \text{ A}$ | | 4.3 | | S |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|---|--------------------|---|--|-----|--|----------|
| Input Capacitance | C_{iss} | $V_{\text{DS}} = 50 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}$ | | 360 | | pF |
| Output Capacitance | C_{oss} | | | 23 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 1.1 | | |
| Effective output capacitance, energy related (Note 6) | $C_{\text{o(er)}}$ | $V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 0 \text{ to } 480 \text{ V}$ | | 17 | | |
| Effective output capacitance, time related (Note 7) | $C_{\text{o(tr)}}$ | $I_D = \text{constant}, V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 0 \text{ to } 480 \text{ V}$ | | 57 | | |
| Total Gate Charge | Q_g | $V_{\text{DS}} = 300 \text{ V}, I_D = 5.9 \text{ A}, V_{\text{GS}} = 10 \text{ V}$ | | 12 | | nC |
| Gate-to-Source Charge | Q_{gs} | | | 2.5 | | |
| Gate-to-Drain ("Miller") Charge | Q_{gd} | | | 5.8 | | |
| Plateau Voltage | V_{GP} | | | 5.4 | | V |
| Gate Resistance | R_g | | | 5 | | Ω |

RESISTIVE SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|----------------------------|---|--|----|--|----|
| Turn-on Delay Time | $t_{\text{d}(\text{on})}$ | $V_{\text{DD}} = 300 \text{ V}, I_D = 5.9 \text{ A}, V_{\text{GS}} = 10 \text{ V}, R_{\text{G}} = 0 \Omega$ | | 7 | | ns |
| Rise Time | t_r | | | 9 | | |
| Turn-off Delay Time | $t_{\text{d}(\text{off})}$ | | | 17 | | |
| Fall Time | t_f | | | 6 | | |

SOURCE-DRAIN DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|-----------------|---|---------------------------|--|------|-----|---------------|
| Diode Forward Voltage | V_{SD} | $I_S = 5.7 \text{ A}, V_{\text{GS}} = 0 \text{ V}$ | $T_J = 25^\circ\text{C}$ | | 0.88 | 1.3 | V |
| | | | $T_J = 100^\circ\text{C}$ | | 0.80 | | |
| Reverse Recovery Time | t_{rr} | $V_{\text{GS}} = 0 \text{ V}, V_{\text{DD}} = 30 \text{ V}$ $I_S = 5.9 \text{ A}, d_i/d_t = 100 \text{ A}/\mu\text{s}$ | | | 270 | | ns |
| Charge Time | t_a | | | | 130 | | |
| Discharge Time | t_b | | | | 140 | | |
| Reverse Recovery Charge | Q_{rr} | | | | 1.8 | | μC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

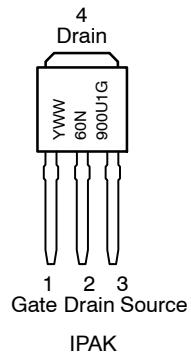
5. Switching characteristics are independent of operating junction temperatures.

6. $C_{\text{o(er)}}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(\text{BR})\text{DSS}}$

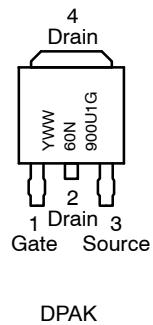
7. $C_{\text{o(tr)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(\text{BR})\text{DSS}}$

NDD60N900U1

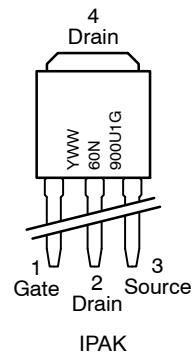
MARKING DIAGRAMS



IPAK



DPAK



IPAK

Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-----------------|---------------------------------|-----------------------|
| NDD60N900U1-1G | IPAK (Pb-Free, Halogen-Free) | 75 Units / Rail |
| NDD60N900U1-35G | IPAK (Pb-Free, Halogen-Free) | 75 Units / Rail |
| NDD60N900U1T4G | DPAK (Pb-Free, Halogen-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

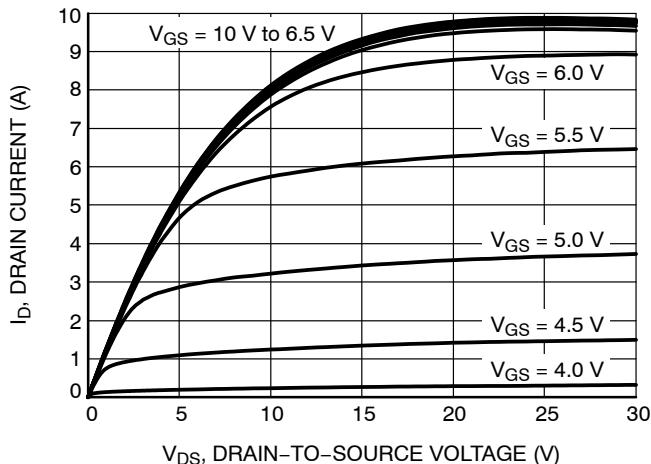


Figure 1. On-Region Characteristics

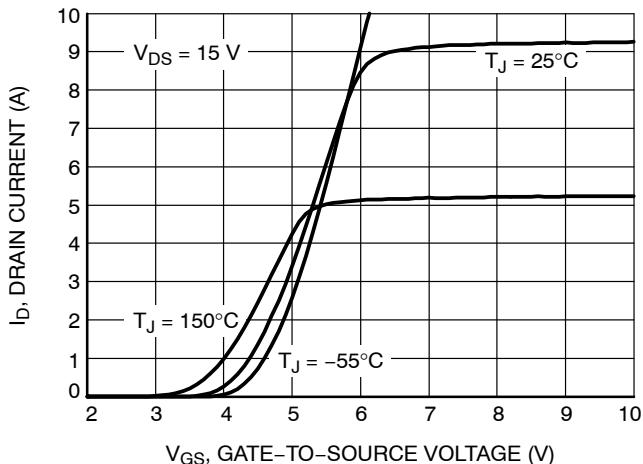


Figure 2. Transfer Characteristics

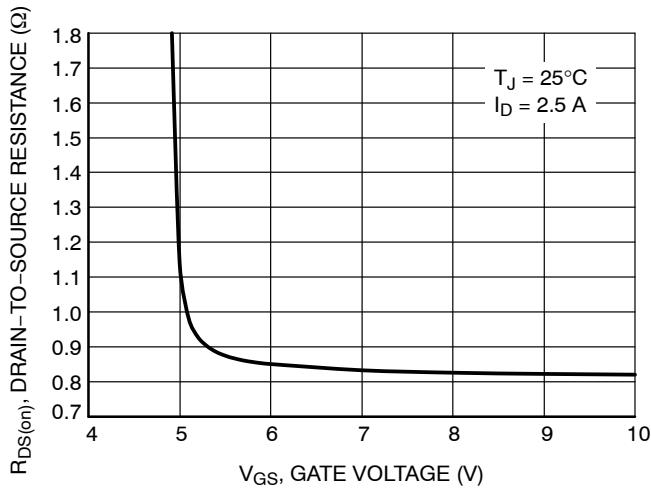


Figure 3. On-Resistance vs. Gate-to-Source Voltage

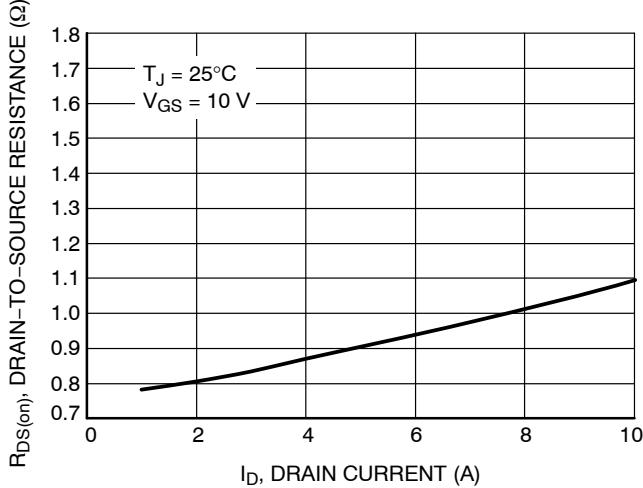


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

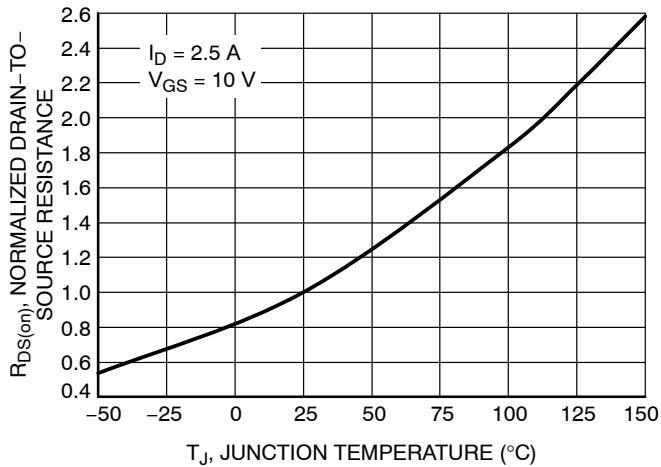


Figure 5. On-Resistance Variation with Temperature

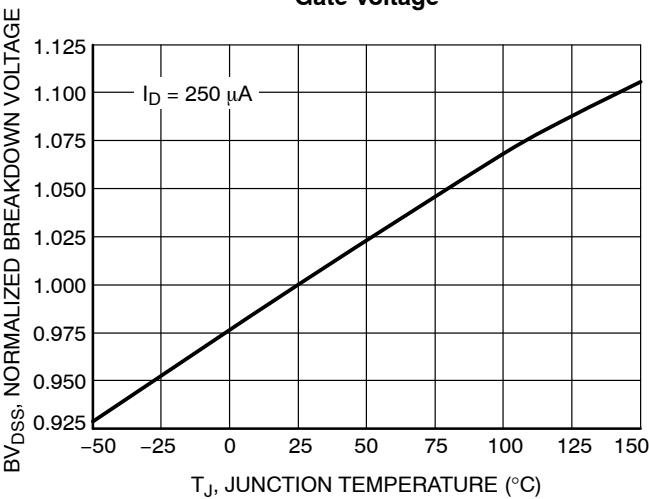


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

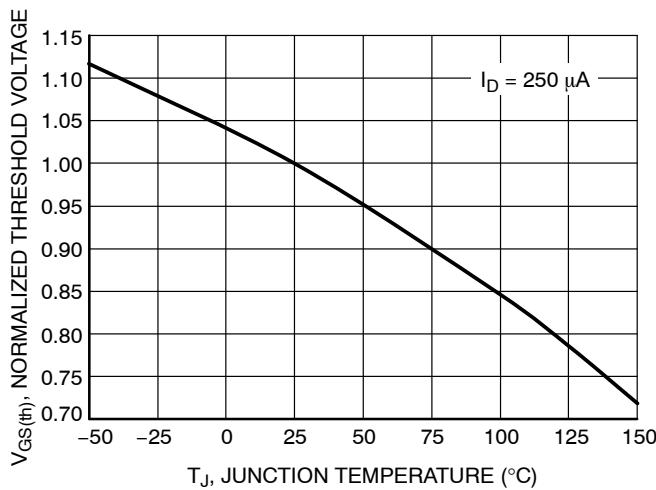


Figure 7. Threshold Voltage Variation with Temperature

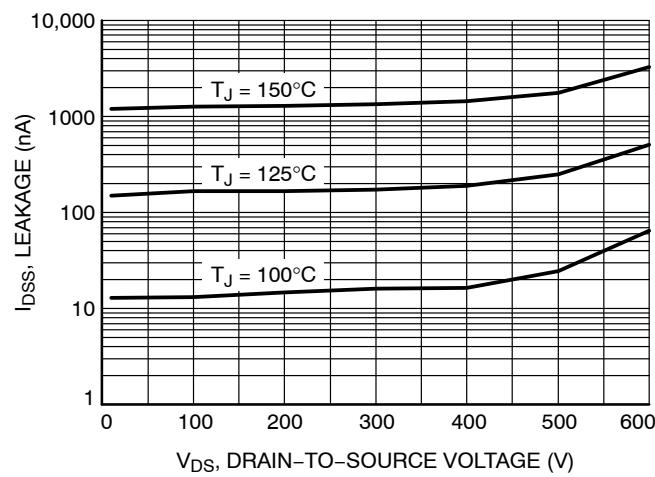


Figure 8. Drain-to-Source Leakage Current vs. Voltage

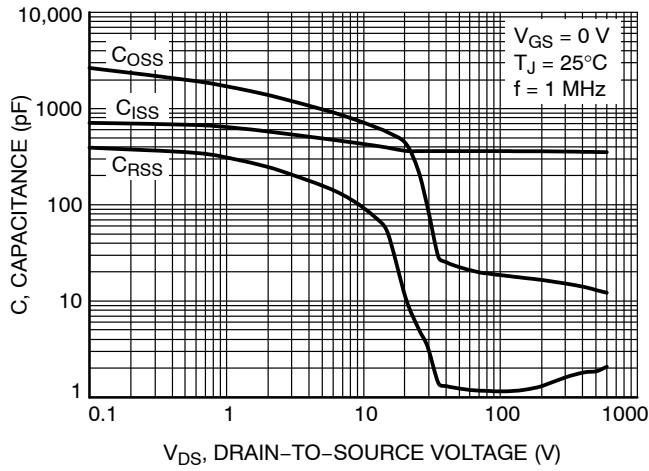


Figure 9. Capacitance Variation

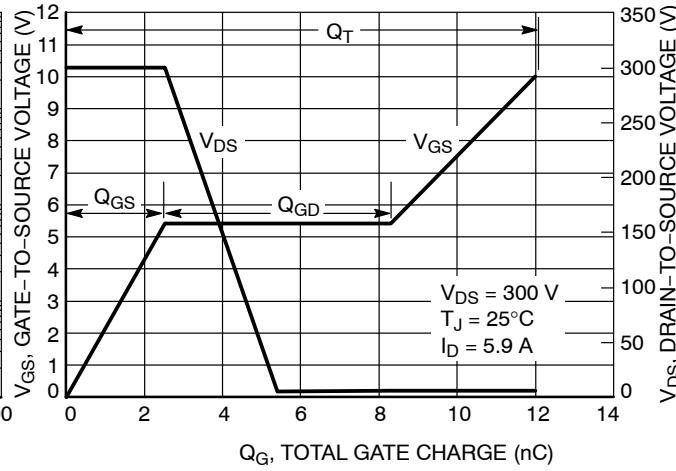


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

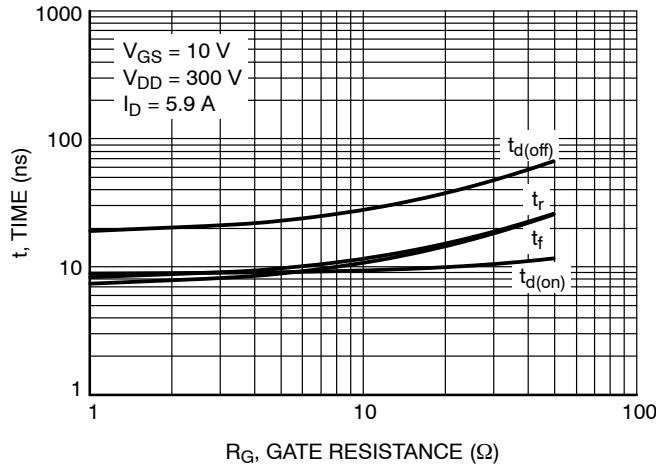


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

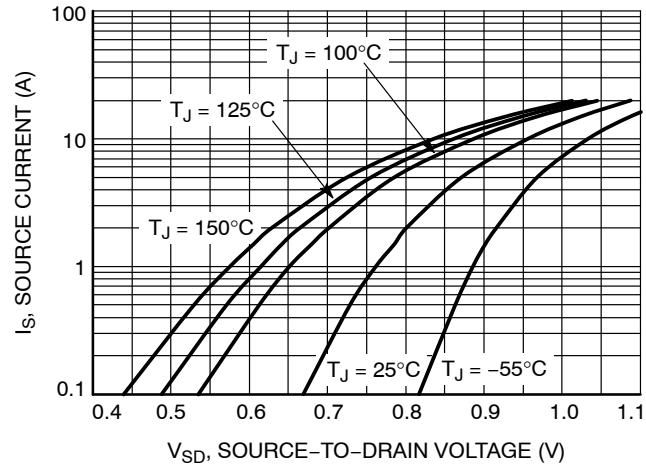


Figure 12. Diode Forward Voltage vs. Current

NDD60N900U1

TYPICAL CHARACTERISTICS

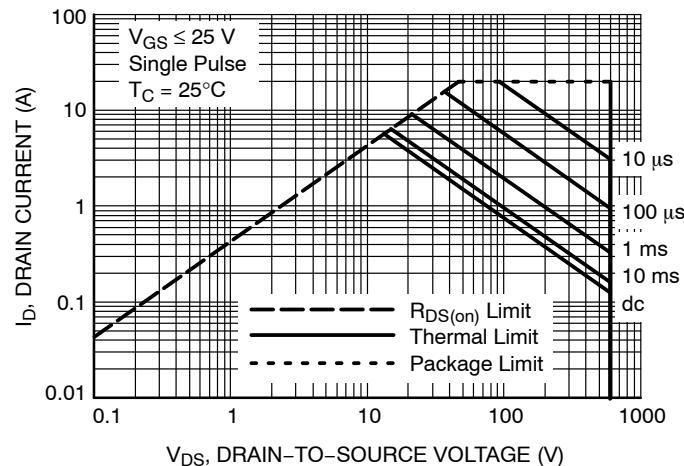


Figure 13. Maximum Rated Forward Biased Safe Operating Area

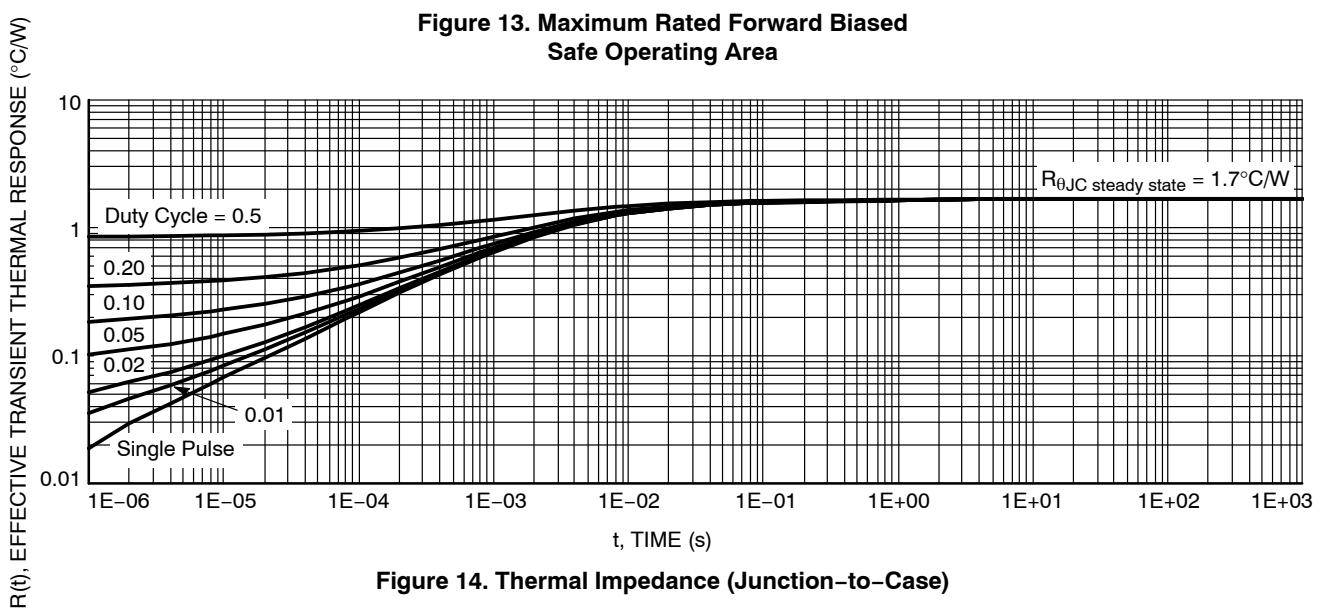
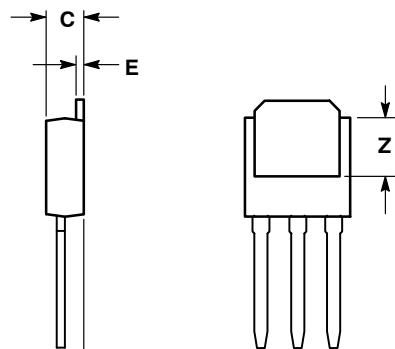
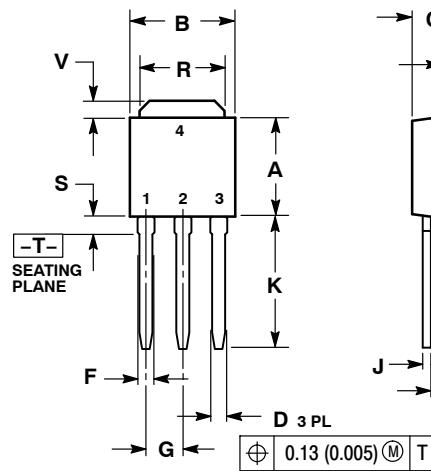


Figure 14. Thermal Impedance (Junction-to-Case)

NDD60N900U1

PACKAGE DIMENSIONS

IPIAK CASE 369D-01 ISSUE C



NOTES:

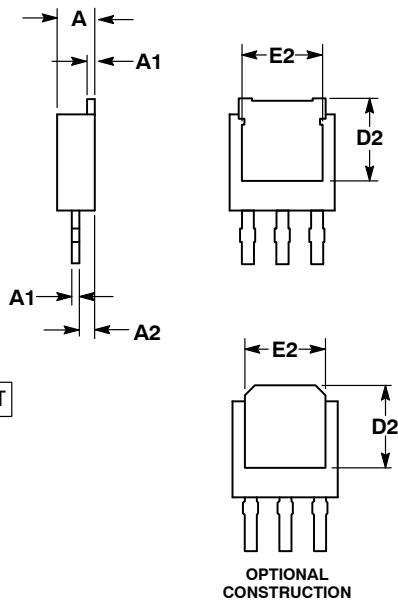
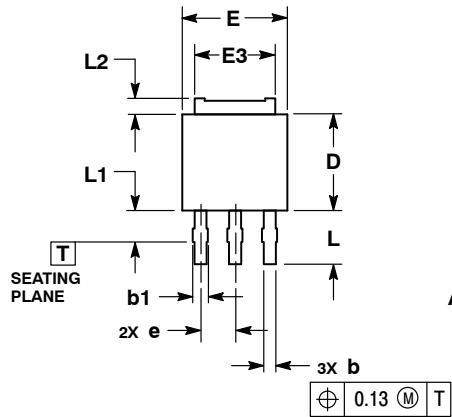
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 | BSC | 2.29 | BSC |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

3.5 MM IPIAK, STRAIGHT LEAD CASE 369AD ISSUE B



NOTES:

- 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2.. CONTROLLING DIMENSION: MILLIMETERS.
- 3.. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
- 4.. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 2.19 | 2.38 |
| A1 | 0.46 | 0.60 |
| A2 | 0.87 | 1.10 |
| b | 0.69 | 0.89 |
| b1 | 0.77 | 1.10 |
| D | 5.97 | 6.22 |
| D2 | 4.80 | --- |
| E | 6.35 | 6.73 |
| E2 | 4.57 | 5.45 |
| E3 | 4.45 | 5.46 |
| e | 2.28 | BSC |
| L | 3.40 | 3.60 |
| L1 | --- | 2.10 |
| L2 | 0.89 | 1.27 |

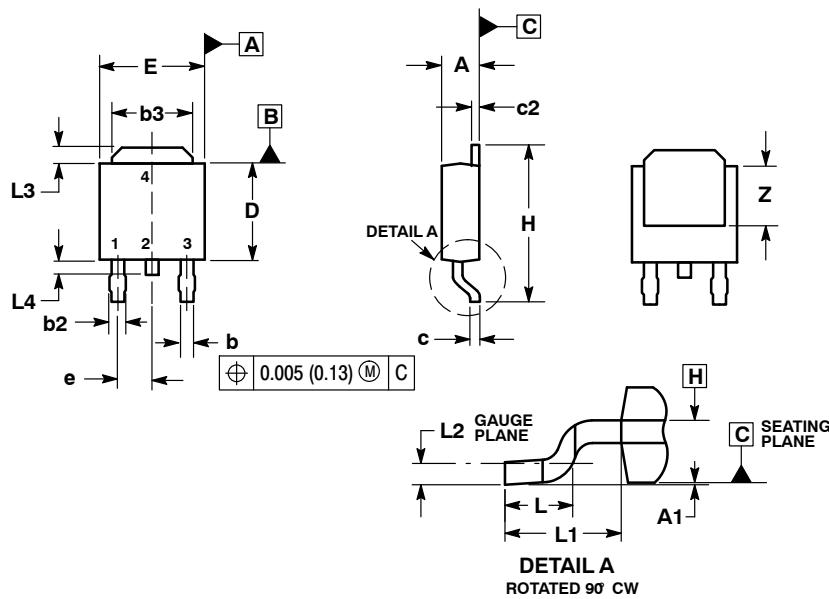
STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NDD60N900U1

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C ISSUE D



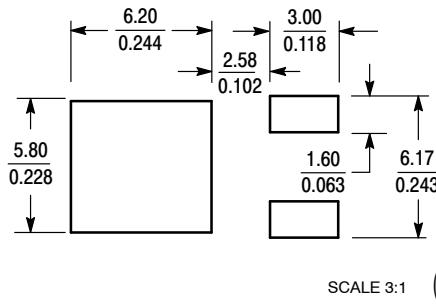
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 | BSC | 2.29 | BSC |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 | REF | 2.74 | REF |
| L2 | 0.020 | BSC | 0.51 | BSC |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:
 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm)
(inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NDD60N900U1/D