



MX553ENR125M000

Ultra-Low Jitter 125MHz LVPECL XO

ClockWorks® FUSION

General Description

The MX553ENR125M000 is an ultra-low phase jitter XO with LVPECL output optimized for high line rate applications.

Applications

- Gigabit Ethernet
- Storage

Features

- 125MHz LVPECL
- Typical phase noise:
 - 115fs (Integration range: 1.875MHz-20MHz)
- ± 50 ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

Absolute Maximum Ratings

Supply Voltage (VIN).....+4.6V
Lead Temperature (soldering, 10s).....260°C
Storage Temperature (T_s).....125°C
ESD Rating (HBM).....2kV

Operating Ratings

Supply Voltage (VIN).....+2.375V to +3.63V
Ambient Temperature (TA).....-40°C to +85°C

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2V.¹

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				120	mA
F0	Center Frequency			125		MHz
	Frequency Stability	Note 2			± 50	ppm
$\emptyset j$	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		159 115		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		85		350	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage	LVPECL output levels	VDD - 1.35	VDD - 1.01	VDD - 0.8	V
VOL	Output Low Voltage	LVPECL output levels	VDD - 2.0	VDD - 1.78	VDD - 1.6	V
Vswing	Peak to Peak Output Voltage Swing		0.65	0.77	0.95	V

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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December 04, 2016
MX553EN2-4608

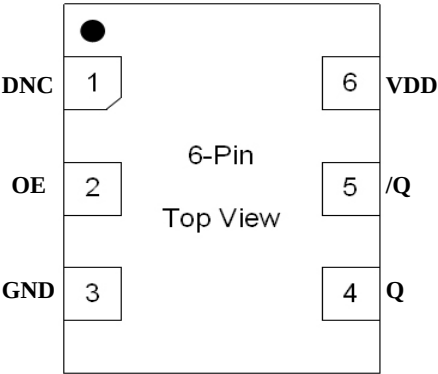
Revision 1.0
tcghelp@microchip.com

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX553ENR125M000	MX553E	NR1250	Tube	6-Pin 5mm x 3.2mm LGA
MX553ENR125M000 TR	MX553E	NR1250	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	DNC			Make no connection, leave floating.
2	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVPECL	Clock Output Frequency = 125MHz
6	VDD	PWR		Power Supply

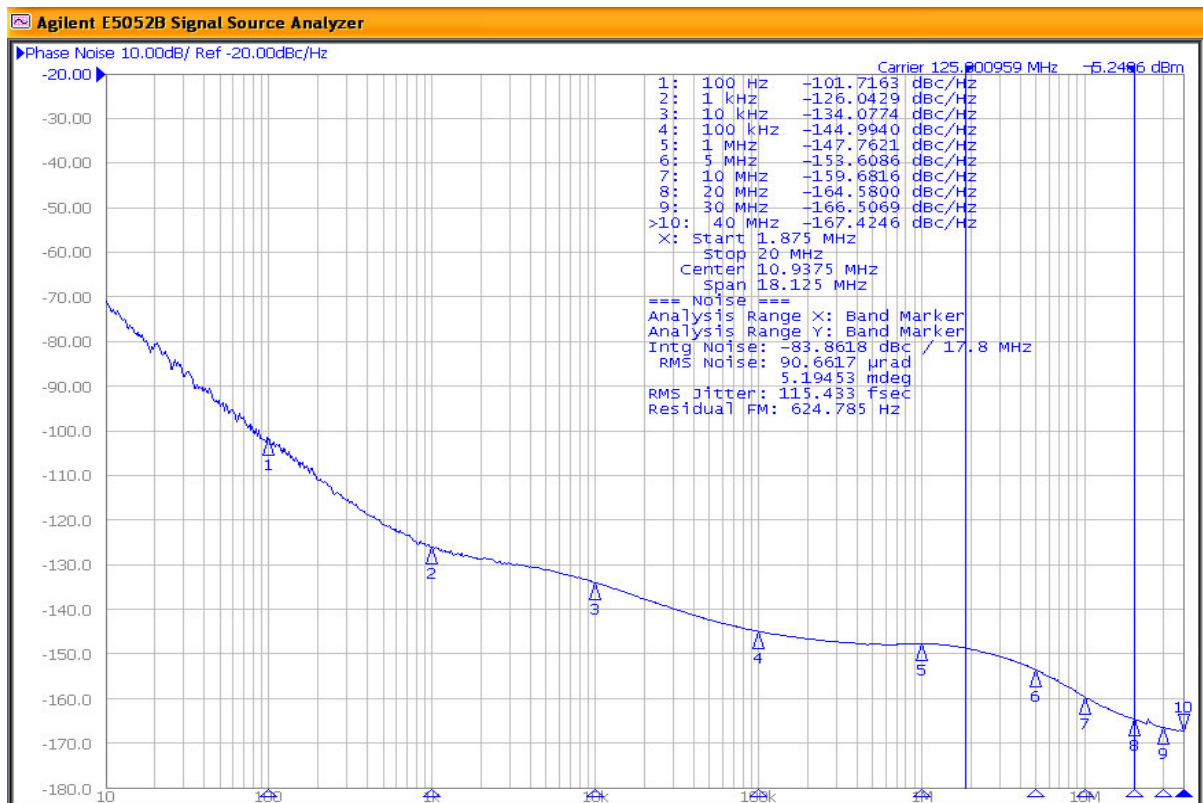


Figure 1. LVPECL Output 125MHz 1.875MHz-20MHz 115fs

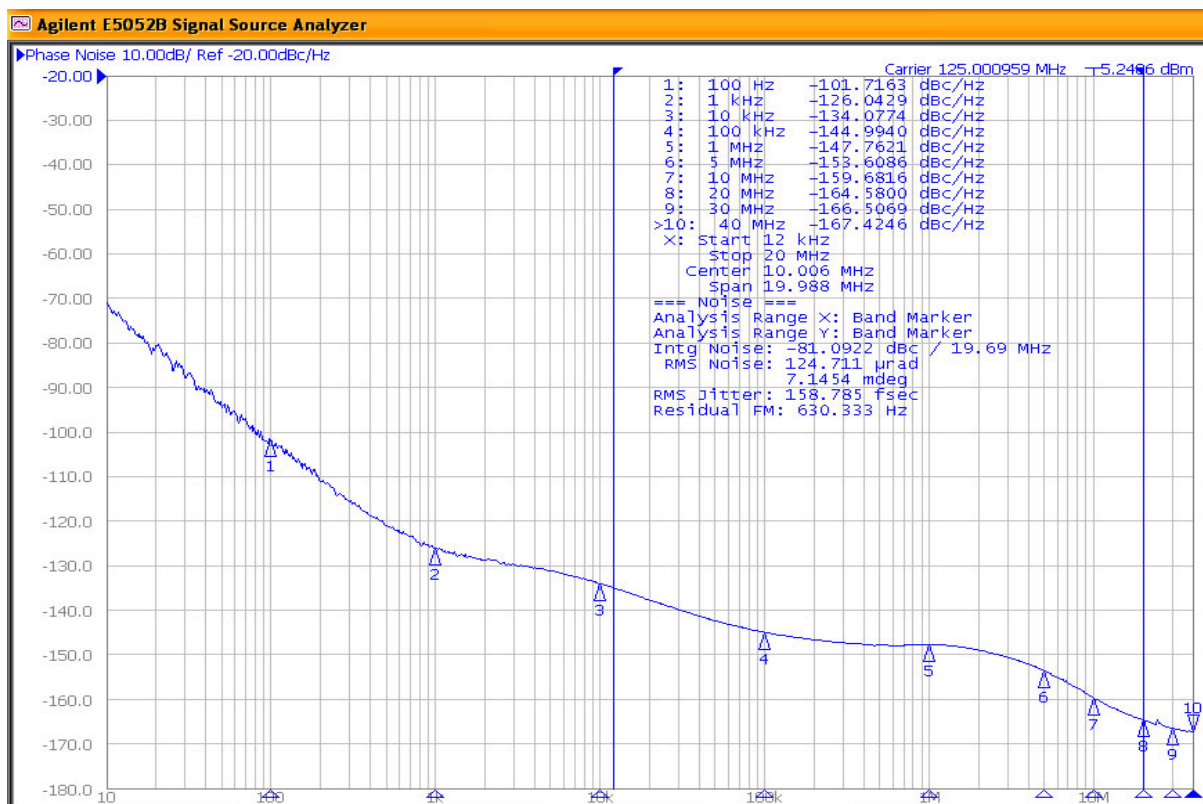
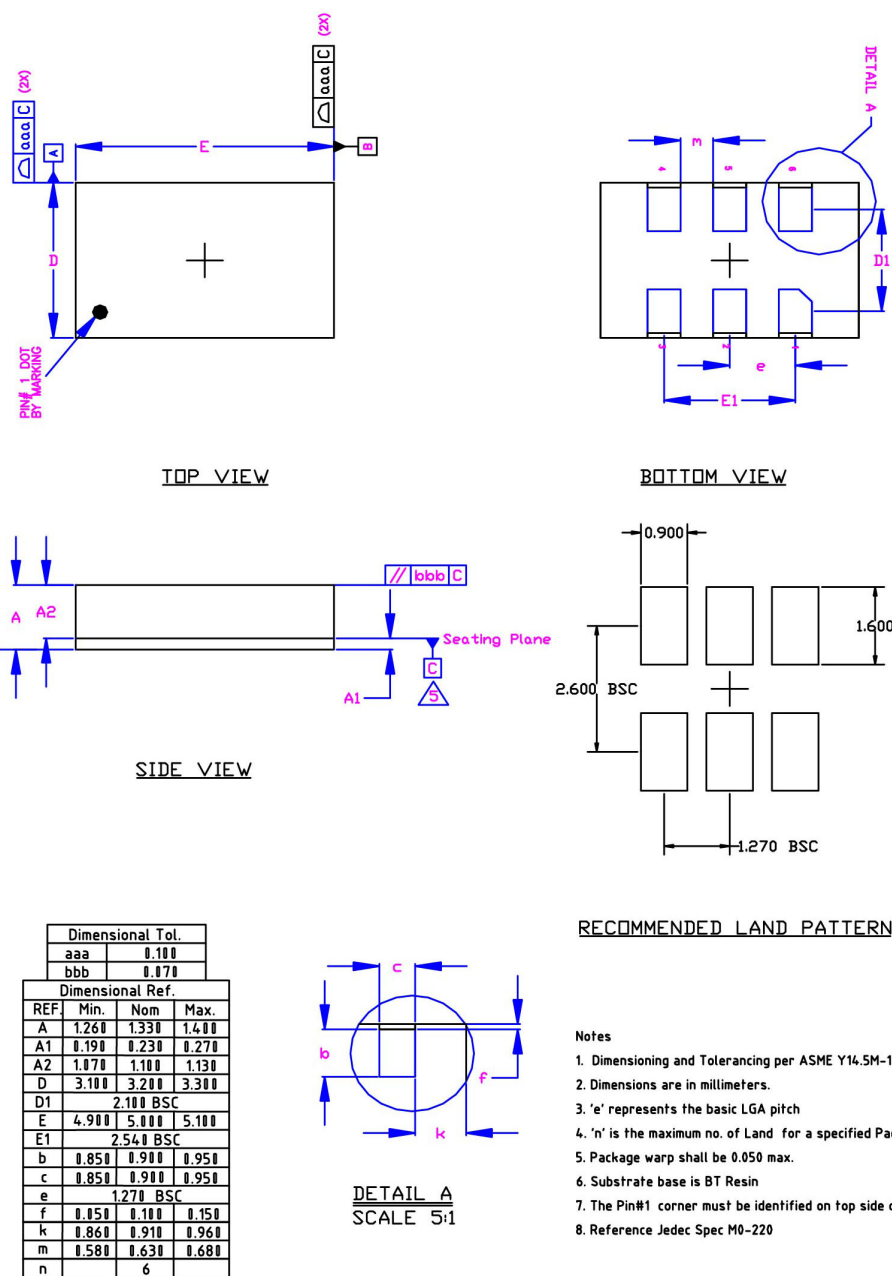


Figure 2. LVPECL Output 125MHz 12kHz-20MHz 159fs

Package Information and Recommended Land Pattern for 6-Pin LGA³



Notes

1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. 'e' represents the basic LGA pitch
4. 'n' is the maximum no. of Land for a specified Package.
5. Package warp shall be 0.050 max.
6. Substrate base is BT Resin
7. The Pin#1 corner must be identified on top side only.
8. Reference Jeduc Spec M0-220

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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