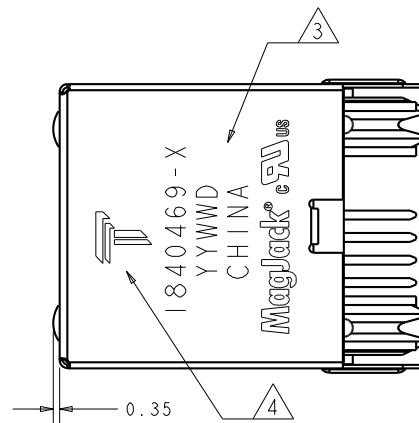
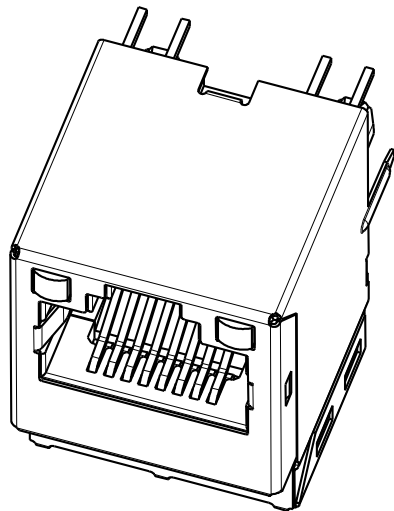


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PRODUCT MAY BE PROTECTED BY ONE OR MORE OF THE FOLLOWING US PATENTS:
5736910 5939955 6425781 6428361 6554638 6840817 7123117
7429195 7717749 7808751 6217391 6149050 7924130

REVISIONS

P	LTR	DESCRIPTION	DATE	DWN	APVD
D		EC-1411035, LOGO CHANGE	19JAN2015	JC	TY



- 1 MATERIALS:
PLASTIC HOUSING: BLACK, THERMOPLASTIC FLAMMABILITY RATING UL 94V-0
SHIELD: BRASS, PREPLATED WITH 0.76um MIN SEMI-BRIGHT NICKEL,
POST DIPPED WITH 2.54um MIN SAC SOLDER ON SOLDER TAILS,
CONTACTS: PHOSPHOR BRONZE, 1.27um MIN OVERALL NICKEL UNDERPLATE WITH
SELECT 1.27um MIN GOLD AT MATING INTERFACE AND 2.54um
MIN MATTE TIN ON SOLDER TAILS.
ALL PC BOARDS: HIGH TEMP PCB, TG>170°C.
LED: DIFFUSED EPOXY LENS, 0.50mm SQUARE CARBON STEEL WIREFRAME LEADS
PREPLATED WITH 2.03um MIN SILVER OVER 1.02um MIN NICKEL
OVER 1.02um MIN COPPER UNDERPLATE POST PLATED WITH 2.54um MIN TIN

- 2 MAGNETICS
APPLICATION: 10/100 BASE-T, EXTENDED TEMPERATURE, PoE
IMPEDANCE: 100 OHMS
TURNS RATIO (CHIP:CABLE): TX = 1:1, RX = 1:1
OPEN CIRCUIT INDUCTANCE (OCL): 350uH MIN @100kHz, 0.1VRMS,
8mADC BIAS FROM -40°C TO +85°C, TX AND RX
POE CURRENT: 350mADC MAX
PERFORMANCE @ 25°C:
INSERTION LOSS (IL): 1.1dB MAX FROM 0.5MHz TO 100MHz
RETURN LOSS (RL): 18dB MIN FROM 0.5MHz TO 30MHz
18-20LOG(f/30)dB MIN FROM 30.1MHz TO 60MHz
12dB MIN FROM 60.1MHz TO 80MHz
CROSSTALK ATTENUATION: 35dB MIN FROM 0.5MHz TO 40MHz
33-20LOG(f/50)dB MIN FROM 40.1MHz TO 100MHz
COMMON MODE REJECTION RATIO (CMRR): 30dB MIN FROM 0.5MHz TO 100MHz
ISOLATION VOLTAGE: COMPLIES WITH IEEE802.3af 2003, PARA 33.4.1, ITEM a.

- 3 PART NUMBER, DATE CODE AND COUNTRY OF ORIGIN LOCATED IN APPROXIMATE AREA SHOWN. DATE CODE: YY IS YEAR, WW IS WORK WEEK, D IS DAY OF WEEK WITH SUNDAY=1.

- 4 TRP CONNECTOR LOGO AND AGENCY APPROVAL LOGO, TO BE LOCATED IN APPROXIMATE AREA SHOWN.

5. OPERATING TEMP: FROM -40°C TO +85°C.

- 6 RJ45 CAVITY CONFORMS TO FCC RULES AND REGULATION PART 68 SUBPART F.


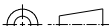
- 7 THE PARTS ARE RECOMMENDED FOR WAVE SOLDERING PROCESS, PEAK TEMPERATURE 260°C MAX. 10 SECONDS MAX.

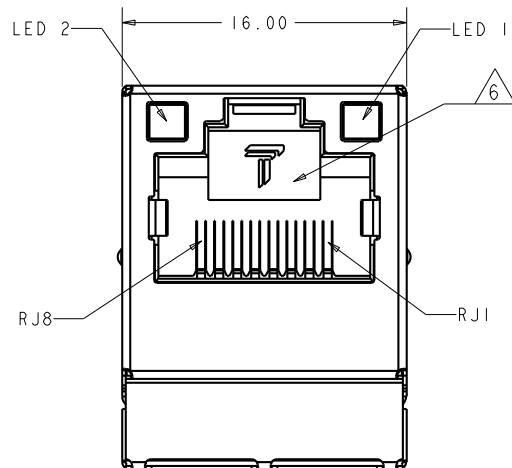
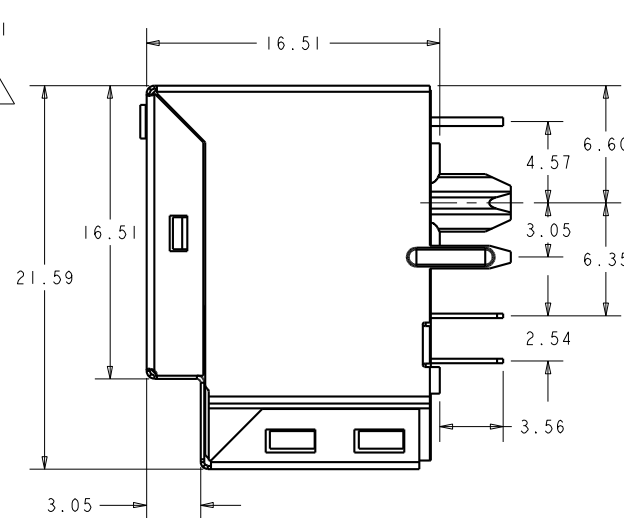
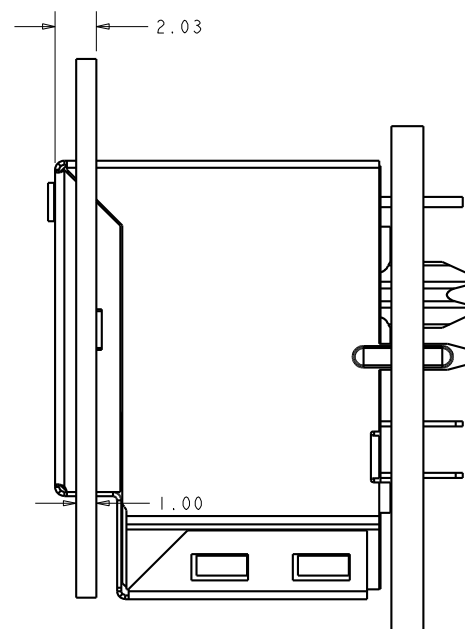
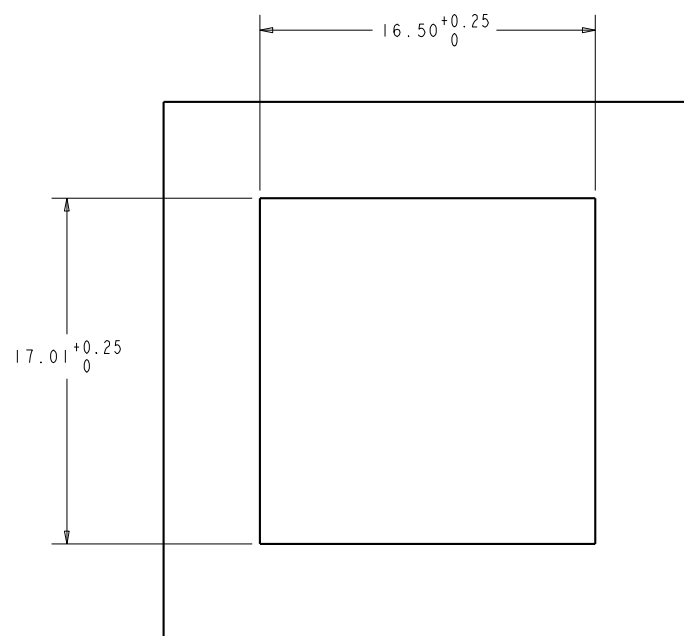
8. LED IS DRIVEN WITH CONSTANT CURRENT AT APPROX 20mA.

DOMINANT WAVELENGTH(λ D)
GREEN 568nm TYP. at IF=20mA
YELLOW 588nm TYP. at IF=20mA

FORWARD VOLTAGE(VF):
GREEN 2.2V TYP. at IF=20mA
YELLOW 2.1V TYP. at IF=20mA

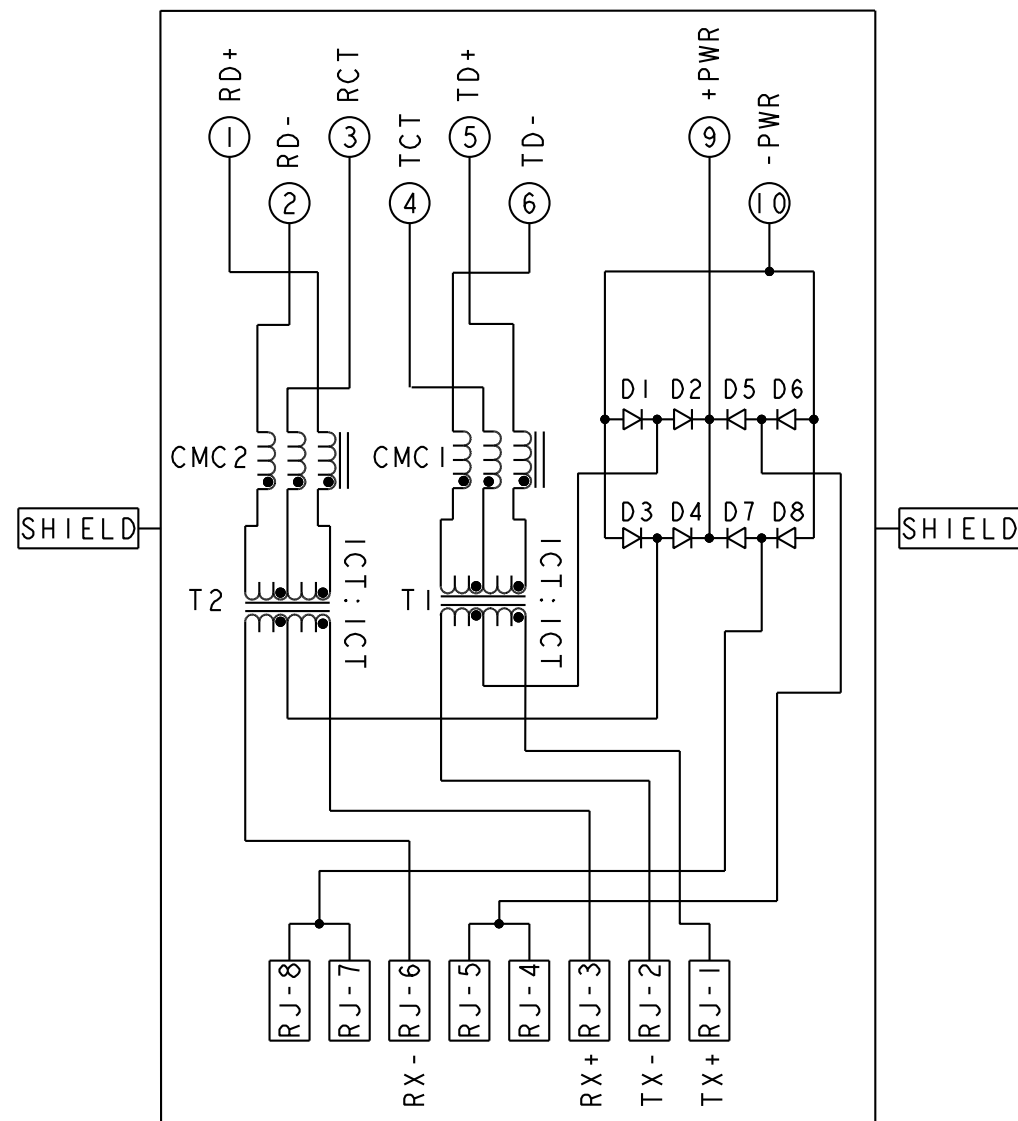
GRN/YEL	GRN/YEL	1840469-4
YELLOW	GREEN	1840469-3
GREEN	YELLOW	1840469-2
GREEN	GREEN	1840469-1
LED 1	LED 2	PART NUMBER

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN WESLEY.YI 25DEC2008	 trp CONNECTOR a bel group		DONGGUAN CHINA	
DIMENSIONS: mm		CHK KEITH ZHU 25DEC2008				
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APVD TEDDY XIONG 25DEC2008	MODEL NAME		DESC	
		MAGJACK		IX1, MAGJACK, VERTICAL 7D52ET, 10/100 CIRCUIT, W/ LEDS		
0 PLC ±0.25 1 PLC ±0.25 2 PLC ±0.25 3 PLC ±0.25 4 PLC ± ANGLES ±		SINGLE NON-POE		SIZE A2	CAGE CODE	DRAWING NO C=1840469
PRODUCT SPEC		APPLICATION SPEC		RESTRICTED TO		
-		-		CUSTOMER DRAWING		SCALE 3.1 SHEET 1 OF 2 REV D



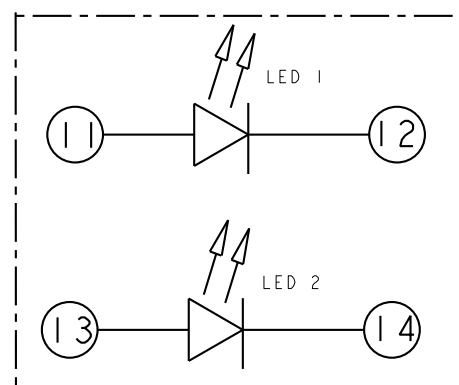
XXXX

7D52ET 10/100 BASE-T POE CIRCUIT ²

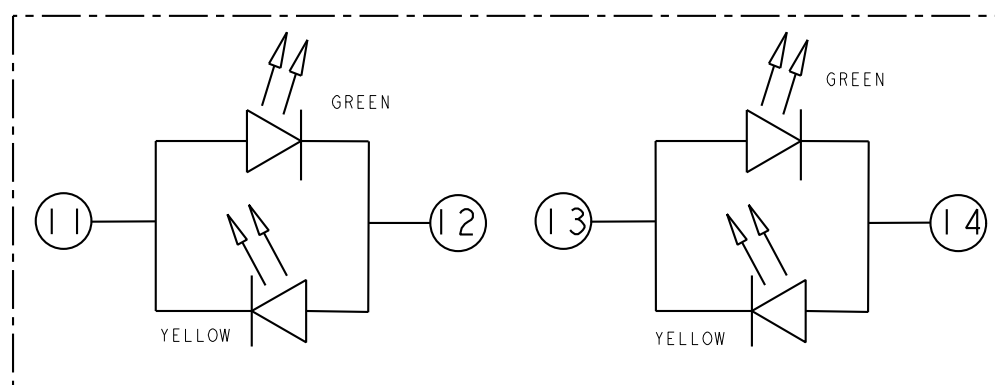


DI-D8 = Rectifier Diode
 Forward Voltage, $V_f = 1.2V$ Max @ $I_f = 0.5A$
 Forward Current, $I_f = 0.5A$ Max
 Reverse Voltage, $V_r = 80V$ Max

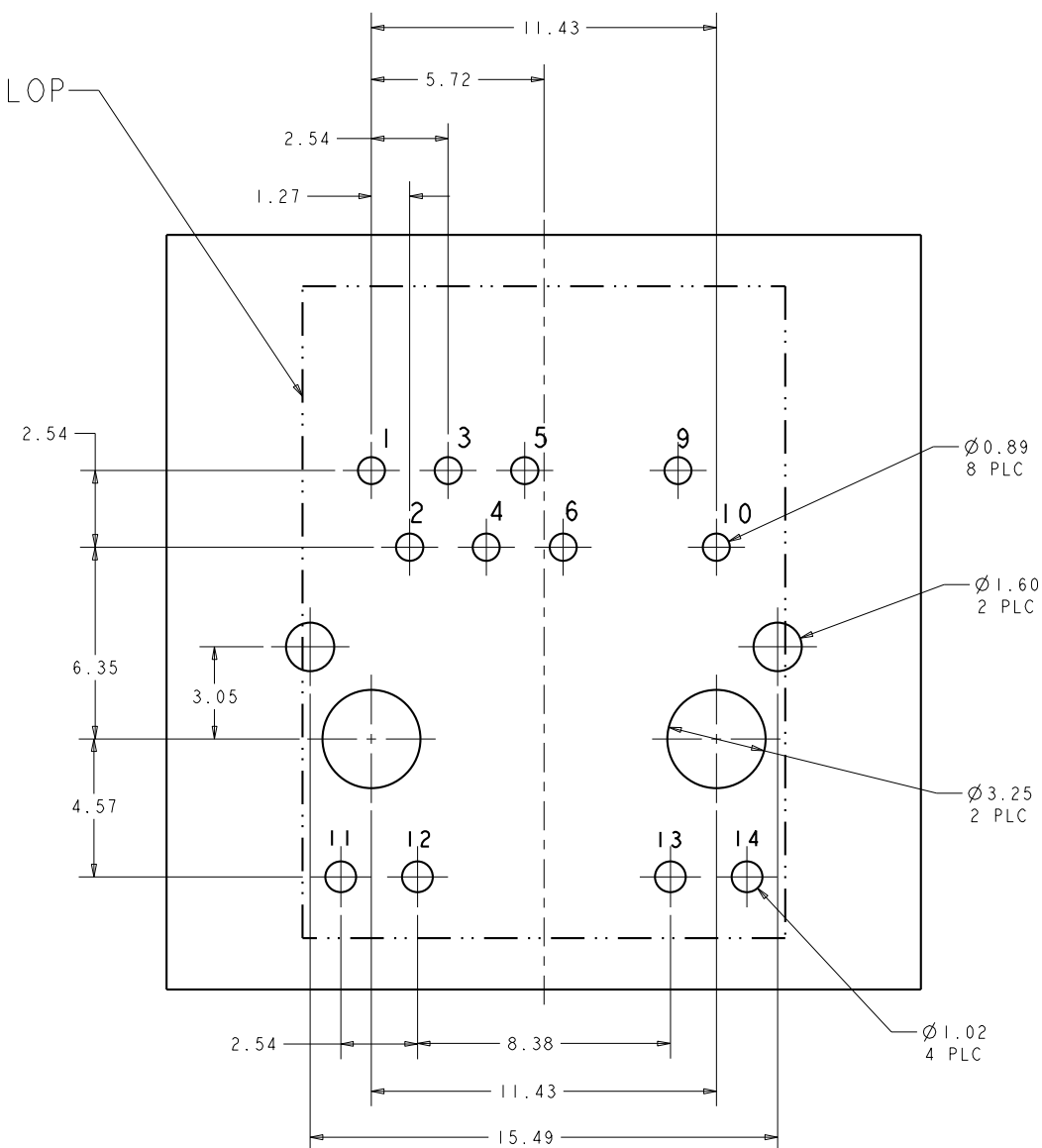
SINGLE COLOR LED





BI-COLOR LED



CONNECTOR ENVELOP



SUGGESTED PCB LAYOUT (TOL: ± 0.05)
 (COMPONENT SIDE VIEW)

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN WESLEY.YI	25DEC2008	 trp CONNECTOR a bel group	DONGGUAN CHINA	
		CHK KEITH.ZHU	25DEC2008			
		APVD TEDDY.XIONG	25DEC2008			
DIMENSIONS: mm	TOLERANCES UNLESS OTHERWISE SPECIFIED:	MODEL NAME MAGJACK		DESC IXI,MAGJACK, VERTICAL 7D52ET, 10/100 CIRCUIT, W/ LEDS	RESTRICTED TO	
	0 PLC ±0.25 1 PLC ±0.25 2 PLC ±0.25 3 PLC ±0.25 4 PLC ± ANGLES ± APPLICATION SPEC	SINGLE NON-POE		SIZE A2		
PRODUCT SPEC				CAGE CODE C=1840469		
				DRAWING NO C=1840469		
CUSTOMER DRAWING				SCALE 3:1	SHEET 2 OF 2	REV D