25-BIT CONFIGURABLE REGISTERED BUFFER

FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **Pinout Optimizes DDR2 DIMM PCB Layout**
- **Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer**
- **Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption**
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line**
- **Supports SSTL_18 Data Inputs**
- **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
- **Supports LVCMOS Switching Levels on the Control and $\overline{\text{RESET}}$ Inputs**
- **Supports Industrial Temperature Range (-40°C to 85°C)**
- **$\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**

DESCRIPTION

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VCC operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL_18, except the reset ($\overline{\text{RESET}}$) and control (Cn) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL_18 specifications.

The SN74SSTUB32864 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and CLK going low.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and are do-not-use (DNU) pins.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared, and the data outputs are driven low quickly, relative to the time required to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time required to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SN74SSTUB32864 ensures that the outputs remain low, thus ensuring there will be no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low, except $\overline{\text{QERR}}$. The LVCMOS $\overline{\text{RESET}}$ and Cn inputs always must be held at a valid logic high or low level.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA–ZKE	Tape and reel	SN74SSTUB32864ZKER	SB864

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

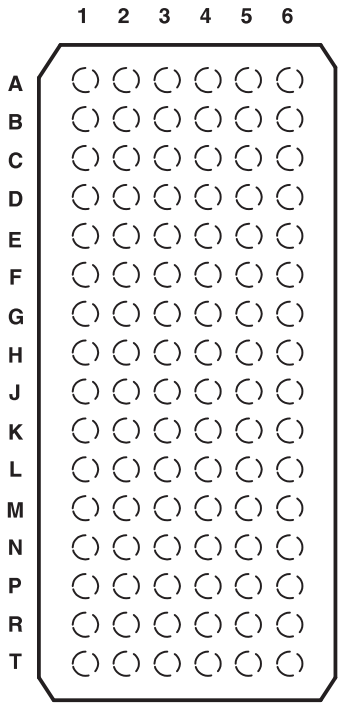
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The device also supports low-power active operation by monitoring both system chip select ($\overline{DCS}$ and $\overline{CSR}$) inputs and gates the Qn outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ inputs are high. If either DCS or CSR input is low, the Qn outputs function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ control and, when driven low, forces the Qn outputs low. If the $\overline{DCS}$ control functionality is not desired, the $\overline{CSR}$ input can be hard-wired to ground, in which case the setup-time requirement for $\overline{DCS}$ is the same as for the other D data inputs. To control the low-power mode with $\overline{DCS}$ only, the $\overline{CSR}$ input should be pulled up to V_{CC} through a pullup resistor.

The two V_{REF} pins (A3 and T3) are connected together internally by approximately 150Ω. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

PACKAGE
(TOP VIEW)

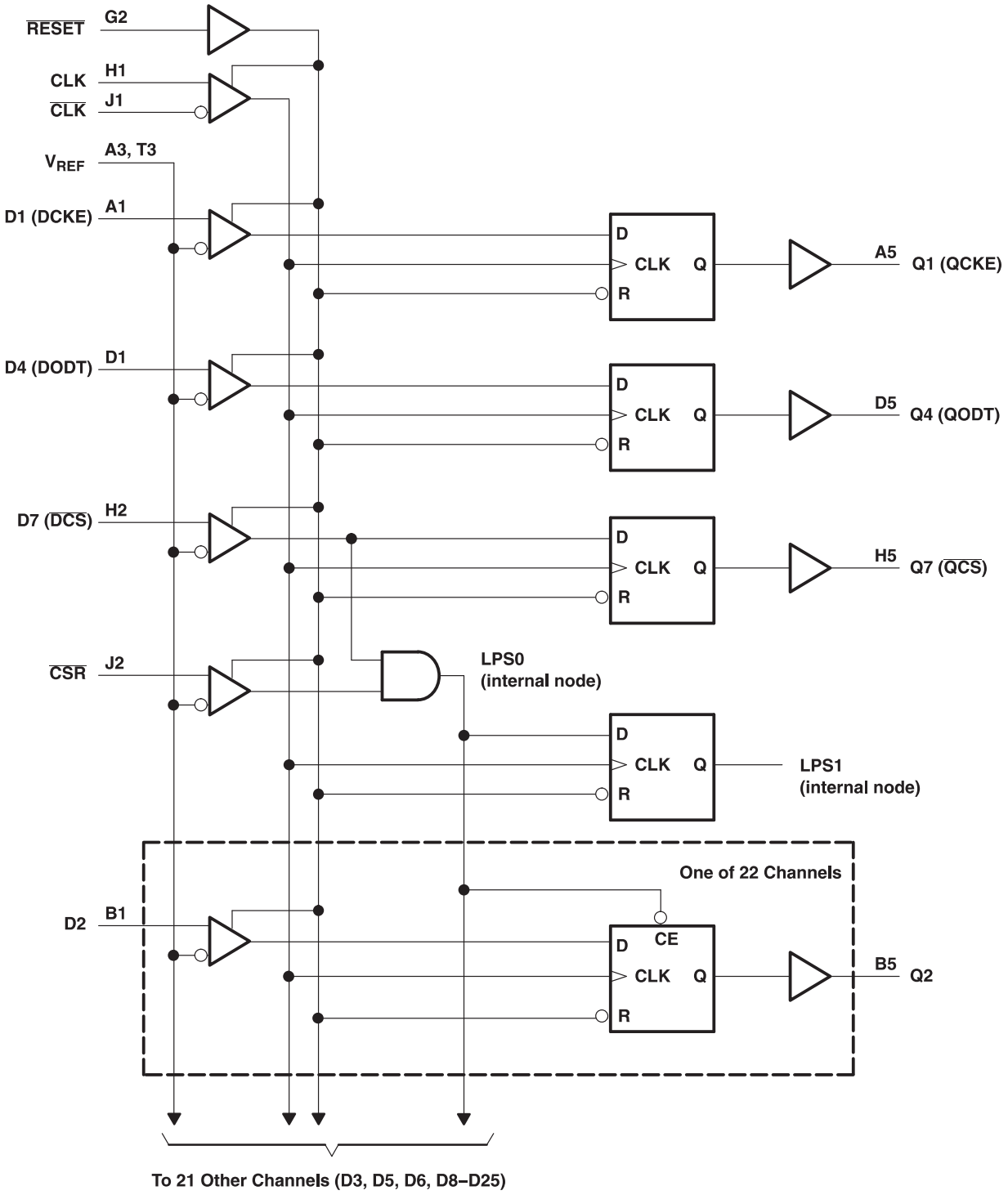


Terminal Assignments for 1:1 Register-A (C0 = 0, C1 = 0)

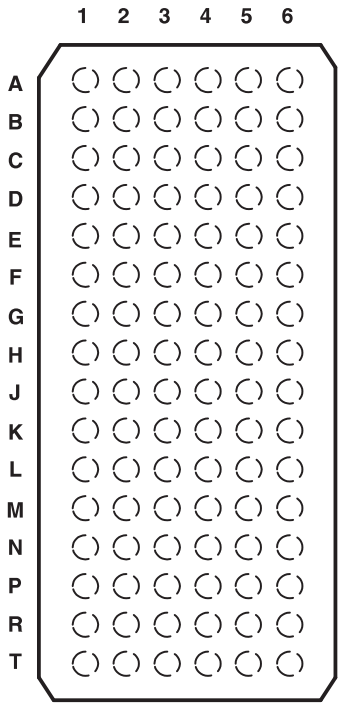
	1	2	3	4	5	6
A	D1 (DCKE)	NC	V_{REF}	V_{CC}	Q1 (QCKE)	DNU
B	D2	D15	GND	GND	Q2	Q15
S	D3	D16	V_{CC}	V_{CC}	Q3	Q16
D	D4 (DODT)	NC	GND	GND	Q4 (QODT)	DNU
E	D5	D17	V_{CC}	V_{CC}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7 ($\overline{\text{QCS}}$)	DNU
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{CC}	V_{CC}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{CC}	V_{CC}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{CC}	V_{CC}	Q13	Q24
T	D14	D25	V_{REF}	V_{CC}	Q14	Q25

Each pin name in parentheses indicates the DDR2 DIMM signal name.
DNU - Do not use
NC - No internal connection

Logic Diagram for 1:1 Register Configuration (Positive Logic); C0 = 0, C1 = 0



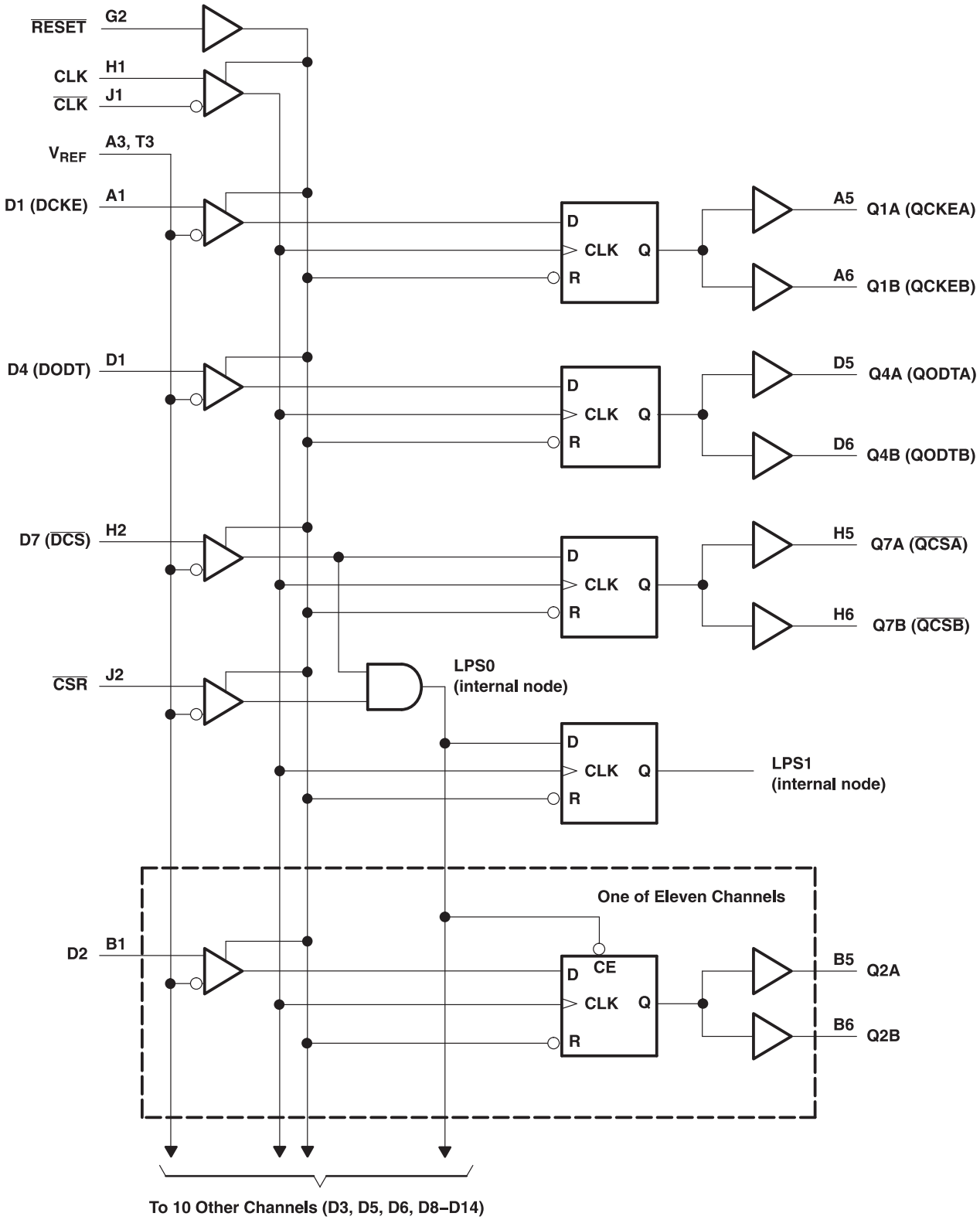
PACKAGE
(TOP VIEW)



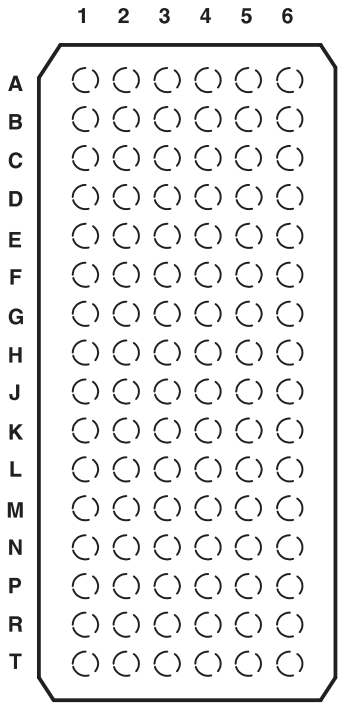
	1	2	3	4	5	6
A	D1 (DCKE)	NC	V_{REF}	V_{CC}	Q1A (QCKEA)	Q1B (QCKEB)
B	D2	DNU	GND	GND	Q2A	Q2B
S	D3	DNU	V_{CC}	V_{CC}	Q3A	Q3B
D	D4 (DODT)	NC	GND	GND	Q4A (QODTA)	Q4B(QODTB)
E	D5	DNU	V_{CC}	V_{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7A ($\overline{\text{QCSA}}$)	Q7B ($\overline{\text{QCSB}}$)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{CC}	V_{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V_{CC}	V_{CC}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{CC}	V_{CC}	Q13A	Q13B
T	D14	DNU	V_{REF}	V_{CC}	Q14A	Q14B

Each pin name in parentheses indicates the DDR2 DIMM signal name.
DNU - Do not use
NC - No internal connection

Logic Diagram for 1:2 Register-A Configuration (Positive Logic); C0 = 0, C1 = 1



PACKAGE
(TOP VIEW)

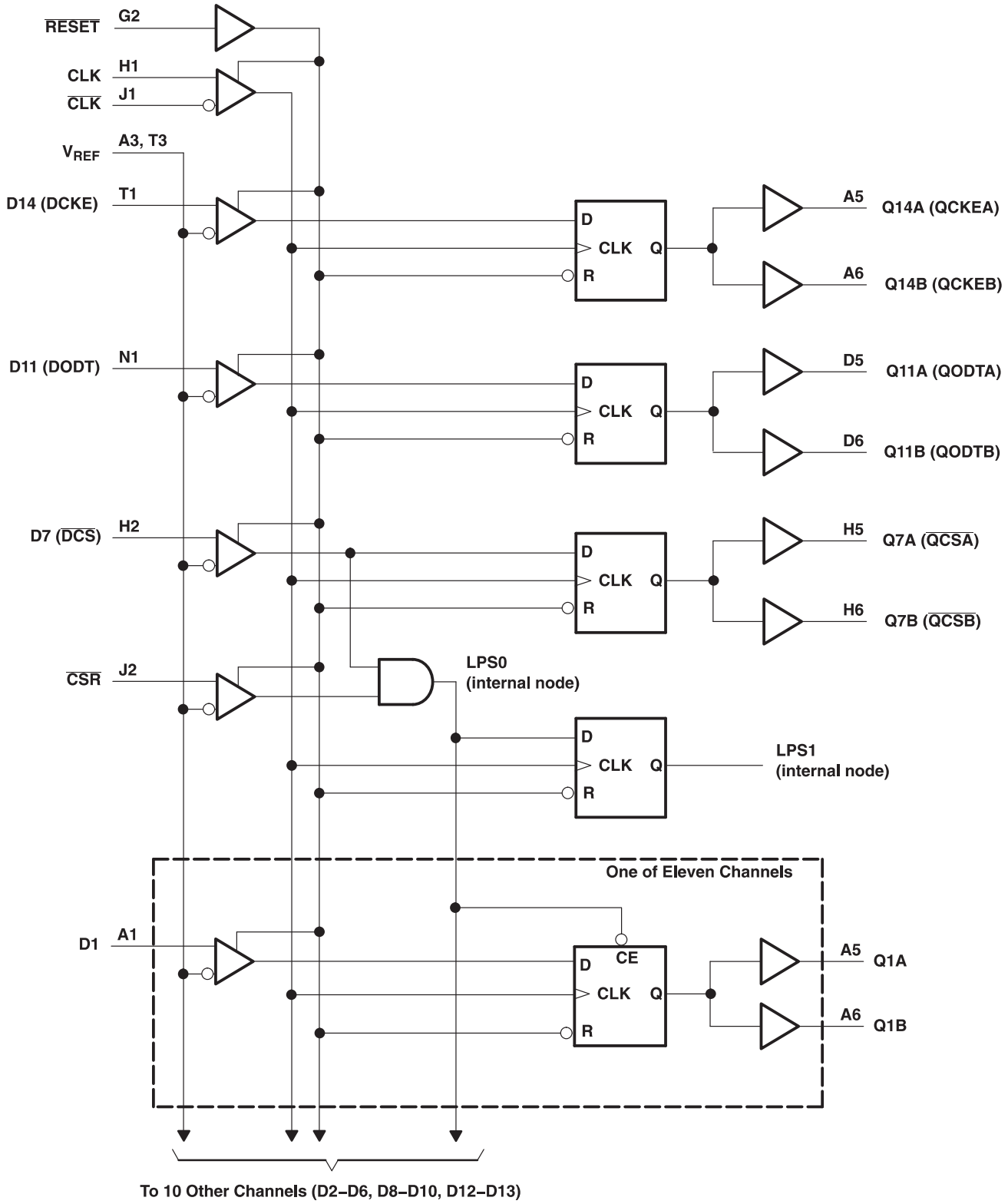


Terminal Assignments for 1:2 Register-b (C0 = 1, C1 = 1)

	1	2	3	4	5	6
A	D1	NC	V_{REF}	V_{CC}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
S	D3	DNU	V_{CC}	V_{CC}	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	V_{CC}	V_{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7A ($\overline{\text{QCSA}}$)	Q7B ($\overline{\text{QCSB}}$)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{CC}	V_{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11 (DODT)	DNU	V_{CC}	V_{CC}	Q11A (QODTA)	Q11B (QODTB)
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{CC}	V_{CC}	Q13A	Q13B
T	D14 (DCKE)	DNU	V_{REF}	V_{CC}	Q14A (QCKEA)	Q14B (QCKEB)

Each pin name in parentheses indicates the DDR2 DIMM signal name.
DNU - Do not use
NC - No internal connection

Logic Diagram for 1:2 Register-B Configuration C0 = 1, C1 = 1



TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V_{CC}	Power-supply voltage	1.8 V nominal
V_{REF}	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
$\overline{CLK}$	Negative master clock input	Differential input
C0, C1	Configuration control input. Register A or Register B and 1:1 mode or 1:2 mode select.	LVCMOS inputs
$\overline{RESET}$	Asynchronous reset input. Resets registers and disables V_{REF}, data, and clock differential-input receivers. When $\overline{RESET}$ is low, all Q outputs are forced low and the $\overline{QERR}$ output is forced high.	LVCMOS input
D1-D25	Data input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$.	SSTL_18 inputs
$\overline{CSR}$, $\overline{DCS}$	Chip select inputs. Disables D1–D25(1) outputs switching when both inputs are high	SSTL_18 inputs
DODT	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	SSTL_18 input
Q1–Q25(2)	Data outputs that are suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	1.8 V CMOS outputs
$\overline{QCS}$	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V CMOS output
QODT	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V CMOS output
QCKE	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V CMOS output
NC	No internal connection	
DNU	Do not use. Inputs are in standby-equivalent mode, and outputs are driven low.	

(1) Data inputs = D2, D3, D5, D6, D8-D25 when C0 = 0 and C1 = 0
Data inputs = D2, D3, D5, D6, D8-D14 when C0 = 0 and C1 = 1
Data inputs = D1-D6, D8-D10, D12, D13 when C0 = 1 and C1 = 1.D
(2) Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0 = 0 and C1 = 0
Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0 = 0 and C1 = 1
Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0 = 1 and C1 = 1.

FUNCTION TABLE

INPUTS						OUTPUTS
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CLK	$\overline{CLK}$	Dn	Qn
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q_0
H	X	X	L or H	L or H	X	Q_0
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L

FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{RESET}$	CLK	$\overline{CLK}$	DCKE, $\overline{DCS}$, $\overline{DODT}$	QCKE, $\overline{QCS}$, QODT
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or Floating	X or Floating	X or Floating	L

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_{CC}	Supply voltage range		–0.5 to 2.5	V
V_I	Input voltage range(2) (3)		-0.5 to V_{CC} + 0.5	V
V_O	Output voltage range(2) (3)		–0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp current, (V_I < 0 or V_I > V_{CC})		±50	mA
I_{OK}	Output clamp current, (V_O < 0 or V_O > V_{CC})		±50	mA
I_O	Continuous output current (V_O = 0 to V_{CC})		±50	mA
I_{CC}	Continuous current through each V_{CC} or GND		±100	mA
$R_{\theta JA}$	Thermal impedance, junction-to-ambient(4)	No airflow	39.8	K/W
		Airflow 150 ft/min	34.1	
		Airflow 250 ft/min	33.6	
		Airflow 500 ft/min	32.5	
$R_{\theta JB}$	Thermal resistance, junction-to-board(4)	No airflow	14.5	
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 2.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1.7		1.9	V
V_{REF}	Reference voltage		0.49 × V_{CC}	0.5 × V_{CC}	0.51 × V_{CC}	V
V_{TT}	Termination voltage		V_{REF}–40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0		VCC	V
V_{IH}	AC high-level input voltage	Data inputs, $\overline{CSR}$	V_{REF} + 250 mV			V
V_{IL}	AC low-level input voltage	Data inputs, $\overline{CSR}$			V_{REF}–250 mV	V
V_{IH}	DC high-level input voltage	Data inputs, $\overline{CSR}$	V_{REF} + 125 mV			V
V_{IL}	DC low-level input voltage	Data inputs, $\overline{CSR}$			V_{REF}–125 mV	V
V_{IH}	High-level input voltage	$\overline{RESET}$, C_n	0.65 × V_{CC}			V
V_{IL}	Low-level input voltage	$\overline{RESET}$, C_n			0.35 × V_{CC}	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{CLK}$	0.675		1.125	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$	600			mV
I_{OH}	High-level output current	Q outputs			–8	mA
I_{OL}	Low-level output current	Q outputs			8	mA
T_A	Operating free-air temperature		-40		85	°C

(1) The $\overline{RESET}$ and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	Q outputs	I_{OH} = –100 µA		1.7V to 1.9V	V_{CC}–0.2			V
		I_{OH} = –6 mA		1.7V	1.3			
V_{OL}	Q outputs	I_{OL} = 100 µA		1.7V to 1.9V			0.2	V
		I_{OL} = 6 mA		1.7V			0.4	
I_I	All inputs(2)	$V_I = V_{CC}$ or GND		1.9V			±5	µA
I_{CC}	Static standby	$\overline{RESET}$ = GND	I_O = 0	1.9V			200	µA
	Static operating	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					40	mA
I_{CCD}	Dynamic operating – clock only	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	1.8V		45		µA/MHz
	Dynamic operating – per each data input, 1:1 configuration	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle				43		µA clock MHz/ D input
	Dynamic operating – per each data input, 1:2 configuration					60		
I_{CCDLP}	Chip-select-enabled low-power active mode – clock only	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	1.8V		45		µA/MHz
	Chip-select-enabled low-power active mode - 1:1 configuration	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle				2		µA clock MHz/ D input
	Chip-select-enabled low-power active mode – 1:2 configuration					3		
C_i	Data inputs, $\overline{CSR}$	$V_I = V_{REF}$ ± 250 mV		1.8V	2.5	3	3.5	pF
	CLK, $\overline{CLK}$	V_{ICR} = 0.9 V, $V_{I(PP)}$ = 600 mV			2		3	
	$\overline{RESET}$	$V_I = V_{CC}$ or GND				4		

(1) All typical values are at V_{CC} = 1.8 V, T_A = 25°C.
(2) Each V_{REF} pin (A3 or T3) should be tested independently, with the other (untested) pin open.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 and (1)

			V_{CC} = 1.8 V ± 0.1 V		UNIT
			MIN	MAX	
fclock	Clock frequency			410	MHz
tw	Pulse duration, CLK, $\overline{CLK}$ high or low		1		ns
tact	Differential inputs active time(2)			10	ns
tinact	Differential inputs inactive time(3)			15	ns
t_{su}	Setup time	$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ high; $\overline{CSR}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS}$ high	600		ps
		$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ low	500		
		DODT, DCKE, and Data before CLK↑, $\overline{CLK}$↓	500		
t_h	Hold time	$\overline{DCS}$, DODT, DCKE, and Data after CLK↑, $\overline{CLK}$↓	400		ps

(1) All inputs slew rate is 1 V/ns ± 20%.
(2) V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after $\overline{RESET}$ is taken high.
(3) V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{RESET}$ is taken low.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.1 V		UNIT
				MIN	MAX	
f_{max}	See Figure 2			410		MHz
t_{pdm}	Production test, See Figure 1	CLK and $\overline{CLK}$	Q	0.4	0.8	ns
t_{RPHL} (1)	See Figure 2	$\overline{RESET}$	Q		3	ns

(1) Includes 350-ps test-load transmission-line delay.

OUTPUT SLEW RATES

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO	V_{CC} = 1.8 V ± 0.1 V		UNIT
			MIN	MAX	
dV/dt_r	20%	80%	1	4	V/ns
dV/dt_f	80%	20%	1	4	V/ns
dV/dt_Δ(1)	20% or 80%	80% or 20%		1	V/ns

(1) Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

PARAMETER MEASUREMENT INFORMATION

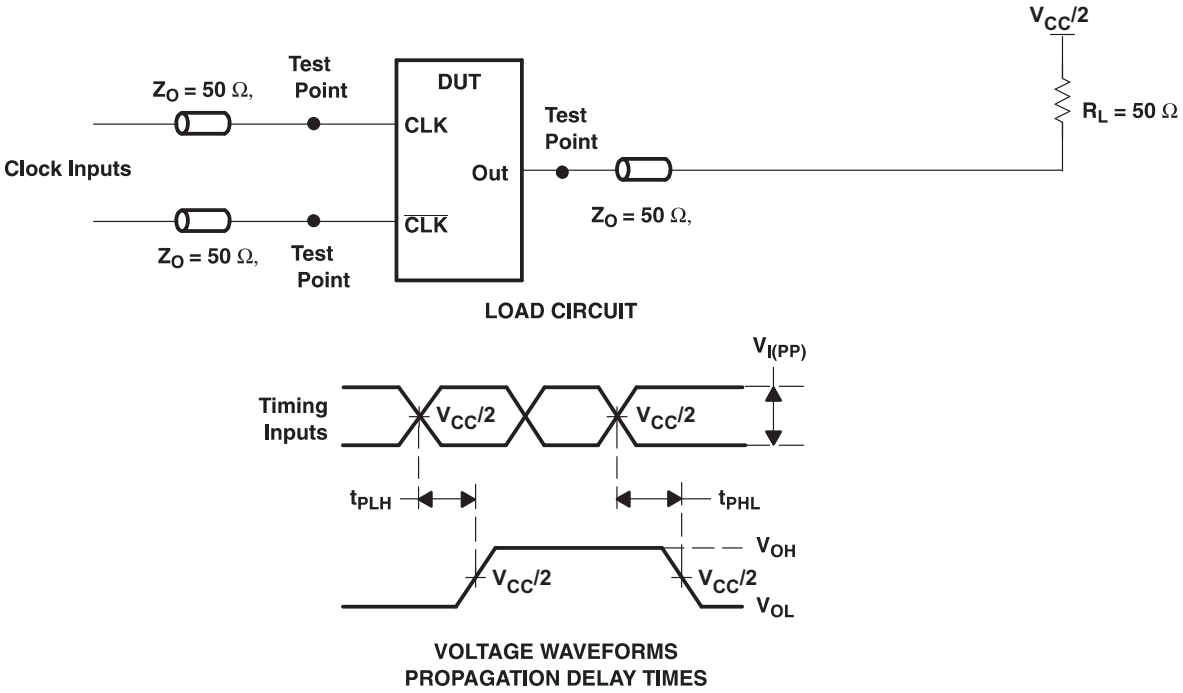
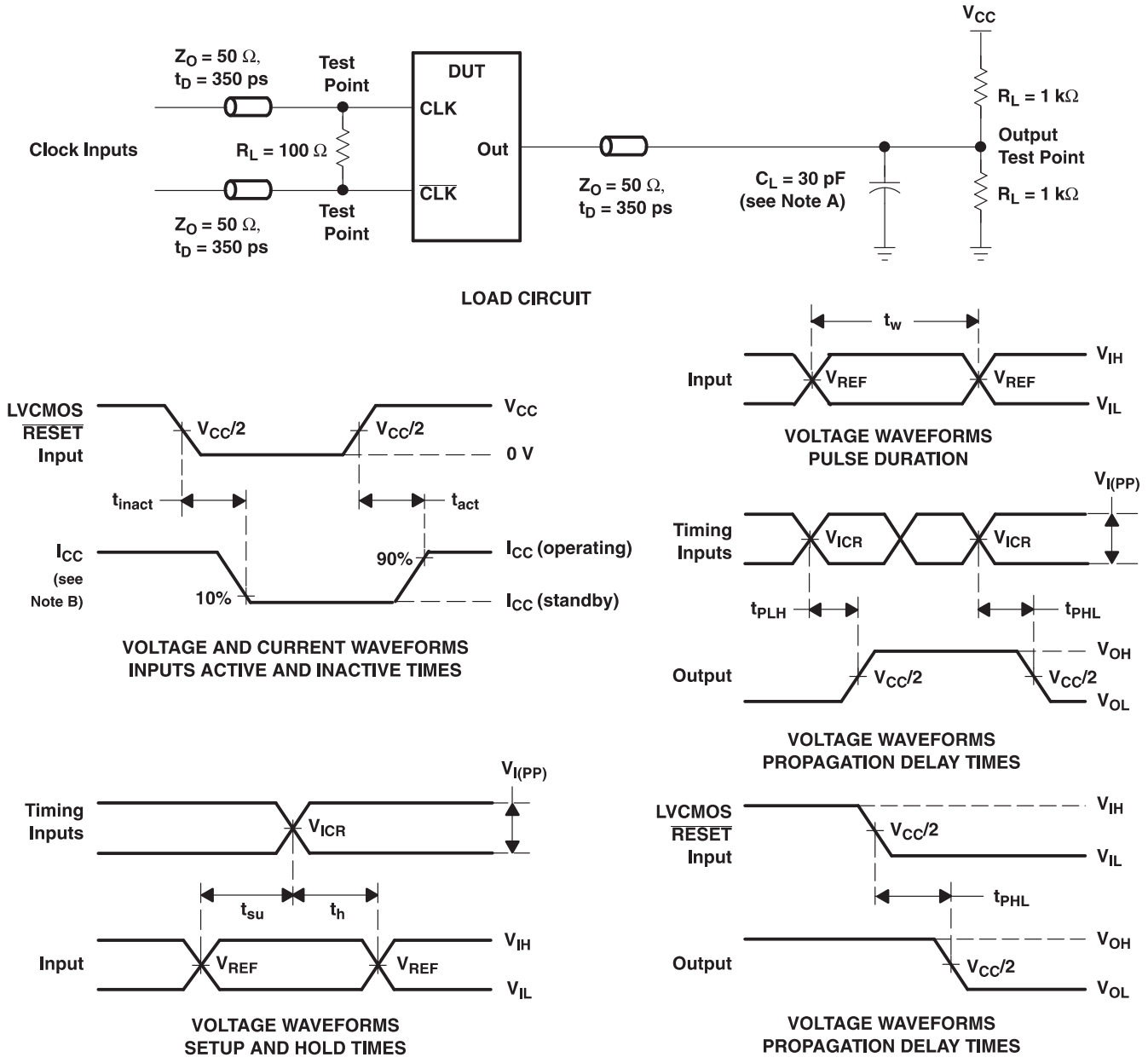


Figure 1. Output Load For Production Test

PROPAGATION DELAY (Design Goal as per JEDEC Specification)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.1 V		UNIT
			MIN	MAX	
t_{pdm} (1)	CLK and $\overline{CLK}$	Q	1.1	1.5	ns
t_{pdmss} (2)	CLK and $\overline{CLK}$	Q		1.6	ns

(1) Includes 350 psi test-load transmission delay line
(2) Includes 350 psi test-load transmission delay line



NOTES:
A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time, with one transition per measurement.
E. $V_{REF} = V_{TT} = V_{CC}/2$
F. $V_{IH} = V_{REF}$ + 250 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. $V_{I(PP)}$ = 600 mV
I. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Data Output Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

The typical values below are for standard raw cards. Test equipment used was the JEDEC register validation board using pattern 0x43, 0x4F, and 0x5A.

Table 1. Raw Card Values (1) (2)

RAW CARD	t_{pdmss}		OVERSHOOT
	MIN	MAX	
A/F	1.2 ns	1.6 ns	140 mV
B/G	1.3 ns	2.0 ns	430 mV
C/H	1.3 ns	2.0 ns	430 mV

(1) All values are valid under nominal conditions and minimum/maximum of typical signals on one typical DIMM.
(2) Measurements include all jitter and ISI effects.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74SSTUB32864NMJR	Active	Production	NFBGA (NMJ) | 96	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	SB864

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

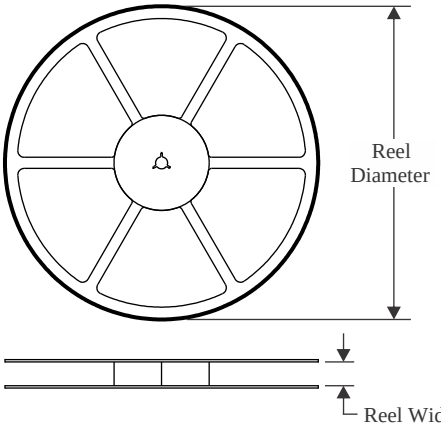
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

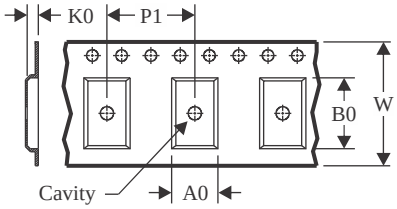
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

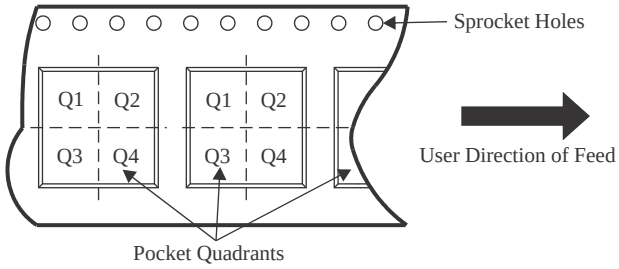


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

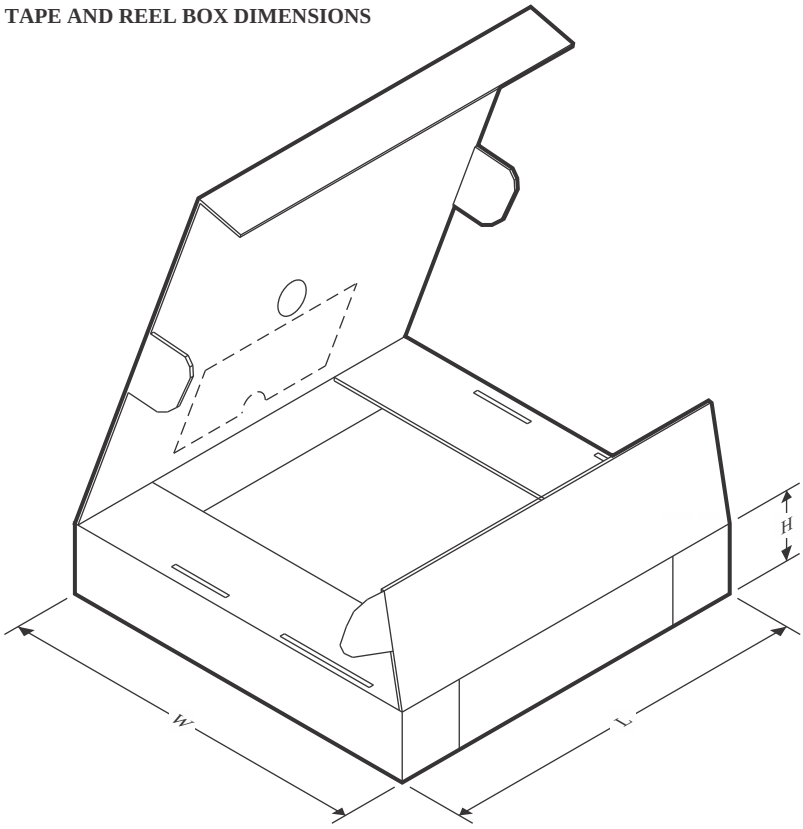
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTUB32864NMJR	NFBGA	NMJ	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

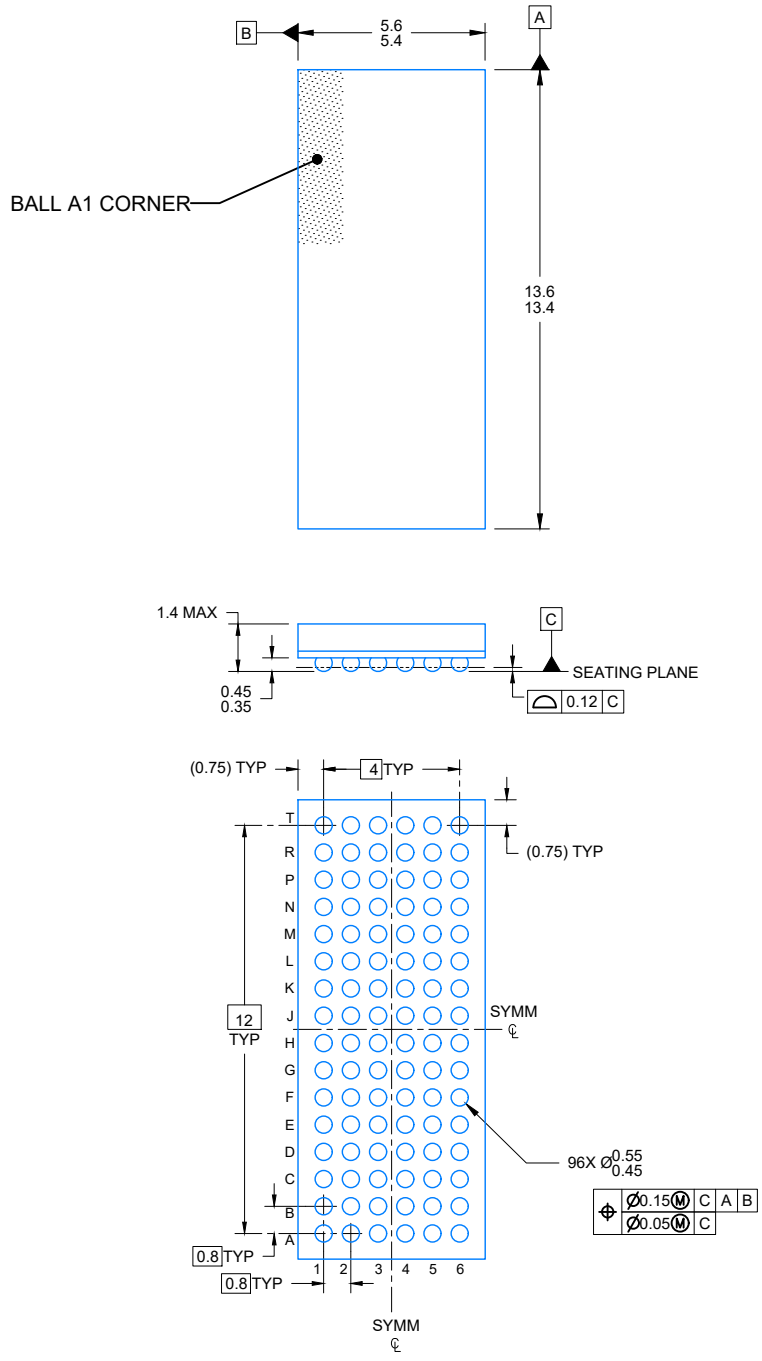
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTUB32864NMJR	NFBGA	NMJ	96	1000	350.0	350.0	43.0

PACKAGE OUTLINE

NMJ0096A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



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NOTES:

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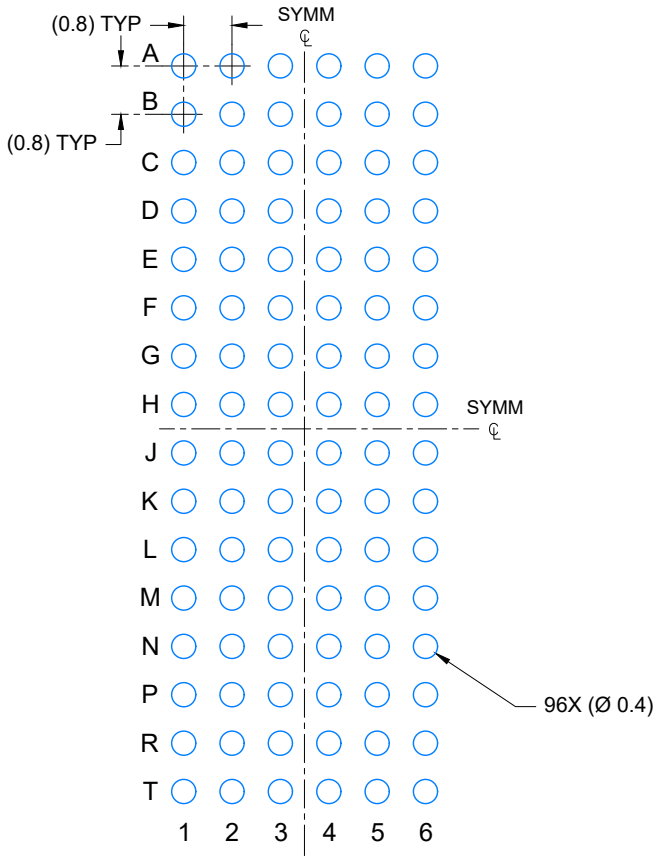
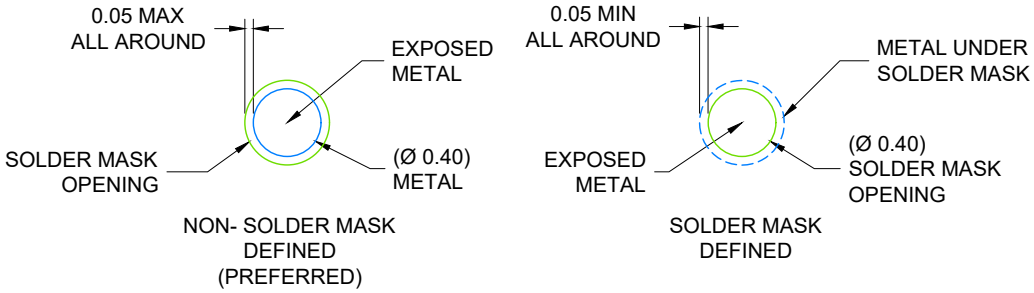
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

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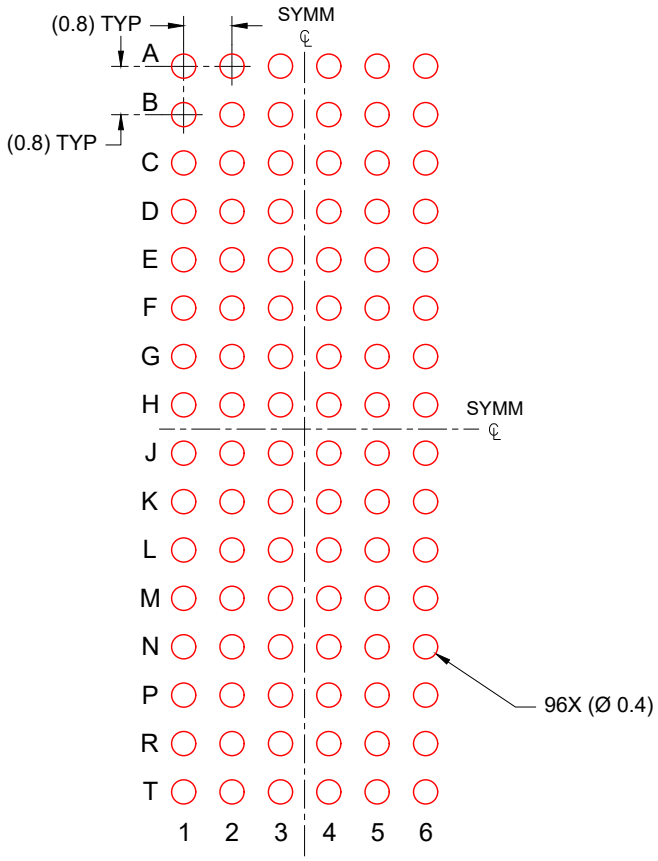
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265