

# MOSFET - Power, Single P-Channel POWERTRENCH® -40 V, -100 A, 4.4 mΩ

## FDD9507L-F085

### Features

- Typical  $R_{DS(on)} = 3.3 \text{ mΩ}$  at  $V_{GS} = -10 \text{ V}$ ,  $I_D = -80 \text{ A}$
- Typical  $G_{g(\text{tot})} = 110 \text{ nC}$  at  $V_{GS} = -10 \text{ V}$ ,  $I_D = -80 \text{ A}$
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	-40	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$I_D$	Drain Current - Continuous, ( $V_{GS} = -10 \text{ V}$ ) $T_C = 25^\circ\text{C}$ (Note 1)	-100	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	(See Figure 4)	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	259	mJ
$P_D$	Power Dissipation	227	W
	Derate Above $25^\circ\text{C}$	1.52	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

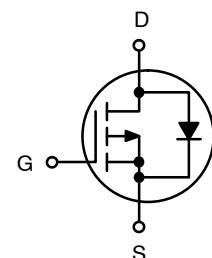
1. Current is limited by bondwire configuration.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.1 \text{ mH}$ ,  $I_{AS} = -72 \text{ A}$ ,  $V_{DD} = -40 \text{ V}$  during inductor charging and  $V_{DD} = 0 \text{ V}$  during time in avalanche.



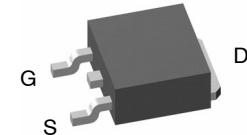
ON Semiconductor®

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$V_{DSS}$	$R_{DS(\text{ON}) \text{ MAX}}$	$I_D \text{ MAX}$
-40 V	4.4 mΩ @ -10 V	-100 A

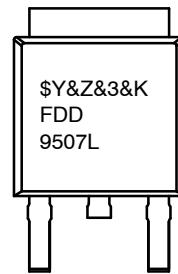


P-CHANNEL MOSFET



DPAK3 (TO-252)  
CASE 369AS

### MARKING DIAGRAM



$\$Y$  = ON Semiconductor Logo  
 $\&Z$  = Assembly Plant Code  
 $\&3$  = Numeric Date Code  
 $\&K$  = Lot Code  
 FDD9507L = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

**THERMAL CHARACTERISTICS**

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.66	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3)	52	

3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

**ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-40	-	-	V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	$V_{DS} = -40 V, V_{GS} = 0 V$ $T_J = 25^\circ C$ $T_J = 175^\circ C$ (Note 4)	-	-	1	$\mu A$
I <sub>GSS</sub>	Gate-to-Source Leakage Current	$V_{GS} = \pm 16 V$	-	-	$\pm 100$	nA

**ON CHARACTERISTICS**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	-1	-2	-3	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5 V, I_D = -80 A, T_J = 25^\circ C$	-	4.9	7.2	$m\Omega$
		$V_{GS} = -10 V, I_D = -80 A$ $T_J = 25^\circ C$ $T_J = 175^\circ C$ (Note 4)	-	3.3	4.4	
			-	5.3	7.1	

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = -20 V, V_{GS} = 0 V, f = 1 MHz$	-	6250	-	pF
$C_{oss}$	Output Capacitance		-	2640	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	61	-	pF
$R_g$	Gate Resistance	$f = 1 MHz$	-	19.3	-	$\Omega$
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 0 V$ to $-10 V, V_{DD} = -20 V, I_D = -80 A$	-	100	130	nC
$Q_{g(-4.5)}$	Total Gate Charge	$V_{GS} = 0 V$ to $-4.5 V, V_{DD} = -20 V, I_D = -80 A$	-	46	-	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 V$ to $-2 V, V_{DD} = -20 V, I_D = -80 A$	-	13	-	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = -20 V, I_D = -80 A$	-	22	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$V_{DD} = -20 V, I_D = -80 A$	-	13	-	nC

**SWITCHING CHARACTERISTICS**

$t_{on}$	Turn-On Time	$V_{DD} = -20 V, I_D = -80 A, V_{GS} = -10 V, R_{GEN} = 6 \Omega$	-	-	21	ns
$t_{d(on)}$	Turn-On Delay		-	10	-	ns
$t_r$	Rise Time		-	6	-	ns
$t_{d(off)}$	Turn-Off Delay		-	400	-	ns
$t_f$	Fall Time		-	132	-	ns
$t_{off}$	Turn-Off Time		-	-	710	ns

**DRAIN-SOURCE DIODE CHARACTERISTICS**

$V_{SD}$	Source to Drain Diode Forward Voltage	$I_{SD} = -80 A, V_{GS} = 0 V$	-	-0.9	-1.3	V
		$I_{SD} = -40 A, V_{GS} = 0 V$	-	-0.85	-1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = -80 A, dI_{SD}/dt = 100 A/\mu s$	-	87	113	ns
$Q_{rr}$	Reverse Recovery Charge		-	115	150	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at  $T_J = 175^\circ C$ . Product is not tested to this condition in production.

## TYPICAL CHARACTERISTICS

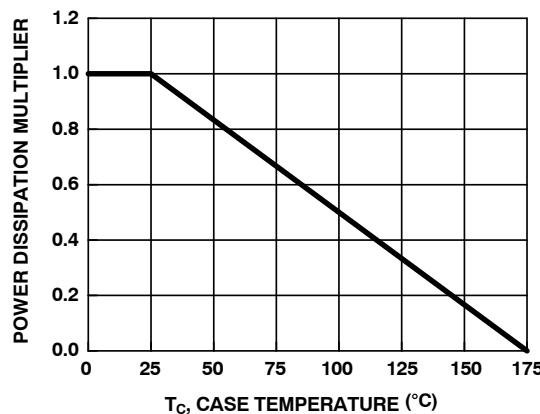


Figure 1. Normalized Power Dissipation vs. Case Temperature

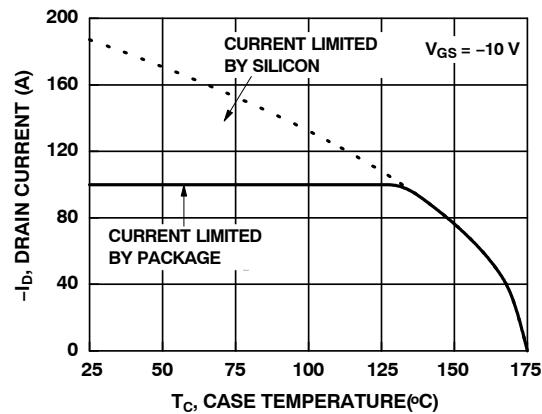


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

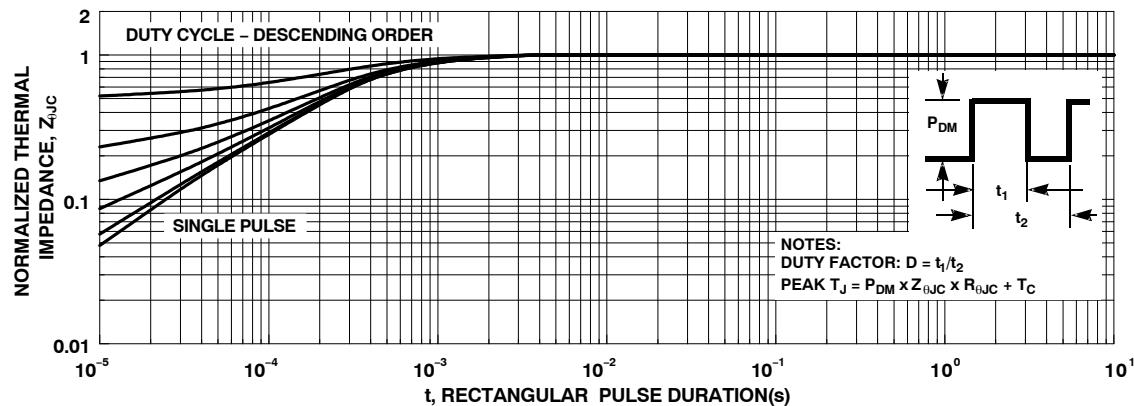


Figure 3. Normalized Maximum Transient Thermal Impedance

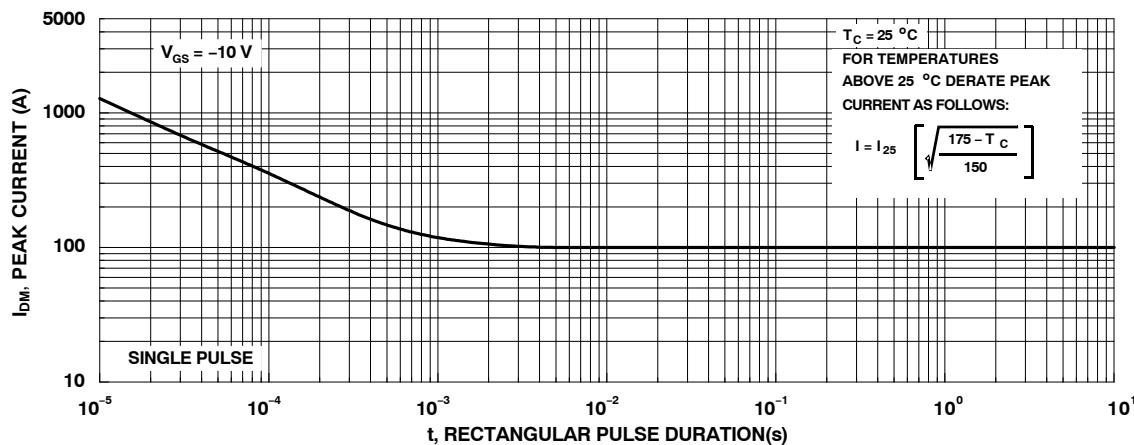


Figure 4. Peak Current Capability

## TYPICAL CHARACTERISTICS

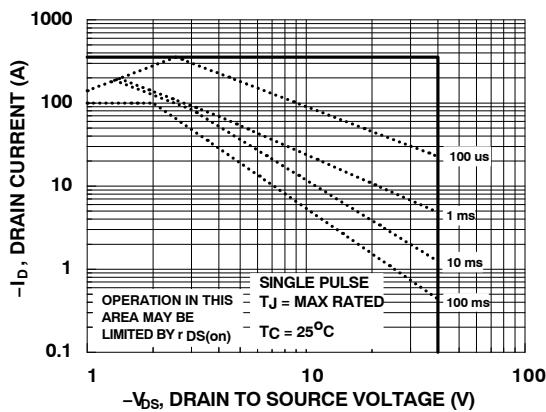


Figure 5. Forward Bias Safe Operating Area

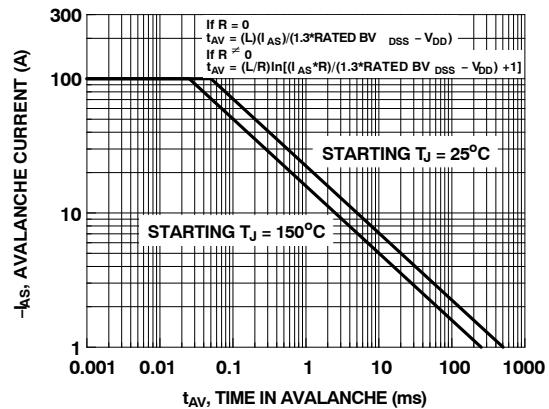


Figure 6. Unclamped Inductive Switching Capability

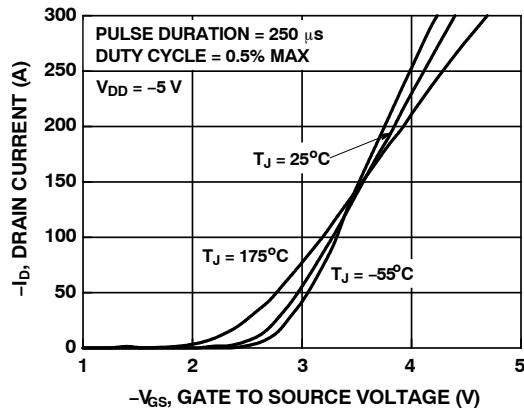


Figure 7. Transfer Characteristics

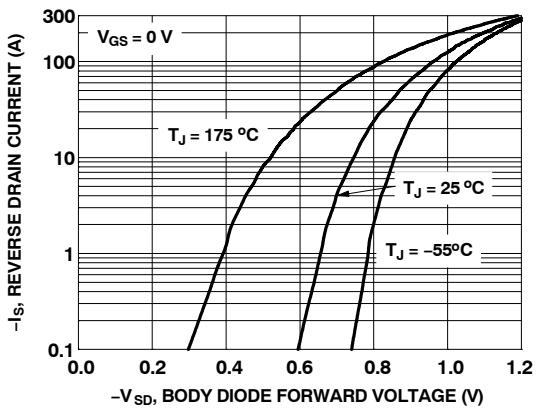


Figure 8. Forward Diode Characteristics

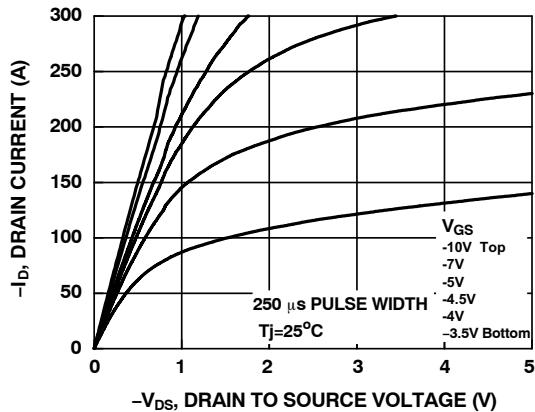


Figure 9. Saturation Characteristics

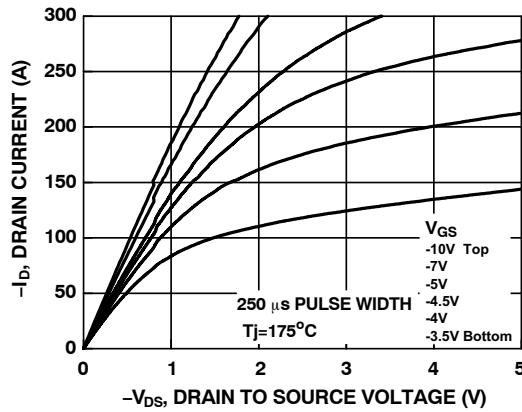


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

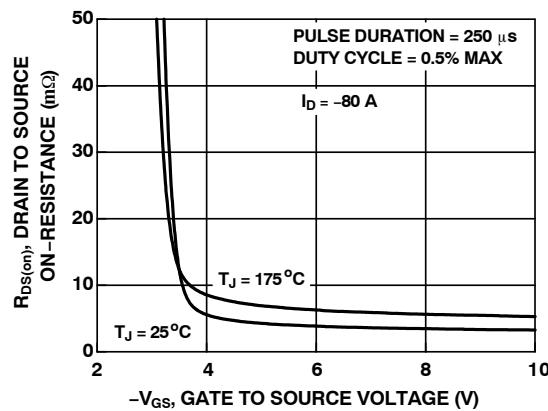


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

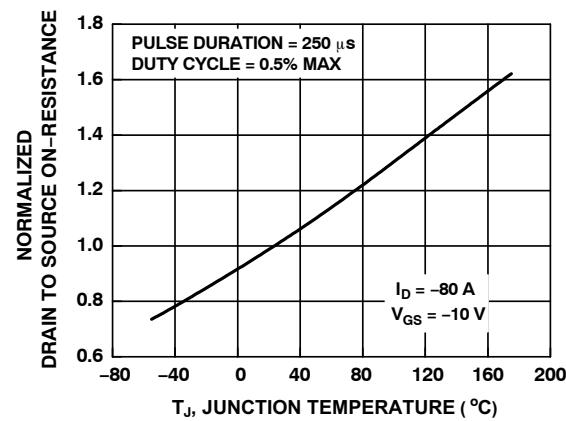


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

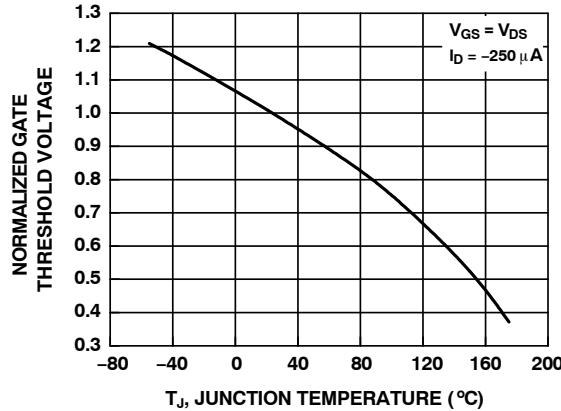


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

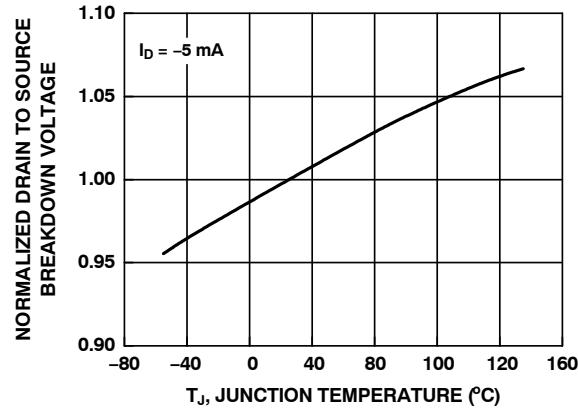


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

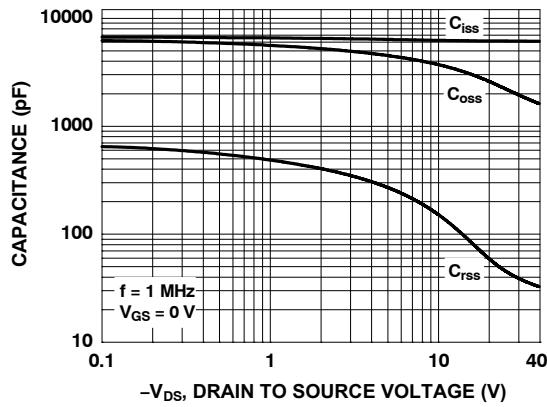


Figure 15. Capacitance vs. Drain to Source Voltage

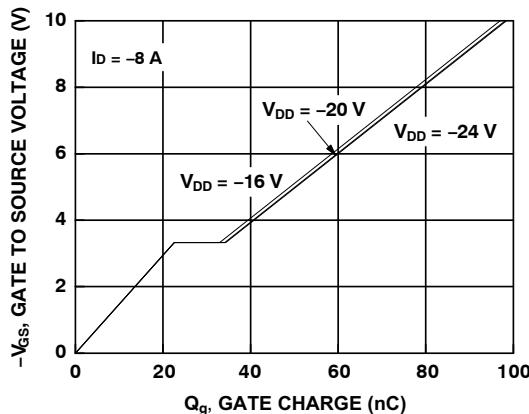
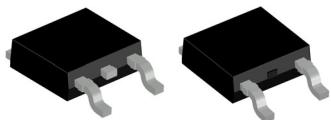


Figure 16. Gate Charge vs. Gate to Source Voltage

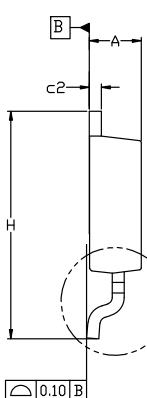
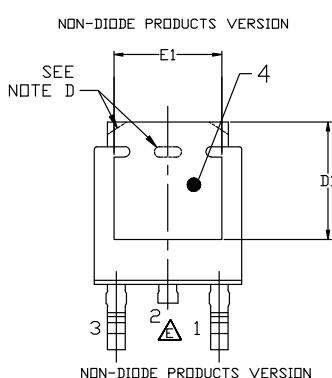
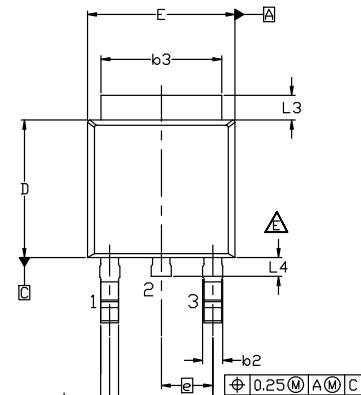
## FDD9507L-F085

### ORDERING INFORMATION

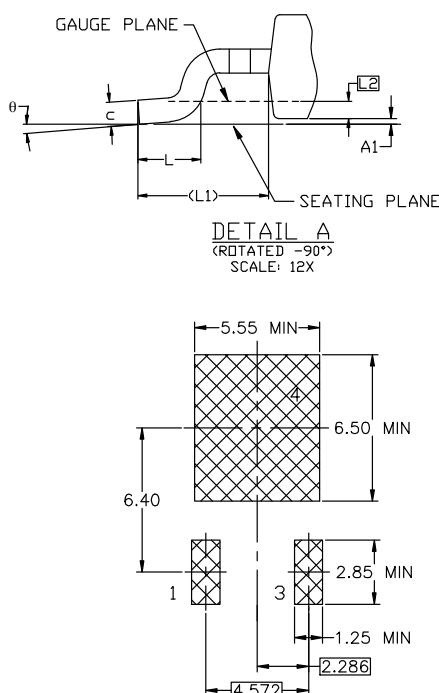
Device	Marking	Package	Reel Size	Tape Width	Quantity
FDD9507L-F085	FDD9507L	DPAK3 (TO-252) (Pb-Free / Halogen Free)	13"	16 mm	2500 Units


**DPAK3 6.10x6.54x2.29, 4.57P**  
CASE 369AS  
ISSUE B

DATE 20 DEC 2023



NOTES: UNLESS OTHERWISE SPECIFIED  
A) THIS PACKAGE CONFORMS TO JEDEC, TD-252,  
ISSUE F, VARIATION AA.  
B) ALL DIMENSIONS ARE IN MILLIMETERS.  
C) DIMENSIONING AND TOLERANCING PER  
ASME Y14.5M-2018.  
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED  
CORNERS OR EDGE PROTRUSION.  
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY  
STUB WITHOUT CENTER LEAD.  
F) DIMENSIONS ARE EXCLUSIVE OF BURRS,  
MOLD FLASH AND TIE BAR EXTRUSIONS.  
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD  
TD228P991X239-3N.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	—	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	—	—
E	6.35	6.54	6.73
E1	4.32	—	—
e	2.286	BSC	
e1	4.572	BSC	
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	1.08	1.27
L4	—	—	1.02
θ	0°	—	10°

## LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

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