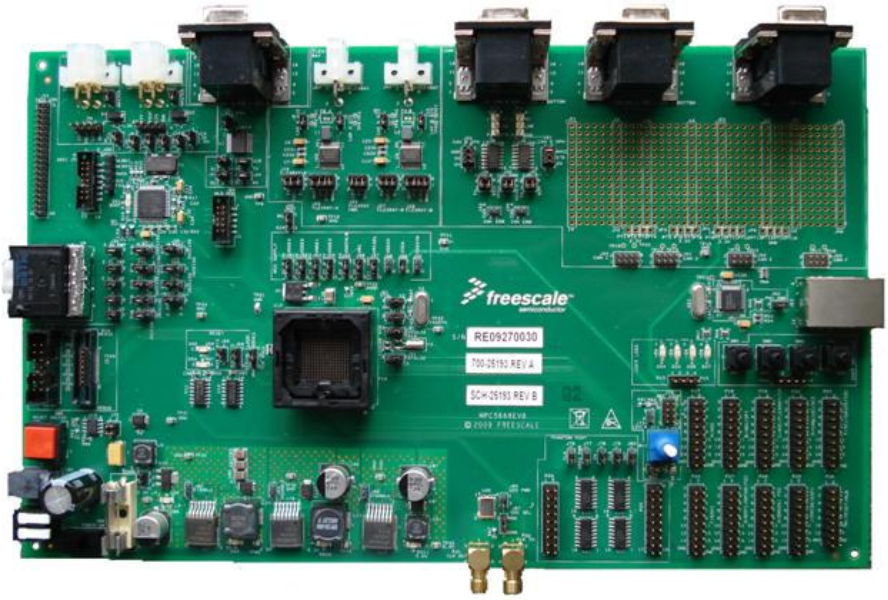


MPC5668EVB Users Manual

Revision 0.1

May 2009

Revision History:

Revision	Date	Author	Comment
0.1	May 2009	D. McMenamin	Initial Release, RevA PCB's only.

INDEX

Index of Figures and Tables

1. Introduction

This user's manual details the setup and configuration of the Freescale Semiconductor MPC5668 Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the MPC5668 family of microprocessors, and to facilitate hardware and software development.

At the time of writing this document, the MPC5668 family is offered in a 208MAPBGA package. A 256MAPBGA package supporting Nexus debug is also available for development purposes. For the latest product information, please speak to your Freescale representative or consult the MPC5668 web pages at www.freescale.com

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

2. EVB Features

The EVB provides the following key features:

- MCU Socket supporting the 208BGA production package and the 256BGA development package.
- Single 12-14V external power supply input with on-board regulators to provide all of the necessary EVB and MCU voltages. Power may be supplied to the EVB via a 2.1mm barrel style power jack or a 2-way level connector. 12V operation allows in-car use if desired.
- Flexible on-board power supply configuration with the option to bypass the internal MCU regulators if desired.
- Master power switch and regulator status LED's – Regulators connected to the ADC to allow monitoring.
- User reset switch with reset status LED's
- User configurable Low Voltage Inhibit to monitor the status of the 3.3V and 5V regulators.
- Control of the BOOTCFG status via a dedicated jumper.
- Flexible MCU clocking options:
  - 40MHz Oscillator Crystal
  - 32Khz Watch Crystal
  - SMA connector to allow external clock support
  - 8Mhz Oscillator circuit.
- SMA connector on MCU-CLKOUT signal for easy access.
- Standard 14-pin ONCE debug connector and 38-pin MICTOR Nexus connectors.
- All MCU signals are accessible on port-ordered groups of 0.1" pitch headers.
- DSPI A signals can be routed to a set of shift registers to allow a 32-bit phantom port to be created.
- SCI channels A and B can be routed to a standard DB9 female connector (PC RS-232 compliant) via a Maxim physical interface.
- SCI channels C and D can be routed to LIN interface header (0.1") and molex connectors, both will full physical transceivers.
- FlexCAN channels A and B can be routed to 0.1" headers and DB9 connector via a Philips high speed CAN transceiver which supports both 3.3V and 5V inputs.
- FlexCAN channels C, D, E and F are routed to the prototyping area with DB9 connectors to allow additions CAN physical interfaces to be easily integrated.
- User prototyping area consisting of a 0,1" grid of through hole pads with easy access to the EVB ground and power supply rails.
- Ethernet signals routed to a National Semiconductor physical interface and Pulsejack RJ45 connector with integrated magnetics.
- MLB signals routed to SMSC MOST INIC with Tyco Optical Transceiver. INIC JTAG and MLB monitor ports. Support for optional ROM INIC or MLB150 daughter card from SMSC.
- 4 active low LED's and 4 pushbutton switches for development purposes.
- Jumper selectable variable resistor connected to ADC channel 0, driving between VRH and VRL.
- Liberal scattering of GND test points (surface mount loops) placed throughout the EVB.

Note – To alleviate confusion between jumpers and headers, all EVB jumpers are implemented as 2mm pitch whereas headers are 0.1inch (2.54mm). This prevents inadvertently fitting a jumper to a header.

IMPORTANT

Before the EVB is used or power is applied, please fully read the following sections on how to correctly configure the board.

Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.

3. Configuration

This section details the configuration of each of the EVB functional blocks.

Throughout this document, all of the default jumper and switch settings are clearly marked with "**(D)**" and are shown in blue text. This should allow a more rapid return to the default state of the EVB if required. Note that the default configuration for 3-way jumpers is a header fitted between pins 1 and 2. On the EVB, 2-way and 3-way jumpers have been aligned such that Pin 1 is either to the top or to the left of the jumper. On 2-way jumpers, the source of the signal is connected to Pin 1.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

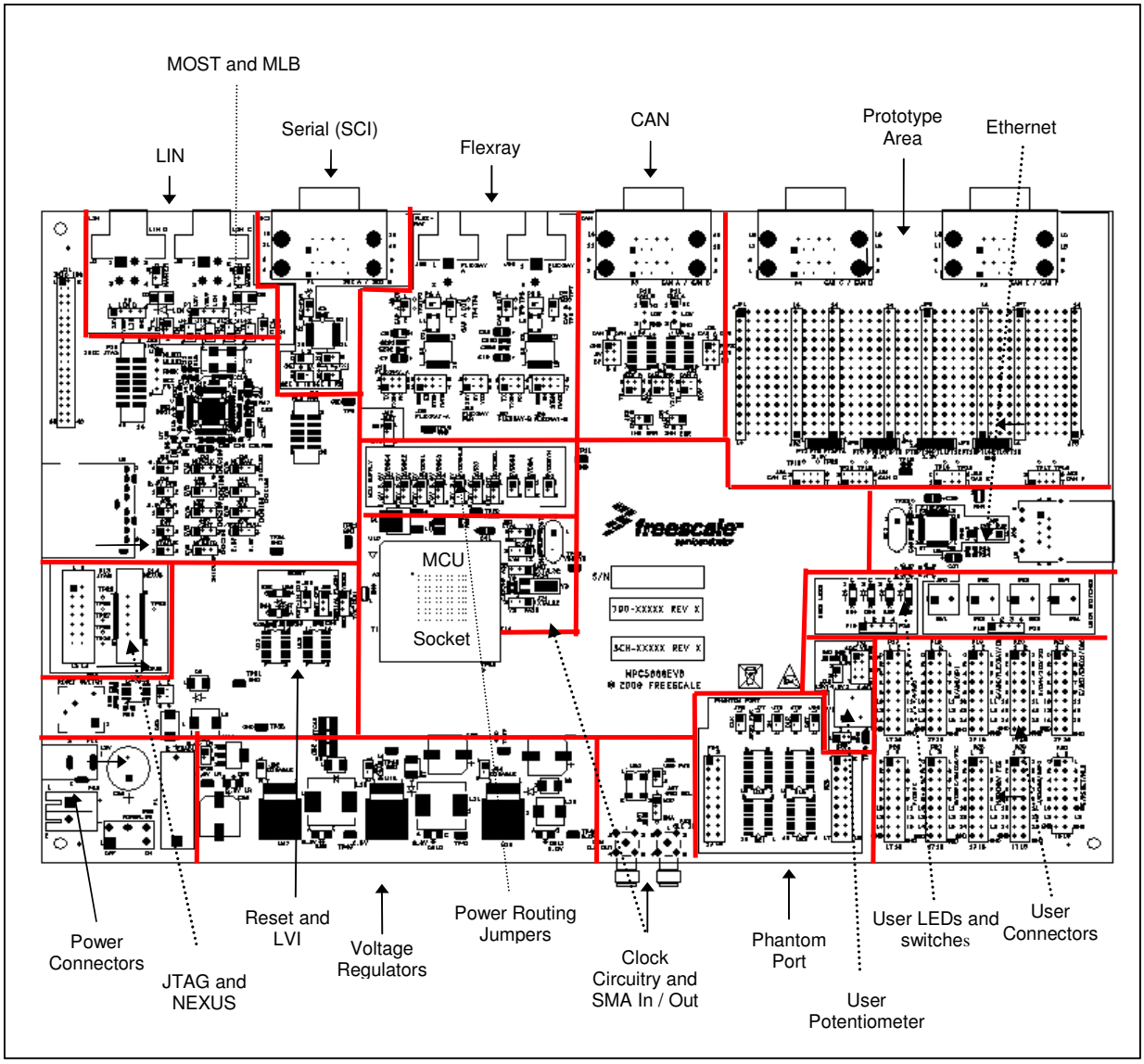
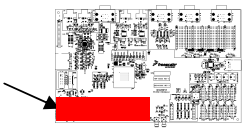


Figure 3-1 EVB Functional Blocks

3.1 Power Supply Configuration

The Power supply section is located in the bottom left area of the EVB



The EVB requires an external power supply voltage of 12V DC, minimum 1A. This allows the EVB to be easily used in a vehicle if required. The single input voltage is regulated on-board using 3 switching and 1 linear regulators to provide the necessary EVB and MCU operating voltages of 5.0V, 3.3V and 2.5V. For flexibility there are two different power supply input connectors on the EVB as detailed below.

3.1.1 Power Supply Connectors

2.1mm Barrel Connector – P22:

This connector should be used to connect the supplied wall-plug mains adapter. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1mm plug uses the correct polarisation as shown below:

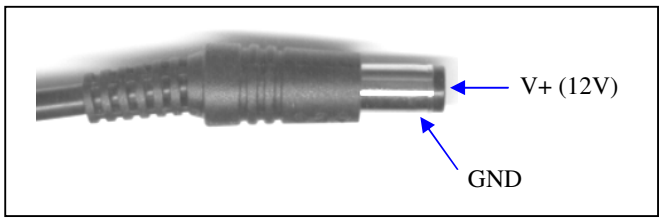


Figure 3-2 2.1mm Power Connector

2-Way Lever Connector – P23:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

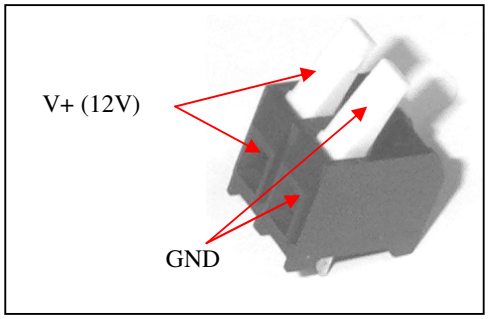


Figure 3-3 2-Lever Power Connector

3.1.2 Power Switch (SW6)

Slide switch SW6 can be used to isolate the power supply input from the EVB voltage regulators if required.

Moving the slide switch to the **right** (away from connector P23) will turn the EVB **on**.
Moving the slide switch to the **left** (towards connector P23) will turn the EVB **off**.

3.1.3 Regulator Power Jumpers (J42, J44, J45 and J46)

The Power supply control jumpers are located adjacent to the respective regulators.

As mentioned above, the EVB has four voltage regulators on board:

- 2.5V switching regulator (U17) to supply the MCU MLB Pads voltage and the SMSC INIC (U6).
- 3.3V switching regulator (U18) for EVB peripherals and MCU regulator, logic and I/O.
- 5.0V switching regulator (U19) for the MCU regulator and I/O and EVB peripherals.
- 5.0V linear regulator (U14) for the MCU ADC power supply.

All of the regulators have the option of being disabled if they are not required. The table below details the jumper configurations for enabling and disabling the regulators. By default, all of the regulators are enabled.

Table 3-1 Regulator Power Jumpers

Jumper	Position	PCB Legend	Description
J81 (2.5V)	FITTED REMOVED **(D)**	DISABLE	2.5V switching regulator output is Disabled 2.5V switching regulator output is Enabled
J82 (3.3V)	FITTED REMOVED **(D)**	DISABLE	3.3V switching regulator output is Disabled 3.3V switching regulator output is Enabled
J83 (5.0V)	FITTED REMOVED **(D)**	DISABLE	5.0V switching regulator output is Disabled 5.0V switching regulator output is Enabled
J84 (5.0V-LINEAR)	FITTED **(D)** REMOVED	ENABLE	5.0V linear regulator output is Enabled 5.0V linear regulator output is Disabled

3.1.4 Power Status LED's and Fuse

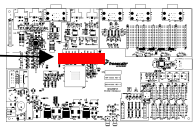
When power is applied to the EVB, four green power LED's adjacent to the voltage regulators show the presence of the supply voltages as follows:

LED DS8 – Indicates that the 5.0V linear regulator is enabled and working correctly
LED DS9 – Indicates that the 1.5V switching regulator is enabled and working correctly
LED DS10 – Indicates that the 3.3V switching regulator is enabled and working correctly
LED DS11 – Indicates that the 5.0V switching regulator is enabled and working correctly

If no LED's are illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW6 is in the "OFF" position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the bias of your power supply connection then replace fuse F1 with a 20mm 500mA fast blow fuse.

3.1.5 MCU Supply Routing and Jumpers (J41, J42, J43, J44, J45, J46, J47, J48, J49, J50)

The MCU power supply jumpers are located in the centre of the EVB in a box titled "MCU Supply"



The MCU can be operated in 5v and 3.3v modes by changing J46. When in 5v mode MCU has internal regulators that can generate the 3.3V supplies for VDDSYN and VDD33. Whilst this is the intended mode of operation for the MCU when VRC = 5v the EVB allows the internal MCU regulators to be disabled by changing VRCSEL to EXT and applying external voltages to the VDDSYN and VDD33 inputs. When in 3.3v mode VDDSYN and VDD33 inputs must always be supplied externally.

The VDDE[1..4] pins control the pad voltages over 4 groupings of pads (see the MCU reference manual for details). Jumpers J41 - J34 allow the VDDEx pins to be connected to the 5.0v or 3.3V switching regulators. The VDDEMLB domain can be 3.3v or 2.5v selectable by J45.

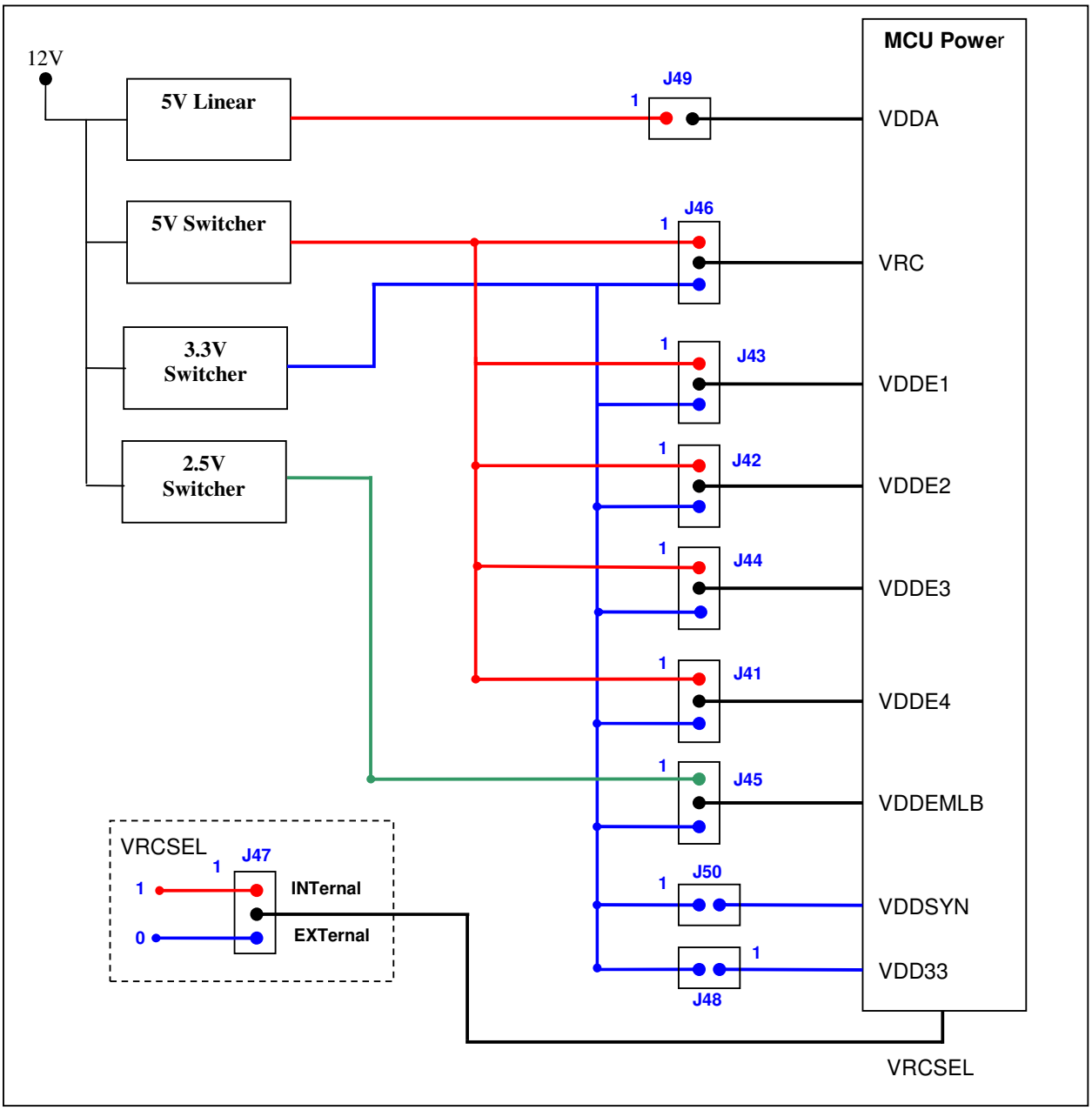


Figure 3-4. Power Supply Routing

Table 3-2 MCU Power Supply Jumpers

Power Domain	Jumper	Position	PCB Legend	Description
5.0V	**J49 (VDDA)**	FITTED **(D)**		MCU VDDA is powered from 5V linear regulator
		REMOVED		MCU VDDA User powered from J49 Pin 2
5.0V / 3.3V	**J46 (VRC)**	1-2 **(D)**	5V	VRC is supplied from the 5V switching regulator
		2-3	3.3v	VRC is supplied from the 3.3V switching regulator
	J47 (VRCSEL)	1-2 **(D)**	INT	3.3 V internal voltage regulator enabled (5 V mode)
		2-3	EXT	3.3 V supplied external (3.3 V mode)
	J43 (VDDE1)	1-2 **(D)**	5.0v	MCU VDDE1 is powered from 5v
		2-3	3.3V	MCU VDDE1 is powered from 3.3V
	J42 (VDDE2)	1-2 **(D)**	5.0v	MCU VDDE2 is powered from 5v
		2-3	3.3V	MCU VDDE2 is powered from 3.3V
	J44 (VDDE3)	1-2 **(D)**	5.0v	MCU VDDE3 is powered from 5v
		2-3	3.3V	MCU VDDE3 is powered from 3.3V
	J41 (VDDE4)	1-2 **(D)**	5.0v	MCU VDDE4 is powered from 5v
		2-3	3.3V	MCU VDDE4 is powered from 3.3V
3.3V	**J48 (VDD33)**	FITTED		MCU VDD33 pin is powered from switching regulator
		REMOVED **(D)**		MCU VDD33 pin is not powered externally
	J50 (VDDSYN)	FITTED		MCU VDDSYN pin is powered from switching regulator
		REMOVED **(D)**		MCU VDDSYN pin is not powered externally
3.3v/ 2.5V	**J45 (VDDEMLB)**	1-2 **(D)**	2.5V	MCU VDD pin is powered from 1.5v switching regulator
		2-3	3.3V	MCU VDD pin is not powered externally

The jumper configuration shown in Table 3-2, details the default state of the EVB. In this configuration all power is supplied from the Linear and Switching regulators.

- VDDA is connected to the 5.0V Linear regulator
- VRC is connected to the 5.0V switching regulator
- VRCSEL is connected to logic 1 enabling the internal 3.3V regulator – J48 and J50 are removed.
- VDDE[1..4] are connected to the 5.0V switching regulator

CAUTION

*When jumper J47 (VRCSEL) is in position 1-2 (INT), the MCU's 3.3V internal voltage regulators are enabled and supply power to the 3.3V power domains. In this case, jumpers J48 (VDD33) and J50 (VDDSYN) **must** be removed.*

Similarly, when jumper J47 is removed, no power is supplied to the MCU internal voltage regulators and jumpers J48 (VDD33) and J50 (VDDSYN) must be fitted to power the respective MCU pins. The 3.3V regulator must also be enabled in this case.

3.1.5.1 Changing VDDE[1..4] Voltage

Before changing the VDDEx voltage from the default 5.0V setting, you need to ensure that this will not impact any of the EVB peripherals that you are using. The table below details what EVB peripherals are tied to a particular VDDEx grouping and also the MCU pin operating voltage suitable for that peripheral.

Table 3-3 VDDE[1..3] Pad Groupings

Item	Port Pins	VDDE Group	Required Pad Voltage
Ethernet	Port G and H	VDDE3	3.3V
CANA and CANB	Port D	VDDE2	5.0V or 3.3V
SCI A and B	Port D	VDDE2	5.0V or 3.3v
LIN C and D	Port E	VDDE2	5.0V or 3.3v
FlexRay	Port K	VDDE2	5.0V or 3.3V
JTAG	Dedicated JTAG	VDDE2	5.0V or 3.3V
Nexus	Custom Domain	VDDENEX	3.3V

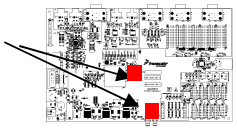
3.1.6 Regulator Power Domains

Before disabling any of the EVB regulators, it is worthwhile considering if any of the EVB components or peripherals you require will be affected. Table 3-4 details a list of the various EVB components and peripherals powered by the regulators.

Table 3-4 Power Supply Distribution

Regulator	Used On
2.5V (Switcher)	MCU VDDEMLB pins MLB INIC 1.5V Power section of Prototype area
3.3V (Switcher)	MCU VDD33 and VDDSYN pins (ONLY use when on-chip MCU regulator is disabled) MCU VDDEx pins (when run in 3.3v mode) Oscillator Module (U20) MLB INIC RS-232 Transceiver (VDDE2 dependant) LIN transceiver (VDDE2 dependant) I/O supply for Flexray interface when VIO is 3.3V LVI circuitry 3.3V Power section of Prototype area
5.0V (Switcher)	MCU VDDEx (5v mode), VPP and VDDR pins LVI circuit main power (affecting Reset Switch) Reset-In / Reset-Out logic Reset configuration circuitry User LED's and Switches. RS-232 Transceiver (VDDE2 dependant) LIN transceiver (VDDE2 dependant) CAN transceivers FlexRay transceivers 5.0V Power section of Prototype area JTAG and Nexus connectors
5.0V (Linear)	MCU VDDA pin LVI circuit monitor

The MCU clock control jumpers are located close to crystal oscillator modules.



3.2 MCU Clock Control

3.2.1 Main Clock Selection (J85, J87, J61 and J66)

The EVB supports three possible MCU clock sources:

(1) The local 40MHz ALC pierce oscillator circuit
(2) An oscillator module on the EVB (U20), driving the MCU EXTAL signal
(3) An external clock input to the EVB via the SMA connector (P32), driving the MCU EXTAL signal

The clock circuitry is shown in the diagram below. Please refer to the appropriate daughter card user manual for specific jumper numbers and circuitry.

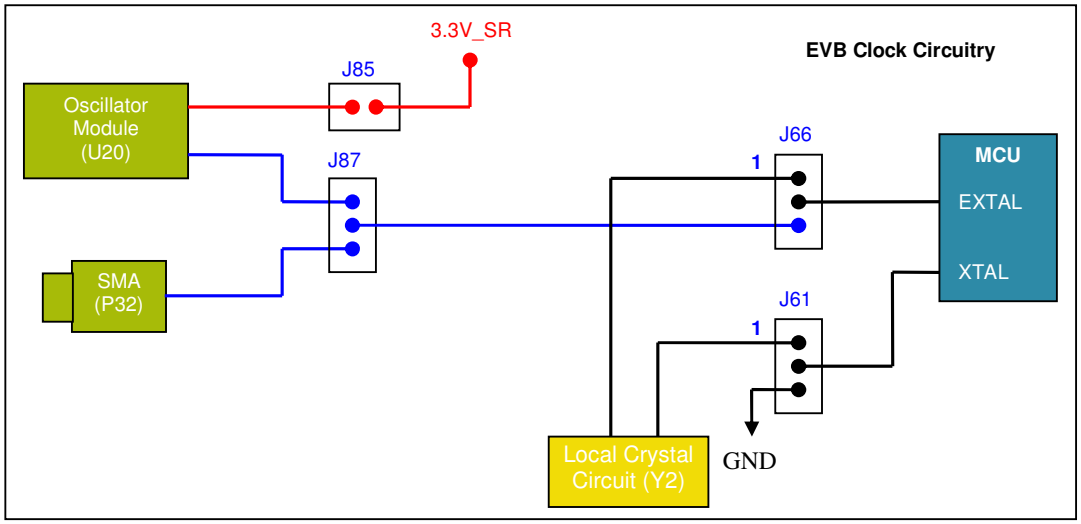


Figure 3-5 EVB Clock Selection

Table 3-5 Clock Source Jumper Selection

Jumper	Position	PCB Legend	Description
J85 (U20 PWR)	FITTED **(D)** REMOVED		EVB oscillator module U20 is powered EVB oscillator module U20 is not powered
J87 (OSC SEL)	1-2 **(D)** 2-3	MOD SMA	Daughter card EXT-CLK is routed from U20 Daughter card EXT-CLK is routed from P32 SMA Connector
J66 **Must Match J61**	1-2 **(D)**	Y2	MCU Clock is Y2
	2-3	GND	MCU Clock is Selected by J87
J61 **Must Match J66**	1-2 **(D)**	Y2	MCU Clock is Y2
	2-3	EVB	MCU Clock is Selected by J87

Note that the 3.3V regulator must be enabled when using oscillator module Y1.

CAUTION

The MPC5668 clock circuitry is all 3.3v based. Any external clock signal driven into the SMA connector must have a maximum voltage of 3.3V.

3.2.2 32Khz External Clock Selection (J67 and J71)

The EVB also supports an external 32KHz watch crystal that can be used as a timing source within the MCU. The 32Khz crystal can be optionally connected to PA[14] and PA[15] of the MCU. When using the 32KHz crystal PA[14] and PA[15] will not be visible on P17 Port A header.

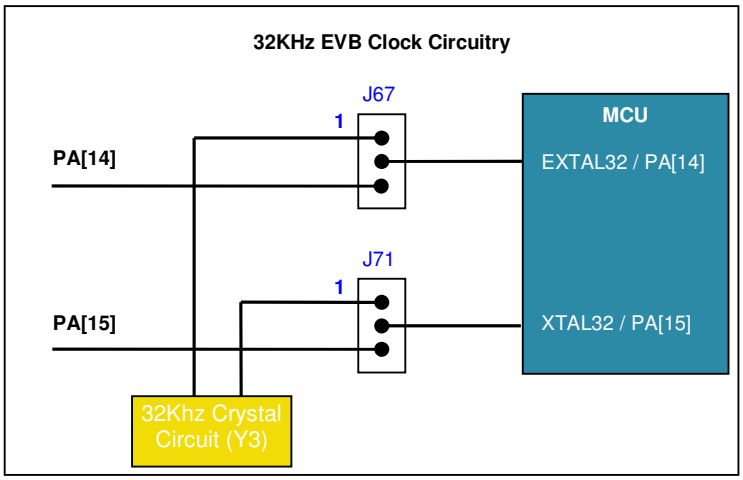


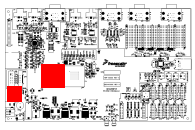
Figure 3-6 EVB Clock Selection

Table 3-6 32Khz Crystal Jumper Selection

Jumper	Position	PCB Legend	Description
J67 **Must Match J71**	1-2 **(D)** 2-3	Y3 PA[14]	32Khz Crystal (Y2) is connected to MCU Pin functions as Normal I/O
J71 **Must Match J67**	1-2 **(D)** 2-3	Y3 PA[15]	32Khz Crystal (Y2) is connected to MCU Pin functions as Normal I/O

3.3 Reset Control (Jumper J75)

The RESET switch (RED) and LVI circuitry is located to the t left of the MCU in the area titled "RESET "



The EVB incorporates an LVI (Low Voltage Inhibit) device to provide under-voltage protection for the two main switching regulators (5v and 3.3v). When either of these regulator voltages drops below a certain threshold level, the LVI will assert the MCU reset line to prevent incorrect operation of the MCU (or EVB circuitry).

The table below shows the approximate threshold voltages for each regulator

Table 3-7 LVI Monitor Threshold Voltages

Regulator	Minimum Voltage Before MCU reset
5.0V Switcher	1.47V
3.3V Switcher	1.47V

The LVI is powered from the 5.0V switching regulator and monitors the 3.3V regulator using a 2nd power fail monitor circuit. The LVI also provides a de-bounced input for EVB reset switch SW5.

Jumpers are provided to disable either the main LVI reset out (which affects the reset from the 5.0V switching regulator and from the reset switch) or the power fail out circuit (which only affects the reset from the 3.3V regulator). If the 5v regulator LVI is disabled, the reset switch will not function.

Table 3-8 LVI Control Jumpers

Jumper	Position	PCB Legend	Description
J75 Posn 1-2	FITTED **(D)**		5.0V switching regulator is monitored, Reset switch active
	REMOVED		5.0V switching regulator is not monitored, Reset switch inactive
J75 Posn 3-4	FITTED **(D)**		3.3V switching regulator is monitored
	REMOVED		3.3V switching regulator is not monitored

Notes:

- *If the 5.0V switching regulator is disabled for any reason, the LVI circuit will attempt to assert the MCU Reset signal. Jumper shunts on jumper J20 position 1-2 and 3-4 must be removed in this situation. This will also leave the reset switch SW5 inoperative.*
- *If the 3.3V regulator is disabled, the shunt on jumper J20 position 3-4 must be removed to prevent the LVI asserting reset.*

3.3.1 Reset LEDs

There are two reset LED's, DS2 (AMBER) and DS3 (RED), placed adjacent to the EVB RESET switch to indicate the RESET status of the EVB and MCU.

LED DS3, titled "RST", will illuminate if the MCU itself issues a reset. In this condition, LED DS2 will not illuminate.

LED DS2, titled "USR", will illuminate when one of the following external hardware devices issues a reset to the MCU:

- LVI circuitry (either an under-voltage detection or the reset switch is being pressed)
- There is a reset being asserted from the user connectors or from the daughter card
- There is a reset being driven from the Nexus or JTAG debug probe

Note that LED DS3 (MCU Reset) will also illuminate during an external (user) reset!

3.3.2 Reset Buffering Scheme

The MPC5668 family has a single reset pin. This single pin functions as a dual purpose input / output signal, providing Reset-In and Reset-Out functionality.

There is a lot of circuitry on the EVB that has access to the reset pin. In order to reduce the loading on the pin (when the MCU is diving the reset signal) and also to allow connection of non open-drain reset inputs, a reset-in and reset-out buffering scheme is implemented as shown in Figure 3-7.

Reset-In - There are 3 possible external sources of reset:
- JTAG / Nexus connector reset
- User reset (from user connectors)
- LVI reset circuitry, including the reset switch.

Each of these reset sources is fed into the input of an AND gate and then converted to an open-drain output which is directly connected to the MCU reset pin.

Reset-Out - The MCU reset pin is buffered to provide a reset-out signal, capable of driving the reset LED and also multiple devices requiring a reset input.

The reset buffering scheme is detailed below:

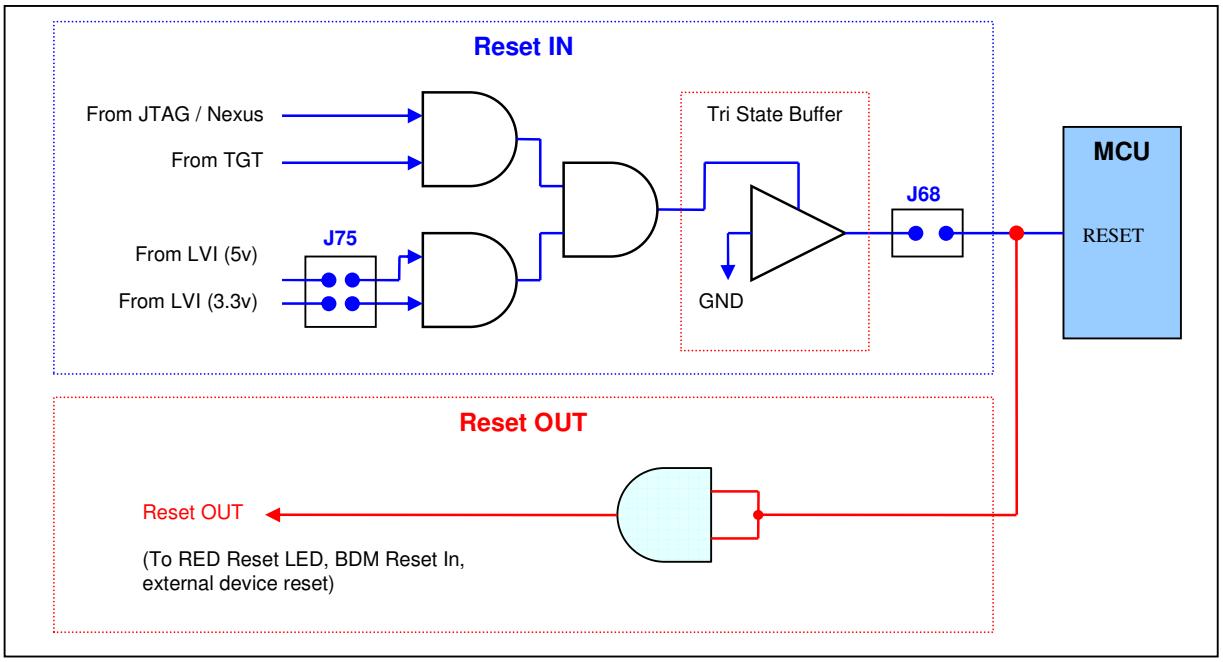


Figure 3-7 EVB Reset Buffering Scheme

Jumper J17 is used to completely disconnect the reset-in buffering if desired. This is for debug purposes only and should normally be left connected. Disconnecting this jumper will mean no external MCU reset can be achieved

Table 3-9 Reset-Out Control Jumper

Jumper	Position	PCB Legend	Description
J68 (RST-IN)	FITTED **(D)**		External reset source (LVI, Debug or Target) will be able to assert MCU reset
	REMOVED		External reset is disabled (Not recommended)

3.3.3 Reset Boot Configuration (J69)

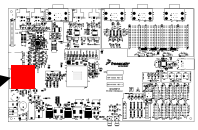
The MPC5668 has a single boot configuration pin (BOOTCFG) which determines the boot location of the MCU based on the state of the pin at POR (Power On Reset). This is shown in the table below:

Table 3-10 BOOTCFG Control

Jumper	Position	PCB Legend	Description
J69 (BOOT CFG)	1-2 **(D)** 2-3	FLASH SERIAL	MCU boots from internal flash MCU boots from external serial source

3.4 ONCE and Nexus Configuration (J32, J70)

The ONCE and NEXUS connectors are located at the left hand edge of the EVB



The EVB supports a standard ONCE cable with a 14-pin 0.1" walled header footprint. There is also a 38-pin MICTOR connector for Nexus debug. Nexus debug is only supported when using a 256MAPBGA MPC5668.

There are two generic jumpers associated with both the ONCE and Nexus, as detailed below

Some debug probes have the ability to assert and also monitor the state of the MCU reset line. This is not possible when the reset signal is buffered so a jumper (J32) is included to allow routing the debug reset signal direct to the MCU reset pin or via the EVB Reset-In buffering.

Table 3-11 JTAG / NEXUS Target Reset Routing

Jumper	Position	PCB Legend	Description
J32 (JRST)	1-2 **(D)** 2-3	BUF DIR	JTAG reset signal is buffered to MCU RESET pin (connected to the MCU Reset-In circuitry) JTAG reset signal is connected direct to MCU RESET pin

Some debug manufacturers specify whether the debug TCLK signal is pulled low or high. Jumper J70 provides the ability to select whether TCLK is pulled to GND or VDDE2. For low power operation, TCLK should be pulled to GND.

Table 3-12 ONCE / NEXUS TCLK Termination Control

Jumper	Position	PCB Legend	Description
J70 (TCLK PULL)	1-2 **(D)** 2-3	VDDE2 GND	JTAG / NEXUS TCLK signal is pulled to VDDE2 via 10KΩ JTAG / NEXUS TCLK signal is pulled to GND via 10KΩ

Note – J70 is located to the right of the reset LED's, out-with the ONCE / Nexus connector area.

3.4.1 Debug Connector Pinouts

The EVB is fitted with 14-pin JTAG / ONCE and 38-pin Nexus debug connectors. The following diagram shows the 14-pin JTAG / ONCE connector pinout (0.1” keyed header).

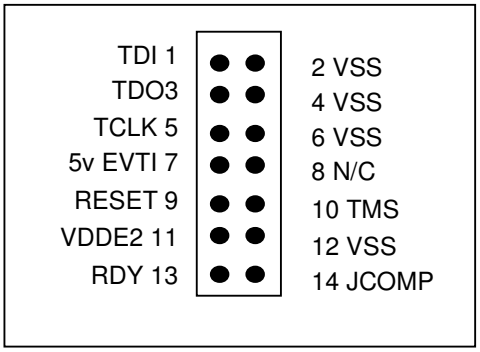


Figure 3-8. MPC5668 JTAG / ONCE Connector

The Nexus module used on the MPC5668 family uses the JTAG pins (for control of the Nexus block) along with additional Nexus pins for trace messages. Nexus mode is entered by a JTAG sequence whereby the Nexus EVTI pin is sampled on the rising edge of the JTAG TRST pin. If the EVTI is asserted on TRST, Nexus is enabled.

The table below shows the pinout of the 38-pin MICTOR Nexus connector for the MPC5668

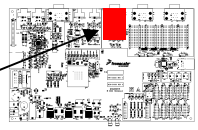
Table 3-13. NEXUS Debug Connector Pinout

Pin No	Function	Connection		Pin No	Function	Connection
1	Reserved	---		2	Reserved	---
3	Reserved	---		4	Reserved	---
5	MDO[9]	MCU M5		6	CLKOUT	MCU PK9
7	Vendor I/O-2	TP25		8	MDO[8]	MCU L5
9	Reset-In	Reset CCT		10	EVTI	MCU M11
11	TDO	MCU M3		12	VREF	3.3V Reg
13	MDO[10]	MCU M6		14	RDY	TP29
15	TCLK	MCU P3		16	MDO[7]	MCU K5
17	TMS	MCU L3		18	MDO[6]	MCU J5
19	TDI	MCU J3		20	MDO[5]	MCU J6
21	TRST	JCOMP		22	MDO[4]	MCU H6
23	MDO[11]	MCU M7		24	MDO[3]	MCU H5
25	Tool I/O-3	TP26		26	MDO[2]	MCU G5
27	Tool I/O-2	TP27		28	MDO[1]	MCU F5
29	Tool I/O-1	TP28		30	MDO[0]	MCU E5
31	UBATT	12V Vin		32	EVTO	MCU M12
33	UBATT	12V Vin		34	MCK0	MCU M10
35	Tool I/O-0	TP30		36	MSE1	MCU M9
37	VALTREF	3.3V Reg		38	MSEO	MCU M8

Note - In order to preserve the ability to accurately measure power consumption on the MCU pins, the JTAG and Nexus connector reference voltages will be sourced directly from the 5V regulator or from the 12V unregulated input.

3.5 CAN Configuration (J20, J21, J29, J30, J31)

The CAN section is located in the top right corner of the EVB in an area marked "CAN"



The EVB has 2x NXP TJA1041T high speed CAN transceiver on the MCU CAN-A and CAN-B channels. These can operate with 5v or 3.3v I/O from the MCU. This is determined by VDDE2 domain. For flexibility, the CAN transceiver I/O is connected to a standard 0.1" connector and DB9 connector at the top edge of the PCB. Connectors P11 and P3A provides the CAN bus level signal interface for CAN-A and connector P10 and P3B for CAN-B. The pinout for these connectors is shown below.

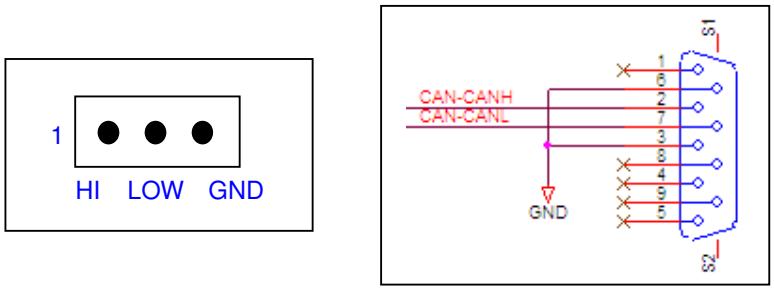


Figure 3-9 CAN Physical Interface Connector

Each of the MCU signals to the CAN transceivers is jumpered, allowing the transceiver to be isolated if that MCU pin is not configured or used for CAN operation. There is a 2x2 jumper for each CAN channel (one for Rx, one for Tx). There are also two power jumpers (J30) to physically remove power (12v and 5v) from both of the CAN transceivers. Jumpers J20 (CAN B) and J21 (CAN A) are configuration jumpers for each of the Transceivers to control Wake, Standby and Enable. Jumpers can be fitted to select default values or wires can be used to connect these pins to the MCU.

Table 3-14 CAN Control Jumpers (J30, J31, J7)

Jumper	Position	PCB Legend	Description
J30 Posn 1-2	FITTED **(D)**		5v is applied to both CAN transceivers VCC
	REMOVED		No 5v power is applied to CAN transceivers
J30 Posn 3-4	FITTED **(D)**		12v Power is applied to both CAN transceivers VBAT
	REMOVED		No 12v power is applied to CAN transceivers
J31 (CAN-A) Posn 1-2	FITTED **(D)**	TX	MCU CNTX-A is connected to CAN controller A
	REMOVED		MCU CNTX-A is NOT routed to CAN controller.
J31 (CAN-A) Posn 3-4	FITTED **(D)**	RX	MCU CNRX-A is connected to CAN controller A
	REMOVED		MCU CNRX-A is NOT routed to CAN controller.
J29 (CAN-B) Posn 1-2	FITTED **(D)**	TX	MCU CNTX-B is connected to CAN controller C
	REMOVED		MCU CNTX-B is NOT routed to CAN controller.
J29 (CAN-B) Posn 3-4	FITTED **(D)**	RX	MCU CNRX-B is connected to CAN controller C
	REMOVED		MCU CNRX-B is NOT routed to CAN controller.
J20 & J21 Posn 1-2	FITTED **(D)**	WAKE	CAN Transceiver WAKE is connected to GND
	REMOVED		WAKE is not connected and available on Pin 2
J20 & J21 Posn 3-4	FITTED **(D)**	STB	CAN Transceiver STB is connected to 5v
	REMOVED		STB is not connected and available on Pin 4
J20 & J21 Posn 3-4	FITTED **(D)**	EN	CAN Transceiver is Enabled
	REMOVED		EN is not connected and available on Pin 6

Access to the Error and inhibit signals from the transceivers is provided on J33 and J34.

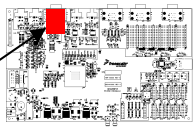
The prototyping area provides features that allow for additional CAN interfaces to be added to the EVB. Please see Section 6.2 for details.

Notes

- Care should be taken when fitting the jumper headers as they can easily be fitted in the incorrect orientation.

3.6 RS232 Configuration (J6, J17, J18, J23, J24)

The RS232 circuitry is located at the top edge of the EVB in an area titled "SCI"



The EVB has a single MAX3223 RS232 transceiver device, providing RS232 signal translation for the MCU SCI channels A and B.

Each of the two RS232 outputs from the MAX232 device is connected to a DB9 connector, allowing a direct RS232 connection to a PC or terminal. Connector P1A provides the RS232 level interface for MCU SCI-A and P1B for MCU SCI-B. The pinout of these connectors is detailed below. Note that hardware flow control is not supported on this implementation.

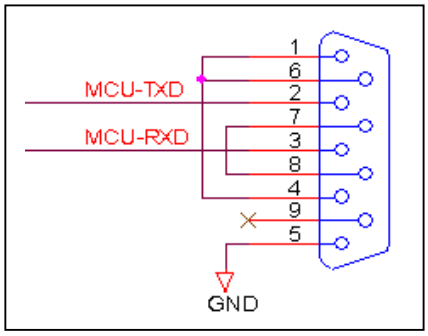


Figure 3-10 RS232 Physical Interface Connector

The MPC5668 eSCI also provides hardware LIN master capability which is supported on the EVB via LIN transceivers. Jumpers J17, J18, J23 and J24 are provided to isolate the MCU SCI signals from the RS232 interface as described below. There is also a global power jumper (J9) controlling the power to the RS232 transceiver.

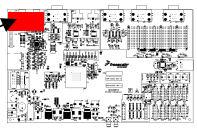
Table 3-15 RS232 Control Jumpers

Jumper	Position	PCB Legend	Description
J6 (SCI-PWR)	FITTED **(D)**		Power is applied to the MAX3223 transceiver
	REMOVED		No power is applied to the MAX3223 transceiver
J18 (SCI-A)	FITTED **(D)**	TXD	MCU TXD-A is routed to MAX3223
	REMOVED		MCU TXD-A signal is disconnected from CAN/LIN
J17 (SCI-A)	FITTED **(D)**	RXD	MCU RXD-A is routed via MAX3223
	REMOVED		MCU RXD-A signal is disconnected from CAN/LIN
J23 (SCI-B)	FITTED **(D)**	TXD	MCU TXD-B is routed via MAX3223
	REMOVED		MCU TXD-B signal is disconnected from CAN/LIN
J24 (SCI-B)	FITTED **(D)**	RXD	MCU RXD-B is routed via MAX3223
	REMOVED		MCU RXD-B signal is disconnected from CAN/LIN

The default configuration enables SCI-A and SCI-B channels. RS232 compliant interfaces (with no hardware flow control) are available at DB9 connector P1. If the MCU is configured such that SCI-A or SCI-B is set as a normal I/O port, then the relevant jumpers must be removed to avoid any conflicts occurring. If required, jumper J6 can be used to completely disable the SCI transceiver.

3.7 LIN Configuration (J3, J4, J5, J12, J13, J14, J15,J16)

The LIN circuitry is located in the top edge of the EVB in an area titled "LIN"



The EVB is fitted with two Freescale MCZ33661EF LIN transceivers. The eSCI module incorporates a hardware controlled LIN master, and as such, the LIN transceivers are connected to the TX and RX signals of SCI C and D.

For flexibility, the LIN transceivers are connected to a standard 0.1" connector (P7 for LIN-C and P6 for LIN-D) and a 4 pin molex connector (J2 for LIN-C and J1 for LIN-D) at the top edge of the PCB as shown in the figure below. For ease of use, the 12V EVB supply is fed to pin1 of the connectors and the LIN transceiver power input to pin 2. This allows the LIN transceiver to be powered directly from the EVB supply by simply linking pins 1 and 2 of connector P7/P6 using a 0.1" jumper shunt.

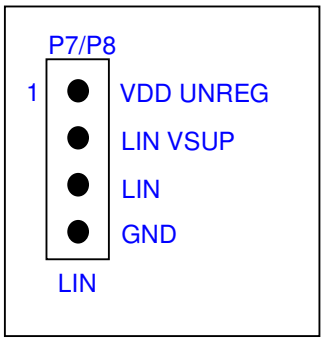


Figure 3-11 LIN Physical Interface Connectors

Along with the MCU signal routing jumpers (J10 / J11), there is are jumpers (J5 / J6) to enable or disable the LIN transceiver and jumpers (J1 and J2) which determines if the LIN transceiver is operating in master or slave mode, as defined in the table below.

Table 3-16 LIN Control Jumpers

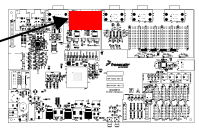
Jumper	Position	PCB Legend	Description
J5 (LIN C-M)	FITTED **(D)** REMOVED		LIN-C transceiver is configured for LIN Master mode LIN-C transceiver is configured for LIN Slave mode
J3 (LIN D-M)	FITTED **(D)** REMOVED		LIN-D transceiver is configured for LIN Master mode LIN-D transceiver is configured for LIN Slave mode
J16* **(LIN C-EN)**	FITTED **(D)** REMOVED		The LIN-C transceiver is enabled The LIN-C transceiver is disabled
J12* **(LIN D-EN)**	FITTED **(D)** REMOVED		The LIN-D transceiver is enabled The LIN-D transceiver is disabled
J14 (SCI-C)	FITTED **(D)** REMOVED	TXD	MCU TXD-C is routed to LIN Physical MCU TXD-C signal is disconnected LIN Physical
J15 (SCI-C)	FITTED **(D)** REMOVED	RXD	MCU RXD-C is routed to LIN Physical MCU RXD-C signal is disconnected LIN Physical
J14 (SCI-D)	FITTED **(D)** REMOVED	TXD	MCU TXD-D is routed to LIN Physical MCU TXD-D signal is disconnected LIN Physical
J15 (SCI-D)	FITTED **(D)** REMOVED	RXD	MCU RXD-D is routed to LIN Physical MCU RXD-D signal is disconnected LIN Physical

** Note – Jumpers J3/J5 do NOT route power to LIN transceivers, they only control an enable line on the LIN device. Power to the LIN transceiver is supplied via connectors P7 / P8, Pin 2.*

The Default LIN configuration is with the module enabled in master mode, LIN slave mode can be enabled by removing jumpers J3 / J5.

3.8 FlexRAY Configuration (J19, J27, J25, J26, J28)

The Flexray circuitry is located in the top edge of the EVB in an area titled "Flexray"



The EVB is fitted with 2 FlexRAY physical interfaces connected to MCU FlexRAY channels A and B. Jumpers J19 and J27 are provided to route the respective MCU signals to the physical interfaces as described below.

Table 3-17 Flexray MCU Signal Routing Jumpers (J19, J27)

Jumper	Position	PCB Legend	Description
J19 (Flex-A) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU PK4 is connected to Flexray A transceiver TX MCU PK4 is not connected to Flexray A transceiver TX
J19 (Flex-A) Posn 3-4	FITTED **(D)** REMOVED	TXEN	MCU PK5 is connected to Flexray A transceiver TXEN MCU PK5 is not connected to Flexray A transceiver TXEN
J19 (Flex-A) Posn 5-6	FITTED **(D)** REMOVED	RX	MCU PK3 is connected to Flexray A transceiver RX MCU PK3 is not connected to Flexray A transceiver RXEN
J27 (Flex-B) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU PK7 is connected to Flexray B transceiver TX MCU PK7 is not connected to Flexray B transceiver TX
J27 (Flex-B) Posn 3-4	FITTED **(D)** REMOVED	TXEN	MCU PK8 is connected to Flexray B transceiver TXEN MCU PK8 is not connected to Flexray B transceiver TXEN
J27(Flex-B) Posn 5-6	FITTED **(D)** REMOVED	RX	MCU PK6 is connected to Flexray B transceiver RX MCU PK6 is not connected to Flexray B transceiver RXEN

The power to the Flexray physical interface is controlled via jumper J25 to allow disconnection if required. The Flexray physical interface is capable of interfacing with MCU I/O voltages of 3.3V or 5.0V as defined by the voltage supplied VDDE2 via jumper J42.

Table 3-18 Flexray Power Control Jumpers (J25)

Jumper	Position	PCB Legend	Description
J25 (Flex-PWR) Posn 1-2	FITTED **(D)** REMOVED	12V	12V Flexray circuitry is powered from main 12V input 12V Flexray circuitry is not powered
J25 (Flex-PWR) Posn 3-4	FITTED **(D)** REMOVED	5V	5V Flexray circuitry is powered from 5.0V switching reg 5V Flexray circuitry is not powered
J25 (Flex-PWR) Posn 5-6	FITTED **(D)** REMOVED	VIO	VIO Flexray circuitry is powered from VDDE2 VIO Flexray circuitry is not powered

The flexray interface has 4 pins which are used for configuration and are pulled high or low controlled by a jumper as described in the table below. By default, all of the jumper headers are fitted. Please consult the Flexray physical interface specification before changing any of these jumpers.

Table 3-19 Flexray Control Jumpers (J26, J28)

Jumper	Position	PCB Legend	Description
J26 (Flex-A) Posn 1-2	FITTED **(D)** REMOVED	BGE	Flexray-A interface BGE signal is pulled to VIO Flexray-A interface BGE signal is unterminated
J26 (Flex-A) Posn 3-4	FITTED **(D)** REMOVED	EN	Flexray-A interface EN signal is pulled to VIO Flexray-A interface EN signal is unterminated
J26 (Flex-A) Posn 5-6	FITTED **(D)** REMOVED	STBEN	Flexray-A interface STBN signal is pulled to VIO Flexray-A interface STBN signal is unterminated
J26 (Flex-A) Posn 7-8	FITTED **(D)** REMOVED	WAKE	Flexray-A interface WAKE signal is pulled to GND Flexray-A interface WAKE signal is unterminated
J28 (Flex-B) Posn 1-2	FITTED **(D)** REMOVED	BGE	Flexray-B interface BGE signal is pulled to VIO Flexray-B interface BGE signal is unterminated
J28 (Flex-B) Posn 3-4	FITTED **(D)** REMOVED	EN	Flexray-B interface EN signal is pulled to VIO Flexray-B interface EN signal is unterminated
J28 (Flex-B) Posn 5-6	FITTED **(D)** REMOVED	STBEN	Flexray-B interface STBN signal is pulled to VIO Flexray-B interface STBN signal is unterminated
J28 (Flex-B) Posn 7-8	FITTED **(D)** REMOVED	WAKE	Flexray-B interface WAKE signal is pulled to GND Flexray-B interface WAKE signal is unterminated

Notes:

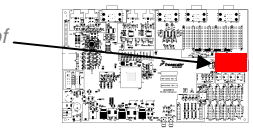
- *The flexray physical interfaces are connected to 2 pin molex connectors (FlexRAY A) 1.25mm shrouded 2-pin connectors to connect to the flexray bus (as are standard fit on many Freescale development platforms using flexray).*

Important:

A 40Mhz oscillator is required for the correct operation of the flexray controller. Please ensure that the 40Mhz crystal is selected as the system clock or use a 40Mhz external clock source.

3.9 Ethernet

The Ethernet circuitry is located in the right edge of the EVB in an area titled "Ethernet"



The EVB is fitted with a National Semiconductor DP8348C Ethernet physical interface (U9) and a Pulse Jack J1011F21PNL RJ45 connector with integrated activity LED's and magnetics (J63).

The National Semiconductor DP8348C physical interface is connected to the MII on the MPC5668. This is a fixed connection with no means of isolation. Pullups are also also present on some of these signals. These are detailed in the table below. Please be aware of this when using I/O on ports G and H.

Table 3-20 Pull up/ Pull down resistors on Ports G and H for Ethernet Physical

Port Pin	Pull Direction	Strength
PG[9]	Down (GND)	2.2kΩ
PG[7]	Up (3.3v SR)	1.5kΩ
PG[12]	Down (GND)	2.2kΩ
PG[13]	Down (GND)	2.2kΩ
PG[14]	Down (GND)	2.2kΩ
PG[15]	Down (GND)	2.2kΩ
PH[1]	Down (GND)	2.2kΩ
PH[2]	Down (GND)	2.2kΩ
PH[3]	Down (GND)	2.2kΩ
PH[4]	Down (GND)	2.2kΩ
PH[5]	Down (GND)	2.2kΩ
PH[6]	Down (GND)	2.2kΩ
PH[7]	Down (GND)	2.2kΩ

The VDDE3 voltage domain that is used by ports G and H should be set to 3.3v (J44 Pos 2-3) when power is applied to the physical interface.

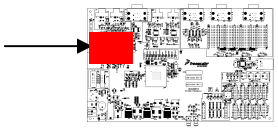
Power can be removed from the physical interface via J62.

Table 3-21 Ehternet Physical Interface Power Supply Enabled (J26)

Jumper	Position	PCB Legend	Description
J62 (PHY PWR)	FITTED (D) REMOVED	**PHY PWR**	The DP4348C Ethernet Physical Interface is powered from the 3.3v SR. The DP4348C Ethernet Physical Interface is not powered

3.10 MLB and Most

The MLB and MOST circuitry is located on the left edge of the EVB .



The EVB is fitted with a range of hardware to support the MOST communication protocol. These include:

- SMSC OS81050 (U6) INIC interfaced to the MPC5668 via 3 pin Media Local Bus (MLB) interface.
- INIC JTAG port (P12) and MLB monitor port (J88)
- Tyco Physical optical transceiver (U8) interfaced to the SMSC OS81050
- Dual footprint layout to allow the SMSC OS81050 to be replaced with the smaller ROM alternative
- 40 Pin header to allow the EVB to be interfaced to the MOST 150 EVB from SMSC.

Power Jumpers on the EVB are configured to allow the EVB to supply power to both the ROM and Flash versions of the SMSC OS81050 INIC that are supported by the dual footprint on the EVB. By default the Flash version of the OS81050 is fitted to the EVB. The jumpers also allow power to be removed from the INIC. The power supply jumpers are detailed below. All Power supplies domains referred to in this table are for the Flash based INIC. Please refer to the schematics to see how this affects the supply domains of the ROM INIC if it has been fitted.

Table 3-22 INIC Power Supply Control (J35, J36, J55)

Jumper	Position	PCB Legend	Description
J35	FITTED **(D)**	3.3v PWR	3.3v is applied to VDDP1 and VDDP2 of the INIC
	REMOVED		No 3.3v power is applied to VDDP1 and VDDP2
J36	FITTED **(D)**	2.5v PWR	2.5v is applied to VDDA1 and VDDA2.
	REMOVED		No power is applied to VDDA1 and VDDA2.
J55	FITTED **(D)**	2.5v PWR	2.5v is applied to VDDC1 and VDDC2.
	REMOVED		No power is applied to VDDC1 and VDDC2.

The Pin out for the INIC JTAG connector filled to the EVB is show in Figure x below:

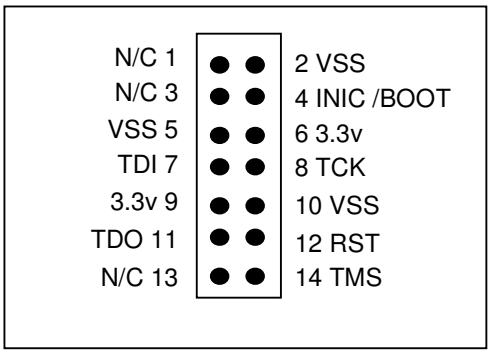


Figure 3-12. INC5668 JTAG Connector

The INIC pins MLBDI, MLBSI, RMCK, SCK and FSY are brought out to the header J22, to allow for monitoring and control if required. J88 provides the MLB monitor header that is compatible with the SMSC MLB Monitor hardware. The Pin out of this is shown in Figure x below.

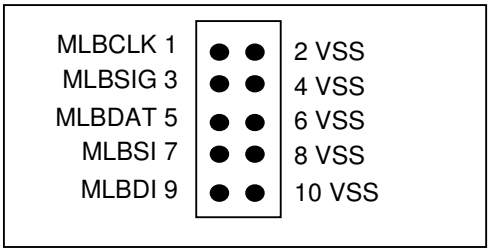


Figure 3-13. MLB Monitor Connector

Port J11 is placed on the edge of the EVB to allow the SMSC MOST 150 EVB to be interfaced to the MPC5668EVB. This allows for evaluation of the MOST150 INIC with the MPC5668. To use this connector the signals must be routed from the on chip INIC to this connector using the Jumpers detailed in table x below. Removing these Jumpers also allow the signals between the INIC and the MCU to be isolated.

Table 3-23 INIC Signal Control

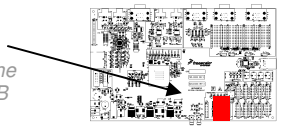
Jumper	Position	PCB Legend	Description
J37(MLBCLK)	1-2 **(D)**	EVB	MLBCLK is Routed to the EVB INIC
	2-3	INIC150	MLBCLK is Routed to the MOST150 header
J38(PSO)	1-2 **(D)**	EVB	PSO is Routed to the EVB INIC
	2-3	INIC150	PSO is Routed to the MOST150 header
J39(MLBDAT)	1-2 **(D)**	EVB	MLBDAT is Routed to the EVB INIC
	2-3	INIC150	MLBDAT is Routed to the MOST150 header
J40(SDA)	1-2 **(D)**	EVB	SDA is Routed to the EVB INIC
	2-3	INIC150	SDA is Routed to the MOST150 header
J57(PS1)	1-2 **(D)**	EVB	PS1 is Routed to the EVB INIC
	2-3	INIC150	PS1 is Routed to the MOST150 header
J58 (/INT)	1-2 **(D)**	EVB	/INT is Routed to the EVB INIC
	2-3	INIC150	/INT is Routed to the MOST150 header
J59 (SCL)	1-2 **(D)**	EVB	SCL is Routed to the EVB INIC
	2-3	INIC150	SCL is Routed to the MOST150 header
J65 (MLBSIG)	1-2 **(D)**	EVB	MLBSIG is Routed to the EVB INIC
	2-3	INIC150	MLBSIG is Routed to the MOST150 header

The status and reset lines can also be isolated via J56 and J64.

If required the standard fit INIC can be removed and replaced with the ROM memory alternate. Please observe the power supply requirements of the device.

3.11 Phantom Ports (J76, J77, J78, J79, J80)

The Phantom port circuitry is located on the bottom edge of the EVB



To support the de-serialisation feature of the MPC5668 DSPI module, the EVB features 4 chained SIPO shift registers interfaced to DSPI A. This allows a 32-bit phantom port to be created. The port can operate at either 5V or 3.3V depending on the VDDE2 supply voltage (J42). This is outputted on P24 and P25. Please refer to the MPC5668 Reference manual for guideline on how to create software to interface to the phantom part.

Five jumpers are used to allow the signals and power to be isolated from the phantom port circuitry. These are detailed in table x below.

Table 3-24 Phantom Port Control (J35, J36, J55)

Jumper	Position	PCB Legend	Description
J76	FITTED **(D)**	CLK	PF0 DSPI A CLK is connected to the phantom port circuitry.
	REMOVED		PF0 DSPI A CLK is disconnected from the phantom port circuitry.
J77	FITTED **(D)**	SREG PWR	VDDE2 Domain power is applied to the 4 shift registers (U15, U16, U21, U22)
	REMOVED		No power is applied to the 4 shift registers (U15, U16, U21, U22)
J78	FITTED **(D)**	IN	PF1 DSPI_A Serial Data Out is connected to the phantom port circuitry.
	REMOVED		PF1 DSPI_A Serial Data Out is disconnected from the phantom port circuitry.
J79	FITTED **(D)**	CLR	PF11 is connected to the phantom port circuitry. Allows for software to reset the Shift registers.
	REMOVED		PF11 is disconnected from the phantom port circuitry.
J80	FITTED **(D)**	OUT	PF3 DSPI A PCS is connected to the phantom port circuitry.
	REMOVED		PF3 DSPI A PCS is disconnected from the phantom port circuitry.

4. MCU Pin Usage Map

The table below provides a useful cross reference to see what MCU port pins are used by the various EVB peripherals and functions. Note that there are some overlapping functions for example the Nexus and External bus as shown by the shaded boxes in the table below.

Table 4-1. EVB MCU Pin Usage

Function	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J	Port k
Enabled By Default										
CANA				PD[0..1]						
CANB				PD[2..3]						
SCIA				PD[12,13]						
SCIB				PD[14,15]						
LINC					PE[0,1]					
LIND					PE[2,3]					
FlexRay A										PK[3..5]
FlexRay B										PK[6..8]
Reset Config										PK[9]
Ethernet							PG[6..9] PG[12..15]	PH[0,1] PH[3..7]		
MOST/MLB		PB[0,1]					PG[0] PG[2..5]			PK[0..2]
User RVAR	PA[0]									
Phantom Port						PF[0,1,3, 11]				

5. Default Jumper Summary Table

The following table details the DEFAULT jumper configuration of the EVB as explained in detail in section 3.

Table 5-1 Default Jumper Positions

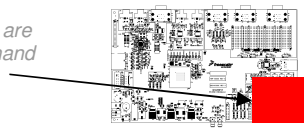
Jumper	Default Posn	PCB Legend	Description
J1	LIN MOLEX – No Jumpers		
J2	LIN MOLEX – No Jumpers		
J3 (LIN-D)	FITTED	MASTER	LIN D Bus Master Mode Enabled
J4 (LIN D)	FITTED	LIN D RX	LIN D RX from MCU Connected to LIN Interface
J5 (LIN C)	FITTED	MASTER	LIN C Bus Master Mode Enabled
J6 (SCI-PWR)	FITTED		Power is applied to the SCI transceiver
J7 (FlexRAY)	FITTED	CAP A DIS	FlexRAY Decoupling CAP Disable
J8 (FlexRAY)	FITTED	CAP A DIS	FlexRAY Decoupling CAP Disable
J9 (FlexRAY)	FITTED	CAP B DIS	FlexRAY Decoupling CAP Disable
J10 (FlexRAY)	FITTED	CAP B DIS	FlexRAY Decoupling CAP Disable
J11	External Port No Jumpers		
J12 (LIN-D)	FITTED	LIN D EN	LIN D Bus Enable Physical Interface
J13 (LIN D)	FITTED	LIN D TX	LIN D TX from MCU Connected to LIN Interface
J14 (LIN C)	FITTED	LIN C TX	LIN C TX from MCU Connected to LIN Interface
J15 (LIN C)	FITTED	LIN C RX	LIN C RX from MCU Connected to LIN Interface
J16 (LIN C)	FITTED	LIN C EN	LIN D Bus Enable Physical Interface
J17 (SCI A)	FITTED	SCI A RX	MCU RXD-A is routed to MAX3223
J18 (SCI A)	FITTED	SCI A TX	MCU TXD-A is routed to MAX3223
J19 (Flex-A) Posn 1-2	FITTED	TX	MCU PK4 is connected to FlexRay A transceiver TX
J19 (Flex-A) Posn 3-4	FITTED	TXEN	MCU PK5 is connected to FlexRay A transceiver TXEN
J19 (Flex-A) Posn 5-6	FITTED	RX	MCU PK3 is connected to Flexray A transceiver RXEN
J20 (CAN A) Posn 1-2	FITTED	WAKE	CAN Transceiver WAKE is connected to GND
J20 (CAN A) Posn 3-4	FITTED	STB	CAN Transceiver STB is connected to 5v
J20 (CAN A) Posn 3-4	FITTED	EN	CAN Transceiver is Enabled
J21 (CAN B) Posn 1-2	FITTED	WAKE	CAN Transceiver WAKE is connected to GND
J21 (CAN B) Posn 3-4	FITTED	STB	CAN Transceiver STB is connected to 5v
J21 (CAN B) Posn 3-4	FITTED	EN	CAN Transceiver is Enabled
J22	MLB Monitor No Jumpers		
J23 (SCI-B)	FITTED	TXD	MCU TXD-B is routed via MAX3223
J24 (SCI-B)	FITTED	RXD	MCU RXD-B is routed via MAX3223
J25 (Flex-PWR) Posn 1-2	FITTED	12V	12V Flexray circuitry is powered from main 12V input
J25 (Flex-PWR) Posn 3-4	FITTED	5V	5V Flexray circuitry is powered from 5.0V switching reg
J25 (Flex-PWR) Posn 5-6	FITTED	VIO	VIO Flexray circuitry is powered from VDDE2

Jumper	Default Posn	PCB Legend	Description
J26 (Flex-A) Posn 1-2	FITTED	BGE	Flexray-A interface BGE signal is pulled to VIO
J26 (Flex-A) Posn 3-4	FITTED	EN	Flexray-A interface EN signal is pulled to VIO
J26 (Flex-A) Posn 5-6	FITTED	STBEN	Flexray-A interface STBN signal is pulled to VIO
J26 (Flex-A) Posn 7-8	FITTED	WAKE	Flexray-A interface WAKE signal is pulled to GND
J27 (Flex-B) Posn 1-2	FITTED	TX	MCU PK7 is connected to Flexray B transceiver TX
J27 (Flex-B) Posn 3-4	FITTED	TXEN	MCU PK8 is connected to Flexray B transceiver TXEN
J27(Flex-B) Posn 5-6	FITTED	RX	MCU PK6 is connected to Flexray B transceiver RX
J28 (Flex-B) Posn 1-2	FITTED	BGE	Flexray-B interface BGE signal is pulled to VIO
J28 (Flex-B) Posn 3-4	FITTED	EN	Flexray-B interface EN signal is pulled to VIO
J28 (Flex-B) Posn 5-6	FITTED	STBEN	Flexray-B interface STBN signal is pulled to VIO
J28 (Flex-B) Posn 7-8	FITTED	WAKE	Flexray-B interface WAKE signal is pulled to GND
J29 (CAN-B) Posn 1-2	FITTED	TX	MCU CNTX-B is connected to CAN controller C
J29 (CAN-B) Posn 3-4	FITTED	RX	MCU CNRX-B is connected to CAN controller C
J30 (CAN) Posn 1-2	FITTED	VCC	5v is applied to both CAN transceivers VCC
J30 (CAN) Posn 3-4	FITTED	VIO	Power is applied to both CAN transceivers VIO
J31 (CAN-A) Posn 1-2	FITTED	TX	MCU CNTX-A is connected to CAN controller A
J31 (CAN-A) Posn 3-4	FITTED	RX	MCU CNRX-A is connected to CAN controller A
J32 (JRST)	1-2	BUF	JTAG reset signal is buffered to MCU RESET pin (connected to the MCU Reset-In circuitry)
J33	CAN Status – No Jumpers		
J34	CAN Status – No Jumpers		
J35	FITTED	3.3v PWR	3.3v is applied to VDDP1 and VDDP2 of the INIC
J36	FITTED	2.5v PWR	2.5v is applied to VDDA1 and VDDA2.
J37(MLBCLK)	1-2	EVB	MLBCLK is Routed to the EVB INIC
J38(PSO)	1-2	EVB	PSO is Routed to the EVB INIC
J39(MLBDAT)	1-2	EVB	MLBDAT is Routed to the EVB INIC
J40(SDA)	1-2	EVB	SDA is Routed to the EVB INIC
J41 (VDDE4)	1-2	5.0v	MCU VDDE4 is powered from 5v
J42 (VDDE2)	1-2	5.0v	MCU VDDE2 is powered from 5v
J43 (VDDE1)	1-2	5.0v	MCU VDDE1 is powered from 5v
J44 (VDDE3)	1-2	5.0v	MCU VDDE3 is powered from 5v
J45 (VDDEMLB)	1-2	2.5V	MCU VDD pin is powered from 1.5v switching regulator
J46 (VRC)	1-2	5V	VRC is supplied from the 5V switching regulator
J47 (VRCSEL)	1-2	INT	3.3 V internal voltage regulator enabled (5 V mode)
J48 (VDD33)	REMOVED		MCU VDD33 pin is powered from switching regulator
J49 (VDDA)	FITTED		MCU VDDA is powered from 5V linear regulator
J50 (VDDSYN)	REMOVED		MCU VDDSYN pin is powered from switching regulator

Jumper	Default Posn	PCB Legend	Description
J51 (CAN F)	REMOVED		Do not route CAN F to Prototype Area
J52 (CAN D)	REMOVED		Do not route CAN D to Prototype Area
J53 (CAN E)	REMOVED		Do not route CAN E to Prototype Area
J54 (CAN C)	REMOVED		Do not route CAN C to Prototype Area
J55 (INIC PWR)	FITTED	2.5v PWR	2.5v is applied to VDDC1 and VDDC2.
J56 (INIC RST)	FITTED	RST	INIC Reset is connected to PB0
J57(INIC PS1)	1-2	EVB	MLB PS1 is Routed to the EVB INIC
J58 (INIC /INT)	1-2	EVB	/INT is Routed to the EVB INIC
J59 (INIC SCL)	1-2	EVB	SCL is Routed to the EVB INIC
J60 (INIC BOOT)	1-2	EVB	INIC Boot pin is pulled up to 2.5v Rail
J61 (MCU CLK)	1-2	Y2	MCU Clock is Y2
J62 (PHY PWR)	FITTED	PHY PWR	The DP4348C Ethernet Physical Interface is powered from the 3.3v SR.
J63	RJ45 No Jumpers		
J64 (MOST FOT)	1-2	STATUS	MOST FOT is Status is connected to PB1
J65 (MLBSIG)	1-2	EVB	MLBSIG is Routed to the EVB INIC
J66 (MCU CLK)	1-2	Y2	MCU Clock is Y2
J67 (32KHz CLK)	1-2	Y3	32Khz Crystal (Y2) is connected to MCU
J68 (RST-IN)	FITTED		External reset source (LVI, Debug or Target) will be able to assert MCU reset
J69 (BOOT CFG)	1-2	FLASH	MCU boots from internal flash
J70 (TCLK PULL)	1-2	VDDE2	JTAG / NEXUS TCLK signal is pulled to VDDE2 via 10KΩ
J71 (32KHz CLK)	1-2	Y3	32Khz Crystal (Y2) is connected to MCU
J72	Not Implemented		
J73 (ADC VSUP)	REMOVED		Output from variable resistor RV1 is applied to MCU PA0
J74	REMOVED		On board Voltage levels not connected to EVB
J75 (1-2)	FITTED		Enables 3.3v board level LVI
J75 (3-4)	FITTED		Enables 5v board level LVI
J76	FITTED	CLK	PF0 DSPI A CLK is connected to the phantom port circuitry.
J77	FITTED	SREG PWR	VDDE2 Domain power is applied to the 4 shift registers (U15, U16, U21, U22)
J78	FITTED	IN	PF1 DSPI_A Serial Data Out is connected to the phantom port circuitry.
J79	FITTED	CLR	PF11 is connected to the phantom port circuitry. Allows for software to reset the Shift registers.
J80	FITTED	OUT	PF3 DSPI A PCS is connected to the phantom port circuitry.
J81 (5.0v-LINEAR)	FITTED	DISABLE	5.0v linear regulator output is Enabled
J82 (2.5v)	REMOVED	DISABLE	2.5v switching regulator output is Enabled
J83 (3.3v)	REMOVED	DISABLE	3.3v switching regulator output is Enabled
J84 (5.0v)	REMOVED	DISABLE	5.0v switching regulator output is Enabled
J85 (U20 PWR)	FITTED		EVB oscillator module U20 is powered
J86 (RV1)	FITTED		Output from variable resistor RV1 is applied to MCU PA0
J87 (OSC SEL)	1-2	MOD	Daughter card EXT-CLK is routed from U20

6. User Connector Descriptions

The user connectors are located on the right hand side of the PCB



This section details the pinout of the EVB user connectors. The connectors are 0.1 inch pitch turned pin headers and are located to the right hand side of the EVB. Pins are grouped by port functionality and the PCB legend shows the respective port number adjacent to each pin.

6.1.1 Port A / ADC (Connector J86, RV1, J73 and J74)

Table 6-1. Port A Connector Pinout (P17)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PA0	AN0		2	PA1	AN1
3	PA2	AN2		4	PA3	AN3
5	PA4	AN4		6	PA5	AN5
7	PA6	AN6		8	PA7	AN7
9	PA8	AN8		10	PA9	AN9
11	PA10	AN10		12	PA11	AN11
13	PA12	AN12		14	PA13	AN13
15	PA14	AN14		16	PA15	AN15
17	GND			18	GND	

To provide a quick means of supplying input to the ATD (Analogue To Digital converter), a 2KΩ variable resistor (RV1) will is connected between P5V and GND, with the output (centre tap) connected to PA0 / AN0 via jumper J86. By removing jumper J86, PA0 is disconnected from the variable resistor and can function as a normal I/O port. J86 and RV1 are located next to P17.

To allow the EVB core voltages to be monitors by the ATD J74 allows the 2.5v, 3.3v and 5v Switcher and Linear regulator outputs to be connected to the ATD inputs. J73 allows the 12v EVB supply to be monitored via resister ladder to reduce the voltage to a level that is in spec of the ATD's range. 65% of the 12v supply is applied to the ADC via the resistor ladder.

Table 6-2 RV1 Connection Jumper J8

Jumper	Position	PCB Legend	Description
J86 (RV1)	FITTED		Output from variable resistor RV1 is applied to PA0
	REMOVED (D)		Output from RV1 is not connected to MCU (disabled)
J73 (ADC VSUP)	FITTED		65% of the output from 12v Reg is applied to PA14
	REMOVED (D)		12v Reg Output is not connected to PA14
J74 POSN 1-2	FITTED		Output from 2.5v Reg is connected to PA10
	REMOVED (D)		Output from 2.5v Reg is NOT connected to PA10
J74 POSN 3-4	FITTED		Output from 3.3v Reg is connected to PA10
	REMOVED (D)		Output from 3.3v Reg is NOT connected to PA10
J74 POSN 5-6	FITTED		Output from 5v Switching Reg is connected to PA10
	REMOVED (D)		Output from 5v Switching Reg is NOT connected to PA10
J74 POSN 7-8	FITTED		Output from 5v Linear Reg is connected to PA10
	REMOVED (D)		Output from 5v Linear Reg is NOT connected to PA10

Note - PA14 and PA15 can also be used for the EXTAL32 and XTAL32 32Khz reference clock. If these pins are used for this purpose, they will not be available for GPIO / ADC input.

6.1.2 Port B / ADC / SPI (P18)

Table 6-3. Port B Connector Pinout (P18)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PB0	AN16		2	PB1	AN17
3	PB2	AN18		4	PB3	AN19
5	PB4	AN20		6	PB5	AN21
7	PB6	AN22		8	PB7	AN23
9	PB8	AN24		10	PB9	AN25
11	PB10	AN26		12	PB11	AN27
13	PB12	AN28		14	PB13	AN29
15	PB14	AN30		16	PB15	AN31
17	GND			18	GND	

6.1.3 Port C / ADC / FLEXRAY / I2C (P19)

Table 6-4. Port C Connector Pinout (P19)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PC0	AN32		2	PC1	AN33
3	PC2	AN34		4	PC3	AN35
5	PC4	AN36		6	PC5	AN37
7	PC6	AN38		8	PC7	AN39
9	PC8	AN40		10	PC9	AN41
11	PC10	AN42		12	PC11	AN43
13	PC12	AN44		14	PC13	AN45
15	PC14	AN46		16	PC15	AN47
17	GND			18	GND	

6.1.4 Port D / CAN / I2C / SCI (P20)

Table 6-5. Port D Connector Pinout (P20)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PD0	CNTX_A		2	PD1	CNRX_A
3	PD2	CNTX_B		4	PD3	CNRX_B
5	PD4	CNTX_C		6	PD5	CNRX_C
7	PD6	CNTX_D		8	PD7	CNRX_D
9	PD8	CNTX_E		10	PD9	CNRX_E
11	PD10	CNTX_F		12	PD11	CNRX_F
13	PD12	TXD_A		14	PD13	RXD_A
15	PD14	TXD_B		16	PD15	TXD_B
17	GND			18	GND	

6.1.5 Port E / SCI / eMIOS / I2C (P21)

Table 6-6. Port E Connector Pinout (P21)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PE0	TXD_C		2	PE1	RXD_C
3	PE2	TXD_D		4	PE3	RXD_D
5	PE4	TXD_E		6	PE5	RXD_E
7	PE6	TXD_F		8	PE7	RXD_F
9	PE8	TXD_G		10	PE9	RXD_G
11	PE10	TXD_H		12	PE11	RXD_H
13	PE12	TXD_J		14	PE13	RXD_J
15	PE14	SCL_A		16	PE15	SDA_A
17	GND			18	GND	

6.1.6 Port F / DSPI (P26)

Table 6-7. Port F Connector Pinout (P26)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PF0	SCK_A		2	PF1	SOUT_A
3	PF2	SIN_A		4	PF3	PCS_A[0]
5	PF4	SCK_B		6	PF5	SOUT_B
7	PF6	SIN_B		8	PF7	PCS_B[0]
9	PF8	SCK_C		10	PF9	SOUT_C
11	PF10	SIN_C		12	PF11	PCS_C[0]
13	PF12	SCK_D		14	PF13	SOUT_D
15	PF14	SIN_D		16	PF15	PCS_D[0]
17	GND			18	GND	

6.1.7 Port G / DSPI / eMIOS / FEC (P27)

Table 6-8. Port F Connector Pinout (P27)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PG0	PCS_A[4]		2	PG1	PCS_A[5]
3	PG2	PCS_D[1]		4	PG3	PCS_D[2]
5	PG4	PCS_D[3]		6	PG5	PCS_D[4]
7	PG6	PCS_C[1]		8	PG7	PCS_C[2]
9	PG8	eMIOS[7]		10	PG9	eMIOS[6]
11	PG10	eMIOS[5]		12	PG11	eMIOS[4]
13	PG12	eMIOS[3]		14	PG13	eMIOS[2]
15	PG14	eMIOS[1]		16	PG15	eMIOS[0]
17	GND			18	GND	

6.1.8 Port H / eMIOS / FEC (P28)

Table 6-9. Port H Connector Pinout (P28)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PH0	eMIOS[31]		2	PH1	eMIOS[30]
3	PH2	eMIOS[29]		4	PH3	eMIOS[28]
5	PH4	eMIOS[27]		6	PH5	eMIOS[26]
7	PH6	eMIOS[25]		8	PH7	eMIOS[24]
9	PH8	eMIOS[23]		10	PH9	eMIOS[22]
11	PH10	eMIOS[21]		12	PH11	eMIOS[20]
13	PH12	eMIOS[19]		14	PH13	eMIOS[18]
15	PH14	eMIOS[17]		16	PH15	eMIOS[16]
17	GND			18	GND	

6.1.9 Port J / eMIOS / FEC (P29)

Table 6-10. Port J Connector Pinout (P29)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PJ0	eMIOS[15]		2	PJ1	eMIOS[14]
3	PJ2	eMIOS[13]		4	PJ3	eMIOS[12]
5	PJ4	eMIOS[11]		6	PJ5	eMIOS[10]
7	PJ6	eMIOS[9]		8	PJ7	eMIOS[8]
9	PJ8	eMIOS[7]		10	PJ9	eMIOS[6]
11	PJ10	eMIOS[5]		12	PJ11	eMIOS[4]
13	PJ12	eMIOS[3]		14	PJ13	eMIOS[2]
15	PJ14	eMIOS[1]		16	PJ15	eMIOS[0]
17	GND			18	GND	

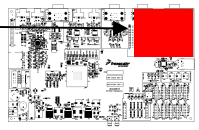
6.1.10 Port K / RESET / MLB (Connector P30)

Table 6-11. Port K Connector Pinout (P30)

Pin	Function			Pin	Function	
	GPIO	1st Alt			GPIO	1st Alt
1	PK0	MLBCLK		2	PK1	MLBSIG
3	PK2	MLBDAT		4	PK3	FR_A_RX
5	PK4	FR_A_TX		6	PK5	FR_A_TX_EN
7	PK6	FR_B_RX		8	PK7	FR_B_TX
9	PK8	FR_B_TX_EN		10	PK9	CLKOUT
11	PK10	PCS_B[5]		12	GND	
13	RST OUT			14	TST RST	
15	GND			16	GND	

6.2 Prototyping Area and User LED's / Switches

The prototyping area is located on the right hand side of the EVB, above the user connectors.



There is a rectangular prototype area on the EVB, consisting of a 0.1inch pitch array of through-hole plated pads. Power from all three voltage regulators is readily accessible along with GND. This area is ideal for the addition of any custom circuitry. Adapters are available to convert SMD devices to 0.1inch pitch through-hole.

Some of the pads in the prototyping area are connected to the CAN C – F pins of the MCU as well as power and the DB9 connectors. This allows an additional 4 CAN physical interfaces to be added to the EVB for evaluation with the MCU. The layout of this is shown in Figure X below.

Note: The power supply lines to the prototype area are connected directly to the regulator outputs and not connected to the jumpered MCU supply.

There are 4 active low user LED's DS4, DS5, DS6 and DS7, These are driven by connecting a logic 0 signal to the corresponding pin on 0.1" header P15 (user LED's).

There are 4 active high pushbutton switches SW2, SW3, SW4 and SW5 which will drive 5V onto the respective pins on 0.1" connector P16 when pressed. The switch outputs are pulled to GND with a 10K resistor network.

Appendix A - EVB Schematics

MPC5668 Evaluation Board

Table of Contents

Revisions

Rev	Description	Date	Designer
A	Original Release	July 23rd 2008	D.McMenamin & D.McKenna
B	Changes based on reviews	March 10th 2009	D.McMenamin

freescale semiconductor

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