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64 Mbit SPI Serial Dual I/O Flash

SST25VF064C

EOL Data Sheet

The SST 25 series Serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. SST25VF064C SPI serial flash memory is manufactured with SST proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

Features

- **Single Voltage Read and Write Operations**
  - 2.7-3.6V
- **Serial Interface Architecture**
  - SPI Compatible: Mode 0 and Mode 3
- **Dual Input/Output Support**
  - Fast-Read Dual-Output Instruction
  - Fast-Read Dual I/O Instruction
- **High Speed Clock Frequency**
  - 80 MHz for High-Speed Read (0BH)
  - 75 MHz for Fast-Read Dual-Output (3BH)
  - 50 MHz for Fast-Read Dual I/O (BBH)
  - 33 MHz for Read Instruction (03H)
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Read Current: 12 mA (typical @ 80 MHz) for single-bit read)
  - Active Read Current: 14 mA (typical @ 75MHz) for dual-bit read)
  - Standby Current: 5 µA (typical)
- **Flexible Erase Capability**
  - Uniform 4 KByte sectors
  - Uniform 32 KByte overlay blocks
  - Uniform 64 KByte overlay blocks
- **Fast Erase**
  - Chip-Erase Time: 35 ms (typical)
  - Sector-/Block-Erase Time: 18 ms (typical)
- **Page-Program**
  - 256 Bytes per page
  - Single and Dual Input support
  - Fast Page-Program time in 1.5 ms (typical)
- **End-of-Write Detection**
  - Software polling the BUSY bit in Status Register
- **Write Protection (WP#)**
  - Enables/Disables the Lock-Down function of the status register
- **Software Write Protection**
  - Write protection through Block-Protection bits in status register
- **Security ID**
  - One-Time Programmable (OTP) 256 bit, Secure ID
    - 64 bit Unique, Factory Pre-Programmed identifier
    - 192 bit User-Programmable
- **Temperature Range**
  - Commercial = 0°C to +70°C
  - Industrial: -40°C to +85°C
- **Packages Available**
  - 16-lead SOIC (300 mils)
  - 8-contact WSON (6mm x 8mm)
  - 8-lead SOIC (200 mils)
- **All devices are RoHS compliant**

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Product Description

The SST 25 series Serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. SST25VF064C SPI serial flash memory is manufactured with SST proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST25VF064C significantly improves performance and reliability, while lowering power consumption. The device writes (Program or Erase) with a single power supply of 2.7-3.6V. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

The SST25VF064C device is offered in 16-lead SOIC (300 mils), 8-contact WSON (6mm x 8mm), and 8-lead SOIC (200 mils) packages. See Figure 2 for pin assignments.

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Block Diagram

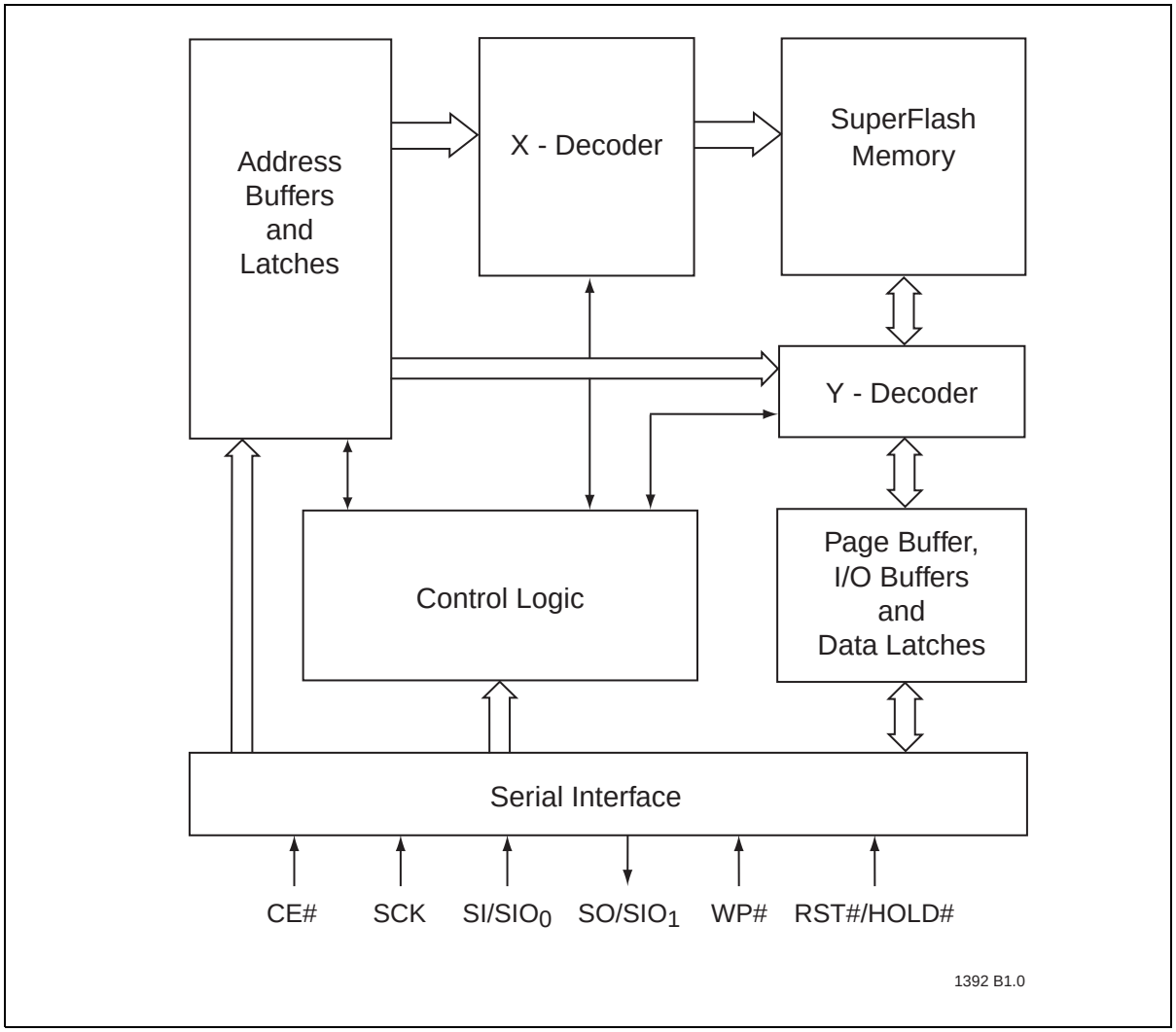

Figure 1: Functional Block Diagram

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Pin Description

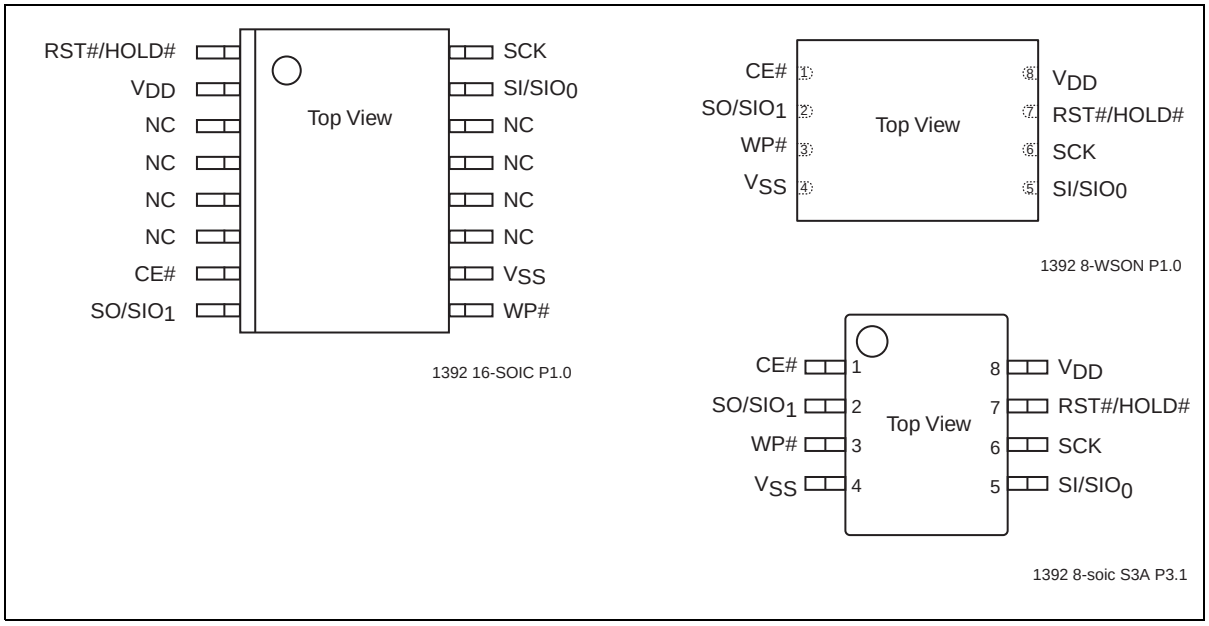

Figure 2: Pin Assignments for 16-Lead SOIC, 8-Contact WSON, and 8-Lead SOIC

Table 1: Pin Description

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
SIO[0:1]	Serial Data Input/ Output for Dual I/ O Mode	To transfer commands, addresses, or data serially into the device, or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. These pins are for Dual I/O mode.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
RST#/HOLD#	Reset	To reset the operation of the device and the internal logic. The device powers on with RST# pin functionality as default.
	Hold	To temporarily stop serial communication with SPI Flash memory while device is selected. This is selected by an instruction sequence. See “Reset/ Hold Mode” page 5 for details.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	

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Memory Organization

The SST25VF064C SuperFlash memory array is organized in uniform 4 KByte erasable sectors with 32 KByte overlay blocks and 64 KByte overlay erasable blocks.

Device Operation

The SST25VF064C is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consists of four control lines; Chip Enable (CE#) is used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The SST25VF064C supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 3, is the state of the SCK signal when the bus master is in Stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

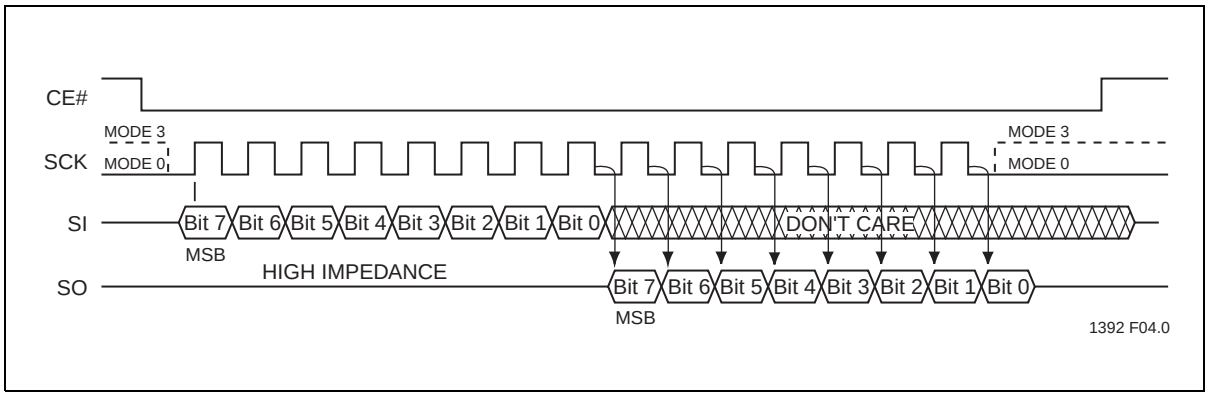

Figure 3: SPI Protocol

Reset/Hold Mode

The RST#/HOLD# pin provides either a hardware reset or a hold pin. From power-on, the RST#/HOLD# pin defaults as a hardware reset pin (RST#). The Hold mode for this pin is a user selected option where an EHLD instruction enables the Hold mode. Once selected as a hold pin (HOLD#), the RST#/HOLD# pin will be configured as a HOLD# pin, and goes back to RST# pin only after a power-off and power-on sequence.

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Reset

If the RST#/HOLD# pin is used as a reset pin, RST# pin provides a hardware method for resetting the device. Driving the RST# pin high puts the device in normal operating mode. The RST# pin must be driven low for a minimum of T_{RST} time to reset the device. The SO pin is in high impedance state while the device is in reset. A successful reset will reset the status register to its power-up state (BPL, BUSY and WEL = 0; BP3, BP2, BP1, and BP0 = 1). See Table 2 for default power-up modes. A device reset during an active Program or Erase operation aborts the operation and data of the targeted address range may be corrupted or lost due to the aborted erase or program operation.

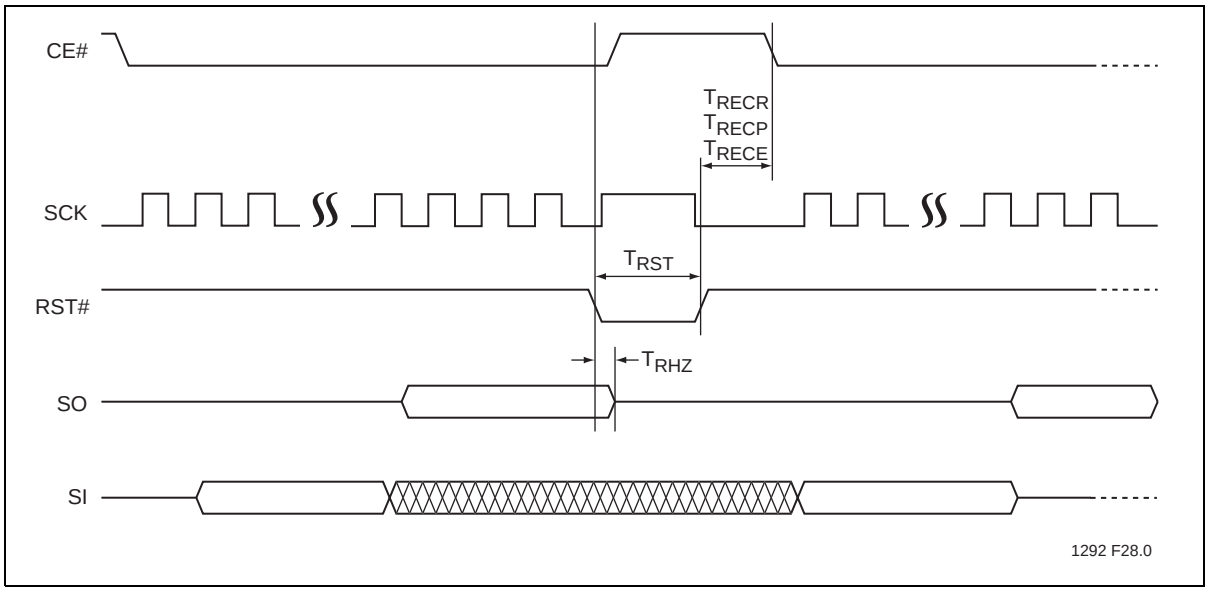

Figure 4: Reset Timing Diagram

Table 2: Reset Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{RST}	Reset Pulse Width	100		ns
T_{RHZ}	Reset to High-Z Output		105	ns
T_{RECR}	Reset Recovery from Read		100	ns
T_{RECP}	Reset Recovery from Program		10	µs
T_{RECE}	Reset Recovery from Erase		1	ms

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Hold Operation

The EHLD instruction enables the hold pin functionality of the RST#/HOLD# pin. Once converted to a hold pin, the RST#/HOLD# pin functions as a hold pin until the device is powered off and on. After the power cycle, the pin functionality returns as a reset pin (RST#) after the power on.

The HOLD# pin is used to pause a serial sequence using the SPI flash memory, but without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active low state. The HOLD# mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The HOLD mode ends when the HOLD# signal's rising edge coincides with the SCK active low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active low state, then the device exits from Hold mode when the SCK next reaches the active low state. See Figure 5 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven high during a Hold condition, the device returns to Standby mode. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low. See Figure 5 for Hold timing.

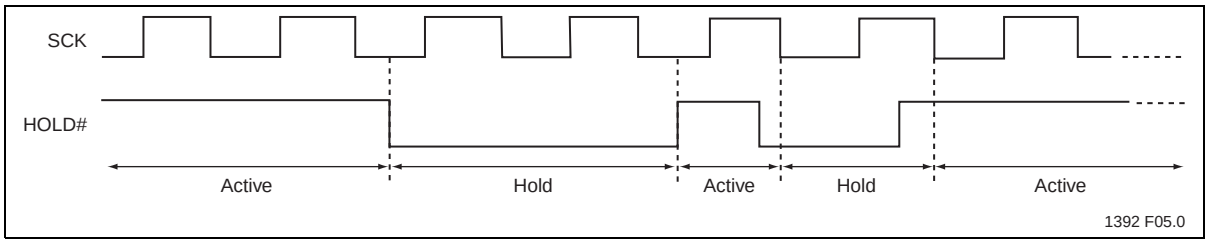

Figure 5: Hold Condition Waveform

Write Protection

SST25VF064C provides software Write protection. The Write Protect pin (WP#) enables or disables the lock-down function of the status register. The Block-Protection bits (BP3, BP2, BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 5 for the Block-Protection description.

Write Protect Pin (WP#)

The Write Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When WP# is driven low, the execution of the Write-Status-Register (WRSR) instruction is determined by the value of the BPL bit (see Table 3). When WP# is high, the lock-down function of the BPL bit is disabled.

Table 3: Conditions to execute Write-Status-Register (WRSR) Instruction

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

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Security ID

SST25VF064C offers a 256-bit Security ID (Sec ID) feature. The Security ID space is divided into two parts – one factory-programmed, 64-bit segment and one user-programmable 192-bit segment. The factory-programmed segment is programmed at SST with a unique number and cannot be changed. The user-programmable segment is left unprogrammed for the customer to program as desired.

Use the Program SID command to program the Security ID using the address shown in Table 7. Once programmed, the Security ID can be locked using the Lockout SID command. This prevents any future write to the Security ID.

The factory-programmed portion of the Security ID can never be programmed, and none of the Security ID can be erased.

Status Register

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the Memory Write protection. During an internal Erase or Program operation, the status register may be read only to determine the completion of an operation in progress. Table 4 describes the function of each bit in the software status register.

Table 4: Status Register

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 5)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 5)	1	R/W
4	BP2	Indicate current level of block write protection (See Table 5)	1	R/W
5	BP3	Indicate current level of block write protection (See Table 5)	1	R/W
6	SEC[1]	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0[1]	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are readable/writable	0	R/W

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1. The Security ID status will always be ‘1’ at power-up after a successful execution of the Lockout SID instruction; otherwise, the default at power up is ‘0’.

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Busy

The Busy bit determines whether there is an internal Erase or Program operation in progress. A ‘1’ for the Busy bit indicates the device is busy with an operation in progress. A ‘0’ indicates the device is ready for the next valid operation.

Write Enable Latch (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If the Write-Enable-Latch bit is set to ‘1’, it indicates the device is Write enabled. If the bit is set to ‘0’ (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Power-up
- Write-Disable (WRDI) instruction completion
- Write-Status Register instruction completion
- Page-Program instruction completion
- Dual-Input Page-Program instruction completion
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Program SID instruction completion
- Lockout SID instruction completion

Block Protection (BP3,BP2, BP1, BP0)

The Block-Protection (BP3, BP2, BP1, BP0) bits define the size of the memory area, as shown in Table 5, to be software protected against any memory Write (Program or Erase) operation. The Write-Status-Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits as long as WP# is high or the Block-Protect-Lock (BPL) bit is 0. Chip-Erase can only be executed if Block-Protection bits are all 0. After power-up, BP3, BP2, BP1 and BP0 are set to the defaults specified in Table 5.

Block Protection Lock-Down (BPL)

WP# pin driven low (V_{IL}), enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP3, BP2, BP1, and BP0 bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is “Don’t Care”. After power-up, the BPL bit is reset to 0.

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Security ID Status (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a Write command. The SEC is ‘1’ after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to ‘0.’

Table 5: Software Status Register Block Protection FOR SST25VF064C

Protection Level	Status Register Bit[1]				Protected Memory Address
	BP3	BP2	BP1	BP0	64 Mbit
None	0	0	0	0	None
Upper 1/128	0	0	0	1	7F0000H-7FFFFFH
Upper 1/64	0	0	1	0	7E0000H-7FFFFFH
Upper 1/32	0	0	1	1	7C0000H-7FFFFFH
Upper 1/16	0	1	0	0	780000H-7FFFFFH
Upper 1/8	0	1	0	1	700000H-7FFFFFH
Upper 1/4	0	1	1	0	600000H-7FFFFFH
Upper 1/2	0	1	1	1	400000H-7FFFFFH
All Blocks	1	0	0	0	000000H-7FFFFFH
All Blocks	1	0	0	1	000000H-7FFFFFH
All Blocks	1	0	1	0	000000H-7FFFFFH
All Blocks	1	0	1	1	000000H-7FFFFFH
All Blocks	1	1	0	0	000000H-7FFFFFH
All Blocks	1	1	0	1	000000H-7FFFFFH
All Blocks	1	1	1	0	000000H-7FFFFFH
All Blocks	1	1	1	1	000000H-7FFFFFH

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1. Default at power-up for BP3, BP2, BP1, and BP0 is ‘1111’. (All Blocks Protected)

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Instructions

Instructions are used to read, write (Erase and Program), and configure the SST25VF064C. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. The Write-Enable (WREN) instruction must be executed prior any Page-Program, Dual-Input Page-Program, Sector-Erase, Block-Erase, Write-Status-Register, Chip-Erase, Program SID, or Lockout SID instructions. The complete list of instructions is provided in Table 6.

All instructions are synchronized off a high to low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read-Status-Register instructions). Any low to high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

Table 6: Device Operation Instructions

Instruction	Description	Op Code Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞
Fast-Read Dual I/O	Read Memory with Dual Address Input and Data Output	1011 1011b (BBH)	3[3]	1[3]	1 to ∞[3]
Fast-Read Dual-Output	Read Memory with Dual Output	0011 1011b (3BH)	3	1	1 to ∞[3]
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞
Sector-Erase[4]	Erase 4 KByte of memory array	0010 0000b (20H)	3	0	0
32 KByte Block-Erase[5]	Erase 32KByte block of memory array	0101 0010b (52H)	3	0	0
64 KByte Block-Erase[6]	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0
Page-Program	To Program 1 to 256 Data Bytes	0000 0010b (02H)	3	0	1 to 256
Dual-Input Page-Program	To Program 1 to 256 Data Bytes	1010 0010b (A2H)	3	0	1 to 128[3]
RDSR[7]	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞
EWSR	Enable-Write-Status-Register	0101 0000b (50H)	0	0	0
WRSR	Write-Status-Register	0000 0001b (01H)	0	0	1
WREN	Write-Enable	0000 0110b (06H)	0	0	0
WRDI	Write-Disable	0000 0100b (04H)	0	0	0
RDID[8]	Read-ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞
JEDEC-ID	JEDEC ID Read	1001 1111b (9FH)	0	0	3 to ∞
EHLD	Enable HOLD# pin functionality of the RST#/HOLD# pin	1010 1010b (AAH)	0	0	0
Read SID	Read Security ID	1000 1000b (88H)	1	1	1 to 32
Program SID[9]	Program User Security ID area	1010 0101b (A5H)	1	0	1 to 24
Lockout SID[9]	Lockout Security ID Programming	1000 0101b (85H)	0	0	0

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1. One bus cycle is eight clock periods.

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2. Address bits above the most significant bit can be either V_{IL} or V_{IH}.
3. One bus cycle is four clock periods (dual operation)
4. 4KByte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
5. 32KByte Block Erase addresses: use A_{MS}-A_{15}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
6. 64KByte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
8. Manufacturer's ID is read with A_0 = 0, and Device ID is read with A_0 = 1. All other address bits are 00H. The Manufacturer's ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.
9. Requires a prior WREN command.

Read (33 MHz)

The Read instruction, 03H, supports up to 33 MHz Read. The device outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. For example, once the data from address location 7FFFFFH has been read, the next output will be from address location 000000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits A_{23}-A_0. CE# must remain active low for the duration of the Read cycle. See Figure 6 for the Read sequence.

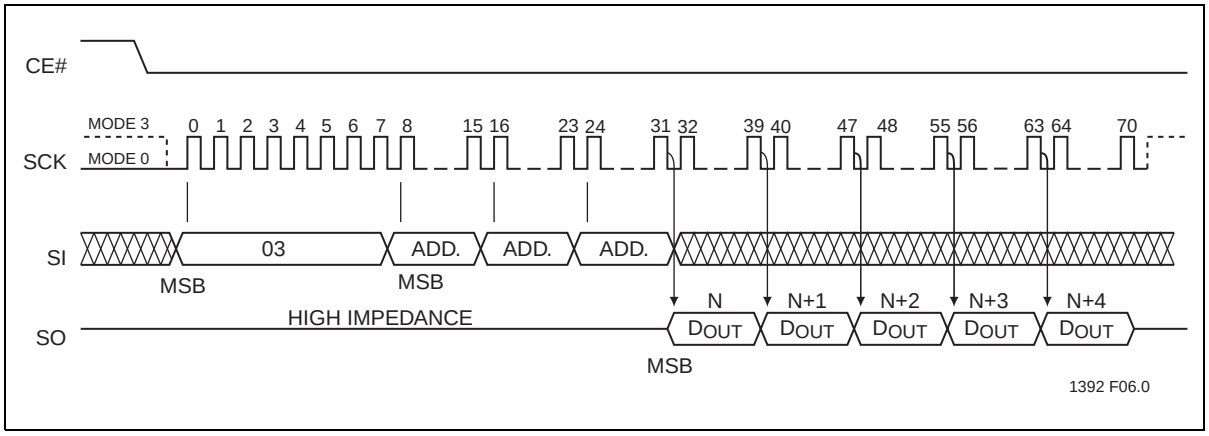

Figure 6: Read Sequence

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High-Speed Read (80 MHz)

The High-Speed Read instruction supporting up to 80 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits A_{23}-A_0 and a dummy byte. CE# must remain active low for the duration of the High-Speed Read cycle. See Figure 7 for the High-Speed Read sequence.

Following a dummy cycle, the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. For example, once the data from address location 7FFFFFH is read, the next output is from address location 000000H.

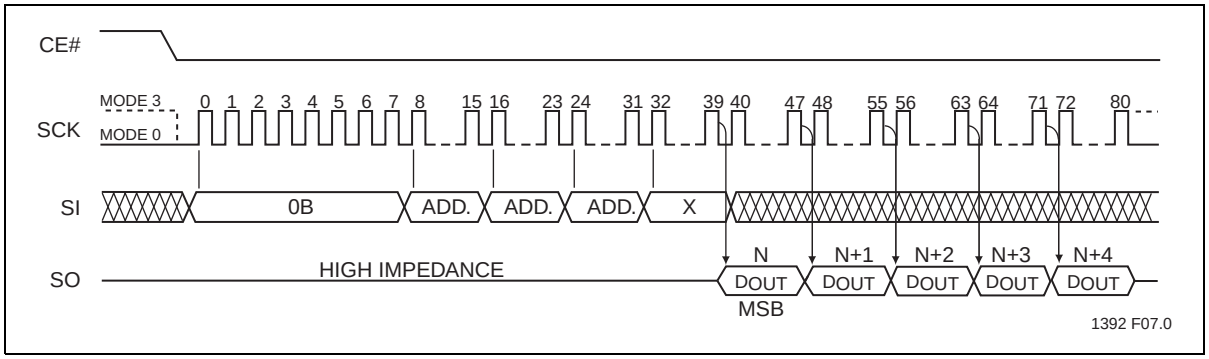

Figure 7: High-Speed Read Sequence

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Fast-Read Dual-Output (75 MHz)

The Fast-Read Dual-Output (3BH) instruction outputs data up to 75 MHz from the SIO_0 and SIO_1 pins. To initiate the instruction, execute an 8-bit command (3BH) followed by address bits A23-A0 and a dummy byte on SI/SIO_0. Following a dummy cycle, the Fast-Read Dual-Output instruction outputs the data starting from the specified address location on the SIO_1 and SIO_0 lines. SIO_1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO_0 outputs even data bits D6, D4, D2, and D0. CE# must remain active low for the duration of the Fast-Read Dual-Output instruction cycle. See Figure 8 for the Fast-Read Dual-Output sequence.

The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wraparound) of the address space. for 64 Mbit density, once the data from address location 7FFFFFH has been read the next output will be from address location 000000H.

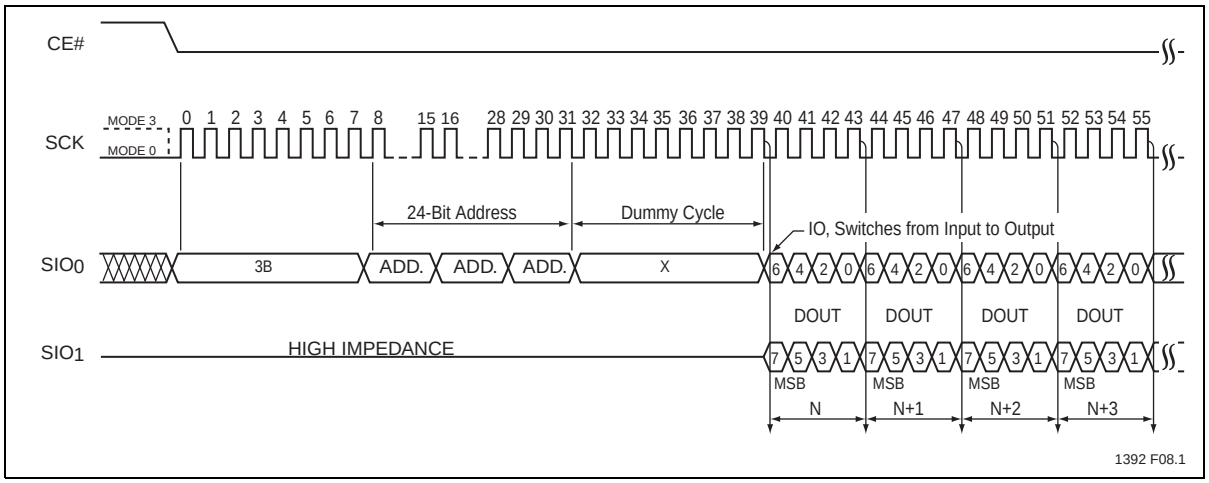

Figure 8: Fast-Read Dual Output Sequence

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Fast-Read Dual I/O (50 MHz)

The Fast-Read Dual I/O (BBH) instruction reduces the total number of input clock cycles, which results in faster data access. The device is first selected by driving Chip Enable CE# low. Fast-Read Dual I/O is initiated by executing an 8-bit command (BBH) on SI/SIO_0, thereafter, the device accepts address bits A23-A0 and a dummy byte on SI/SIO_0 and SO/SIO_1. It offers the capability to input address bits A23-A0 at a rate of two bits per clock. Odd address bits A23 through A1 are input on SIO_1 and even address bits A22 through A0 are input on SIO_0, alternately For example the most significant bit is input first followed by A23/22, A21/A20, and so on. Each bit is latched at the same rising edge of the Serial Clock (SCK). The input data during the dummy clocks is “don’t care”. However, the SIO_0 and SIO_1 pin must be in high-impedance prior to the falling edge of the first data output clock.

Following a dummy cycle, the Fast-Read Dual I/O instruction outputs the data starting from the specified address location on the SIO_1 and SIO_0 lines. SIO_1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO_0 outputs even data bits D6, D4, D2, and D0 per clock edge. CE# must remain active low for the duration of the Fast-Read Dual I/O instruction cycle. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wraparound) of the address space. For example, once the data from address location 7FFFFFH is read, the next output is from address location 000000H. See Figure 9 for the Fast-Read Dual I/o sequence.

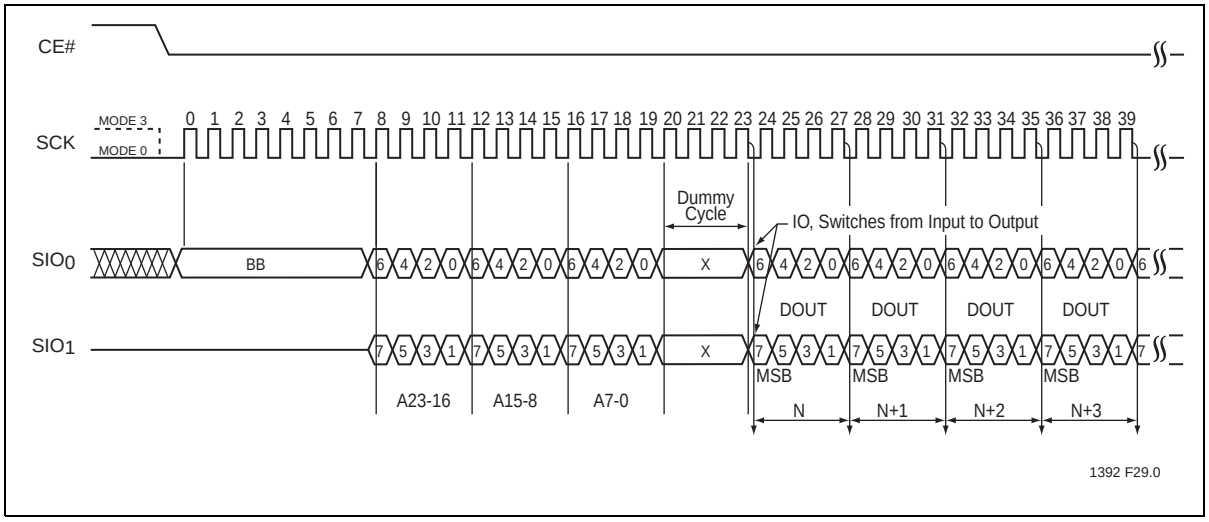

Figure 9: Fast-Read Dual I/O Sequence

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Page-Program

The page-Program instruction programs up to 256 bytes of data in the memory. The selected page address must be in the erased state (FFH) before initiating the Page-Program operation. A Page-Program applied to a protected memory area will be ignored.

Prior to the program operation, the Write-Enabled (WREN) instruction must be executed. CE# must remain active low for the duration of the Page-Program instruction. The Page-Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits A23-A0. Following the address, at least one byte is needed for the data input. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T_{PP} for the completion of the internal self-timed Page-Program operation. See Figure 10 for the Page-Program sequence.

For Page-Program, the memory range for SST25VF064C is set in 256 byte page boundaries. The device handles shifting of more than 256 bytes of data by keeping the last 256 bytes of data shifted as the correct data to be programmed. If the target address for the Page-Program instruction is not the beginning of the page boundary (A7-A0 are not all zero) and the number of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs will wrap around and will be programmed at the start of that target page.

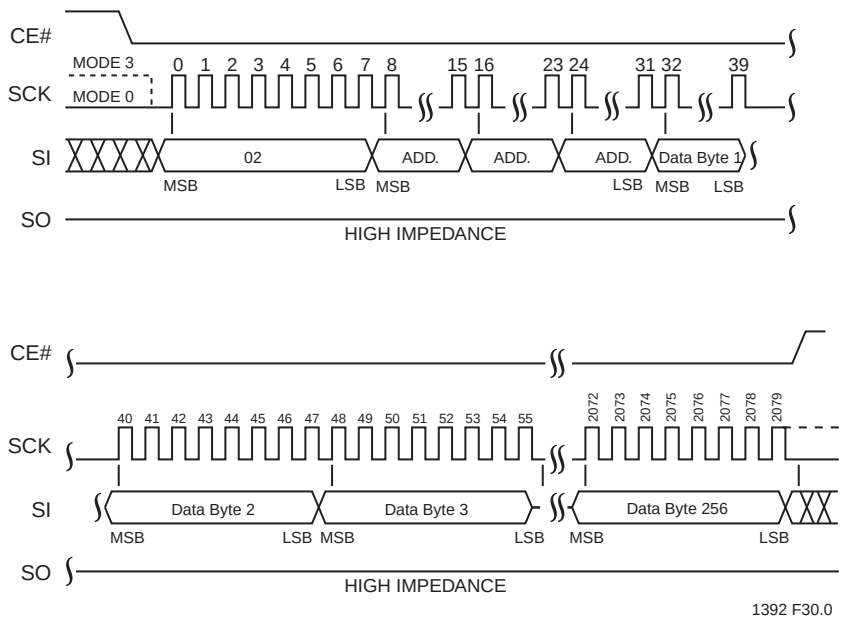

Figure 10: Page-Program Sequence

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Dual-Input Page-Program (50 MHz)

Dual-Input Page-Program instruction A2H, doubles the data input transfer of normal Page-Program instruction and supports up to 50MHz. Data to be programmed is entered using two I/O pins, SIO_1 and SIO_0. Prior to the program operation the Write-Enable (WREN) instruction must be executed. The Dual-Input Page-Program instruction is entered by driving CE# low, followed by the instruction code, A2H, three address bytes, and at least one data byte on serial data inputs SIO_1 and SIO_0 pins. CE# must be driven low for the entire duration of the sequence. The Dual-Input Page-Program instruction programs up to 256 bytes of data in the memory. The selected page address must be in the erased state (FFH) before initiating the Page-Program operation. A Dual-Input Page-Program applied to a protected memory area will be ignored.

CE# must be driven high after the seventh and eight bit of the last data byte has been latched; otherwise, the dual input program instruction is not executed. Once CE# is driven high the instruction is executed and the user may poll the WEL and Busy bit of the software status register or wait TPP for the completion of the internal self-timed Page-Program operation. See Figure 10 for the Dual-Input-Page-Program sequence.

For Dual-Input Page-Program, the memory range for the SST25VF064C is set in 256 byte page boundaries. The device handles shifting of more than 256 bytes of data by keeping the last 256 bytes of data shifted as the correct data to be programmed. If the target address for the Page-Program instruction is not the beginning of the page boundary (A7-A0 are not all zero) and the number of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs will wrap around and will be programmed at the start of that target page.

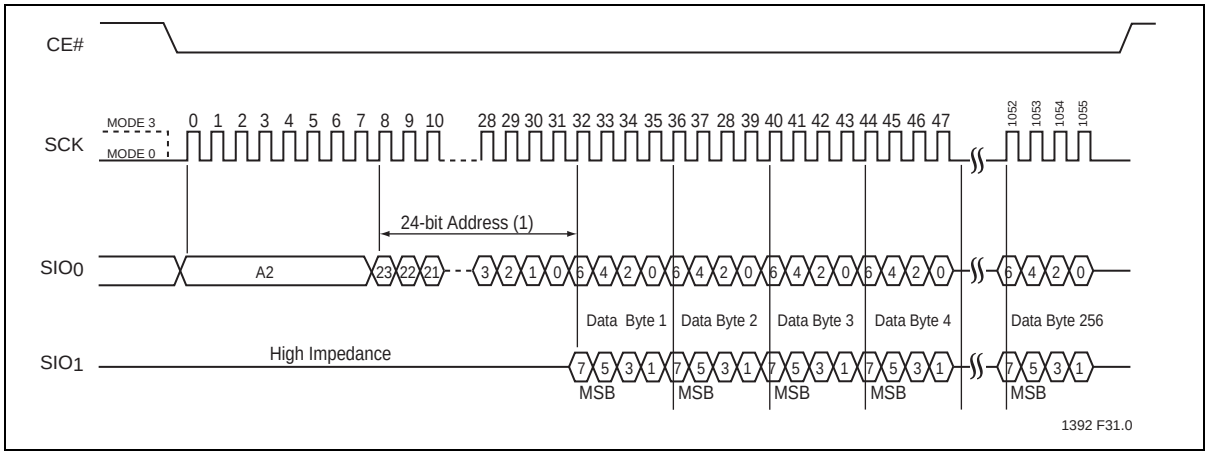

Figure 11: Dual-Input Page-Program

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Sector-Erase

The Sector-Erase instruction clears all bits in the selected 4 KByte sector to FFH. A Sector-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The Sector-Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits A_{23}-A_0. Address bits A_{MS}-A_{12} (A_{MS} = Most Significant address) are used to determine the sector address (SA_X), remaining address bits can be V_{IL} or $V_{IH.}$ CE# must be driven high before the instruction is executed. Poll the Busy bit in the software status register or wait T_{SE} for the completion of the internal self-timed Sector-Erase cycle. See Figure 12 for the Sector-Erase sequence.

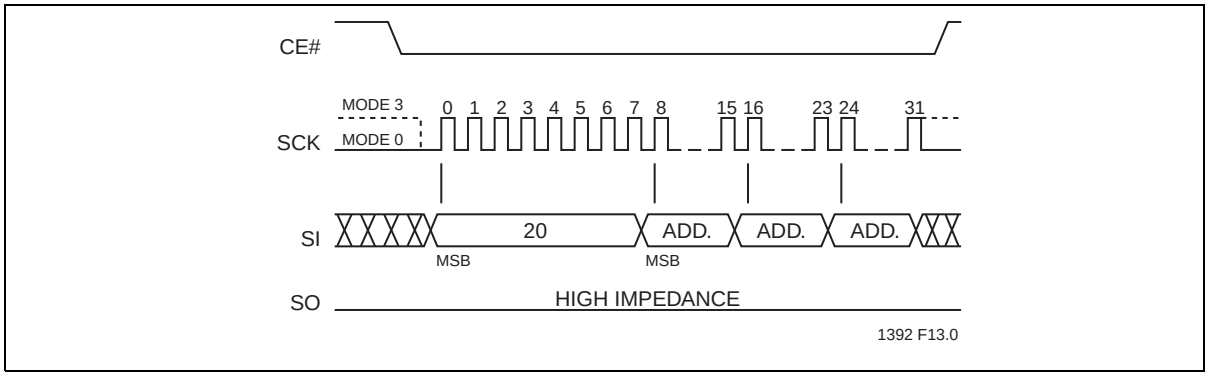

Figure 12: Sector-Erase Sequence

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32-KByte and 64-KByte Block-Erase

The 32-KByte Block-Erase instruction clears all bits in the selected 32 KByte block to FFH. A Block-Erase instruction applied to a protected memory area will be ignored. The 64-KByte Block-Erase instruction clears all bits in the selected 64 KByte block to FFH. A Block-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The 32-KByte Block-Erase instruction is initiated by executing an 8-bit command, 52H, followed by address bits A_{23}-A_0. Address bits A_{MS}-A_{15} (A_{MS} = Most Significant Address) are used to determine block address (BA_X), remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The 64-KByte Block-Erase instruction is initiated by executing an 8-bit command D8H, followed by address bits A_{23}-A_0. Address bits A_{MS}-A_{15} are used to determine block address (BA_X), remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. Poll the Busy bit in the software status register or wait T_{BE} for the completion of the internal self-timed 32-KByte Block-Erase or 64-KByte Block-Erase cycles. See Figure 13 for the 32-KByte Block-Erase sequence and Figure 14 for the 64-KByte Block-Erase sequence.

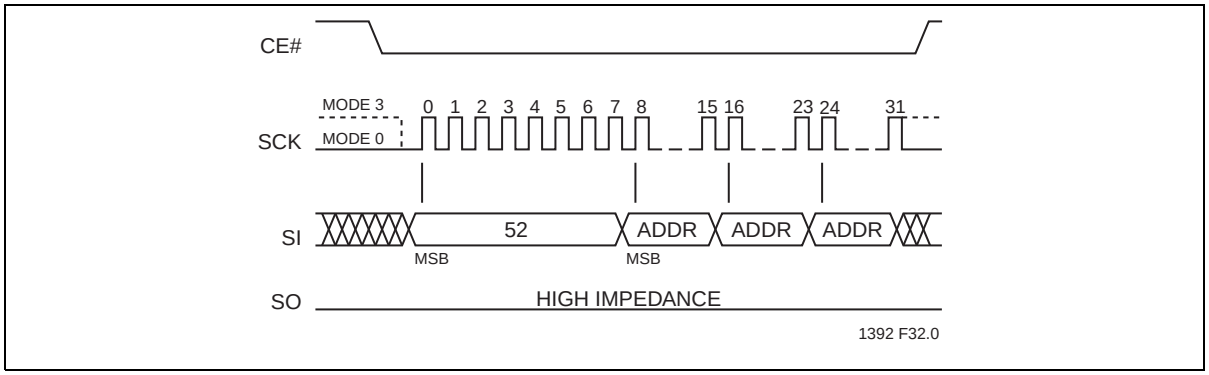

Figure 13: 32-KByte Block-Erase Sequence

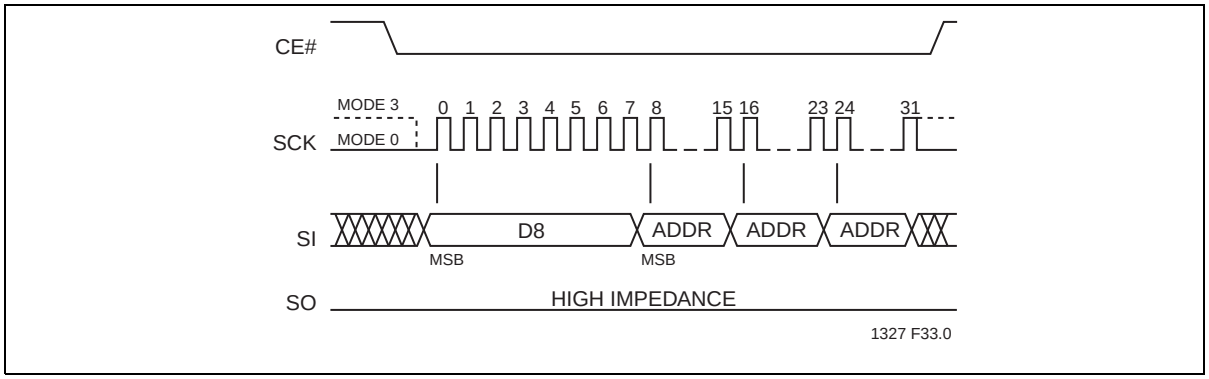

Figure 14: 64-KByte Block-Erase Sequence

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Chip-Erase

The Chip-Erase instruction clears all bits in the device to FFH. A Chip-Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of the Chip-Erase instruction sequence. Initiate the Chip-Erase instruction by executing an 8-bit command, 60H or C7H. CE# must be driven high before the instruction is executed. Poll the Busy bit in the software status register or wait T_{CE} for the completion of the internal self-timed Chip-Erase cycle. See Figure 15 for the Chip-Erase sequence.

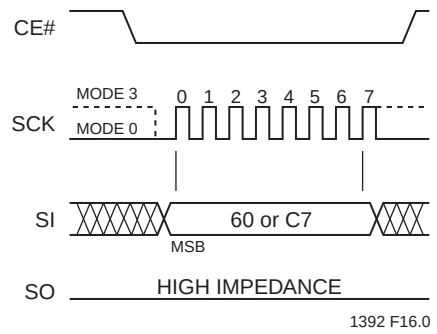

Figure 15: Chip-Erase Sequence

Read Security ID

To execute a Read SID operation, the host drives CE# low, sends the Read SID command cycle (88H), one address cycle, and then one dummy cycle. Each cycle is eight bits long, most significant bit first.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal, starting from the specified address location. The data output stream is continuous through all SID addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the last SID address is reached, then outputs wrap around until CE# goes high.

Lockout Security ID

The Lockout SID instruction prevents any future changes to the Security ID. Prior to the Lockout SID operation, the Write-Enable (WREN) instruction must be executed. To execute a Lockout SID, the host drives CE# low, sends the Lockout SID command cycle (85H), then drives CE# high. A cycle is 8 bits long, most significant bit first. The user may poll the BUSY bit in the software status register or waits T_{PSID} for the completion of the Lockout SID operation.

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Program Security ID

The Program SID instruction programs one to 24 bytes of data in the user-programmable, Security ID space. The device ignores a Program SID instruction pointing to an invalid or protected address, see Table 7. Prior to the program operation, execute WREN.

To execute a Program SID operation, the host drives CE# low, sends the Program SID command cycle (A5H), one address cycle, the data to be programmed, then drives CE# high. The programmed data must be between 1 to 24 Bytes and in whole Byte increments. To determine the completion of the internal, self-timed Program SID operation, poll the BUSY bit in the software status register, or wait T_{PSID} for the completion of the internal self-timed Program SID operation.

Table 7: Program Security ID

Program Security ID	Address Range
Pre-Programmed at factory	00H – 07H
User Programmable	08H – 1FH

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Read-Status-Register (RDSR)

The Read-Status-Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation. When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are properly received by the device. CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read-Status-Register is continuous with ongoing clock cycles until it is terminated by a low to high transition of the CE#. See Figure 16 for the RDSR instruction sequence.

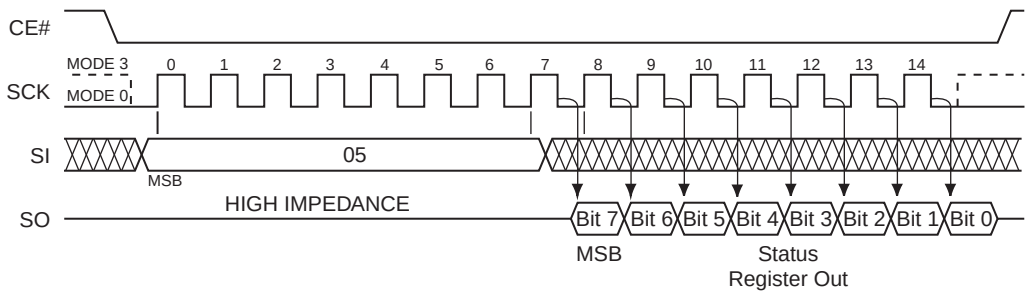

Figure 16: Read-Status-Register (RDSR) Sequence

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Write-Enable (WREN)

The Write-Enable (WREN) instruction sets the Write-Enable-Latch bit in the Status Register to ‘1’ allowing Write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. The WREN instruction may also be used to allow execution of the Write-Status-Register (WRSR) instruction; however, the Write-Enable-Latch bit in the Status Register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven high before the WREN instruction is executed.

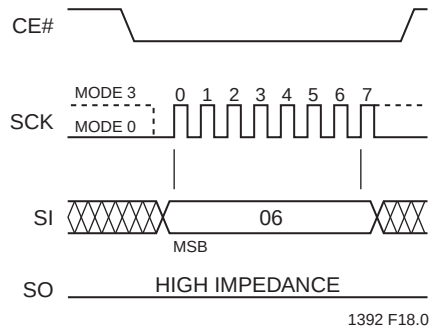

Figure 17: Write Enable (WREN) Sequence

Write-Disable (WRDI)

The Write-Disable (WRDI) instruction resets the Write-Enable-Latch bit to ‘0,’ thereby, preventing any new Write operations. The WRDI instruction will not terminate any program or erase operation in progress. Any program or erase operation in progress will continue after executing the WRDI instruction. CE# must be driven high before the WRDI instruction is executed.

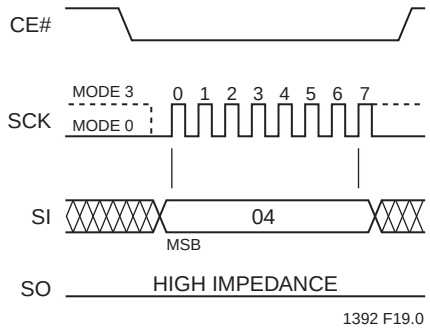

Figure 18: Write Disable (WRDI) Sequence

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Enable-Write-Status-Register (EWSR)

The Enable-Write-Status-Register (EWSR) instruction arms the Write-Status-Register (WRSR) instruction and opens the status register for alteration. The Write-Status-Register instruction must be executed immediately after the execution of the Enable-Write-Status-Register instruction. This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like software data protection (SDP) command structure which prevents any accidental alteration of the status register values. CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

Write-Status-Register (WRSR)

The Write-Status-Register instruction writes new values to the BP3, BP2, BP1, BP0, and BPL bits of the status register. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 19 for EWSR or WREN and WRSR instruction sequences.

Executing the Write-Status-Register instruction will be ignored when WP# is low and BPL bit is set to ‘1’. When the WP# is low, the BPL bit can only be set from ‘0’ to ‘1’ to lock-down the status register, but cannot be reset from ‘1’ to ‘0’. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, BP1, BP2, and BP3 bits in the status register can all be changed. As long as BPL bit is set to ‘0’ or WP# pin is driven high (V_{IH}) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to ‘1’ to lock down the status register as well as altering the BP0, BP1, BP2, and BP3 bits at the same time. See Table 3 for a summary description of WP# and BPL functions.

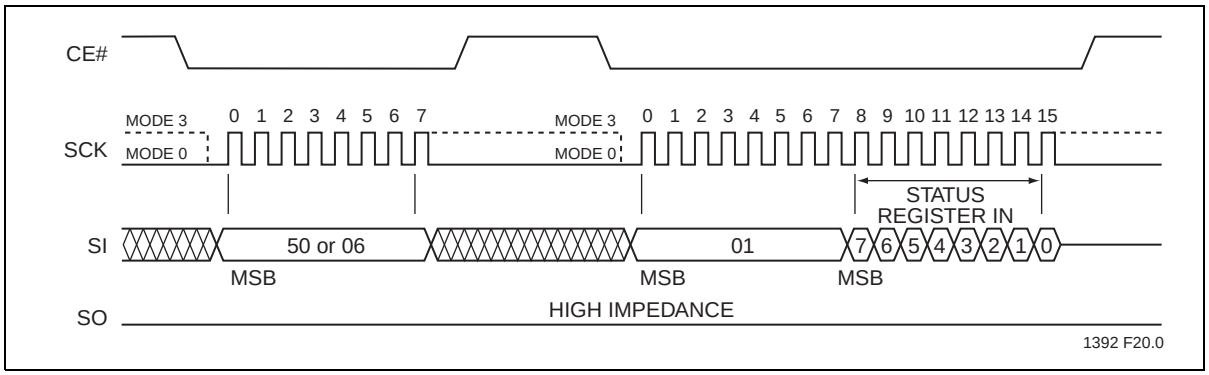

Figure 19: Enable-Write-Status-Register (EWSR) or Write-Enable (WREN) and Write-Status-Register (WRSR) Sequence

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Enable-Hold (EHLD)

The 8-bit command, AAH, Enable-Hold instruction enables the HOLD functionality of the RST#/HOLD# pin. CE# must remain active low for the duration of the Enable-Hold instruction sequence. CE# must be driven high before the instruction is executed. See Figure 20 for the Enable-Hold instruction sequence.

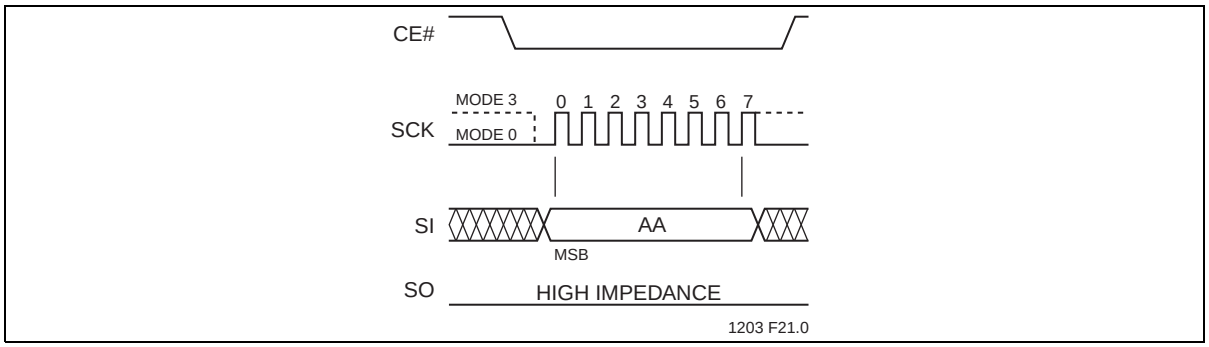

Figure 20: Enable-Hold Sequence

Read-ID (RDID)

The Read-ID instruction (RDID) identifies the device as SST25VF064C and manufacturer as SST. The device information can be read from executing an 8-bit command, 90H or ABH, followed by address bits A_{23}-A_0. Following the Read-ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H. Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low to high transition on CE#. After CE# is driven high, the device is put into standby mode.

Refer to Tables 8 and 9 for device identification data.

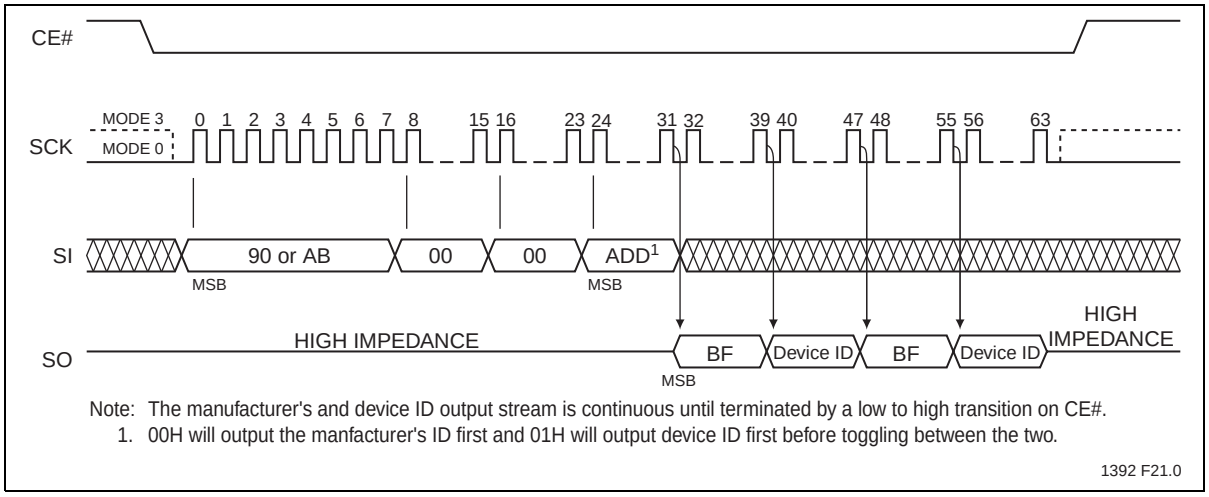

Figure 21: Read-ID Sequence

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Table 8: Product Identification

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID SST25VF064C	00001H	4BH

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JEDEC Read-ID

The JEDEC Read-ID instruction identifies the device as SST25VF064C and the manufacturer as SST. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, the 8-bit manufacturer's ID, BFH, is output from the device. After that, a 24-bit device ID is shifted out on the SO pin. Byte 1, BFH, identifies the manufacturer as SST. Byte 2, 25H, identifies the memory type as SPI Serial Flash. Byte 3, 4BH, identifies the device as SST25VF064C. The instruction sequence is shown in Figure 22. The JEDEC Read ID instruction is terminated by a low to high transition on CE# at any time during data output.

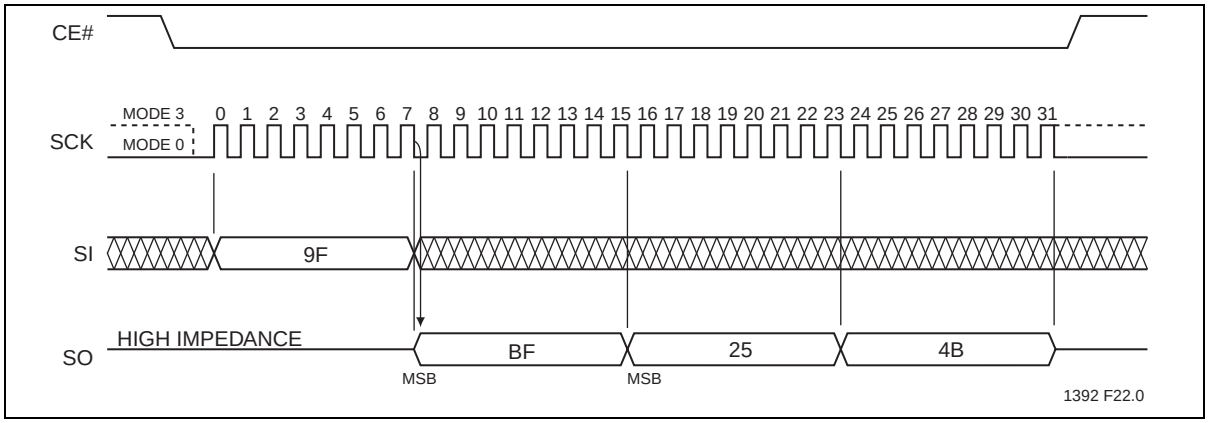

Figure 22: JEDEC Read-ID Sequence

Table 9: JEDEC Read-ID Data

Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
BFH	25H	4BH

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Electrical Specifications

Absolute Maximum Stress Ratings Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[1]. . . . . 50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

Table 10: Operating Range

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

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Table 11: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
5ns	C_L = 30 pF

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1. See Figure 28

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Table 12: DC Operating Characteristics (VDD = 2.7-3.6V)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DDR}	Read Current		12	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@33 MHz, SO = open
I_{DDR2}	High-Speed Read Current		25	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@80 MHz, SO = open
I_{DDR3}	Fast-Read Dual-Output/Dual I/O Current		25	mA	CE# = 0.1 V_{DD}/0.9 V_{DD}@75/50 MHz
I_{DDW}	Program and Erase Current		25	mA	CE# = V_{DD}
I_{SB1}	Standby Current		20	µA	CE# = V_{DD}, V_{IN} = V_{DD} or V_{SS}
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD} = V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD} = V_{DD} Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min

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Table 13: Capacitance (T_A = 25°C, f = 1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 14: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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Table 15: AC Operating Characteristics

Symbol	Parameter	33 MHz		50 MHz		75/80 MHz		Units
		Min	Max	Min	Max	Min	Max	
F_{CLK}[1]	Serial Clock Frequency High-Speed Read		33		50		75/80	MHz
T_{SCKH}	Serial Clock High Time	13		9		6		ns
T_{SCKL}	Serial Clock Low Time	13		9		6		ns
T_{SCKR}[2]	Serial Clock Rise Time (Slew Rate)	0.1		0.1		0.1		V/ns
T_{SCKF}	Serial Clock Fall Time (Slew Rate)	0.1		0.1		0.1		V/ns
T_{CES}[3]	CE# Active Setup Time	5		5		5		ns
T_{CEH}[3]	CE# Active Hold Time	5		5		5		ns
T_{CHS}[3]	CE# Not Active Setup Time	5		5		5		ns
T_{CHH}[3]	CE# Not Active Hold Time	5		5		5		ns
T_{CPH}	CE# High Time	50		50		50		ns
T_{CHZ}[4]	CE# High to High-Z Output		7		7		7	ns
T_{CLZ}	SCK Low to Low-Z Output	0		0		0		ns
T_{DS}	Data In Setup Time	3		3		2		ns
T_{DH}	Data In Hold Time	5		5		4		ns
T_{HLS}	HOLD# Low Setup Time	5		5		5		ns
T_{HHS}	HOLD# High Setup Time	5		5		5		ns
T_{HLH}	HOLD# Low Hold Time	5		5		5		ns
T_{HHH}	HOLD# High Hold Time	5		5		5		ns
T_{HZ}[4]	HOLD# Low to High-Z Output		7		7		7	ns
T_{LZ}[4]	HOLD# High to Low-Z Output		7		7		7	ns
T_{OH}	Output Hold from SCK Change	0		0		0		ns
T_V	Output Valid from SCK		15		10		6	ns
T_{SE}	Sector-Erase		25		25		25	ms
T_{BE}	Block-Erase		25		25		25	ms
T_{SCE}	Chip-Erase		50		50		50	ms
T_{PP}	Page-Program		2.5		2.5		2.5	ms
T_{PSID}	Program Security ID		1.0		1.0		1.0	ms

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1. Maximum clock frequency for Read Instruction, 03H, is 33 MHz
   Maximum clock frequency Fast-Read Dual-Output (3BH) is 75 MHz
   Maximum clock frequency Fast-Read Dual I/O (BBH) is 50 MHz
   Maximum clock frequency for High-Speed Read, OBH, is 80 MHz
   Maximum clock frequency for Dual-Input Page-Program, A2H, is 50 Mhz
2. Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements
3. Relative to SCK.
4. Not 100% tested in production.

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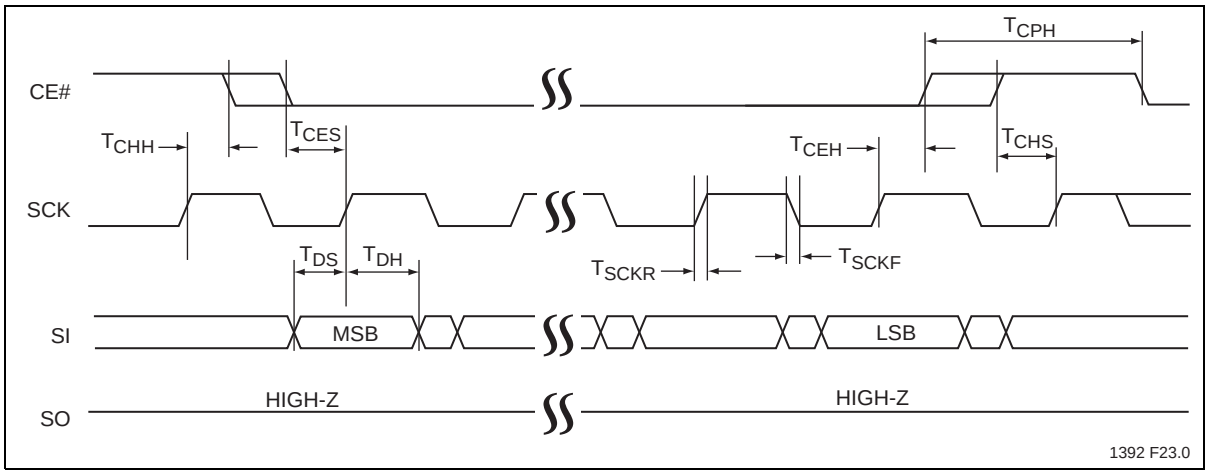

Figure 23: Serial Input Timing Diagram

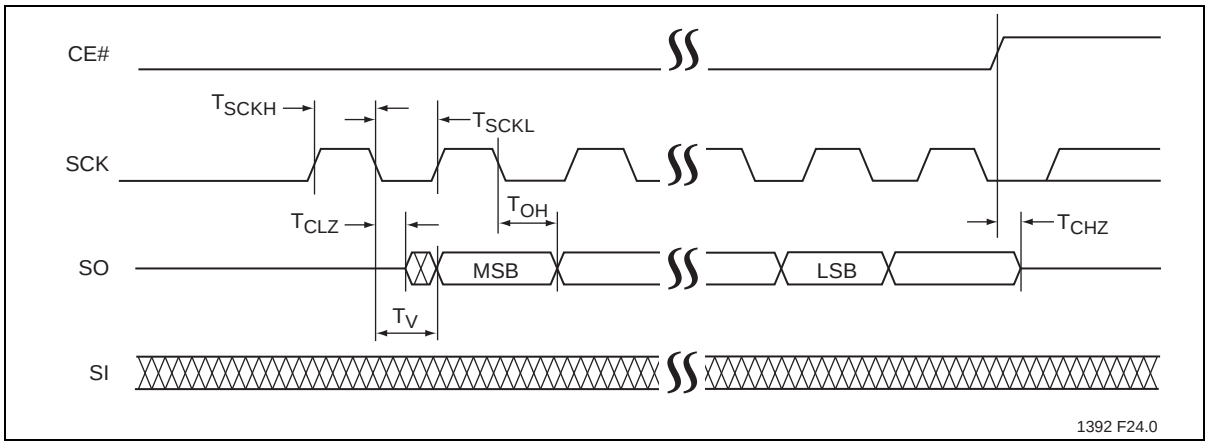

Figure 24: Serial Output Timing Diagram

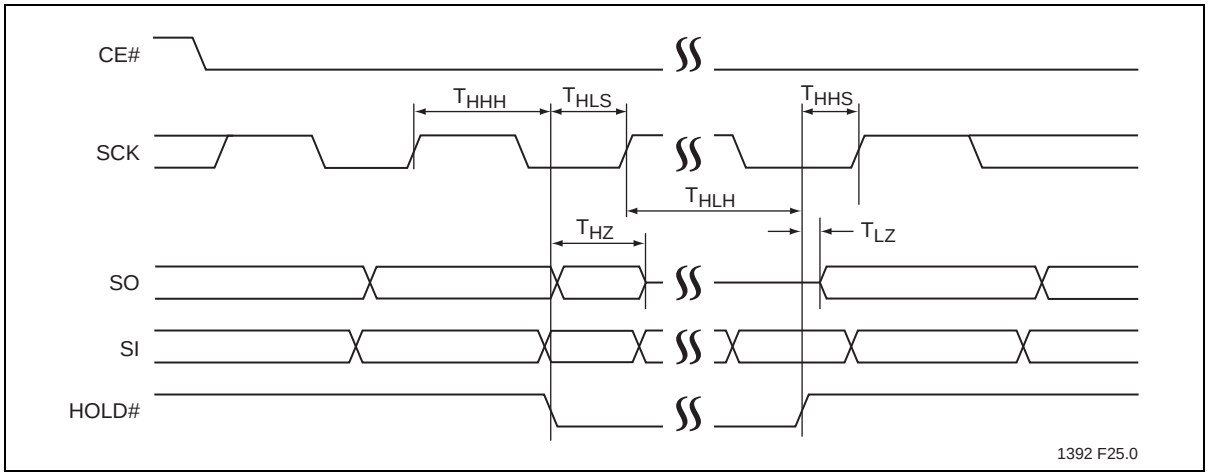

Figure 25: Hold Timing Diagram

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Power-Up Specifications

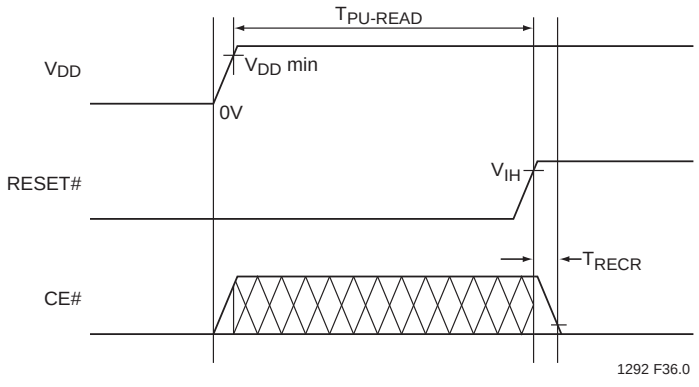
All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3V in less than 300 ms). If the VDD ramp rate is slower than 1V/100 ms, a hardware reset is required. The recommended V_{DD} power-up to RESET# high time should be greater than 100 µs to ensure a proper reset. See Table 16 and Figures 26 and 27 for more information.

Table 16: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	100	µs
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	100	µs

T16.0 25036

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



Note: See Table 2

Figure 26: Power-Up Reset Diagram

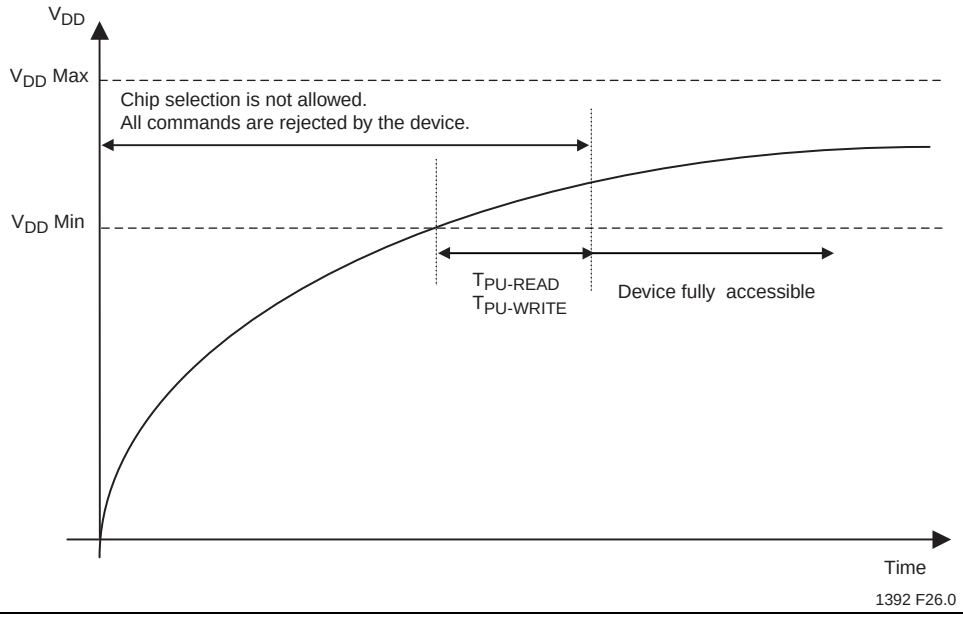


Figure 27: Power-up Timing Diagram

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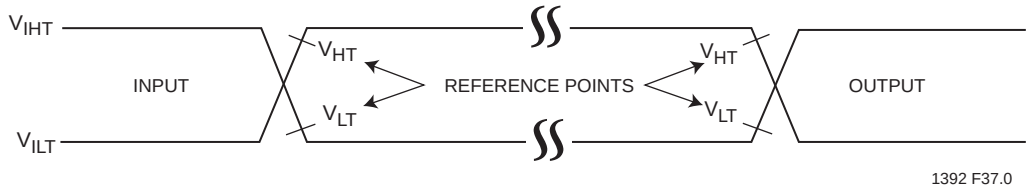

AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic “1” and V_{ILT} ($0.1V_{DD}$) for a logic “0”. Measurement reference points for inputs and outputs are V_{HT} ($0.6V_{DD}$) and V_{LT} ($0.4V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

Figure 28: AC Input/Output Reference Waveforms

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Product Ordering Information

SST 25 VF 064C - 80 - 4I - SAE

XX XX XXXX - XX - XX - XXX

Environmental Attribute
E[1] = non-Pb

Package Modifier
C = 16 leads
A = 8 contacts

Package Type
S = SOIC (300 mil body width)
Q2 = WSON (6mm x 8mm)
S3 = SOIC (200 mil body width)

Temperature Range
C = Commercial = 0°C to +70°C
I = Industrial = -40°C to +85°C

Minimum Endurance
4 = 10,000 cycles

Operating Frequency
80 = 80 MHz

Version
C = Page-Program

Device Density
064 = 64 Mbit

Voltage
V = 2.7-3.6V

Product Series
25 = Serial Peripheral Interface flash memory

1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST25VF064C

SST25VF064C-80-4I-SCE

SST25VF064C-80-4I-S3AE

SST25VF064C-80-4I-Q2AE SST25VF064C-80-4C-Q2AE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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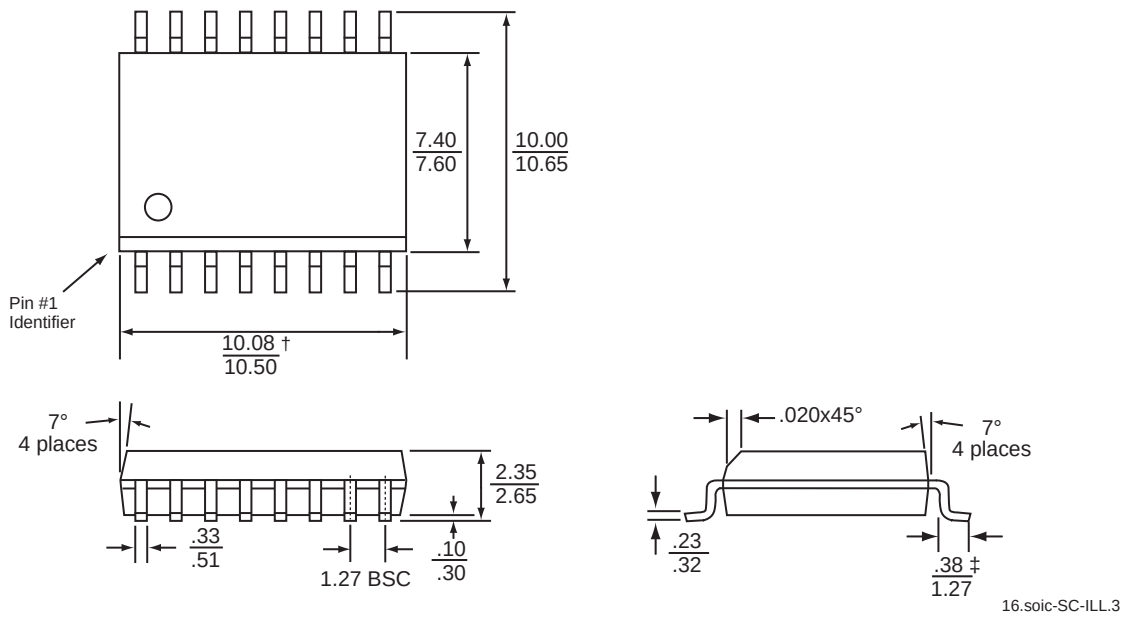
Packaging Diagrams



Note: 1. Complies with JEDEC publication 95 MS-013 AA dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is 10.10; SST min (10.08) is **less** stringent
‡ = JEDEC min is 0.40; SST min (0.38) is **less** stringent
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15mm at the package ends, and 0.25mm between leads.

Figure 29: 16-Lead Plastic Small Outline Integrated Circuit (SOIC) SST Package Code SC

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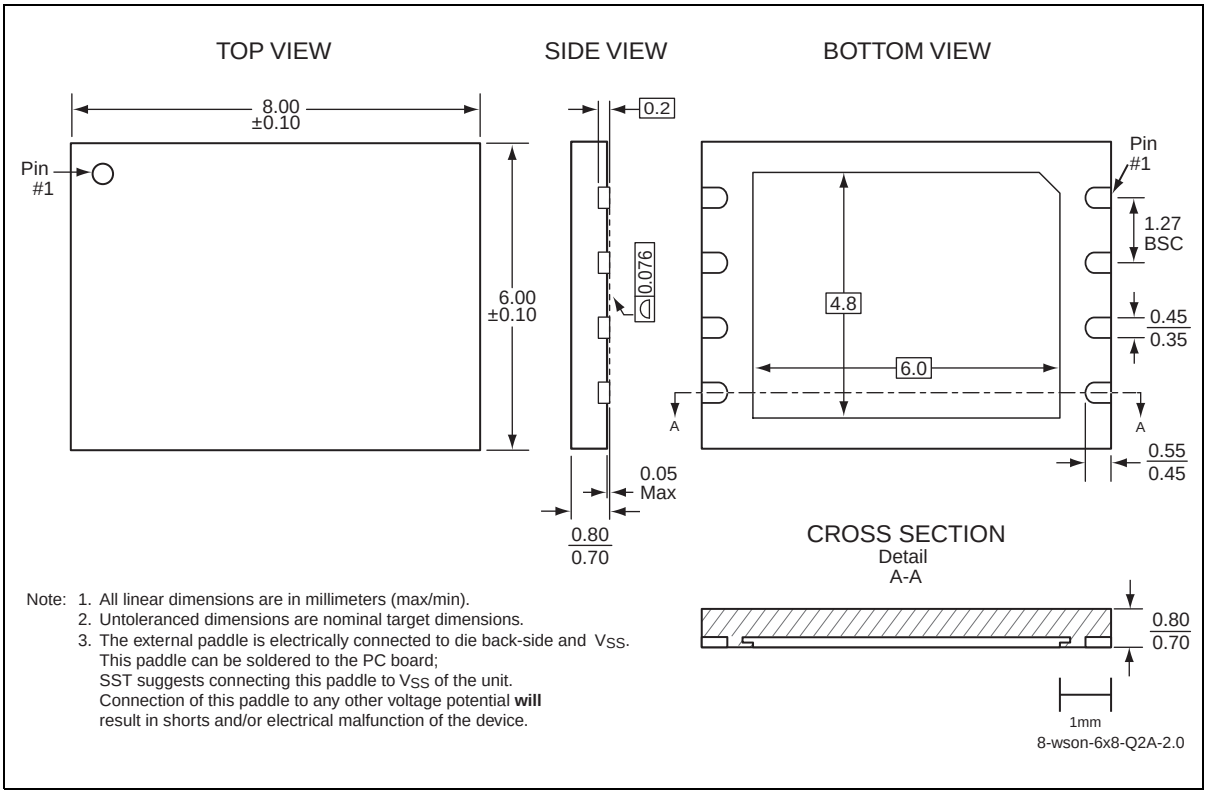

Note: 1. All linear dimensions are in millimeters (max/min).
2. Untoleranced dimensions are nominal target dimensions.
3. The external paddle is electrically connected to die back-side and V_{SS}. This paddle can be soldered to the PC board; SST suggests connecting this paddle to V_{SS} of the unit. Connection of this paddle to any other voltage potential **will** result in shorts and/or electrical malfunction of the device.

Figure 30: 8-Contact Very-very-thin Small Outline No-lead (WSON) SST Package Code: Q2A

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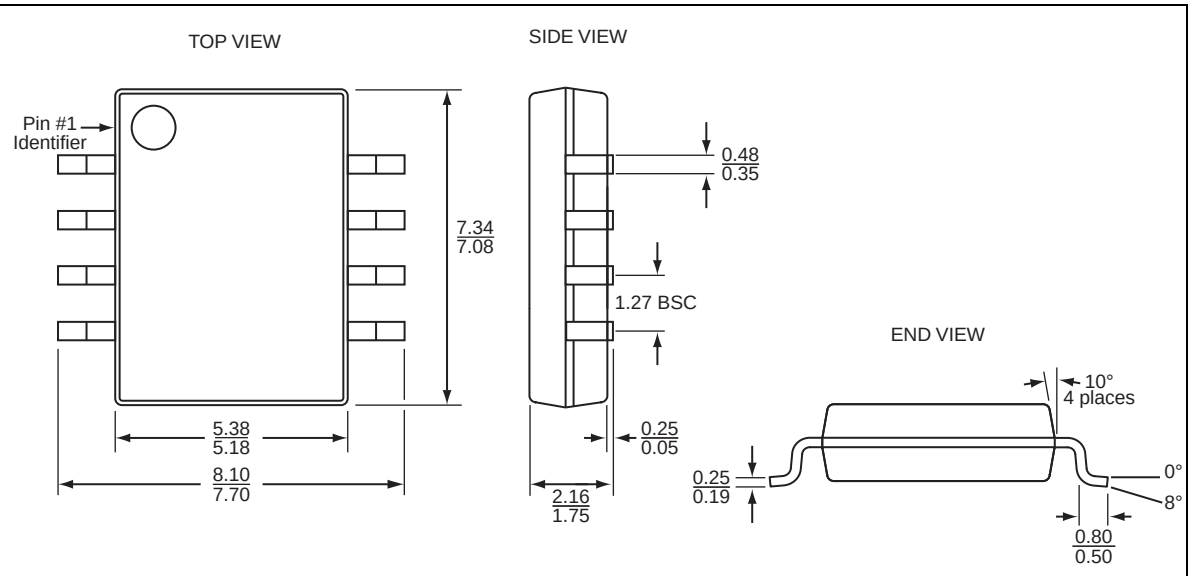

Note: 1. All linear dimensions are in millimeters (max/min).
2. Coplanarity: 0.1 mm
3. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

Figure 31: 8-Lead Small Outline Integrated Circuit (SOIC) SST Package Code S3A

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Table 17: Revision History

Number	Description	Date
00	• Initial release of data sheet	Sep 2008
01	• Added 8-contact WSON Q2A package • Added Security ID information throughout • Updated Table 6 on page 11 • Revised “Fast-Read Dual-Output (75 MHz)” on page 14 and “Fast-Read Dual I/O (50 MHz)” on page 15. • Modified Figure 8 on page 14. • Updated Table 15 on page 29 • Added Commercial temperature range in Features, page 1; Operating Range, page 23; and Product Ordering Information, page 28	Apr 2009
02	• Added 8-lead SOIC S3A package	Sep 2009
03	• Changed Max Value of I_{DDR2} and I_{DDW} to 25mA in Table 12 on page 28	Dec 2009
04	• Revised Table 6 on page 11 • Updated address information on page 31.	Apr 2010
A	• Applied new document format. • Released document under letter revision system. • Updated Spec number from S71392 to DS25036	Jun 2011
B	• Correct pin description for 8-lead SOIC on page 4	Aug 2012
C	• EOL of all SST25VF064C devices. • Document marked obsolete.	Apr 2015

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Memory sizes denote raw storage capacity; actual usable capacity may be less.

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