

μPD720115

ASSP (Four-port USB2.0 Hub Controller)

R19DS0078EJ0410

Rev.4.10

Sep 25, 2023

1. OVERVIEW

The μPD720115 is a USB 2.0 hub controller that complies with the Universal Serial Bus (USB) Specification Revision 2.0 and operates at up to 480 Mbps. The device incorporates Renesas' market proven design expertise in USB 2.0 interface technologies and market proven USB 2.0 hub core. It integrates several commonly required external components, making it ideally suited for applications with limited PCB space. In addition, the μPD720115 incorporates Renesas' low-power technologies and supports all mainstream battery charging specifications.

1.1 Features

- Compliant with Universal Serial Bus Specification Revision 2.0, which is released by USB Implementers Forum, Inc
 - Supports the following data rates as follows: Low-speed (1.5 Mbps) / Full-speed (12 Mbps) / High-speed (480 Mbps)
 - Supports USB 2.0 link power management (LPM: L0/L1/L2/L3)
- Supports four downstream ports
- Configurable downstream port counts of 2, 3, or 4 ports
- Supports all VBUS control options
 - Individual or global over-current detection
 - Individual or ganged power control
- Supports USB 2.0 Compound (non-removable) devices by I/O pin configuration
- Supports clock output (24 MHz) for Compound (non-removal) device on downstream ports
- Supports Energy Star and EuP specifications for low-power PC peripheral system
- Single 5 V Power Supply
 - On chip LDO for 3.3 V from 5 V input and for 1.05 V from 3.3 V input
- System clock: 24 MHz Crystal or Oscillator
- Supports USB Battery Charging Specification Revision 1.2 and other portable devices
 - DCP mode of BC 1.2
 - CDP mode of BC 1.2
 - ACA-Dock function of BC 1.2
 - China Mobile Phone Chargers
 - EU Mobile Phone Chargers
 - Apple iOS products
 - Other major portable devices
- Small Footprint
 - Small and low pin count package with simple pin assignment for PCB layout
 - Integration of many peripheral components
 - Integrated termination resistors for USB
 - Direct routing of all USB signal traces to connector pins using one layer of the PCB
- Provides SUSPEND status output
- Supports Port Indicator control (only Green color)

1.2 Ordering Information

Part Number	Package	Packing form	Operating Temperature	Remark
μ PD720115K8-611-BAK-A	40-pin QFN (6 × 6)	Fraction (any vacancy in the tray and any free space in the carton)	0 to +85°C	Lead-free product
μ PD720115K8-611-BAK-M1-A		Full Carton (tray and Carton is packed with every product)		
μ PD720115K8-711-BAK-A		Fraction	-40 to +85°C	Lead-free product
μ PD720115K8-711-BAK-M1-A		Full Carton		

1.3 Block Diagram

Figure 1-1. μPD720115 Block Diagram

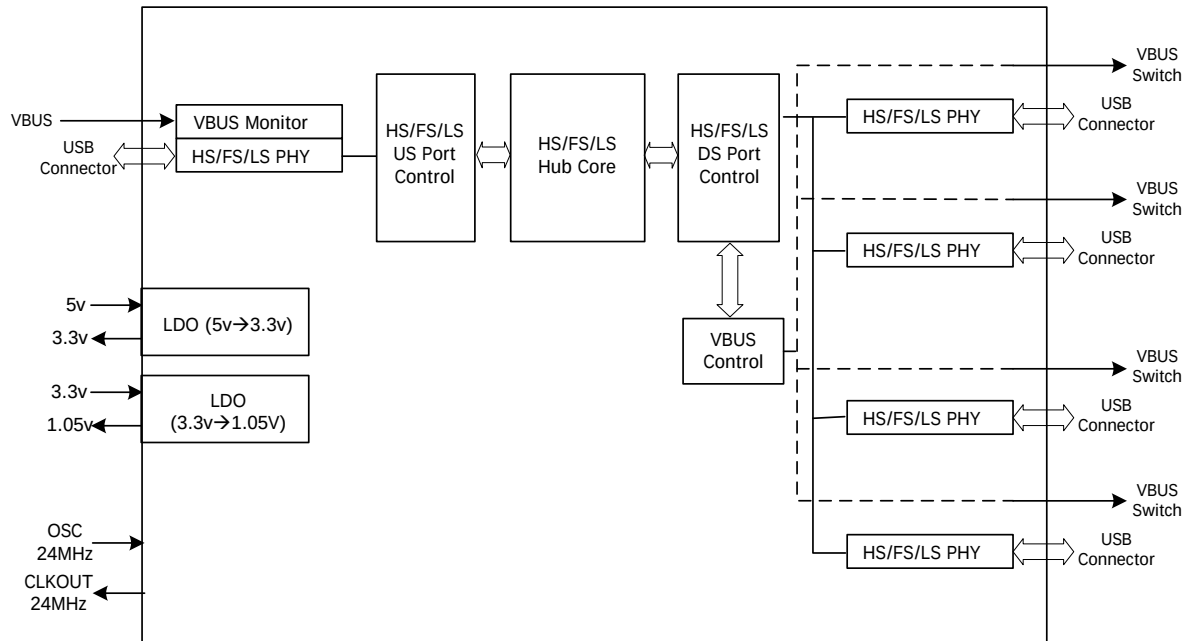


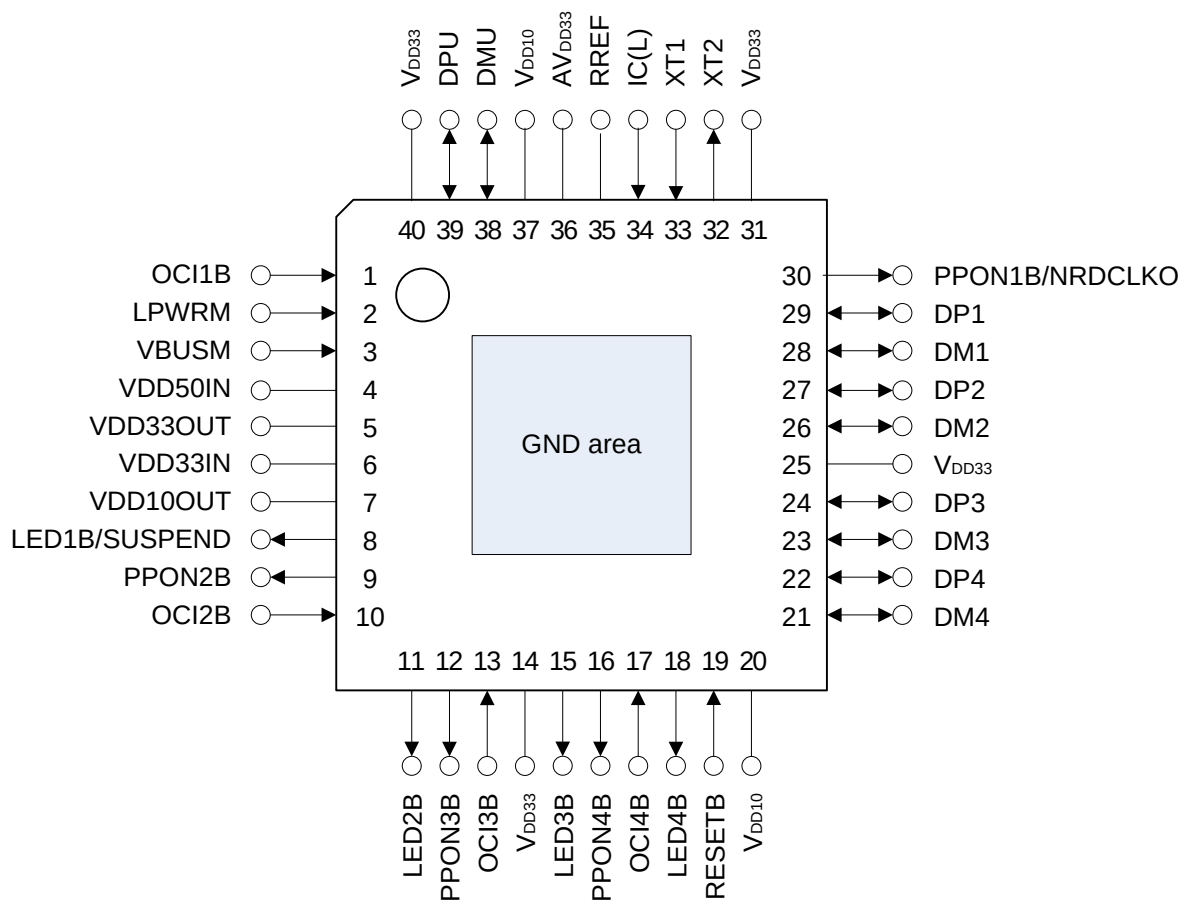
Table 1-1. Terminology

Block Name	Description
HS/FS/LS PHY	High-/Full-/Low-speed transceiver
VBUS Monitor	Monitors the VBUS voltage level of the upstream port.
HS/FS/LS US Port Control	Upstream port control logic for High-/Full-/Low-speed
HS/FS/LS Hub Core	Central control logic for HS/FS/LS-Hub.
HS/FS/LS DS Port Control	Downstream port control logic for HS/FS/LS
VBUS Control	Controls all the port power switches
LDO	Low Drop Out regulator integrated in this hub

1.4 Pin Configuration

- 40-pin QFN (6 × 6)
μPD720115K8-611-BAK-A
μPD720115K8-611-BAK-M1-A
μPD720115K8-711-BAK-A
μPD720115K8-711-BAK-M1-A

Figure 1-2. Pin Configuration of μPD720115 (Top View)



2. PIN FUNCTION

This section describes each pin functions.

Strapping information in the tables shows the pin can be used to configure the functional settings of this controller when it is pulled up/down. See μPD720115 User's Manual for detail.

2.1 Power Supply

Pin Name	Pin No.	I/O Type	Function
VDD10	20, 37	Power	1.05 V power supply for Core Logic
VDD33	14, 25, 31, 40	Power	3.3 V power supply for IO buffers
AVDD33	36	Power	3.3 V power supply for Analog circuit
VDD50IN	4	Power	LDO 5 V Input Need to be connected to GND, when on-chip LDO is not used.
VDD33OUT	5	Power	LDO 3.3 V Output. It is necessary to put 4.7 μF capacitor on this pin. It is prohibited to connect this pin to other external parts.
VDD33IN	6	-	LDO 3.3 V Input Need to be connected to VDD33, when on-chip LDO is not used.
VDD10OUT	7	-	LDO 1.05 V Output. It is necessary to put 4.7 μF capacitor on this pin. It is prohibited to connect this pin to other external parts.

2.2 Analog Interface

Pin Name	Pin No.	I/O Type	Function
RREF	35	-	Reference Voltage Input for USB 2.0 RREF must be connected to a 1.6 kΩ resistor with a tolerance of +/- 1%. It is strongly recommended to use a single resistor of 1.6 kΩ, versus the combined resistance with multiple resistors to achieve the value and tolerance.

2.3 System Clock

Pin Name	Pin No.	I/O Type	Function
XT1	33	IN	External Oscillator Input Connect to 24 MHz crystal. Alternatively, this pin can accept a 3.3 V Oscillator input.
XT2	32	OUT	External Oscillator Output Connect to 24 MHz crystal. When using single-ended clock input to XT1, this pin should be left open.

2.4 System Interface Pins

Pin Name	Pin No.	I/O Type	Active Level	Function
VBUSM	3	IN	High	Upstream Port VBUS Monitor
LPWRM	2	IN	N/A	Local power monitor input 0: Local power is lost. 1: Local power is supplied. This value is set to Self Powered field of Device Status dynamically.
LED1B/SUSPEND	8	I/O	Low	[Function] LED1B is LED control output signal to indicate port enable. 0: Port is enabled. Hi-Z: Port is disabled. SUSPEND is Suspend state output. (no LED support) 0: This device is in suspend state. 1: This device is not in suspend state.
				[Pin strapping option] This pin is used to select LED support. 0: LED support is disabled and Suspend state output is enabled. 1: LED support is enabled and Suspend state output is disabled.
LED2B	11	I/O	Low	[Function] LED control output signal to indicate port enable. 0: Port is enabled. Hi-Z: Port is disabled. When ACA-Dock function is selected, this pin is used for ACA-Dock function. This signal is the control of RID. (High active, Push-pull output) See User's Manual for additional details about ACA-Dock function.
				[Pin strapping option] See User's Manual for additional details.
LED3B	15	I/O	Low	[Function] LED control output signal to indicate port enable. 0: Port is enabled. Hi-Z: Port is disabled. When ACA-Dock function is selected, this pin is used for ACA-Dock function. This signal is the control of VBUS. (Low active, Open-drain output) See User's Manual for additional details about ACA-Dock function.
				[Pin strapping option] See User's Manual for additional details.
LED4B	18	I/O	Low	[Function] LED control output signal to indicate port enable. 0: Port is enabled. Hi-Z: Port is disabled.
				[Pin strapping option] See User's Manual for additional details.
RESETB	19	IN	Low	Chip Reset Input

2.5 USB Port Control Pins

Pin Name	Pin No.	I/O Type	Active Level	Function
OCI1B, OCI2B, OCI3B, OCI4B	1, 10, 13, 17	IN	Low	[Function] Over Current Input 0: Over-current condition is detected. 1: Non over-current condition is detected.
				[Pin strapping option] These pins are used to select non-removable setting. 0: Port is non-removal. 1: Port is removal.
PPON1B/NRDCKO	30	OUT	Low	[Function] PPON1B is Port Power Control 0: Power supply for VBUS is on. Hi-Z: Power supply for VBUS is off. NRDCKO is output 24MHz clock, when enabled. See User's Manual for additional details.
PPON2B, PPON3B, PPON4B	9, 12, 16	I/O	Low	[Function] Port Power Control 0: Power supply for VBUS is on. Hi-Z: Power supply for VBUS is off.
				[Pin strapping option] These pins are used for pin strapping option of port management. PPON4B, PPON3B: Number of Ports 00: Port 1 and 2 are active. 01: Port 1, 2 and 3 are active. 11: Port 1, 2, 3, and 4 are active. PPON2B: Gang/Individual Power Control 0: gang power management mode. 1: individual power management mode.

Note OCI1B operates as over current detection pin under gang power management mode. Thus over current detection is not available in the case that Port1 is set as Non-removable device port.

2.6 USB Data Pins

Pin Name	Pin No.	I/O Type	Function
DMU	38	I/O	USB 2.0 Upstream D- signal for High-/Full-/Low-speed
DPU	39	I/O	USB 2.0 Upstream D+ signal for High-/Full-/Low-speed
DM1, DM2, DM3, DM4	28, 26, 23, 21	I/O	USB 2.0 Downstream D- signal for High-/Full-/Low-speed
DP1, DP2, DP3, DP4	29, 27, 24, 22	I/O	USB 2.0 Downstream D+ signal for High-/Full-/Low-speed

2.7 Test Pin

Pin Name	Pin No.	I/O Type	Active Level	Function
IC(L)	34	IN	High	Test Pin to be connected to GND

3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

- 3.3 V input buffer

IC(L)

- 3.3 V input Schmitt buffer

RESETB, OCI2B, OCI3B, OCI4B

- 3.3 V $I_{OLH} = 4$ mA output buffer

PPON1B/NRDCLKO

Note : When PPON1B is selected, Nch Open Drain buffer is selected for output. When NRDCLKO is selected, Push-Pull type buffer is selected for output.

- 3.3 V $I_{OL} = 4$ mA bi-directional buffer (Nch Open Drain)

PPON2B, PPON3B, PPON4B

- 3.3 V $I_{OL} = 12$ mA bi-directional buffer

LED1B/SUSPEND, LED2B, LED3B, LED4B

Note : When LED1B is selected, Nch Open-Drain buffer type is selected for LED1B / LED2B / LED3B / LED4B output. When SUSPEND is selected, Push-Pull type buffer is selected for output.

- 3.3 V input Schmitt buffer (5 V tolerant)

VBUSM, LPWRM, OCI1B

- 3.3 V oscillator interface

XT1, XT2

- USB 2.0 interface

DPU, DMU, DP(4:1), DM(4:1)

- LDO Interface (5V to 3.3V)

VDD33OUT, VDD50IN

- LDO Interface (3.3V to 1.05V)

VDD10OUT, VDD33IN

3.2 Terminology

Table 3-1. Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33} , V_{DD10} , AV_{DD33}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a VDD pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Table 3-2. Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33} , V_{DD10} , AV_{DD33}	Indicates the voltage range for normal logic operations occur when GND = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage which is applied to an input pin of the device to indicate the high level state for normal operation of the input buffer. * If a voltage that is equal to or greater than the "Min." value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage which is applied to an input pin of the device to indicate the low level state for normal operation of the input buffer. * If a voltage that is equal to or less than the "Max." value is applied, the input voltage is guaranteed as low level voltage.
Input rise time	T_{ri}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device rises from 10% to 90%.
Input fall time	T_{fi}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device falls from 90% to 10%.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.

Table 3-3. Term Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.

3.3 Absolute Maximum Ratings

Table 3-4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Units
Power supply voltage	V_{DD33} , AV_{DD33}		–0.5 to +4.6	V
	V_{DD10}		–0.5 to +1.4	V
	V_{DD50IN}		5.5	V
	V_{DD33IN}			
Input voltage, 3.3 V buffer	V_I	$V_I < V_{DD33} + 0.5 \text{ V}$	–0.5 to +4.6	V
Output voltage, 3.3 V buffer	V_O	$V_O < V_{DD33} + 0.5 \text{ V}$	–0.5 to +4.6	V
Input voltage, 5 V tolerant buffer	V_I	$V_I < V_{DD33} + 3.0 \text{ V}$	–0.5 to +6.6	V
Output current	I_O	4 mA Type	8	mA
	I_O	12 mA Type	24	mA
Storage temperature	T_{stg}		–65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

3.4 Recommended Operating Ranges

Table 3-5. Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating voltage With external power source	V_{DD33} , AV_{DD33}		3.0	3.3	3.6	V
	V_{DD10}		0.9975	1.05	1.1025	V
Operating voltage With on-chip Regulators	V_{DD50IN}		4.4	5.0	5.25	V
Operating voltage With on-chip Regulators	V_{DD33IN}		3.0	3.3	3.6	V
High-level input voltage	V_{IH}		2.0		$V_{DD33}+0.3$	V
Low-level input voltage	V_{IL}		-0.3		0.8	V
Input rise time	T_{ri}	Normal Buffer	0		200	ns
		Schmitt Buffer	0		10	ms
Input fall time	T_{fi}	Normal Buffer	0		200	ns
		Schmitt Buffer	0		10	ms
Operating ambient temperature (μ PD720115K8-611-BAK-A, μ PD720115K8-611-BAK-M1-A)	T_A		0		+85	°C
Operating ambient temperature (μ PD720115K8-711-BAK-A, μ PD720115K8-711-BAK-M1-A)	T_A		-40		+85	°C

3.5 DC Characteristics

Table 3-6. DC Characteristics ($V_{DD33} = 3.3 \text{ V} \pm 10\%$, $V_{DD10} = 1.05 \text{ V} \pm 5\%$, $T_A = -0 \text{ to } +70^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Max.	Units
Off-state output current	I_{OZ}	$V_I = V_{DD33} \text{ or GND}$		± 10	μA
Input leakage current	I_I	$V_I = V_{DD33} \text{ or GND}$		± 10	μA
Low-level output voltage	V_{OL}	$I_{OL} = 0 \text{ mA}$		0.1	V
High-level output voltage	V_{OH}	$I_{OH} = 0 \text{ mA}$	$V_{DD33} - 0.1$		V

Table 3-7. USB Interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z _{HSDRV}		40.5	49.5	Ω
Input Levels for Low-/Full-speed:					
High-level input voltage (drive)	V _{IH}		2.0		V
High-level input voltage (floating)	V _{IHZ}		2.7	3.6	V
Low-level input voltage	V _{IL}			0.8	V
Differential input sensitivity	V _{DI}	(D+) – (D–)	0.2		V
Differential common mode range	V _{CM}	Includes V _{DI} range	0.8	2.5	V
Output Levels for Low-/Full-speed:					
High-level output voltage	V _{OH}	RL of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V _{OL}	RL of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V _{OSE1}		0.8		V
Output signal crossover point voltage	V _{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V _{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V _{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V _{HSCM}		–50	+500	mV
High-speed differential input signaling level	See Figure 3-4				
Output Levels for High-speed:					
High-speed idle state	V _{HSOI}		–10	+10	mV
High-speed data signaling high	V _{HSOH}		360	440	mV
High-speed data signaling low	V _{HSOL}		–10	+10	mV
Chirp J level (differential signal)	V _{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V _{CHIRPK}		–900	–500	mV

Figure 3-1. Differential Input Sensitivity Range for Low-/Full-speed

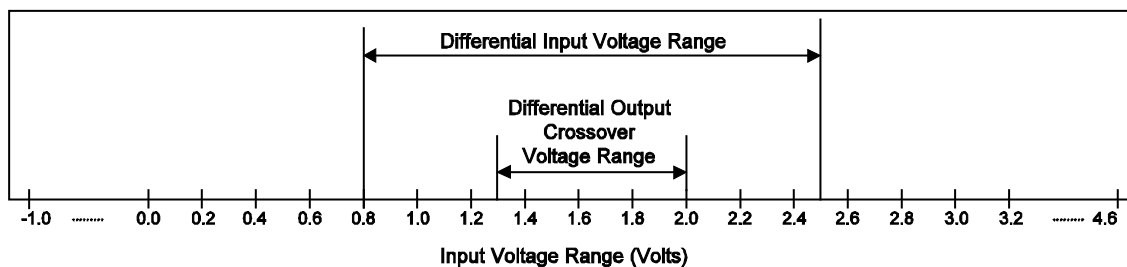


Figure 3-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

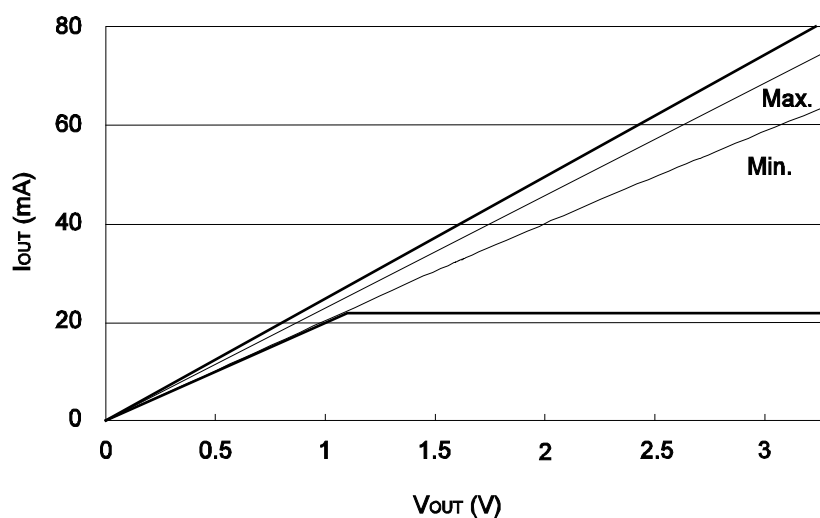


Figure 3-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

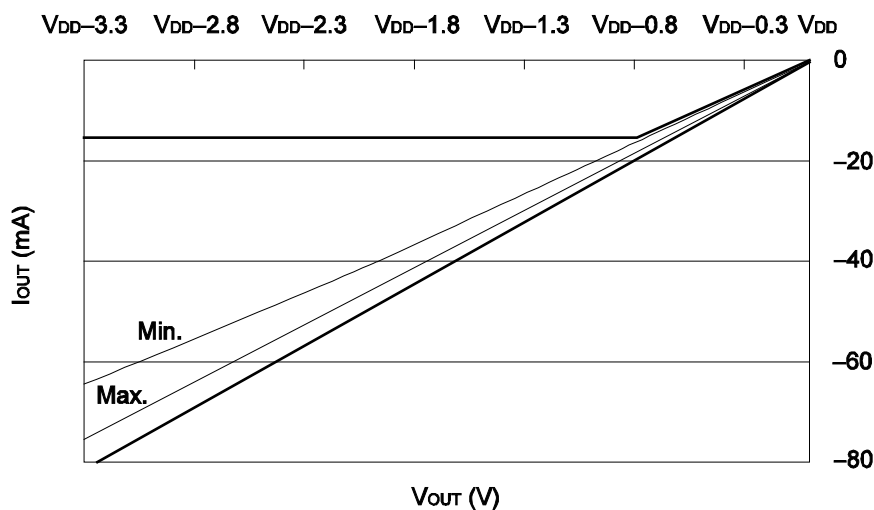


Figure 3-4. Receiver Sensitivity for Transceiver at DP/DM

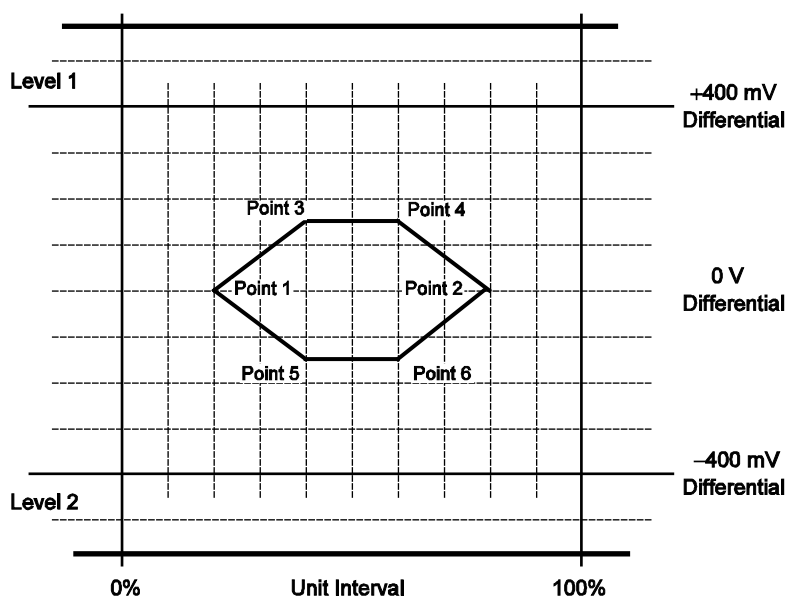
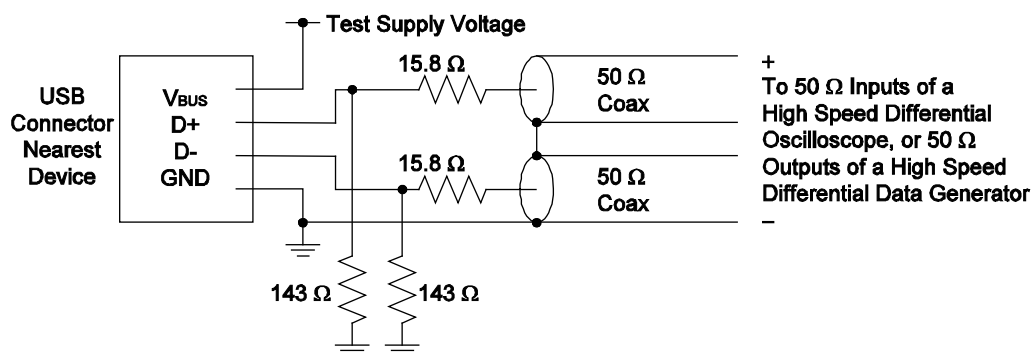


Figure 3-5. Receiver Measurement Fixtures



3.6 Pin Capacitance

Table 3-8. Pin Capacitance

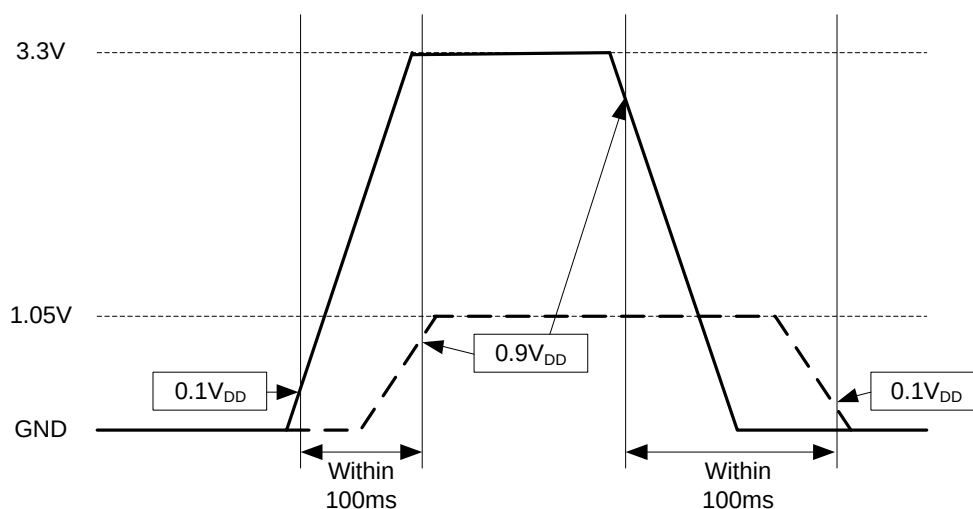
Parameter	Symbol	Condition	Min.	Max.	Units
Pin capacitance	C_{PIN}			5	pF

3.7 Sequence for Turning On or Off Power

When the external power source for 1.05 V and/or 3.3 V power is used, it is recommended that the time difference between the start of power-supply rise (3.3 V or 1.05 V) and the point where both power supplies are stabilized should be within 100 ms, regardless of the order of power sequence. A voltage of $0.1V_{DD}$ has to be raised to $0.9V_{DD}$ within the specified time.

When the on-chip LDO and the switching regulator are used, this timing is controlled by the internal circuit as defined here.

Figure 3-6. Order of Power Sequence



3.8 AC Characteristics

3.8.1 System Clock

Table 3-9. System clock (XT1/XT2) ratings ($V_{DD33} = 3.3\text{ V} \pm 10\%$, $V_{DD10} = 1.05\text{ V} \pm 5\%$, $T_A = -0\text{ to }+70^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Clock frequency	F_{CLK}	Crystal	-100 ppm	24	+100 ppm	MHz
Clock duty cycle	T_{DUTY}		40	50	60	%

Remark Required accuracy of crystal or oscillator block includes initial frequency accuracy, the spread of Crystal capacitor loading, supply voltage, temperature and aging, etc.

3.8.2 Reset and Clock Timing

Table 3-10. Power on Reset (RESETB) Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Power on reset time	T_{PONRST}	See Figure 3-7	10		ms

- Remarks 1.** No order in power-on V_{DD33} , AV_{DD33} , and V_{DD10} .
- 2.** All power sources should be stable within 100 ms from the earliest turned on power sources.
- 3.** RESETB shall be de-asserted after all power sources and the system clock become stable.

Figure 3-7. Power on Reset timing

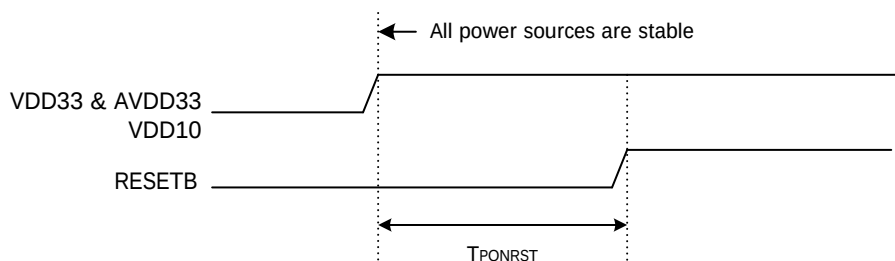
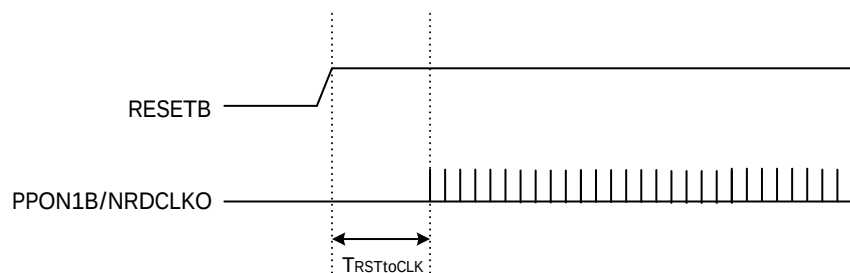


Table 3-11. NRDCCLKO Signal Timing

Parameter	Symbol	Condition	Min.	Max.	Units
VBUS on timing after Clock out starts	$T_{RSTtoCLK}$	See Figure 3-8		3	μs

Figure 3-8. NRDCCLKO Signal Timing



3.8.3 USB2.0 Interface

Table 3-12. USB Interface (1 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{LR}	$C_L = 200 \text{ pF to } 600 \text{ pF}$	75	300	ns
Fall time (90% to 10%)	t_{LF}	$C_L = 200 \text{ pF to } 600 \text{ pF}$	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF}) Note	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Downstream facing port source jitter total (including frequency tolerance) (Figure 3-15):					
To next transition	t_{DDJ1}		-25	+25	ns
For paired transitions	t_{DDJ2}		-14	+14	ns
Downstream facing port differential receiver jitter total (including frequency tolerance) (Figure 3-15):					
To next transition	t_{UJR1}		-152	+152	ns
For paired transitions	t_{UJR2}		-200	+200	ns
Source SE0 interval of EOP (Figure 3-14)	t_{LEOPT}		1.25	1.5	μs
Receiver SE0 interval of EOP (Figure 3-14)	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{LST}			210	ns
Hub differential data delay (Figure 3-11)	t_{LHDD}			300	ns
Hub differential driver jitter (including cable) (Figure 3-11):					
Downstream facing port					
To next transition	t_{LDHJ1}		-45	+45	ns
For paired transitions	t_{LDHJ2}		-15	+15	ns
Upstream facing port					
To next transition	t_{LUHJ1}		-45	+45	ns
For paired transitions	t_{LUHJ2}		-45	+45	ns
Data bit width distortion after SOP (Figure 3-11)	t_{LSOP}		-60	+60	ns
Hub EOP delay relative to t_{HDD} (Figure 3-12)	t_{LEOPD}		0	200	ns
Hub EOP output width skew (Figure 3-12)	t_{LHESK}		-300	+300	ns
Full-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{FR}	$C_L = 50 \text{ pF},$ $R_S = 36 \Omega$	4	20	ns
Fall time (90% to 10%)	t_{FF}	$C_L = 50 \text{ pF},$ $R_S = 36 \Omega$	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms

Note Excluding the first transition from the Idle state.

Table 3-13. USB Interface (2 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Electrical Characteristics (Continued)					
Consecutive frame interval jitter	t _{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (Figure 3-13):		Note			
To next transition	t _{DJ1}		−3.5	+3.5	ns
For paired transitions	t _{DJ2}		−4.0	+4.0	ns
Source jitter for differential transition to SE0 transition (Figure 3-14)	t _{FDEOP}		−2	+5	ns
Receiver jitter (Figure 3-15):					
To Next Transition	t _{JR1}		−18.5	+18.5	ns
For Paired Transitions	t _{JR2}		−9	+9	ns
Source SE0 interval of EOP (Figure 3-14)	t _{FEOPT}		160	175	ns
Receiver SE0 interval of EOP (Figure 3-14)	t _{FEOPR}		82		ns
Width of SE0 interval during differential transition	t _{FST}			14	ns
Hub differential data delay (Figure 3-11)					
(with cable)	t _{HDD1}			70	ns
(without cable)	t _{HDD2}			44	ns
Hub differential driver jitter (including cable) (Figure 3-11):					
To next transition	t _{HDJ1}		−3	+3	ns
For paired transitions	t _{HDJ2}		−1	+1	ns
Data bit width distortion after SOP (Figure 3-11)	t _{FSOP}		−5	+5	ns
Hub EOP delay relative to t _{HDD} (Figure 3-12)	t _{FEOPD}		0	15	ns
Hub EOP output width skew (Figure 3-12)	t _{FHESK}		−15	+15	ns
High-speed Electrical Characteristics					
Rise time (10% to 90%)	t _{HSR}		500		ps
Fall time (90% to 10%)	t _{HSF}		500		ps
Driver waveform	See Figure 3-9.				
High-speed data rate	t _{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t _{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t _{HSRFI}			4 High-speed	Bit times
Data source jitter	See Figure 3-9.				
Receiver jitter tolerance	See Figure 3-4.				
Hub data delay (without cable)	t _{SHDD}			36 High-speed+4 ns	Bit times
Hub data jitter	See Figure 3-4, Figure 3-9.				
Hub delay variation range	t _{SHDV}			5 High-speed	Bit times

Note Excluding the first transition from the Idle state.

Table 3-14. USB Interface (3 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings					
Time to detect a downstream facing port connect event (Figure 3-17):	t_{DCNN}		2.5	2000	μs
Awake hub			2.5	12000	μs
Suspended hub					
Time to detect a disconnect event at a hub's downstream facing port (Figure 3-16)	t_{DDIS}		2.0	2.5	μs
Duration of driving resume to a downstream port (only from a controlling hub)	t_{DRSMDN}		20		ms
Time from detecting downstream resume to rebroadcast	t_{URSM}			1.0	ms
Duration of driving reset to a downstream facing port	t_{DRST}	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	t_{URLK}		2.5	100	μs
Time to detect a long SE0 from upstream	t_{URLSE0}		2.5	10000	μs
Duration of repeating SE0 upstream (for Low-/Full-speed repeater)	t_{URPSE0}			23	FS Bit times
Inter-packet delay (for High-speed) of packets traveling in same direction	$t_{HSIPDSD}$		88		Bit times
Inter-packet delay (for High-speed) of packets traveling in opposite direction	$t_{HSIPDOD}$		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for High-speed	$t_{HSRSPID1}$			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	t_{FILT}		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	t_{WTDCH}			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	t_{DCHBIT}		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t_{DCHSE0}		100	500	μs
Period of idle bus before device can initiate resume	t_{WTRSM}		5		ms
Duration of driving resume upstream	t_{DRSMUP}		1	15	ms

Table 3-15. USB Interface (4 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings (Continued)					
Time to detect a reset from upstream for non High-speed capable devices	t _{DETRST}		2.5	10000	μs
Inter-packet delay for Full-speed	t _{IPD}		2		Bit times
Inter-packet delay for device response with detachable cable for Full-speed	t _{RSPDPD1}			6.5	Bit times
SetAddress() completion time	t _{DSETADDR}			50	ms
Time to complete standard request with no data	t _{DRQCMLTND}			50	ms
Time to deliver first and subsequent (except last) data for standard request	t _{DRETDATA1}			500	ms
Time to deliver last data for standard request	t _{DRETDATAN}			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the High-speed detection handshake	t _{FILTSE0}		2.5		μs
Time a hub operating in non-suspended Full-speed will wait after start of SE0 on upstream before beginning the High-speed detection handshake	t _{WTRSTFS}		2.5	3000	ms
Time a hub operating in High-speed will wait after start of SE0 on upstream before reverting to Full-speed	t _{WTREV}		3.0	3.125	ms
Time a hub will wait after reverting to Full-speed before sampling the bus state on upstream and beginning the High-speed will wait after start of SE0 on upstream before reverting to Full-speed	t _{WTRSTHS}		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t _{UCH}		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t _{UCHEND}			7.0	ms
Time between detection of downstream chip and entering High-speed state	t _{WTHS}			500	μs
Time after end of upstream Chirp at which hub reverts to Full-speed default state if no downstream Chirp is detected	t _{WTFS}		1.0	2.5	ms

Figure 3-9. Transmit Waveform for Transceiver at DP/DM

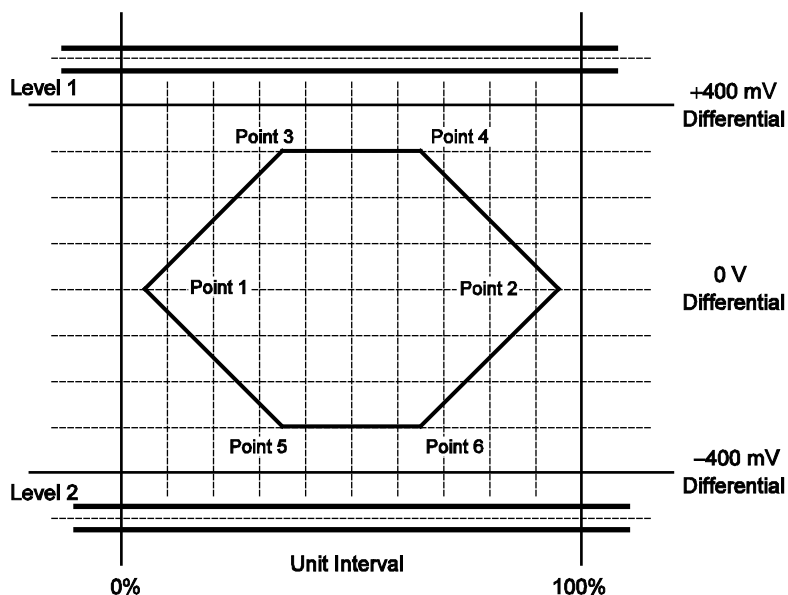


Figure 3-10. Transmitter Measurement Fixtures

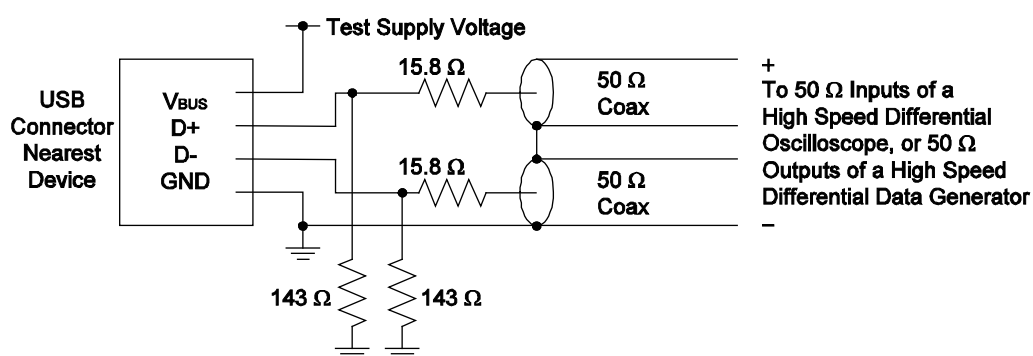
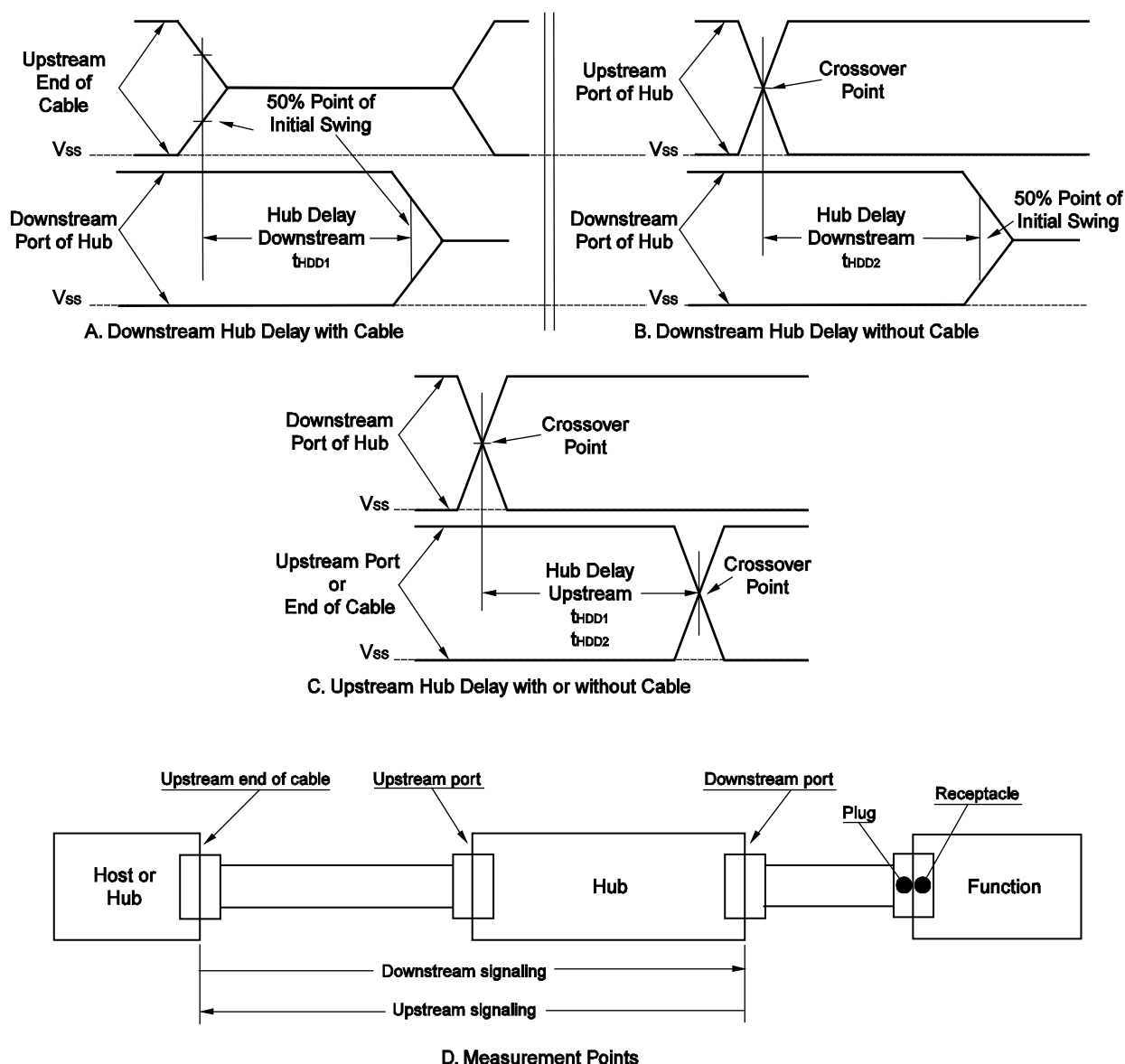


Figure 3-11. Hub Differential Delay, Differential Jitter, and SOP Distortion



Hub Differential Jitter:

$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K)$ or $t_{HDDx}(K) - t_{HDDx}(J)$ Consecutive Transitions
 $t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J)$ or $t_{HDDx}(K) - t_{HDDx}(K)$ Paired Transitions

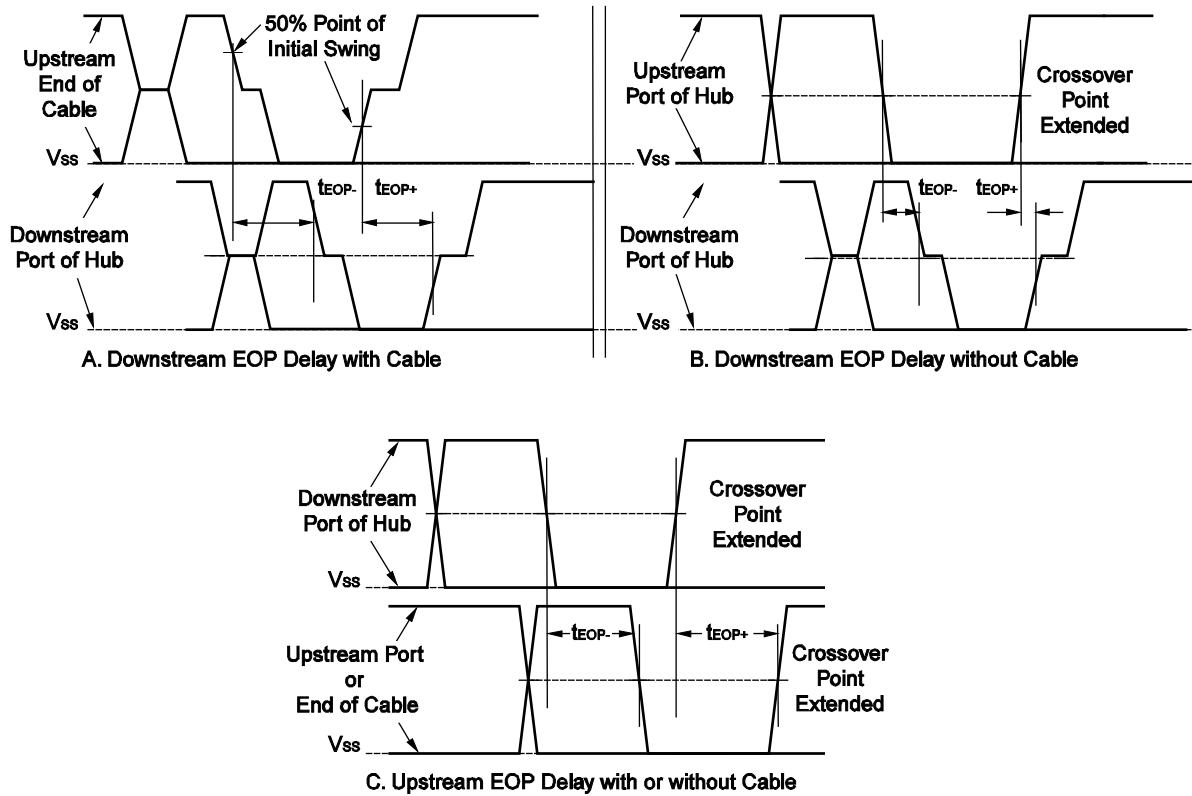
Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):

$t_{FSOP} = t_{HDDx}(\text{next J}) - t_{HDDx}(\text{SOP})$

Low-speed timings are determined in the same way for:

t_{LHDD} , t_{LDHJ1} , t_{LDJH2} , t_{LUHJ1} , t_{LUJH2} , and t_{LSOP}

Figure 3-12. Hub EOP Delay and EOP Skew



EOP Delay:
 $t_{EOPD} = t_{EOPy} - t_{HDDx}$
 (t_{EOPy} means that this equation applies to t_{EOP-} and t_{EOP+})

EOP Skew:
 $t_{HESK} = t_{EOP+} - t_{EOP-}$

Low-speed timings are determined in the same way for:
 t_{LEOPD} and t_{LHESK}

Figure 3-13. USB Differential Data Jitter for Low-/Full-speed

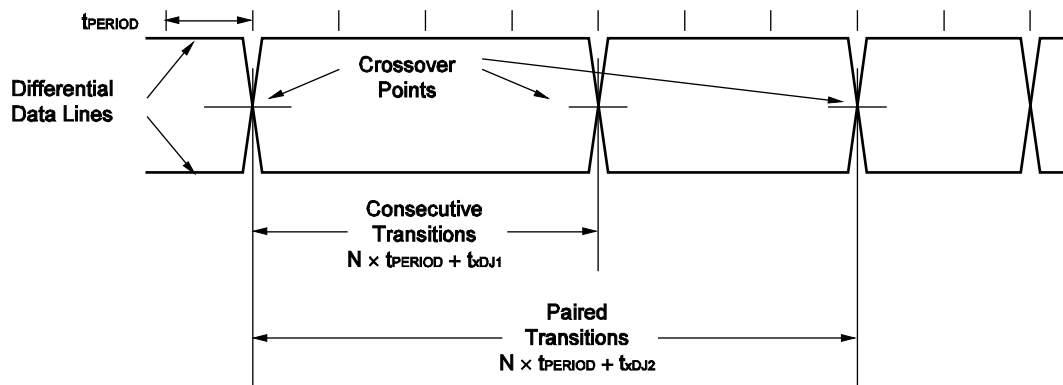


Figure 3-14. USB Differential-to-EOP Transition Skew and EOP Width for Low-/Full-speed

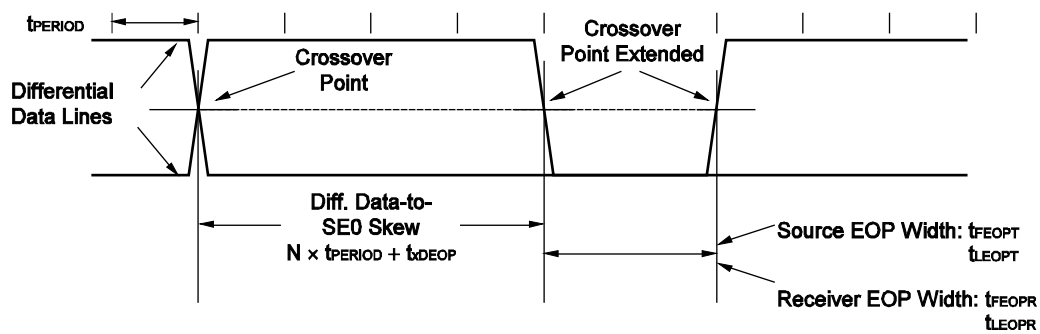


Figure 3-15. USB Receiver Jitter Tolerance for Low-/Full-speed

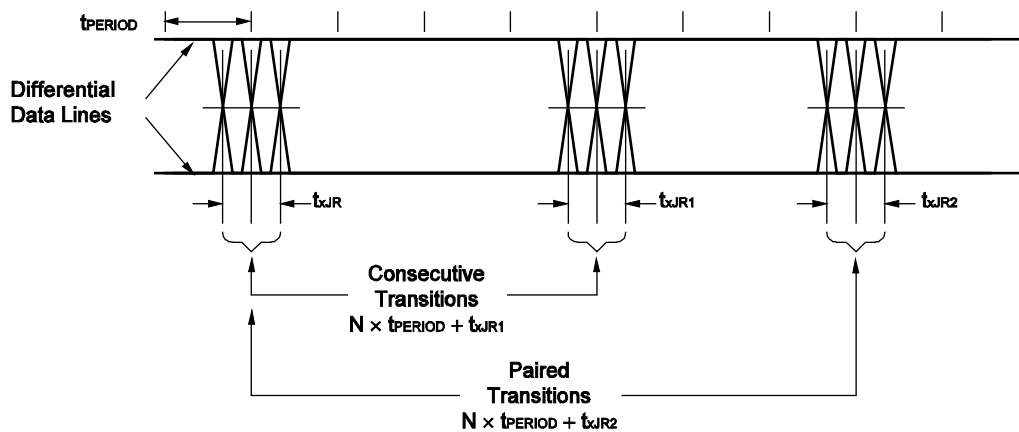


Figure 3-16. Low-/Full-speed Disconnect Detection

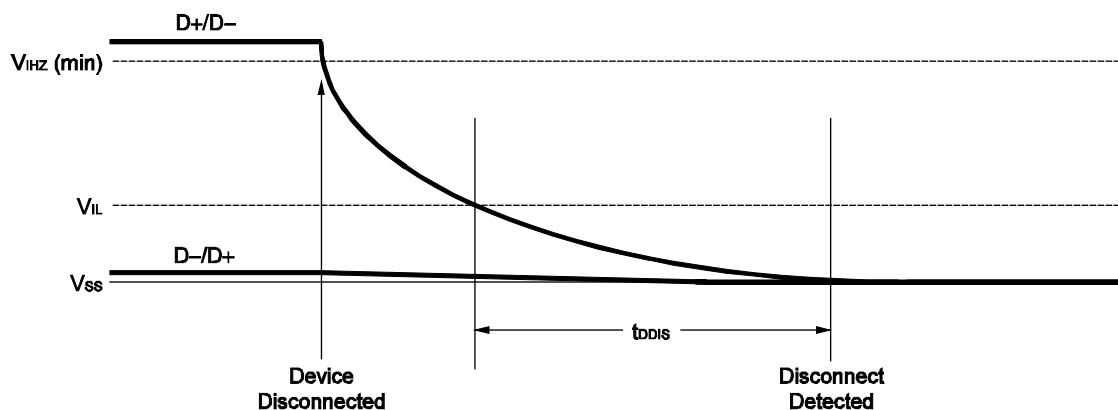
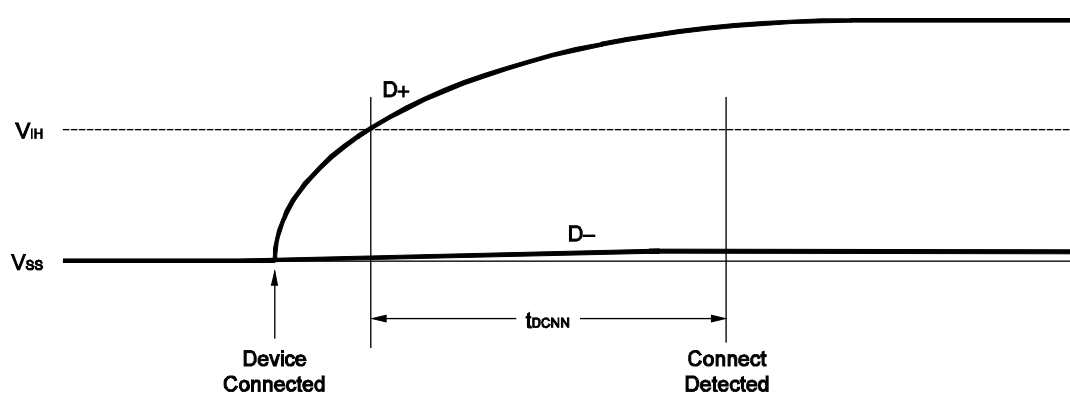


Figure 3-17. Full-/High-speed Device Connect Detection

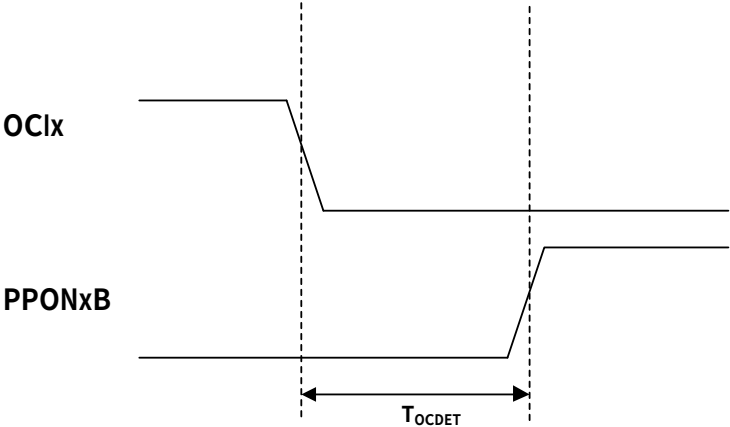


3.8.4 Overcurrent

Table 3-16. Overcurrent Detect Timing

Parameter	Symbol	Min.	Max.	Units
PPONx de-assert time from asserting OC1x	T _{OCDET}		50	ms

Figure 3-18. Overcurrent Detect Timing

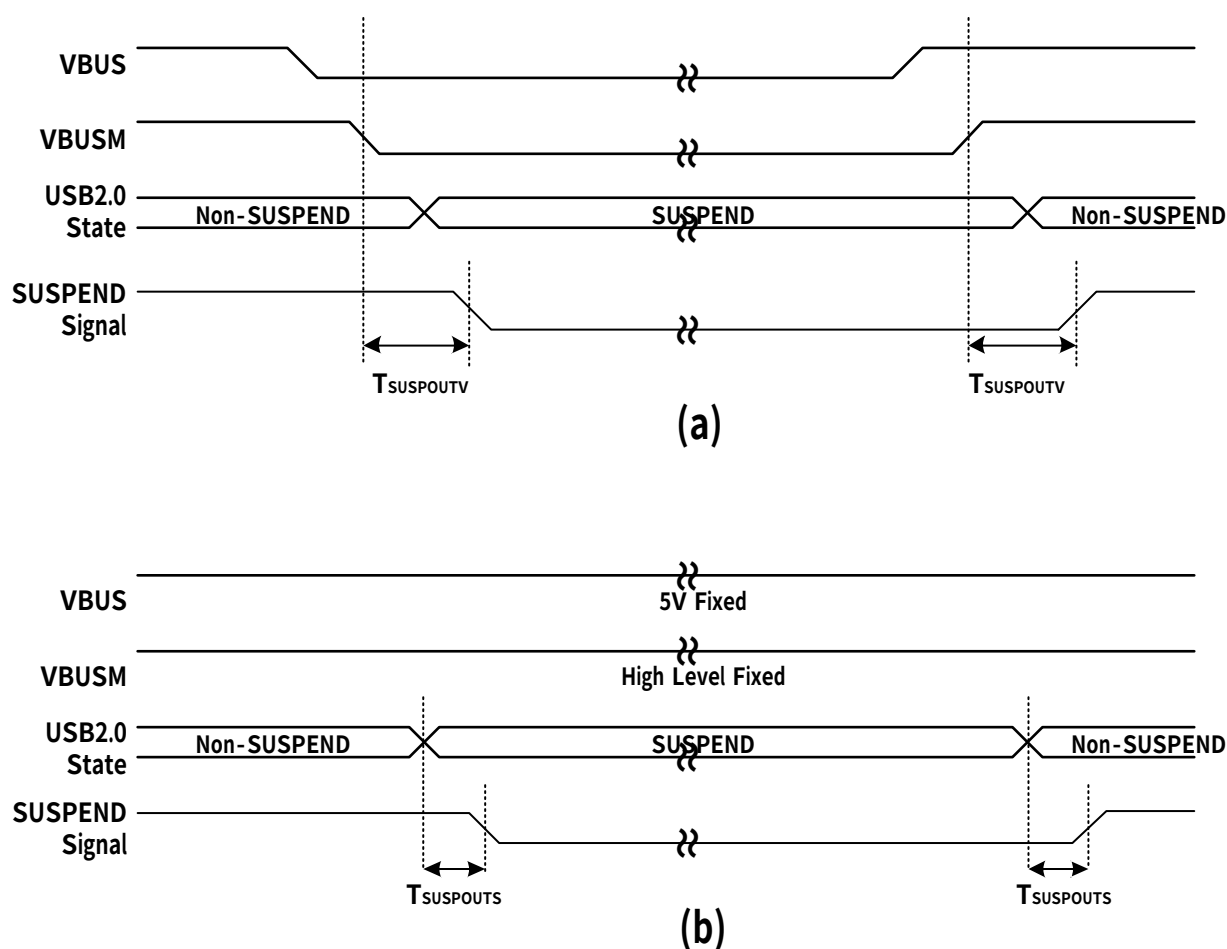


3.8.5 SUSPEND signal output timing

Table 3-17. SUSPEND signal output timing

Parameter	Symbol	Condition	Min.	Max.	Units
SUSPEND signal output timing in case of being changed the VBUSM	T_{SUSPOUTV}	See Figure 3-20 (a)		100	ms
SUSPEND signal output timing in case of being changed the USB2.0 state	T_{SUSPOUTS}	See Figure 3-20 (b)		10	ms

Figure 3-19. SUSPEND signal output timing

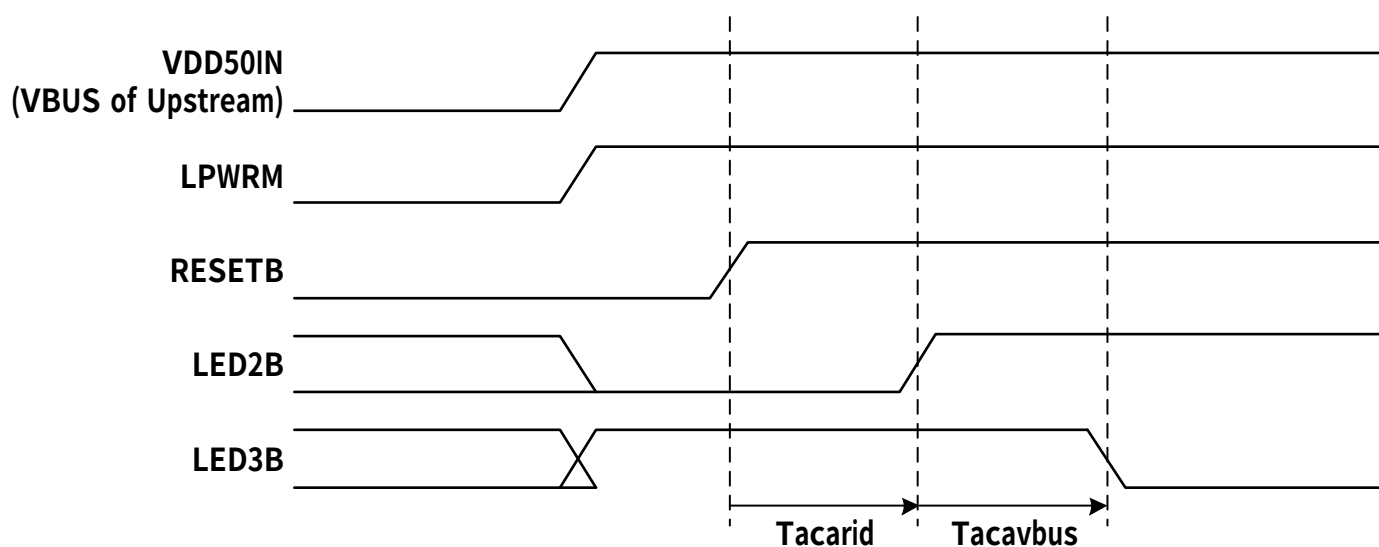


3.8.6 ACA-Dock function control signal output timing

Table 3-18. ACA-Dock function control signal output timing

Parameter	Symbol	Condition	Min.	Max.	Units
RID control signal of ACA-Dock function output timing	Tacarid	See Figure 3-21		100	ms
VBUS control signal of ACA-Dock function output timing	Tacavbus	See Figure 3-21		100	ms

Figure 3-20. ACA-Dock function control signal output timing



3.9 Power Consumption

Table 3-19. Power Consumption of μ PD720115 (without on-chip regulators operating)

Parameter	Device connection	Condition	VDD10 line	VDD33 line	AVDD33 line	Units
Power Consumption	No host connection	Hub is not connected to host controller.	1.2	0.05	0.05	mA
	Suspend	Hub is connected to host controller and, hub goes into Suspend state.	1.2	0.1	0.1	mA
	1 device	Hub is connected to host controller and only one device is connected on the port.				
		Low-speed data transfer on the port.	19	23	11	mA
		Full-speed data transfer on the port.	19	24	11	mA
		High-speed data transfer on the port.	21	48	11	mA
	2 devices	Hub is connected to host controller and two devices are connected on the ports.				
		High-speed data transfer on the both ports.	23	67	11	mA
	3 devices	Hub is connected to host controller and three devices are connected on the ports.				
		High-speed data transfer on the three ports.	24	82	11	mA
	4 devices	Hub is connected to host controller and four devices are connected on the ports.				
		High-speed data transfer on the four ports.	25	96	11	mA

Typical condition ($T_A = 25^\circ\text{C}$, $V_{DD33} = 3.3\text{ V}$, $V_{DD10} = 1.05\text{ V}$)

Table 3-20. Power Consumption of μ PD720115 (with on-chip regulators ^{Note})

Parameter	Device connection	Condition	Total Power	Units
Power Consumption	No host connection	Hub is not connected to host controller.	6.5	mW
	Suspend	Hub is connected to host controller and, hub goes into Suspend state.	7.5	mW
	1 device	Hub is connected to host controller and only one device is connected on the port.		
		Low-speed data transfer on the port.	295	mW
		Full-speed data transfer on the port.	308	mW
		High-speed data transfer on the port.	455	mW
	2 devices	Hub is connected to host controller and two devices are connected on the ports. High-speed data transfer on the both ports.	578	mW
	3 devices	Hub is connected to host controller and three devices are connected on the ports. High-speed data transfer on the three ports.	700	mW
	4 devices	Hub is connected to host controller and four devices are connected on the ports. High-speed data transfer on the four ports.	823	mW

Typical condition ($T_A = 25^\circ\text{C}$, $V_{DD33} = 3.3\text{ V}$, $V_{DD10} = 1.05\text{ V}$)

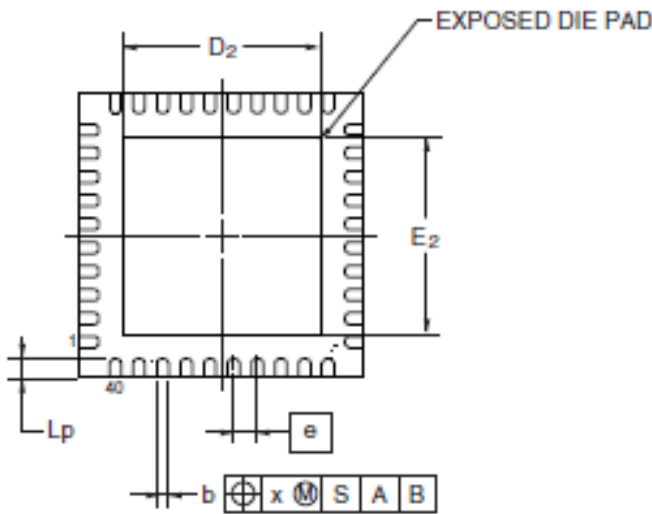
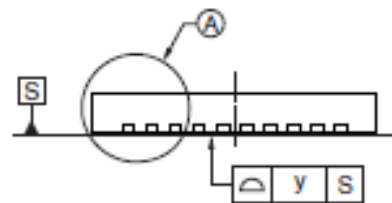
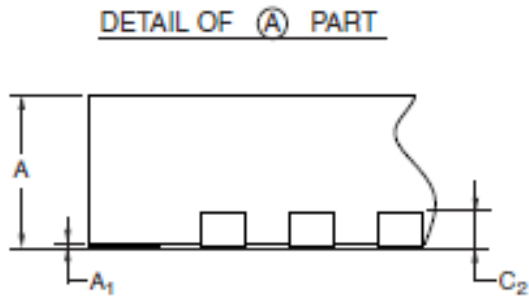
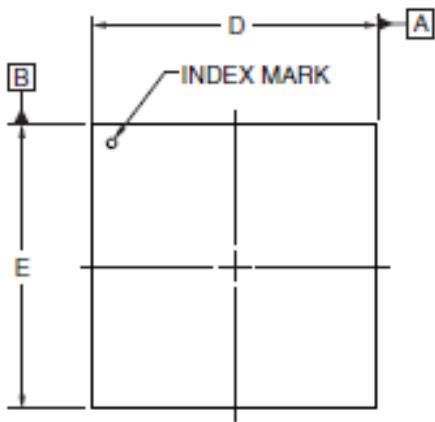
Note Input voltage for on-chip regulators is 5 V.

4. PACKAGE DRAWINGS

- μPD720115K8-611-BAK-A/μPD720115K8-611-BAK-M1-A
- μPD720115K8-711-BAK-A/μPD720115K8-711-BAK-M1-A

40-PIN QFN (6 x 6)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN40-6x6-0.50	PVQN0040KG-A	T40K8-50A-BAK	0.10



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.90	6.00	6.10
E	5.90	6.00	6.10
A	—	—	0.90
A ₁	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
L _p	0.30	0.40	0.50
x	—	—	0.10
y	—	—	0.08
c ₂	—	0.20	—
D ₂	—	4.15	—
E ₂	—	4.15	—

5. RECOMMENDED SOLDERING CONDITIONS

The μ PD720115 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact a Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Package Mount Manual (<http://www.renesas.com/products/package/index.jsp>)

- μ PD720115K8-611-BAK-A / μ PD720115K8-711-BAK-A
- μ PD720115K8-611-BAK-M1-A / μ PD720115K8-711-BAK-M1-A

40-pin QFN (6 x 6)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260°C, Reflow time: 60 seconds or less (220°C or higher), Maximum allowable number of reflow processes: 3, Exposure limit Note : 7 days (10 hours pre-baking is required at 125°C afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3

Note The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

REVISION HISTORY	μPD720115 Data Sheet
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Rev.	Date	Description	
		Page	Summary
0.01	May 16, 2013	-	First Edition issued
0.02	Jul 2, 2013	2, 3, 10, 27, 28	Added final order name.
		3, 5	Changed pin name from BUSSEL to LPWRM
0.03	Jul 18, 2013	1	Modified Features.
		3	Modified pin name from LED1B to LED1B/SUSPEND and from PPON1B to PPON1B/NRDCLKO. Modified pin name from X1 to XT1 and X2 to XT2.
		4	Modified function description of VDD33OUT.
		5	Modified pin numbers of XT1 and XT2. Modified pin name from LED1B to LED1B/SUSPEND. Modified function description of LED1B.
		6	Modified pin name from PPON1B to PPON1B/NRDCLKO. Modified function description of PPON1B. Modified function description of PPON2B, PPON3B and PPON4B. Modified pin numbers of DP1, DP2, DP3 and DP4.
		7	Modified Buffer List.
		10	Modified the Min. value of VDD50IN.
		27	Added Package Drawings.
0.04	Jul 31, 2013	5	Added function description of LPWRM.
		9	Modified the condition of 5V buffer.
		10	Modified the Min. value of VDD50IN and VDD33IN.
		16	Modified the Min. value of power on reset time. Modified Figure 3-7.
0.05	Aug 7, 2013	4	Modified function description of VDD33IN.
0.06	Oct 15, 2013	6	Added description of note for section 2.5
		27	Added Power Consumption data.
1.00	Nov 22, 2013	-	Document Promoted from Preliminary to full data.
		8	Added the description for “3.3 V I _{OL} = 12 mA bi-directional buffer”
2.00	July 15, 2014	1	Modified Features.
		5	Modified function of LED2B and LED3B.
		28	Add AC Characteristics as below.
		29	Section 3.8.4 Overcurrent
3.00	Sep 16, 2015	30	Section 3.8.5 SUSPEND signal output timing
			Section 3.8.6 ACA-Dock function control signal output timing
		21,22	Removed the following parameters t _{SIGATT} , t _{ATTDB} , t _{SUSAVGI} , t _{RSMRCY} , t _{RSTRCY}
		27	Removed Figure 3-18 “Power-on and Connection Events Timing”
		34	Modified the URL

Rev.	Date	Description	
		Page	Summary
4.00	Jun 30, 2023	-	Added new part number Removed unnecessary cross-reference.
4.10	Sep 25, 2023	2	Updated 1.2 Ordering Information

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