STL3NK40

N-channel 400 V, 4.5 Ω typ., 0.43 A, SuperMESH™ Power MOSFET in a PowerFLAT™ 5x5 package

Datasheet - production data

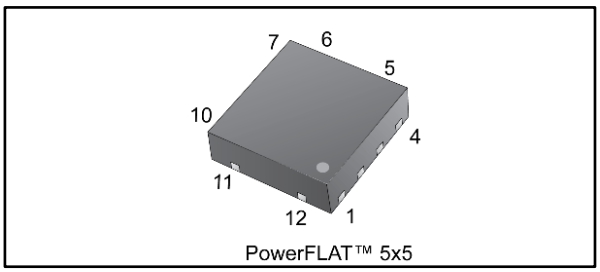
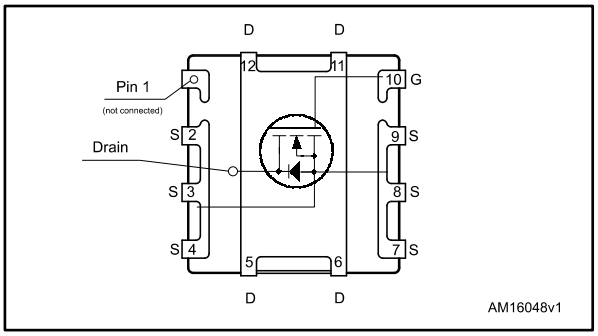


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL3NK40	400 V	5.5 Ω	0.43 A	2.5 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized

Applications

- Switching applications

Description

This high voltage device is an N-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packing
STL3NK40	3NK40	PowerFLAT™ 5x5	Tape and reel

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	400	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	400	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_{pcb} = 25 °C	0.43	A
	Drain current (continuous) at T_{pcb} = 100 °C	0.27	A
I_{DM} (2)	Drain current (pulsed)	1.72	A
P_{TOT} (1)	Total dissipation at T_{pcb} = 25 °C	2.5	W
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
T_j	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)When mounted on FR-4 board of 1 inch², 2 oz Cu (t < 100 s).

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 0.43 A, di/dt ≤ 200 A/µs; V_{DD}< 320 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50	°C/W

Notes:

(1)When mounted on 1 inch² FR-4 board, 2 oz Cu (t < 100 s).

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{jmax.}$)	0.43	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	60	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	400			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 400 V			1	µA
		V_{GS} = 0 V, V_{DS} = 400 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	0.8	1.6	2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.22 A		4.5	5.5	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	128	200	pF
C_{oss}	Output capacitance		-	16	30	pF
C_{rss}	Reverse transfer capacitance		-	4	6	pF
R_G	Gate input resistance	f = 1 MHz gate DC bias = 0 test signal level = 20 mV open-drain	-	12		pF
Q_g	Total gate charge	V_{DD} = 320 V, I_D = 1.4 A V_{GS} = 0 to 10 V (see *Figure 13: "Test circuit for gate charge behavior"*)	-	8.7	13	nC
Q_{gs}	Gate-source charge		-	0.9	-	nC
Q_{gd}	Gate-drain charge		-	3.8	-	nC

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 200 V, I_D = 0.7 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 12: "Test circuit for resistive load switching times"* and *Figure 17: "Switching time waveform"*)	-	3	-	ns
t_r	Rise time		-	4	-	ns
$t_{d(off)}$	Turn-off delay time		-	18	-	ns
t_f	Fall time		-	16	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.43	A
I_{SDM}(1)	Source-drain current (pulsed)		-		1.72	A
V_{SD}(2)	Forward on voltage	I_{SD} = 0.43 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 1.4 A, di/dt = 100 A/µs,V_{DD} = 20 V (see *Figure 14: "Test circuit for inductive load switching and diode recovery times"*)	-	166		ns
Q_{rr}	Reverse recovery charge		-	300		nC
I_{RRM}	Reverse recovery current		-	3.6		A
t_{rr}	Reverse recovery time	I_{SD} = 1.4 A, di/dt = 100 A/µs V_{DD} = 20 V, T_j = 150 °C (see *Figure 14: "Test circuit for inductive load switching and diode recovery times"*)	-	176		ns
Q_{rr}	Reverse recovery charge		-	340		nC
I_{RRM}	Reverse recovery current		-	3.8		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

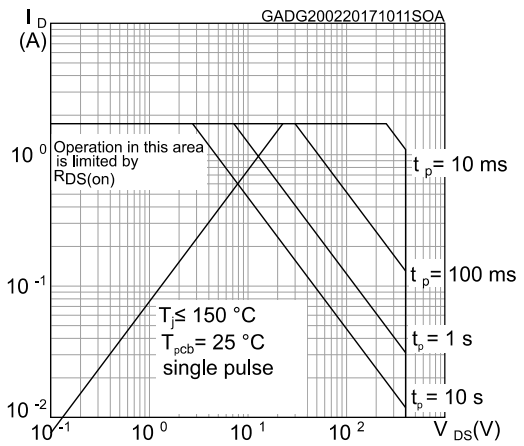


Figure 3: Thermal impedance

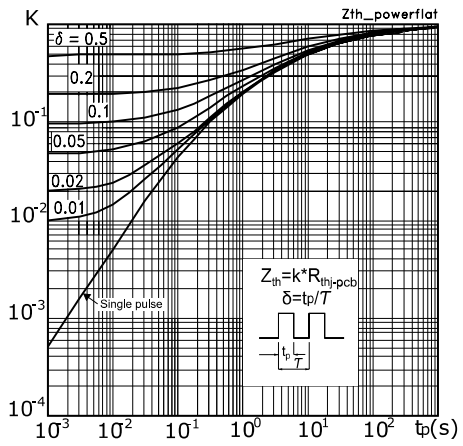


Figure 4: Output characteristics

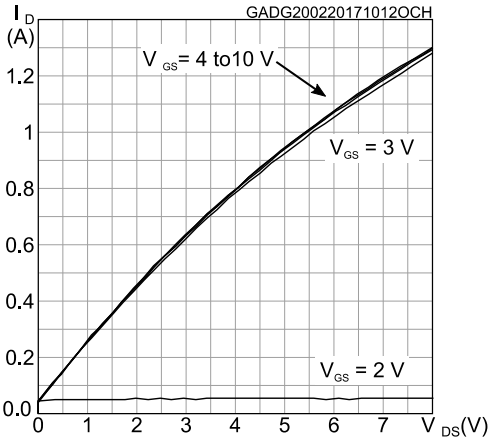


Figure 5: Transfer characteristics

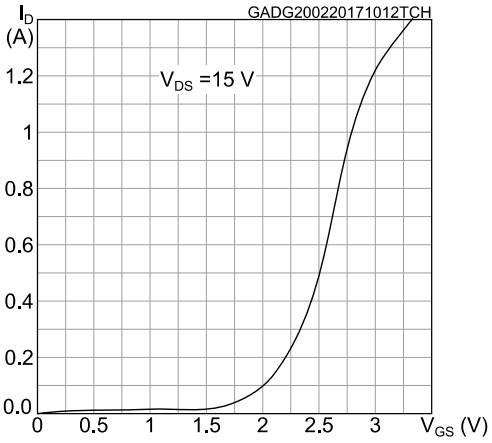


Figure 6: Static drain-source on-resistance

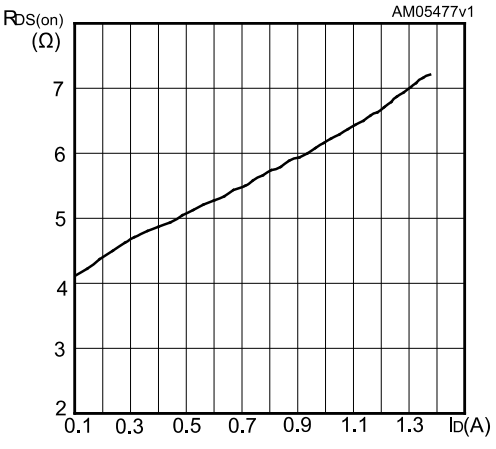


Figure 7: Gate charge vs. gate-source voltage

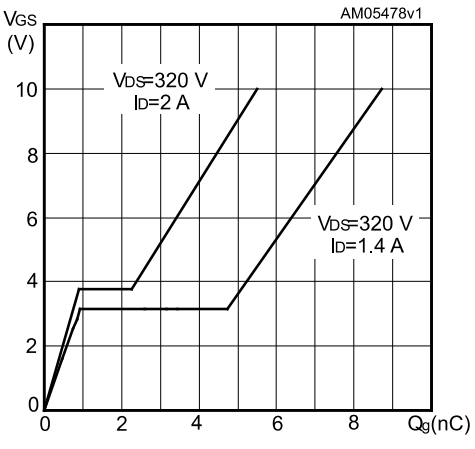


Figure 8: Capacitance variations

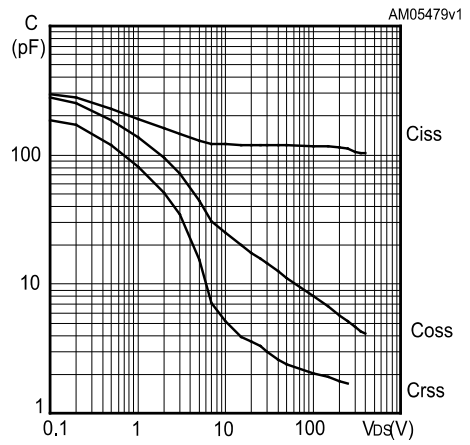


Figure 9: Normalized $V_{(BR)DSS}$ vs. temperature

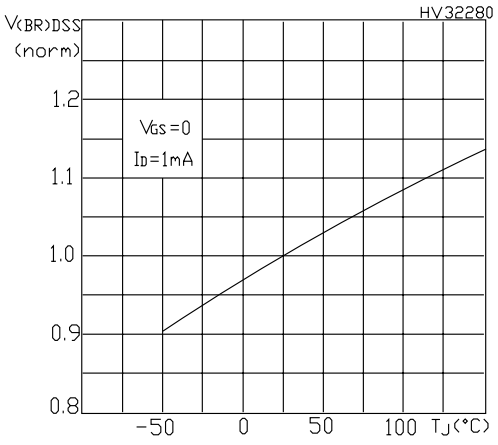


Figure 10: Normalized gate threshold voltage vs. temperature

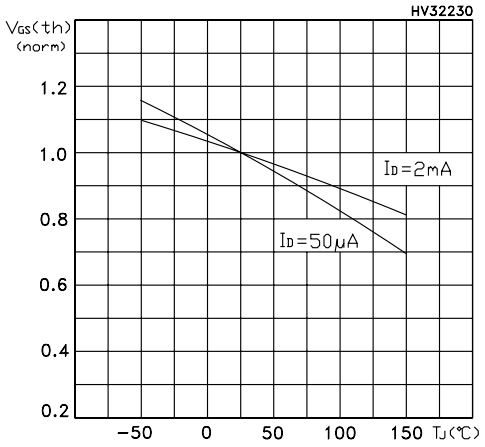
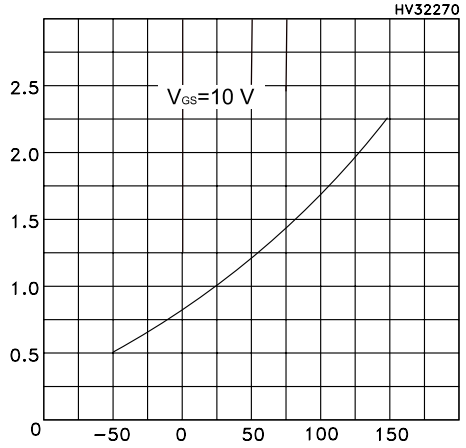


Figure 11: Normalized on-resistance vs. temperature



3 Test circuits

Figure 12: Test circuit for resistive load switching times

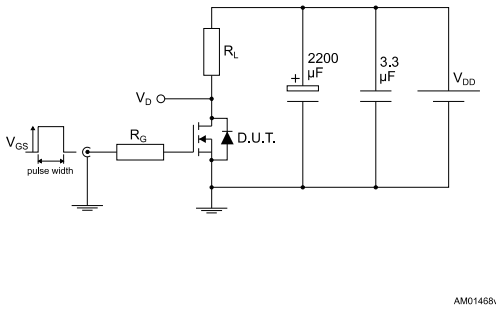


Figure 13: Test circuit for gate charge behavior

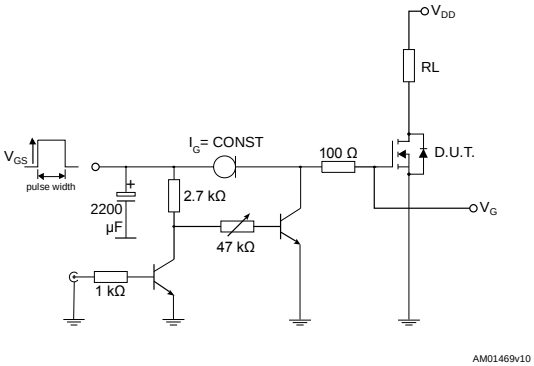


Figure 14: Test circuit for inductive load switching and diode recovery times

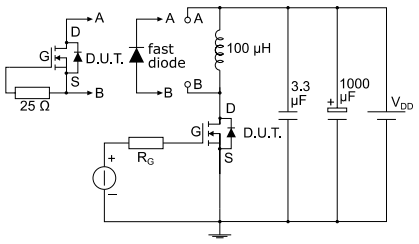


Figure 15: Unclamped inductive load test circuit

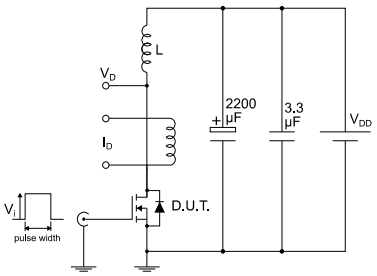


Figure 16: Unclamped inductive waveform

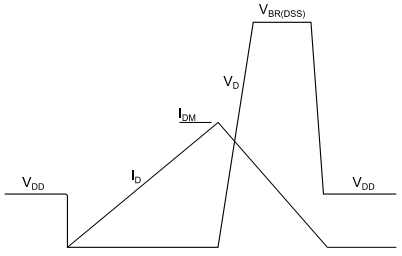
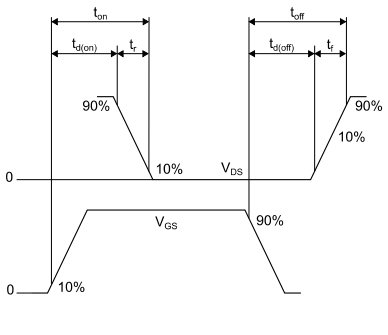


Figure 17: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x5 package information

Figure 18: PowerFLAT™ 5x5 package outline

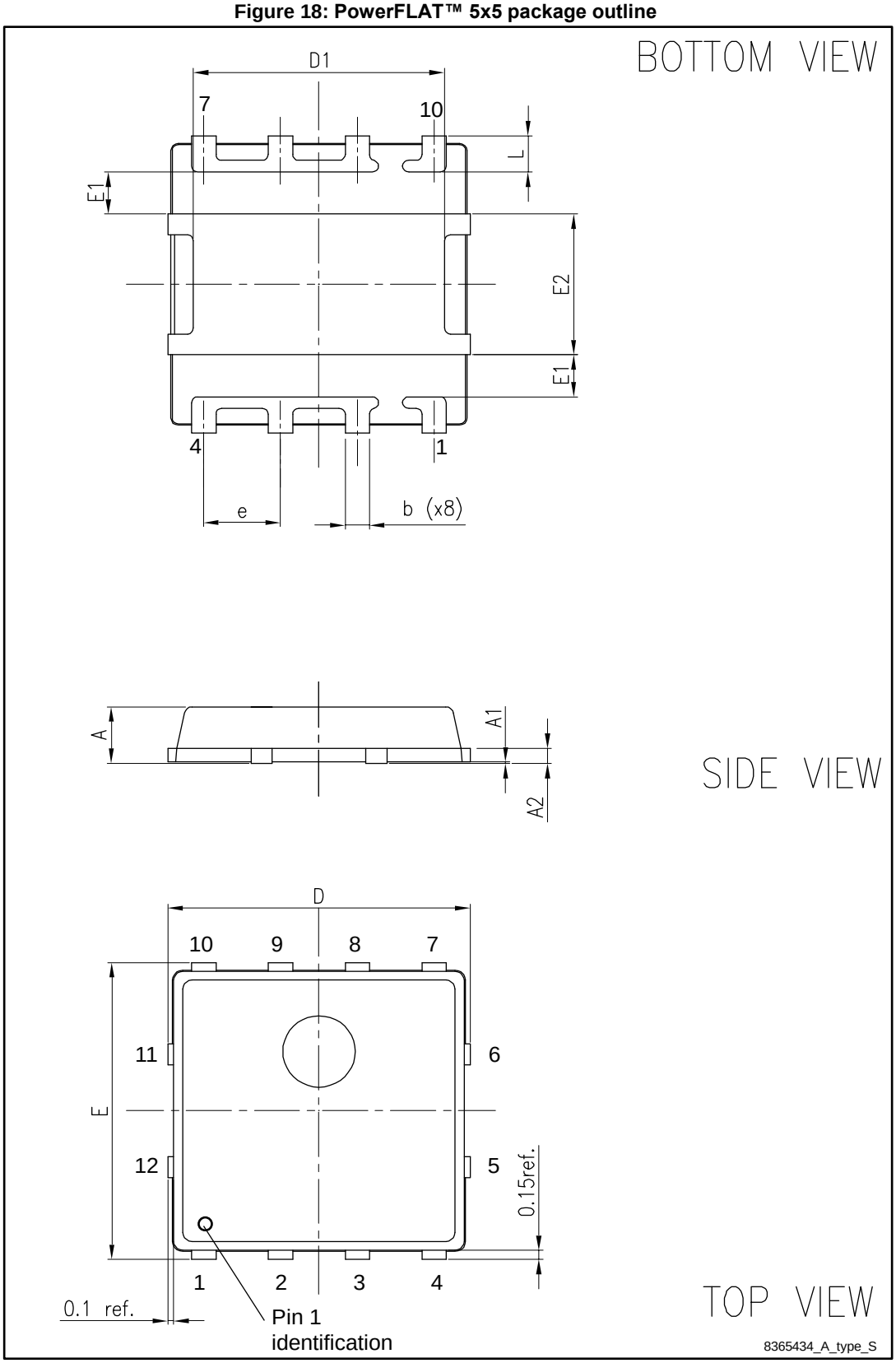
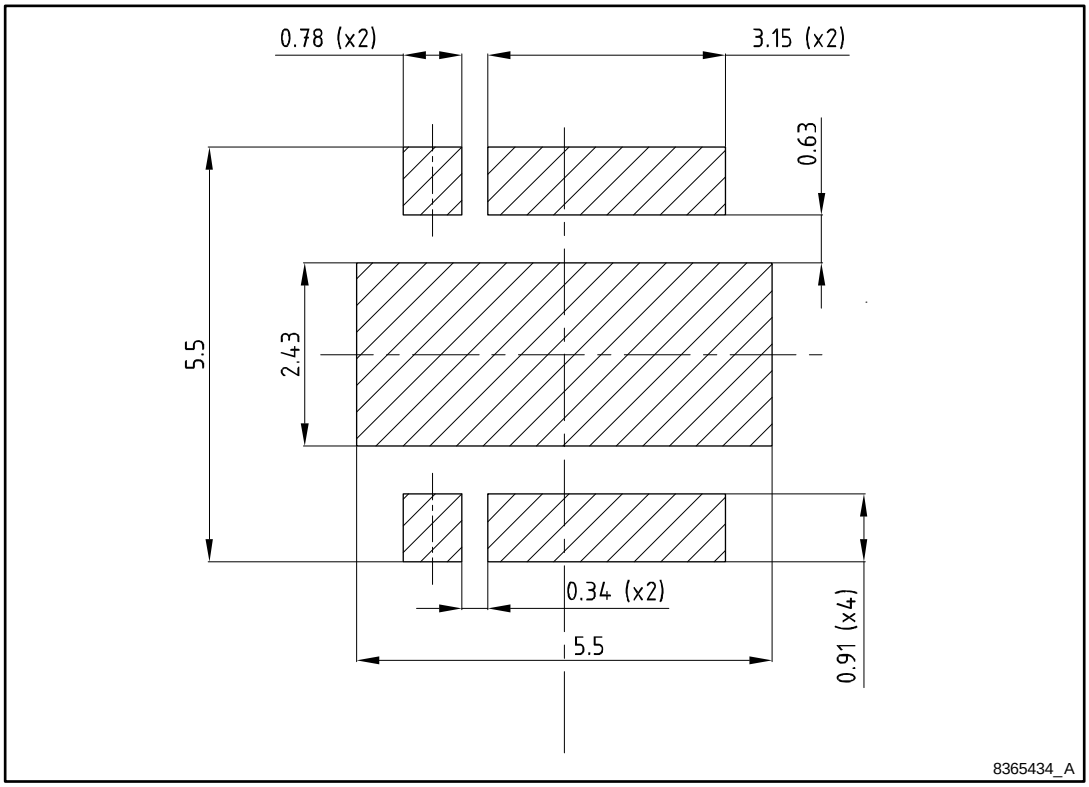


Table 9: PowerFLAT 5x5 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.0
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.00	
D1	4.05		4.25
E		5.00	
E1	0.64		0.79
E2	2.25		2.45
e		1.27	
L	0.45		0.75

Figure 19: PowerFLAT™ 5x5 recommended footprint (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
18-Sep-2009	1	First release.
29-Aug-2013	2	Updated: *Section 4: Package mechanical data* Minor text changes
20-Feb-2017	3	Removed PowerFLAT™ 5x5 type C package information and cover image. Updated *Table 6: "Dynamic"* and *Table 8: "Source-drain diode".* Updated *Section 2.1: "Electrical characteristics (curves)"*. Minor text changes.

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