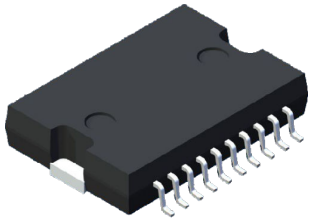
LEO3910

Datasheet

Rad-hard plastic 2 A positive low drop voltage regulator



Power-SO 20
slug-down

Product status link
LEO3910

Features

- Operating input voltage from 3 V to 12 V
- Adjustable output voltage from 1.23 V to 9 V
- Low-dropout voltage: 0.35 V @ I_O = 400 mA
- Overtemperature protection
- Overcurrent protection
- Adjustable current limitation
- Inhibit (ON/OFF) TTL-compatible control
- Gold bonding
- Nickel/palladium/gold-lead-finished (NiPdAu), whisker-free
- RML <1% and CVCM <0.1% guaranteed outgassing
- 50 krad(Si) total ionizing dose
- SEL free up to 62.5 MeV.cm²/mg
- Compliant with ST-LEO-specification

Application

- Low earth orbit (LEO) applications

Description

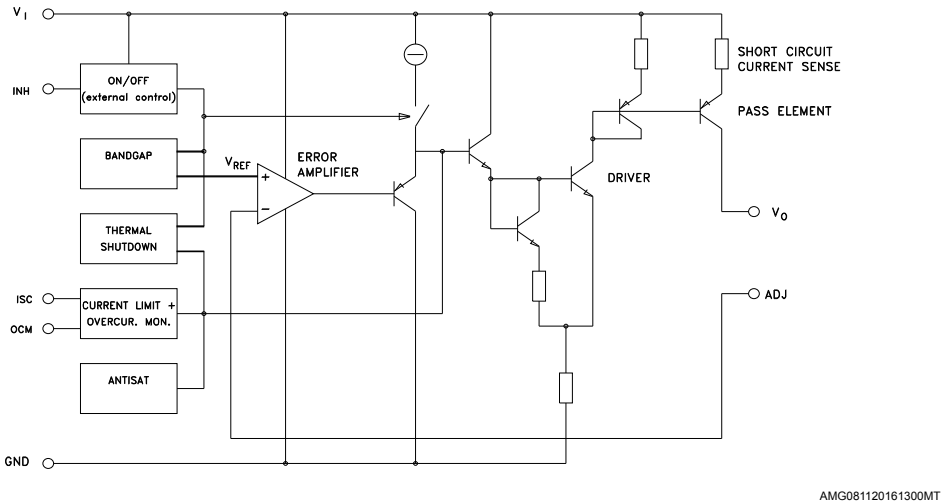
The LEO3910 is a positive adjustable voltage regulator housed into a Power-SO 20L slug-down package, which is able to provide in regulation a maximum output current up to 2 A.

It can operate over a large temperature range of -40 °C to +125 °C.

The LEO3910 is compliant with the ST-LEO-specification, dedicated specifications for space-ready rad-hard plastic products. This AEC-Q100-based specidfication offers a specific trade-off among footprint size savings, cost of ownership and quality assurance together with radiation hardness and a large quantity capability.

1 Block diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin configuration**

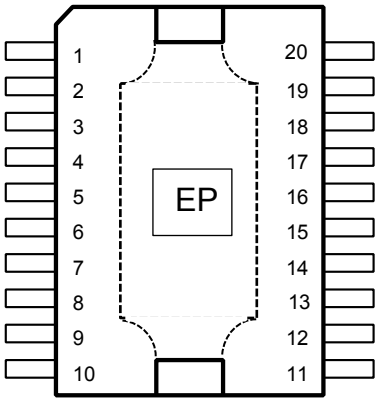


Table 1. **Pin connection table**

Pin	Pin name	Description
16	GND	Ground
2, 3, 8, 9, 13, 14, 15, 18	NC	Not connected
4, 6	VO	Output voltage
5	VI	Input voltage
7	ISC	Current limit setting
12	OCM	Over current monitoring
17	INH	Inhibit
19	ADJ	Adjustable pin
EP (1, 10, 11, 20)	EP	Exposed pad, to be connected to GND. 1, 10, 11, 20 internally connected to EP

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	-0.3 to 14	V
VO	DC output voltage range	-0.3 to (VI + 0.3)	V
V_{ADJ}	ADJ pin voltage	-0.3 to (VO + 0.3)	V
V_{OCM}	Over current monitor pin voltage	-0.3 to (VI + 0.3)	V
V_{ISC}	Current limit pin voltage	-0.3 to (VI + 0.3)	V
V_{INH}	INHIBIT input voltage	-0.3 to (VI + 0.3)	V
I_O	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{stg}	Storage temperature range	-65 to +150	°C

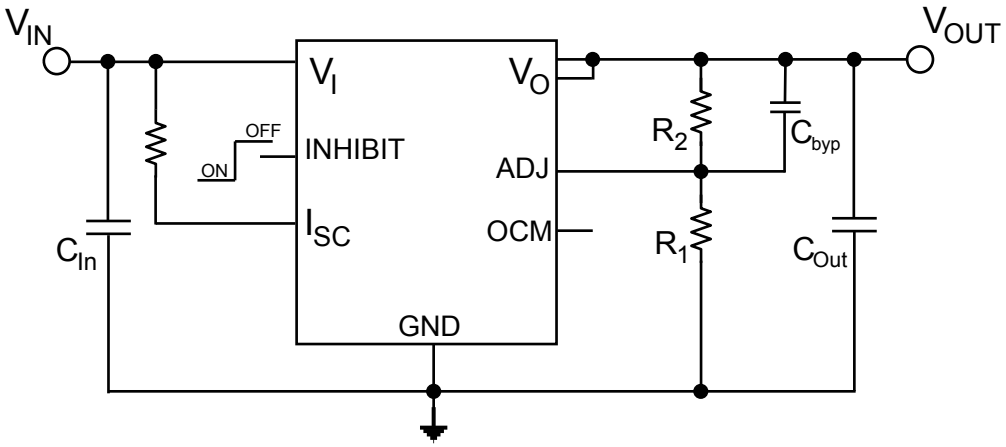
Note: Exceeding maximum ratings may damage the device. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
R_{thJA}	Thermal resistance junction-ambient 2s2p board jedec board	25	°C/W

4 Application circuit

Figure 3. **Typical application circuit**



5 Electrical characteristics

$V_I = V_O + 2.5$ V, $T_j = +25$ °C, $C_I = 10$ µF, $C_O = 10$ µF tantalum, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Input voltage	I_O = 1 A, T_J= -40 to 125 °C	3		12	V
V_{ADJ}	Reference voltage	I_O = 5 mA, $V_O = V_{ADJ}$,T_J= -40 to 125 °C	1.19	1.23	1.27	V
$\Delta V_O/\Delta V_i$	Line regulation	$V_I = V_O$+2.5 V to 12 V, I_O = 5 mA	-	0.07	-	%
$\Delta V_O/\Delta I_O$	Load regulation	$V_I = V_O$+2.5 V, I_O = 5 mA to 1 A	-	0.4	-	%
I_{SHORT}	Output current limit(1)	Adjustable by external resistor	1	3.8	-	A
V_d	Dropout voltage	I_O = 400 mA, V_{out} = 3 V, T_J = -40 to 125 °C	-	0.35	0.7	V
		I_O = 1 A, V_{out} = 3 V, T_J= -40 to 125 °C	-	0.5	1	V
		I_O = 2 A, V_{out} = 3 V, T_J = -40 to 125 °C	-	0.75	1.5	V
I_q	Quiescent current	$V_I = V_O$+2.5 V to 12 V, I_O = 5 mA, on mode	-	1.6	6	mA
		$V_I = V_O$+2.5 V to 12 V, I_O = 30 mA, on mode	-	2.7	8	mA
		$V_I = V_O$+2.5 V to 12 V, I_O = 300 mA, on mode	-	11	25	mA
		$V_I = V_O$+2.5 V to 12 V, I_O = 1 A, on mode	-	32	62	mA
		V_I = 12 V V_{INH} = 3 V, off mode	-	0.3	-	mA
SVR	Supply voltage rejection(1)	$V_I = V_O$+2.5 V ± 1 V, I_O = 5 mA, V_O=3 V, f = 33 kHz	-	50	-	dB
$V_{INH\ (OFF)}$	Inhibit turn-off voltage	I_O = 5 mA, T_J = -40 to 125 °C	2.4	-	-	V
$V_{INH\ (ON)}$	Inhibit turn-on voltage	I_O = 5 mA, T_J= -40 to 125 °C	-	-	0.8	V
I_{INH}	Shutdown input current	V_{INH} = 5 V	-	120	-	µA
V_{OCML}	Overcurrent monitor voltage low	I_{OCM} = 10 mA (sunk current), V_I = 12 V	-	0.4	-	V
V_{OCMH}	Overcurrent monitor voltage high	I_{OCM} = -10 µA (sourced current) $V_I = V_O$+2.5 V to 12 V	-	V_I	-	V
eN	Output noise voltage(1)	B= 10 Hz to 100 kHz I_O = 5 mA to 2 A	-	40	-	µVrms/V

1. *These values are guaranteed by design.*

6 Device functional description

The LEO3910 adjustable voltage regulator contains a PNP type power element controlled by a signal resulting from an amplified comparison between the internal temperature-compensated band-gap and the fraction of the desired output voltage value obtained from an external resistor divider bridge. The device is protected by several functional blocks.

6.1 ADJ pin

The output voltage feedback comes through an external resistor divider (R1, R2 as in the typical application schematic), whose mid-point connected to the ADJ pin (allowing all possible output voltage settings as per user requirements).

6.2 INHIBIT

By setting the INHIBIT pin TTL high, the device switches off the output current and voltage. The device is ON when the INHIBIT pin is set low. Since the INHIBIT pin is pulled down internally, it can be left floating in cases where the inhibit function is not used.

6.3 Overtemperature protection

The LEO3910 is protected by a junction temperature detection circuit, turning the device “OFF” when the temperature attains 175 °C. The recovery of the ON mode occurs with a hysteresis of 40 °C. Combined with the other protection blocks, the device is protected from destructive junction temperature excursions in all load conditions. It should be noted that when the internal temperature detector reaches 175 °C, the active power element can be as high as 225 °C. Prolonged operation under these conditions far exceeds the maximum operating ratings and the device reliability cannot be guaranteed.

6.4 Overcurrent protection

The device is equipped with a circuit having the purpose of limiting the maximum load current, in order to protect the output stage against possible overcurrent-related damages. By denoting ISHORT the maximum current available at output, this value can be modified externally by a resistor between the pins ISC and Vin, with a typical value range of 17 kΩ to 200 kΩ.

As the behavior of the overcurrent protection, when the load current approaches the mentioned ISHORT, the regulation is inhibited.

To maintain optimal VO regulation and at the same time an acceptable accuracy for ISHORT, it is necessary:

- to set an ISHORT> = 1 A
- to set ISHORT 1.6 times greater than the maximum desired application I_O to fix enough margins from the regulation range.

When IO reaches typically ISHORT – 300 mA, the current limiter overrules the regulation, VO starts to drop and the OCM flag rises. When no current limitation adjustment is required, the ISC pin can be left unbiased.

6.5 OCM pin

In the event of an overcurrent at the output, a voltage level of 0.4 V is present at the OCM pin. In other conditions, this voltage equals V_I. The OCM pin is internally pulled up by a 5 kΩ resistor up to V_I. It is buffered and can sink up to 10 mA.

7 Application information

To adjust the output voltage, the R_2 resistor must be connected between the V_O and ADJ pins. The R_1 resistor must be connected between ADJ and ground. Resistor values can be derived from the following formula:

$VO = VADJ (R_1 + R_2) / R_1$

The V_{ADJ} is typically 1.23 V, controlled by the internal temperature-compensated band gap block.

The minimum input voltage is 3 V. The LEO3910 is designed to operate for $V_I - V_O >$ of the minimum specified dropout. The value of R_1, the resistance between ADJ pin and GND, must not be greater than 10 kΩ, in order to keep the output feedback error below 0.2%. A minimum of 0.5 mA I_O must be set to ensure perfect no-load regulation. It is advisable to dissipate this current into the divider bridge resistor.

The inhibit function switches off the output current very quickly. According to Lenz's law, the external circuitry reacts with LdI/dt terms which can be of high amplitude in case somewhere a serial coil inductance exists. Large transient voltage would develop on both device terminals. It is advisable to protect the device with Schottky diodes to prevent negative voltage excursions. In the worst case, a 14 V Zener diode could protect the device input.

All available VO pins should always be externally interconnected, otherwise the stability and reliability of the device cannot be guaranteed.

To ensure regulator stability, input and output capacitors with a minimum 10 µF are mandatory. These capacitors must be connected as close as possible to the device terminals.

In the case of high-current operation, an important factor to look at for the reliability target of the space application is the sustainable surge current of the capacitors used. The surge current is known to be one of the major failure mechanisms for these parts, especially when the equipment is turned ON. Tantalum capacitors manufactured per military specifications (MIL-PRF-55365) are established reliability parts targeted for less than 0.001% of failures per 1000 hours (failure rate< 10 FIT).

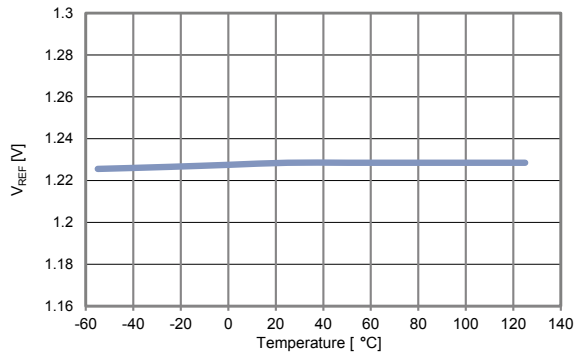
Derating is a means for application engineers of space systems to further reduce the probability of failures by limiting the level of stresses to capacitors during application. Typical derating requirements for solid tantalum capacitors limit the maximum applied voltage to 50% of the rated voltage (VR) and the inrush currents are bounded by additional resistors used in series with the capacitors.

In addition, a ceramic capacitor of at least 100nF in parallel to the input and output bulk capacitors must be used for decoupling purposes. A 470 nF polyester capacitors, put close to the regulator between input and ground, helps further improving the LEO3910 reliability by filtering potentially dangerous over voltages spikes coming out during particular conditions.

A separate kelvin voltage sensing line provides the ADJ pin with exact load "high potential" information (see Figure 4. Application diagram for remote sensing operation). But variable remote load current consumption induces variable Iq current (Iq is roughly the IO current divided by the hFE of the internal PNP series power element) routed through the parasitic series line resistor RW2. To compensate for this parasitic voltage, resistor RW1 can be introduced to provide the necessary compensating voltage signal to the ADJ pin. A ceramic or polyester 47nF CBYP capacitor between ADJ and VO pins is recommended when the remote sensing technique is implemented.

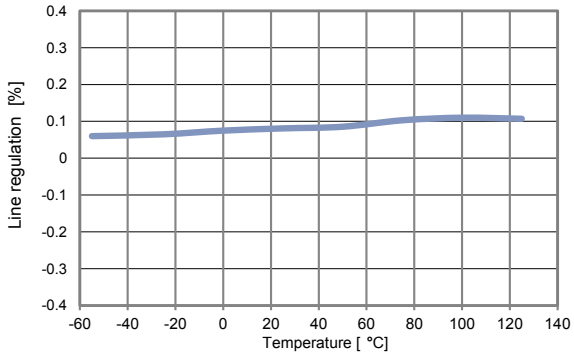
Since the LEO3910 adjustable voltage regulator is manufactured with very high speed bipolar technology (6 GHz fT transistors), the PCB layout must be designed with exceptional care, with very low inductance and low mutually coupling lines. Otherwise, high frequency parasitic signals may be picked up by the device resulting in system self-oscillation. The benefit is an SVR performance extended to far higher frequencies.

Figure 4. Reference voltage vs. temperature (V_{IN}=V_{OUT}+2.5 V)



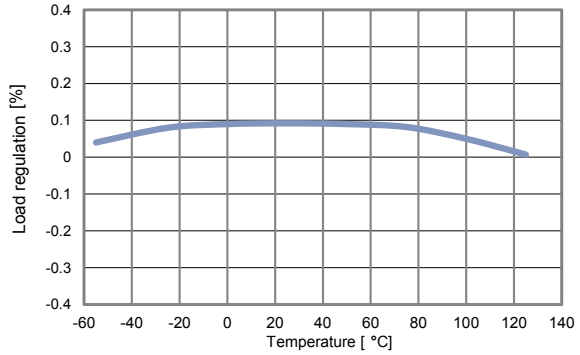
Vin=Vout+2.5V, Vout= Vadj, Cin=0.1Fµ, Cout=1µF (tantalum), Iout = 5 mA

Figure 5. Line regulation vs. temperature



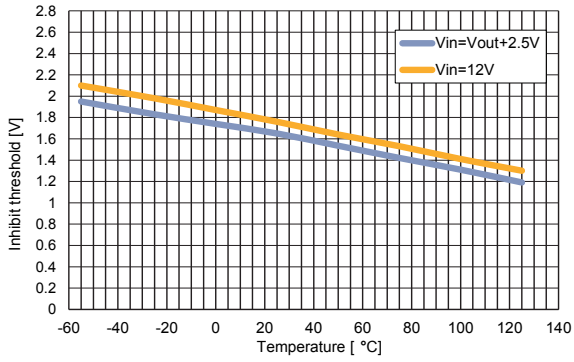
Vout+2.5 V<Vin <12V, Vout= Vadj, Cin=0.1Fµ Cout=1µF (tantalum),Iout=5mA

Figure 6. Load regulation vs. temperature (I_{OUT}= 5 mA to 1 A)



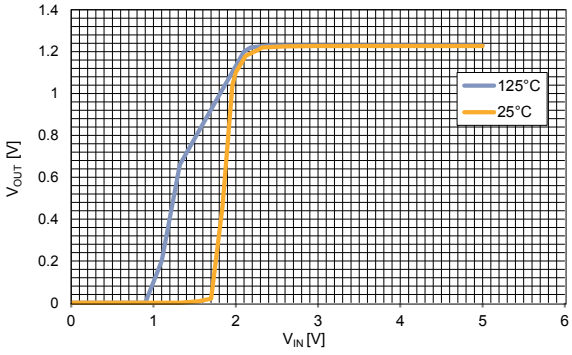
Vin=Vout+2.5V, Vout=Vadj, Cin=0.1µF, Cout=1µF (tantalum),5mA<Iout<1 A

Figure 7. Inhibit threshold vs. temperature



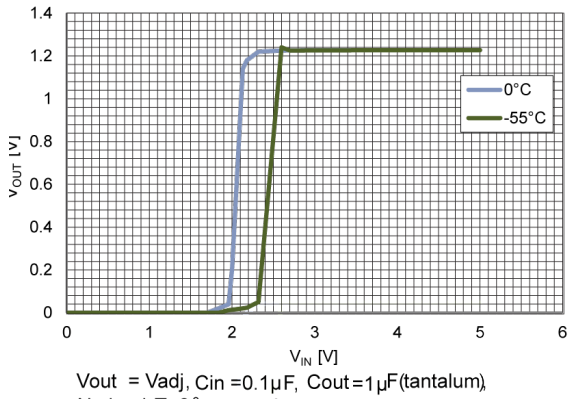
Vout =Vadj, Cin=0.1 µF, Cout =1 µF(tantalum), No load

Figure 8. Output voltage vs input voltage (I_{OUT}=0 mA,T=25 °C and T=125 °C)



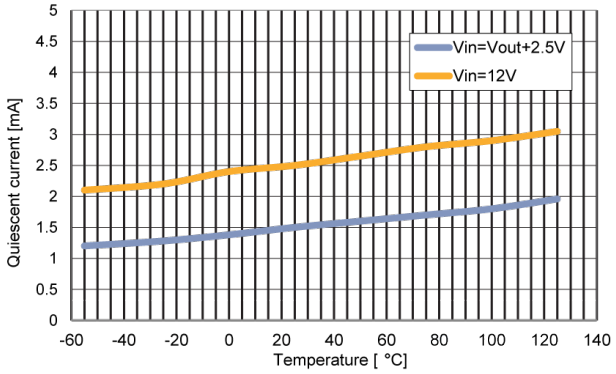
Vout = Vadj, Cin =0.1µF, Cout=1µF(tantalum), No load, T=25 °C, T=125 °C

Figure 9. Output voltage vs input voltage (I_{OUT}=0 mA,T=0 °C and T=-55 °C)



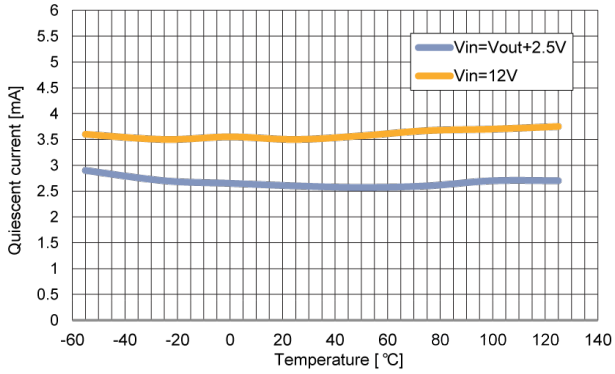
Vout = Vadj, Cin =0.1µF, Cout=1µF(tantalum), No load, T=0 °C, T= 55 °C

Figure 10. Quiescent current vs. temperature (no load)



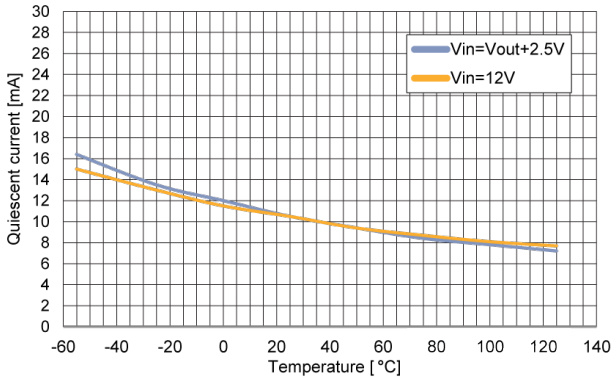
Vout = Vadj, Cin =0.1µF, Cout =1µF(tantalum), no load

Figure 11. Quiescent current vs. temperature (I_{OUT} = 30 mA)



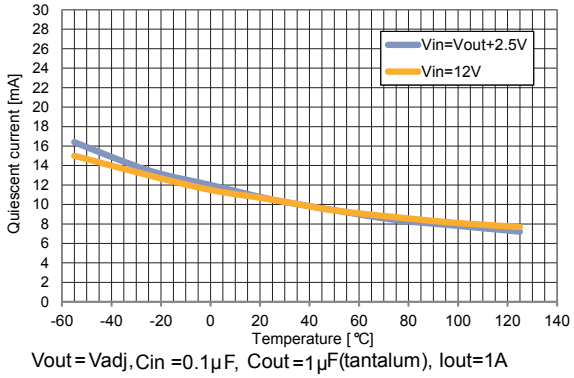
Vout = Vadj, Cin =0.1µF, Cout =1µF(tantalum), Iout=30 mA

Figure 12. Quiescent current vs. temperature (I_{OUT} = 300 mA)



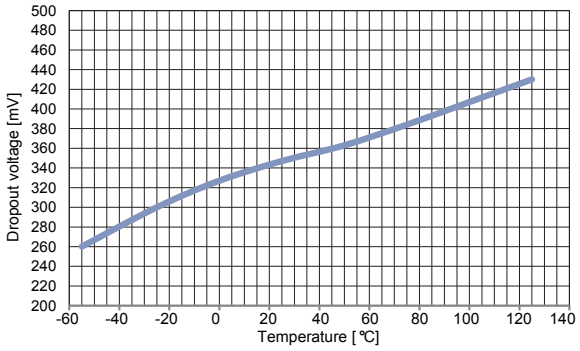
Vout = Vadj, Cin =0.1µF, Cout =1µF(tantalum), Iout=300 mA

Figure 13. Quiescent current vs. temperature (I_{OUT} = 1 A)



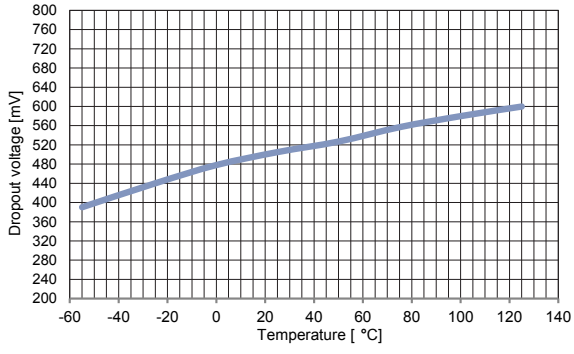
Vout = Vadj, Cin =0.1µF, Cout =1µF(tantalum), Iout=1A

Figure 14. Dropout voltage vs. temperature (V_{OUT}=3 V, I_{OUT}=400 mA)



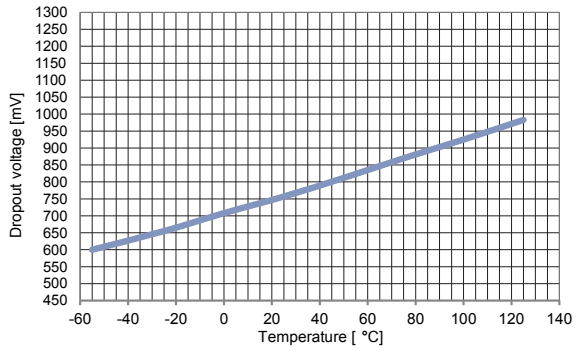
Vout = 3V, Cin = 0 1. µF, Cout =1µF(tantalum), Iout=400 mA

Figure 15. Dropout voltage vs. temperature (V_{OUT}=3 V, I_{OUT}=1 A)



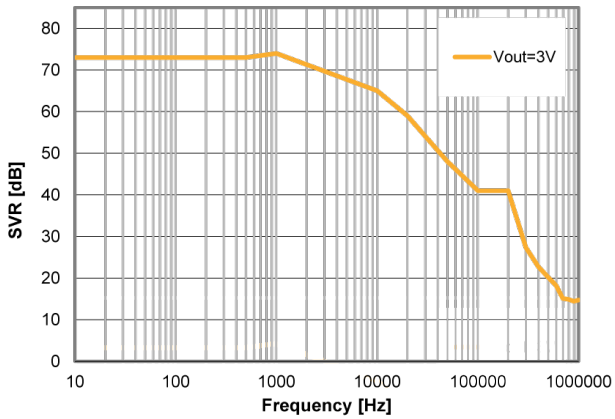
Vout = 3V, Cin = 0 1. µF, Cout =1µF(tantalum), Iout=1 A

Figure 16. Dropout voltage vs. temperature (V_{OUT}=3 V, I_{OUT}=2 A)



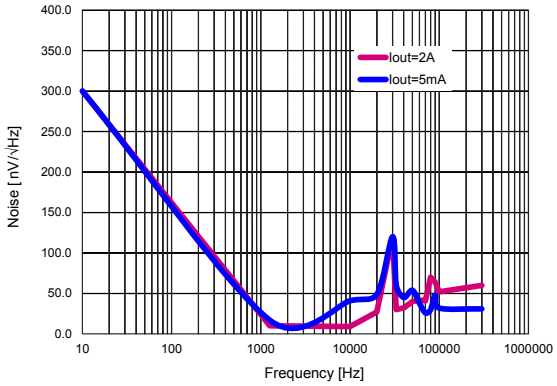
Vout = 3V, Cin = 0 1. µF, Cout = 1 µF(tantalum),Iout=2 A

Figure 17. SVR vs. frequency



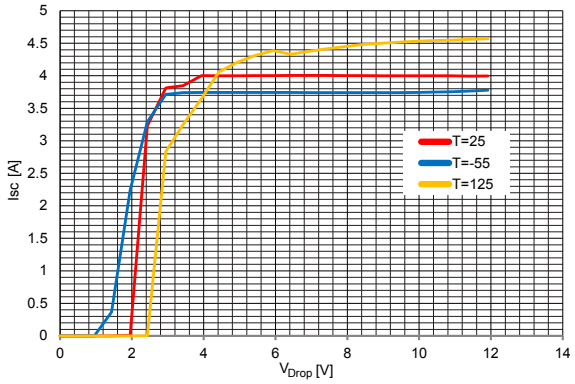
Vripple = ± 1 V, Cin= 0.1 µF, Cout = 1 µF (tant),
Iout = 5 mA, T= 25 °C

Figure 18. Output noise spectrum (V_{OUT}=V_{adj}, C_{OUT}=1 µF)



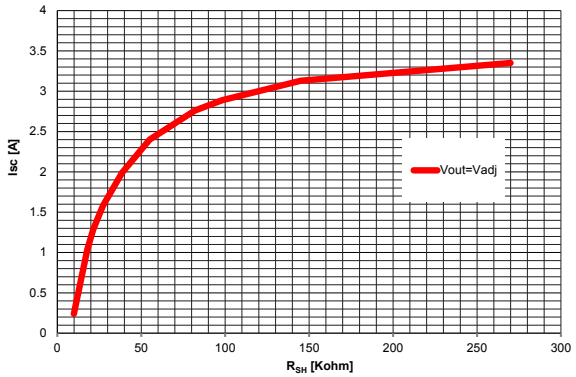
V_{IN} = 3.5V, V_{out}=V_{ADJ}, Cin = 220µF, Cout = 1 µF(tantalum)

Figure 19. Short-circuit current vs. dropout voltage, (V_{OUT}=V_{adj})



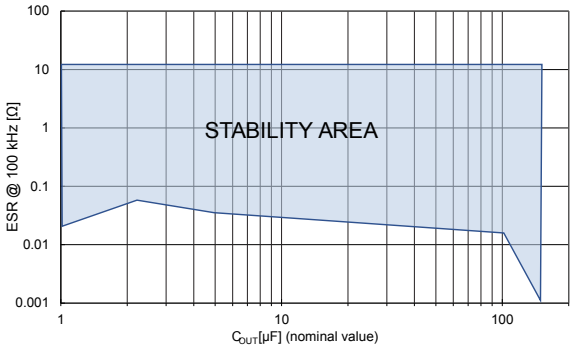
C_{IN}= 0.1µF, Cout = 1 µF(tantalum), T=25°C, No R_{SH}

Figure 20. Short-circuit current vs. R_{SH}



C_{IN}= 0.1µF, Cout = 1 µF(tantalum)

Figure 21. Stability plan



V_{IN} from 3 to 12V; I_{OUT} from 5mA to 2A; V_{OUT} = V_{ADJ}; C_{IN} =1 µF; T= 25 °C

8 Radiations

Total ionizing dose (TID):

The LEO3910 is tested and characterized according to condition A of MIL-STD-883.

All parameters provided in Table 4. Electrical characteristics apply to both pre- and post-irradiation, as follows:

- Total ionizing dose (TID) are performed in accordance with MIL-STD-883
- The initial characterization is performed in qualification only on both biased and unbiased parts
- Each new production lot is tested at high dose rate, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy-ions:

The behavior of the product when submitted to heavy-ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 5. Radiations

Symbol	Characteristics	Value
TID (1)	• High-dose rate (40 krad (Si)/h) – Temperature 25 °C – Performed on 5 biased parts • Low-dose rate (10 mrad (Si)/s)	Within Table 4. Electrical characteristics up to 50 krad(Si)
SEL(2)	• Let: 62.5 MeV.cm^{2}mg (Xenon ions) • Temperature 125 °C • Fluence of 1 x 10^7 n/cm² (10 million of particles per cm²) • Normal incidence	Immune to SEL up to 62.5 MeV.cm²/mg
SET	• Temperature 25 °C	Characterized
TNID	• (with 50 MeV protons)	Up to 3x1011 protons/cm²

1. *A total ionizing dose (TID) of 50 krad(Si) is equivalent to 500 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latchup.*

9 Outgassing

Specification (tested per ASTM E 595)	Value	Unit
Recovered mass loss (RML)[1]	0.06	%
Collected volatile condensable material (CVCM)[2]	0.00	%

1. *RML < 1%.*
2. *CVCM < 0.1%.*

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 POWER-SO 20 package information

Figure 22. **POWER-SO 20 package outline**

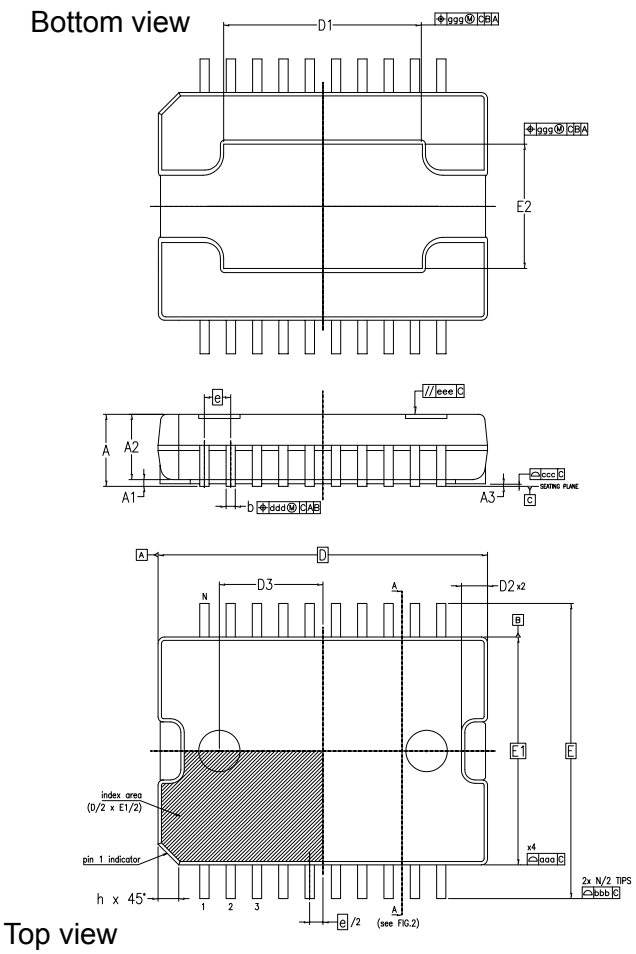


Figure 23. **POWER-SO 20 detail A**

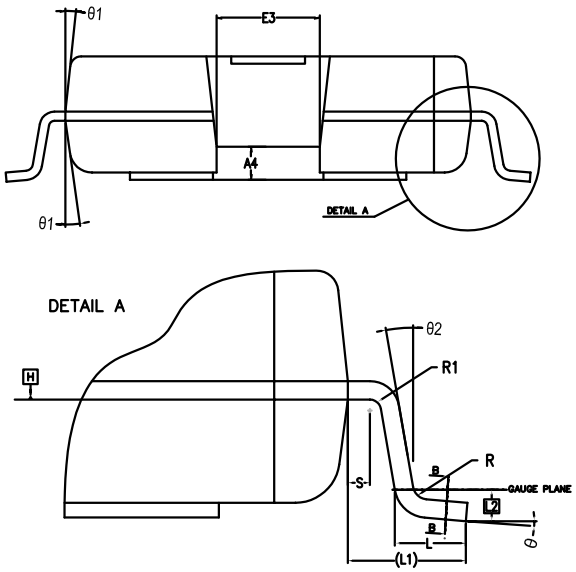


Figure 24. **POWER-SO 20 detail B**

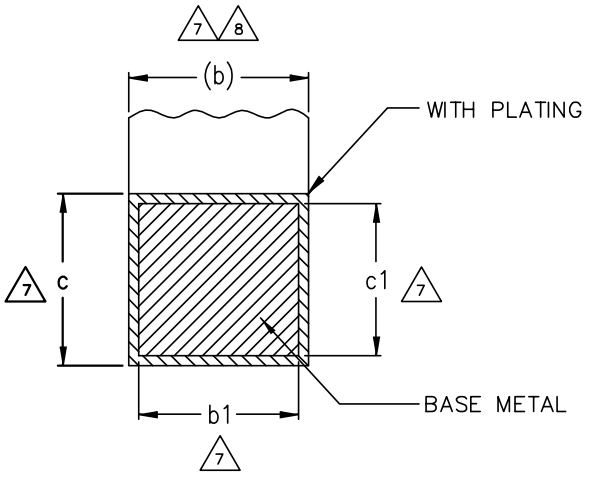


Table 6. **POWER-SO 20 mechanical data**

Symbol	Milimeters		
	Min.	Typ.	Max.
θ	0°	-	8°
θ1	5°	-	10°
θ2	0°	-	-
A	-	-	3.50
A1	0.20	-	0.275
A2	3.10	-	3.20
A3	0.00	-	0.075
A4	0.83	-	0.95
b	0.40	-	0.53
b1	0.40	0.45	0.50
c	0.23	-	0.32
D	15.90 BSC		
D1	Variation		
D2	-	-	1.10
D3	-	5.00	-
e	1.27 BSC		
E	14.20 BSC		
E1	11.00 BSC		
E2	Variation		
E3	-	-	2.85
h	-	-	1.10
L	0.85	-	1.05
L1	1.60 REF		
L2	0.35 BSC		
N	20		
R	0.20	-	-
R1	0.20	-	-
S	0.25	-	-

Table 7. **Tolerance of form and position**

Symbol	Drawing
aaa	0.10
bbb	0.30
ccc	0.10
ddd	0.25
eee	0.10
ggg	0.25
Note	1.2

Table 8. **Variations**

Symbol	Drawing			Opt.
	Min.	Typ.	Max.	
D1	9.00	-	13.00	A
D2	5.60	-	6.20	

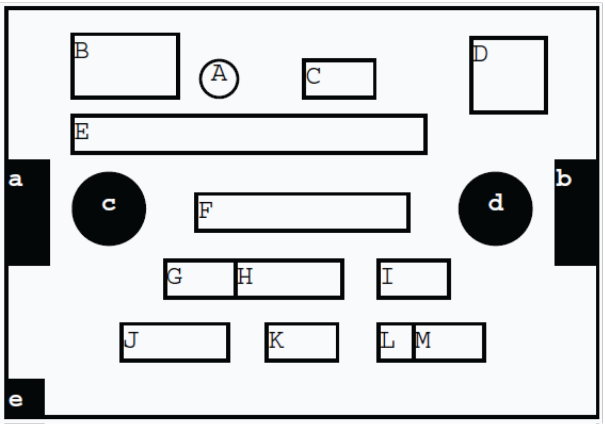
11 Ordering information

Table 9. Ordering information

Order code	Quality level	Package	Lead-finish	Marking	Packing
LEO3910PDT-D	Engineering sample	POWER-SO 20	NiPdAu	DLEO3910	Tape and reel
LEO3910PDT(1)	Flight model	POWER-SO 20	NiPdAu	LEO3910PDT	Tape and reel

1. *Under development*

Figure 25. POWER-SO 20 marking



a – Slug
b – Slug
e – PIN1- REF
B – ST logo
E – Marking
G – Assy plant
J – Country of origin
K – Testing and finishing plant
L – Assy year
M – Assy week

Table 10. Order code

LEO	3910	PD	T
LEO qualification	Product	POWER-SO 20 package	Tape and reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
17-May-2021	1	Initial release.
22-Feb-2022	2	Updated Section 5: Electrical characteristics and Section 7: Application information.
20-Jun-2024	3	Minor text changes.

Contents