

# TinyLogic UHS 2-Input NAND Gate, Open Drain Output

## NC7SZ38

### Description

The NC7SZ38 is a single 2-Input NAND gate with open drain output stage from onsemi's Ultra-High Speed Series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a very broad V<sub>CC</sub> operating range. The device is specified to operate over the 1.65 V to 5.5 V V<sub>CC</sub> range. The inputs and output are high impedance when V<sub>CC</sub> is 0 V. Inputs tolerate voltages up to 5.5 V, independent of V<sub>CC</sub> when in the high impedance state. The open drain output stage tolerates voltages up to 6 V independent of V<sub>CC</sub> when in the high impedance state.

### Features

- Ultra-High Speed: t<sub>PD</sub> = 2.2 ns (Typical) into 50 pF at 5 V V<sub>CC</sub>
- Open Drain Output Stage for OR Tied Applications
- High Output Sink Drive:  $\pm 24$  mA at 3 V V<sub>CC</sub>
- Broad V<sub>CC</sub> Operating Range: 1.65 V to 5.5 V
- Matches Performance of LCX Operated at 3.3 V V<sub>CC</sub>
- Power Down High-Impedance Inputs / Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SOT23-5, SC-74A and SC-88A Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

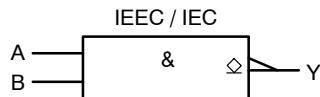
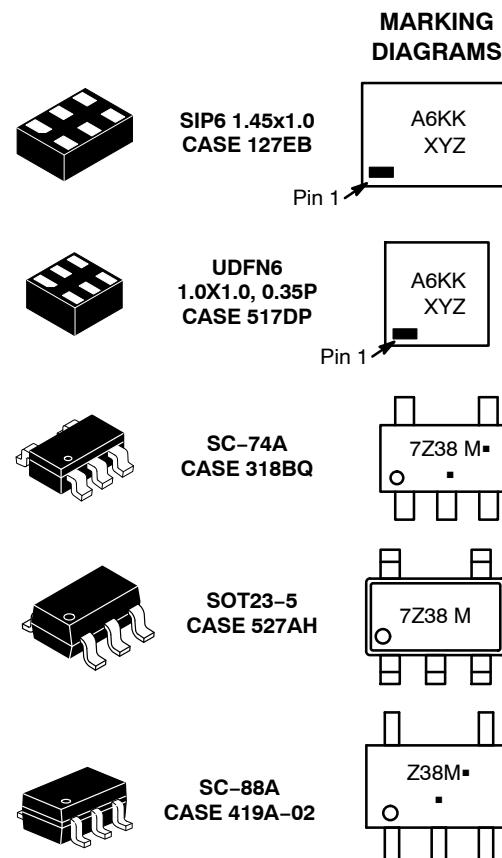


Figure 1. Logic Symbol



A6, 7Z38, Z38 = Specific Device Code  
 KK = 2-Digit Lot Run Traceability Code  
 XY = 2-Digit Date Code Format  
 Z = Assembly Plant Code  
 M = Data Code\*  
 - = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

## Pin Configurations

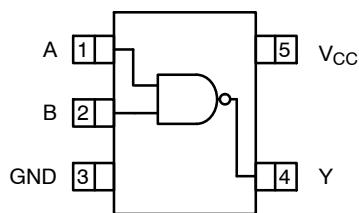


Figure 2. SOT23-5, SC-88A and SC-74A (Top View)

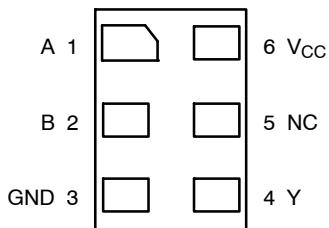


Figure 3. MicroPak (Top Through View)

## PIN DEFINITIONS

Pin # SC-88A / SC-74A/ SOT23-5	Pin # MicroPak	Name	Description
1	1	A	Input
2	2	B	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V <sub>CC</sub>	Supply Voltage
	5	NC	No Connect

## FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	*H
L	H	*H
H	L	*H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

\*H = High Impedance Output State, Open Drain

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
$V_{CC}$	Supply Voltage		-0.5	6.5	V
$V_{IN}$	DC Input Voltage		-0.5	6.5	V
$V_{OUT}$	DC Output Voltage		-0.5	6.5	V
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0$ V	-	-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < 0$ V	-	-50	mA
$I_{OUT}$	DC Output Current		-	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current		-	$\pm 50$	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
$T_J$	Junction Temperature Under Bias		-	+150	°C
$T_L$	Junction Lead Temperature (Soldering, 10 Seconds)		-	+260	°C
$P_D$	Power Dissipation in Still Air	SC-74A / SOT23-5	-	390	mW
		SC-88A	-	332	
		MicroPak-6	-	812	
		MicroPak2™-6	-	812	
ESD	Human Body Model, JEDEC: JESD22-A114		-	4000	V
	Charge Device Model, JEDEC: JESD22-C101		-	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.50	5.5	
$V_{IN}$	Input Voltage		0	5.5	V
$V_{OUT}$	Output Voltage		0	5.5	V
$T_A$	Operating Temperature		-40	+85	°C
$t_r, t_f$	Input Rise and Fall Times	$V_{CC} = 1.8$ V, $2.5$ V $\pm 0.2$ V	0	20	ns/V
		$V_{CC} = 3.3$ V $\pm 0.3$ V	0	10	
		$V_{CC} = 5.0$ V $\pm 0.5$ V	0	5	
$\theta_{JA}$	Thermal Resistance	SC-74A / SOT23-5	-	320	°C/W
		SC-88A	-	377	
		MicroPak-6	-	154	
		MicroPak2-6	-	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- Unused inputs must be held HIGH or LOW. They may not float.

## DC ELECTRICAL CHARACTERISTICS

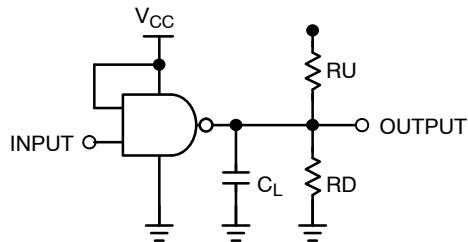
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage	1.65 to 1.95		0.65 V <sub>CC</sub>	—	—	0.65 V <sub>CC</sub>	—	V
		2.30 to 5.50		0.70 V <sub>CC</sub>	—	—	0.70 V <sub>CC</sub>	—	
V <sub>IL</sub>	LOW Level Input Voltage	1.65 to 1.95		—	—	0.35 V <sub>CC</sub>	—	0.35 V <sub>CC</sub>	V
		2.30 to 5.50		—	—	0.30 V <sub>CC</sub>	—	0.30 V <sub>CC</sub>	
I <sub>LKG</sub>	HIGH Level Output Leakage	5.50	V <sub>IN</sub> = V <sub>IL</sub> , V <sub>OUT</sub> = V <sub>CC</sub> or GND	—	—	±5	—	±10	µA
V <sub>OL</sub>	LOW Level Output Voltage	1.65	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 100 µA	—	0.00	0.10	—	0.10	V
		1.80		—	0.00	0.10	—	0.10	
		2.30		—	0.00	0.10	—	0.10	
		3.00		—	0.00	0.10	—	0.10	
		4.50		—	0.00	0.10	—	0.10	
		1.65	I <sub>OL</sub> = 4 mA	—	0.80	0.24	—	0.24	
		2.30	I <sub>OL</sub> = 8 mA	—	0.10	0.30	—	0.30	
		3.00	I <sub>OL</sub> = 16 mA	—	0.15	0.40	—	0.40	
		3.00	I <sub>OL</sub> = 24 mA	—	0.22	0.55	—	0.55	
		4.50	I <sub>OL</sub> = 32 mA	—	0.22	0.55	—	0.55	
I <sub>IN</sub>	Input Leakage Current	5.50	V <sub>IN</sub> = 5.5 V, GND	—	—	±1	—	±10	µA
I <sub>OFF</sub>	Power Off Leakage Current	0	V <sub>IN</sub> or V <sub>OUT</sub> = 5.5 V	—	—	1	—	10	µA
I <sub>CC</sub>	Quiescent Supply Current	5.50	V <sub>IN</sub> = 5.5 V, GND	—	—	2	—	20	µA

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t <sub>PZL</sub>	Propagation Delay (Figure 4, 5)	1.65	C <sub>L</sub> = 50 pF, R <sub>U</sub> = 500 Ω, R <sub>D</sub> = 500 Ω, V <sub>IN</sub> = 2 · V <sub>CC</sub>	—	6.5	12.7	—	13.2	ns
		1.80		—	5.4	10.5	—	11.0	
		2.50 ±0.20		—	3.5	7.0	—	7.5	
		3.30 ±0.30		—	2.8	5.0	—	5.2	
		5.00 ±0.50		—	2.2	4.3	—	4.5	
t <sub>PLZ</sub>		1.65	C <sub>L</sub> = 50 pF, R <sub>U</sub> = 500 Ω, R <sub>D</sub> = 500 Ω, V <sub>IN</sub> = 2 · V <sub>CC</sub>	—	5.5	12.7	—	13.2	ns
		1.80		—	4.6	10.5	—	11.0	
		2.50 ±0.20		—	3.0	7.0	—	7.5	
		3.30 ±0.30		—	2.1	5.0	—	5.2	
		5.00 ±0.50		—	1.3	4.3	—	4.5	
C <sub>IN</sub>	Input Capacitance	0.00		—	4.0	—	—	—	pF
C <sub>OUT</sub>	Output Capacitance	0.00		—	5.0	—	—	—	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 2) (Figure 6)	3.30		—	5.1	—	—	—	pF
		5.00		—	7.3	—	—	—	

2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:  
I<sub>CCD</sub> = (C<sub>PD</sub>) (V<sub>CC</sub>) (f<sub>IN</sub>) + (I<sub>CCDstatic</sub>).

# NC7SZ38



NOTE:

3. CL includes load and stray capacitance.  
Input PRR = 10 MHz  $t_w$  = 500 ns.

Figure 4. AC Test Circuit

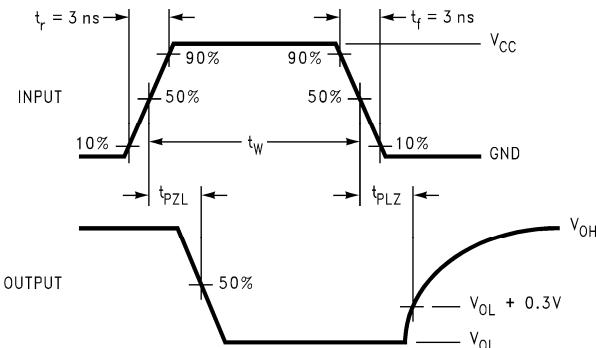
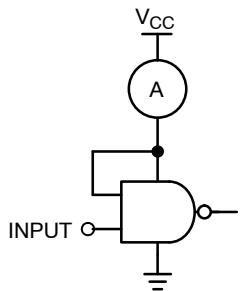


Figure 5. AC Waveforms



NOTE:

4. Input = AC Waveform;  $t_r = t_f = 1.8$  ns;  
PRR = 10 MHz; Duty Cycle = 50%.

Figure 6. Test Circuit

## DEVICE ORDERING INFORMATION

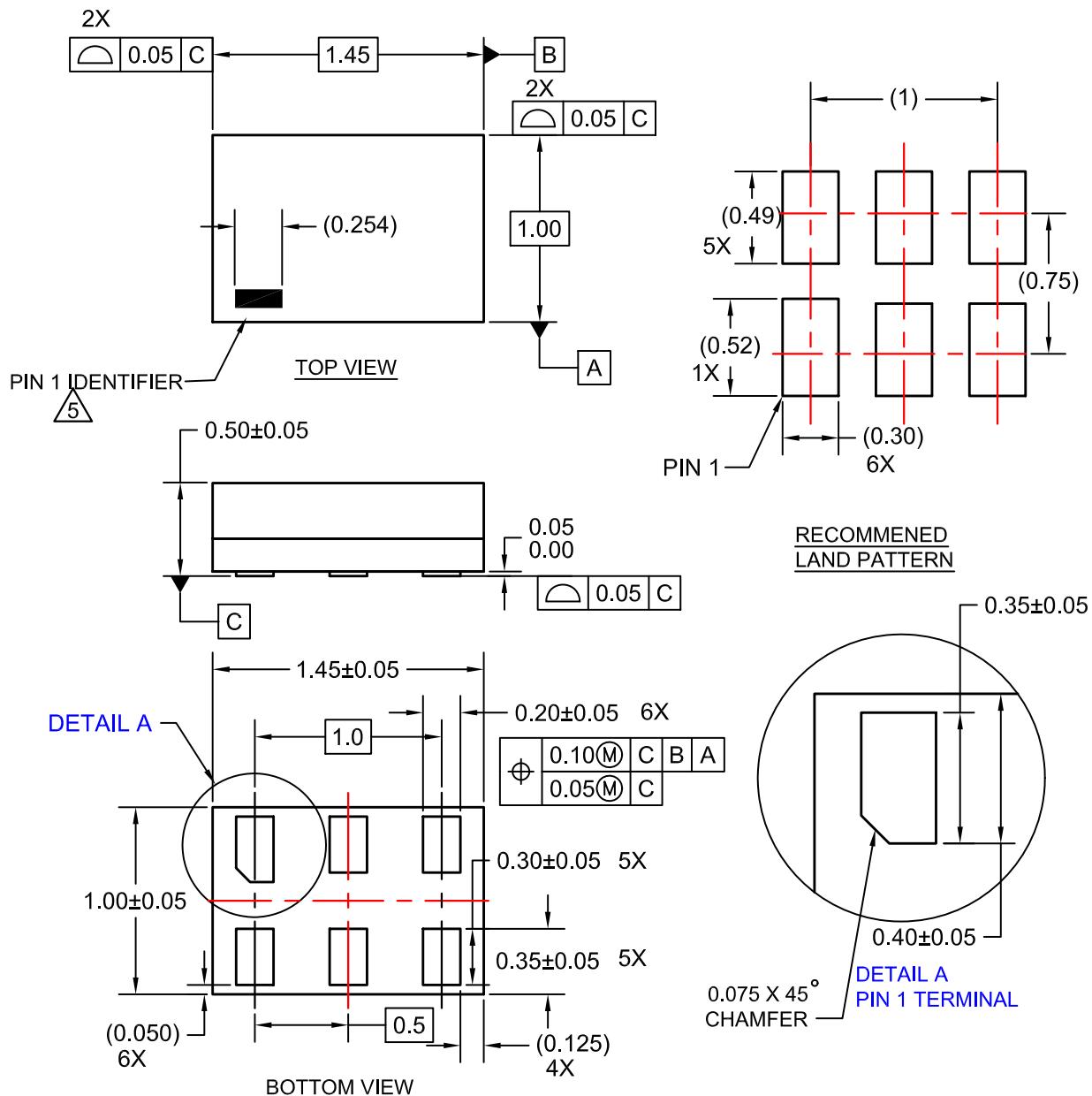
Device	Top Mark	Packages	Shipping <sup>†</sup>
NC7SZ38M5X	7Z38	SC-74A	3000 / Tape & Reel
NC7SZ38M5X-L22090	7Z38	SOT23-5	3000 / Tape & Reel
NC7SZ38P5X	Z38	SC-88A	3000 / Tape & Reel
NC7SZ38P5X-L22057	Z38	SC-88A	3000 / Tape & Reel
NC7SZ38L6X	A6	SIP6, MicroPak	5000 / Tape & Reel
NC7SZ38L6X-L22175	A6	SIP6, MicroPak	5000 / Tape & Reel
NC7SZ38FHX	A6	UDFN6, MicroPak2	5000 / Tape & Reel
NC7SZ38FHX-L22175	A6	UDFN6, MicroPak2	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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**SIP6 1.45X1.0**  
CASE 127EB  
ISSUE O

DATE 31 AUG 2016



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DESCRIPTION:	SIP6 1.45X1.0	PAGE 1 OF 1

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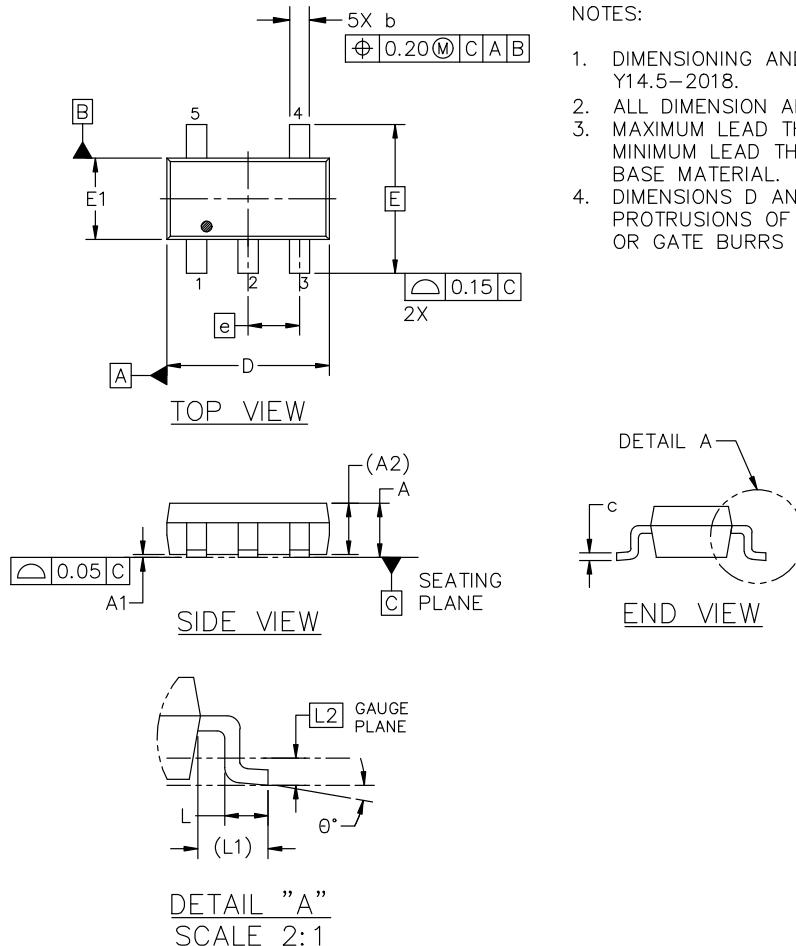
**MECHANICAL CASE OUTLINE**  
PACKAGE DIMENSIONS

**onsemi**<sup>TM</sup>

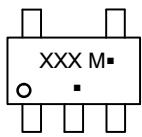


**SC-74A-5 3.00x1.50x0.95, 0.95P**  
CASE 318BQ  
ISSUE C

DATE 26 FEB 2024



**GENERIC  
MARKING DIAGRAM\***



XXX = Specific Device Code  
M = Date Code  
■ = Pb-Free Package

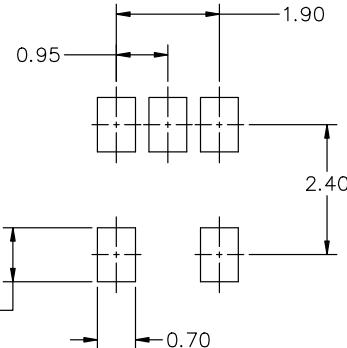
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.01	0.18	0.10
A2	0.95 REF.		
b	0.25	0.37	0.50
c	0.10	0.18	0.26
D	2.85	3.00	3.15
E	2.75 BSC		
E1	1.35	1.50	1.65
e	0.95 BSC		
L	0.20	0.40	0.60
L1	0.62 REF.		
L2	0.25 BSC		
θ	0°	5°	10°

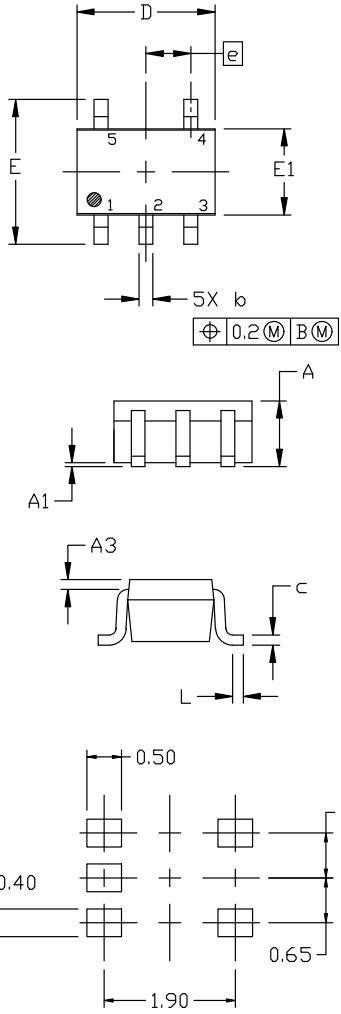


**RECOMMENDED MOUNTING FOOTPRINT\***

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98AON66279G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-74A-5 3.00x1.50x0.95, 0.95P	PAGE 1 OF 1

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**RECOMMENDED  
MOUNTING FOOTPRINT**

- \* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLE 1:**  
PIN 1. BASE  
2. Emitter  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

**STYLE 6:**  
PIN 1. Emitter 2  
2. BASE 2  
3. Emitter 1  
4. COLLECTOR  
5. COLLECTOR 2/BASE 1

**STYLE 2:**  
PIN 1. ANODE  
2. Emitter  
3. BASE  
4. COLLECTOR  
5. CATHODE

**STYLE 7:**  
PIN 1. BASE  
2. Emitter  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

**STYLE 3:**  
PIN 1. ANODE 1  
2. N/C  
3. ANODE 2  
4. CATHODE 2  
5. CATHODE 1

**STYLE 8:**  
PIN 1. CATHODE  
2. COLLECTOR  
3. N/C  
4. BASE  
5. Emitter

**STYLE 4:**  
PIN 1. SOURCE 1  
2. DRAIN 1/2  
3. SOURCE 1  
4. GATE 1  
5. GATE 2

**STYLE 9:**  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. ANODE

**STYLE 5:**  
PIN 1. CATHODE  
2. COMMON ANODE  
3. CATHODE 2  
4. CATHODE 3  
5. CATHODE 4

**Note:** Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

**SC-88A (SC-70-5/SOT-353)**  
CASE 419A-02  
ISSUE M

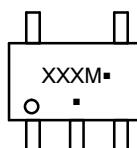
DATE 11 APR 2023

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3 0.20 REF			
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

**GENERIC MARKING  
DIAGRAM\***



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

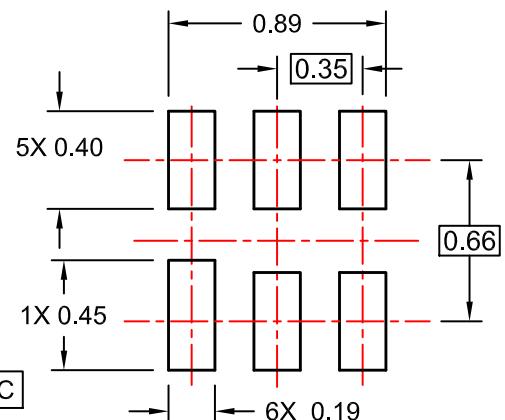
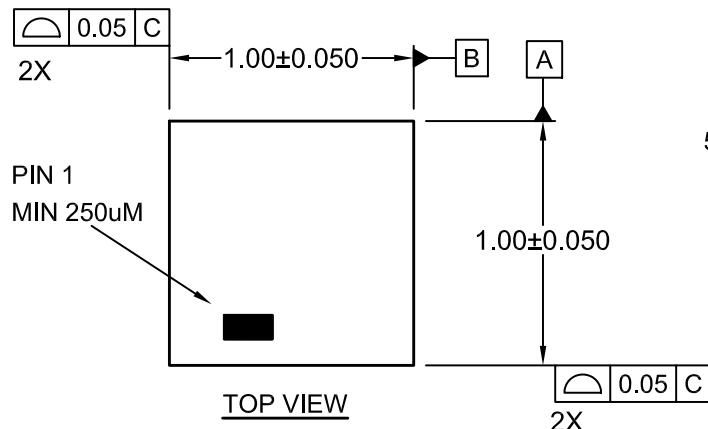
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<b>DESCRIPTION:</b>	SC-88A (SC-70-5/SOT-353)	<b>PAGE 1 OF 1</b>

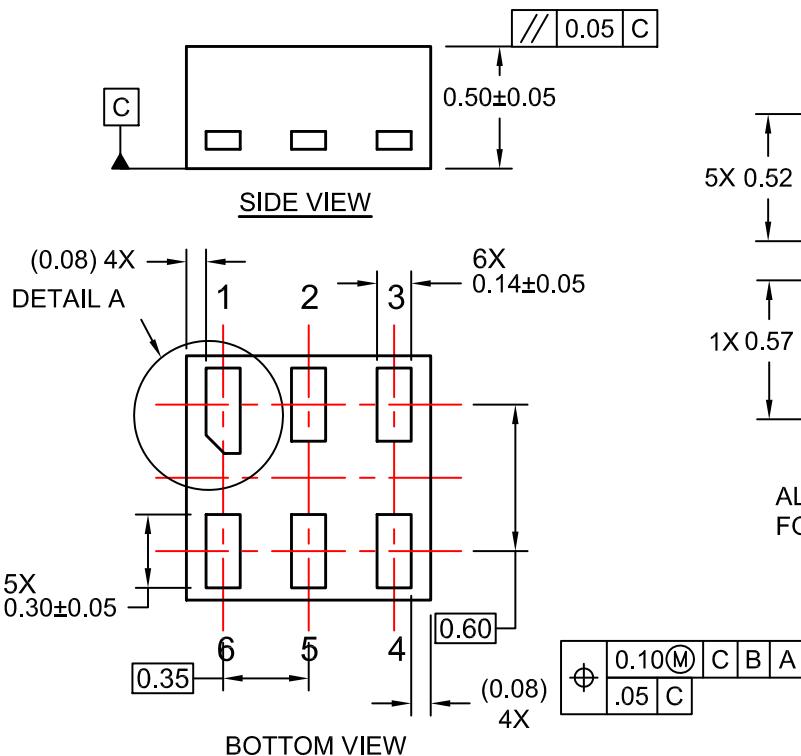
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**UDFN6 1.0X1.0, 0.35P  
CASE 517DP  
ISSUE O**

DATE 31 AUG 2016

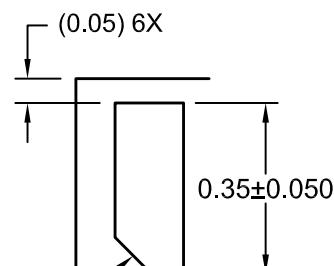


## RECOMMENDED LAND PATTERN FOR SPACE CONSTRAINED PCB



Technical drawing showing a component with three rows of three rectangular cutouts each. The top row has a width of 0.90 and a central cutout of 0.35. The middle row has a height of 5X 0.52. The bottom row has a height of 1X 0.57. The total width of the bottom row is 0.20.6X.

## ALTERNATIVE LAND PATTERN FOR UNIVERSAL APPLICATION



## NOTES:

- A. COMPLIES TO JEDEC MO-252 STANDARD
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

0.075X45° CHAMFER DETAIL A  
PIN 1 LEAD SCALE: 2X

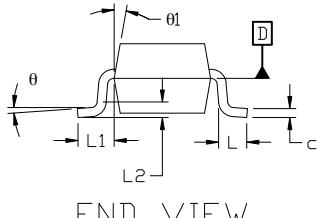
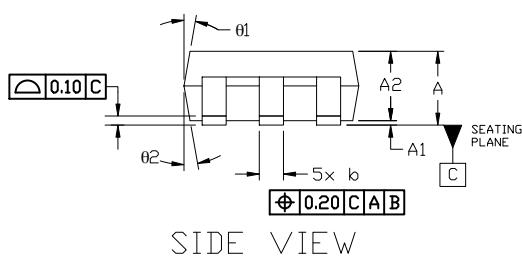
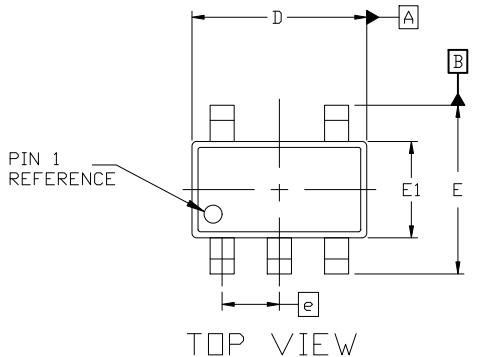
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<b>DESCRIPTION:</b>	<b>UDFN6 1.0X1.0, 0.35P</b>	<b>PAGE 1 OF 1</b>

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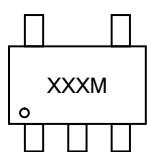


**SOT-23, 5 Lead**  
CASE 527AH  
ISSUE A

DATE 09 JUN 2021



**GENERIC  
MARKING DIAGRAM\***



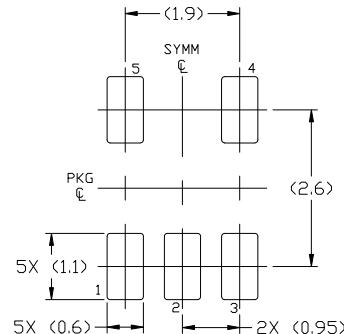
XXX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90	BSC	
E	2.80	BSC	
E1	1.60	BSC	
e	0.95	BSC	
L	0.30	0.45	0.60
L1	0.60	REF	
L2	0.25	REF	
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°



**RECOMMENDED  
MOUNTING FOOTPRINT**

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERMM/D.

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DESCRIPTION:	SOT-23, 5 LEAD	PAGE 1 OF 1

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