

MOSFET
OptiMOS™ 8 Power-Transistor, 100 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- High I_D current rating
- Tight $V_{GS(th)}$ spread
- Soft body diode recovery and low Q_{rr}
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	0.93	mΩ
I_D	484	A
Q_{oss}	498	nC
Q_G (0 V...10 V)	255	nC
Q_{rr} (100 A/μs)	90	nC

Part number	Package	Marking	Related links
IPT009N10NM8	PG-HSOF-8	009N10N8	-

TOLL

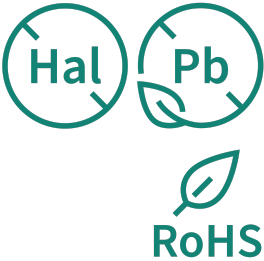
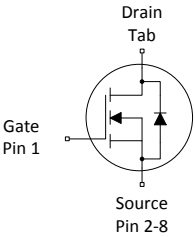
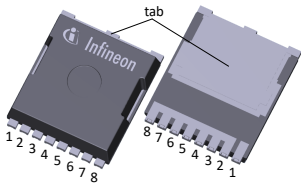




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	484	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				342		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				350		$V_{GS}=15\text{ V}$, $T_C=100\text{ °C}$
				42		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1936	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	1166	mJ	$I_D=100\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	500	W	$T_C=25\text{ °C}$
				3.8		$T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 14 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.2	0.3	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	40		
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}		-	62		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.4	2.8	3.2	V	$V_{DS}=V_{GS}$, $I_D=279\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
Zero gate voltage drain current ⁶⁾	I_{DSS}	-	10	100	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.79	0.93	m Ω	$V_{GS}=15\text{ V}$, $I_D=100\text{ A}$
			0.84	0.97		$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$
			0.90	1.0		$V_{GS}=8\text{ V}$, $I_D=50\text{ A}$
Gate resistance ⁶⁾	R_G	-	1.1	2.3	Ω	-
Transconductance ⁶⁾	g_{fs}	160	320	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁷⁾	C_{iss}	-	16000	21000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}		2400	3100		
Reverse transfer capacitance ⁷⁾	C_{rss}		450	790		
Turn-on delay time	$t_{d(on)}$	-	27.5	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		15			
Turn-off delay time	$t_{d(off)}$		86			
Fall time	t_f		31.5			

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	69	-	nC	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		46	-	nC	
Gate to drain charge ⁹⁾	Q_{gd}		62	93	nC	
Switching charge	Q_{sw}		85	-	nC	
Gate charge total ⁹⁾	Q_g		255	319	nC	
Gate plateau voltage	$V_{plateau}$		4.2	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	213	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ⁹⁾	Q_{oss}	-	498	662	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See "Gate charge waveforms" for parameter definition

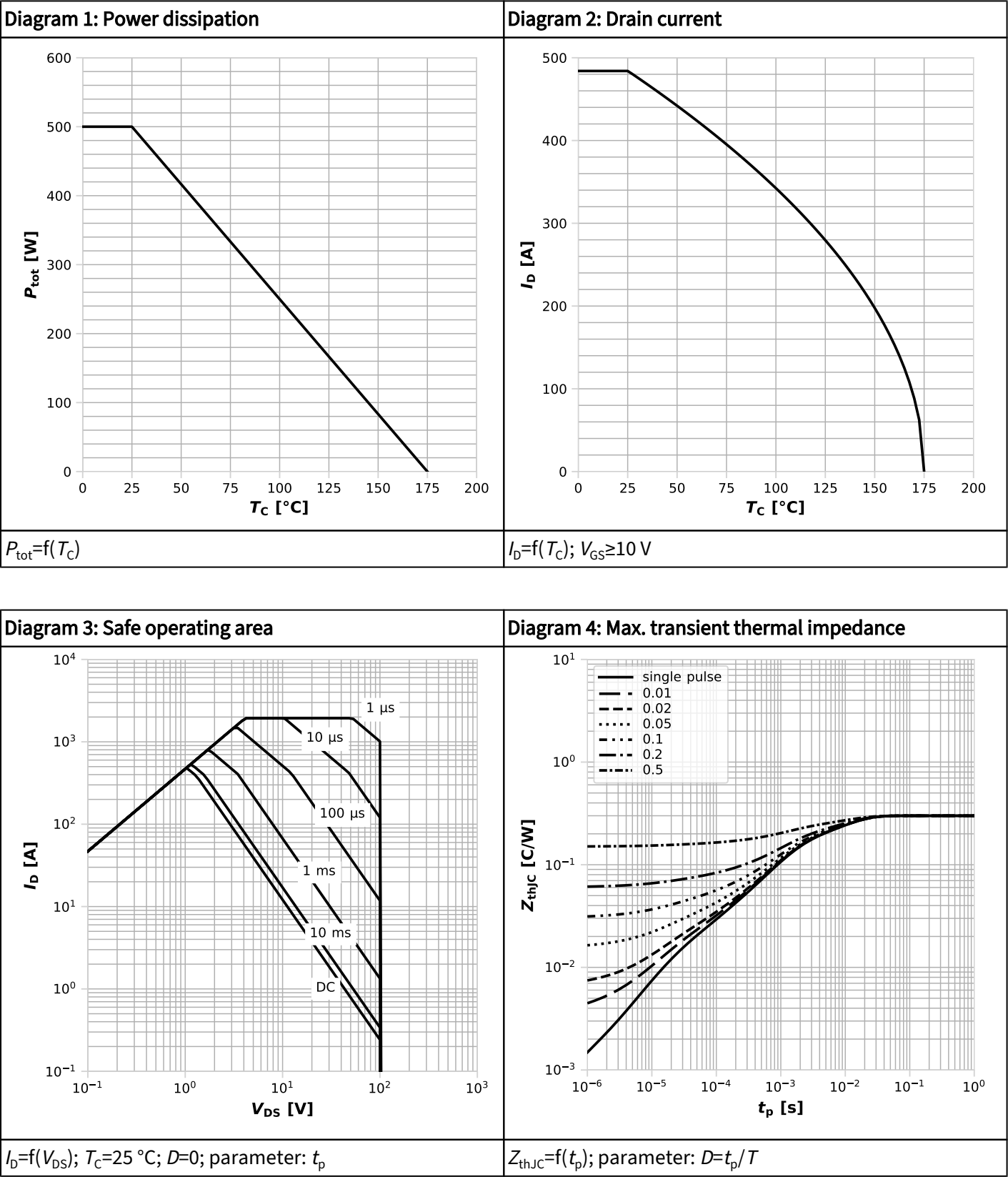
⁹⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	406	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			1936		
Diode forward voltage	V_{SD}	-	0.82	1	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁰⁾	t_{rr}	-	48	96	ns	$V_R=50\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		90	180	nC	
Reverse recovery time ¹⁰⁾	t_{rr}	-	53	106	ns	$V_R=50\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		805	1610	nC	

¹⁰⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams



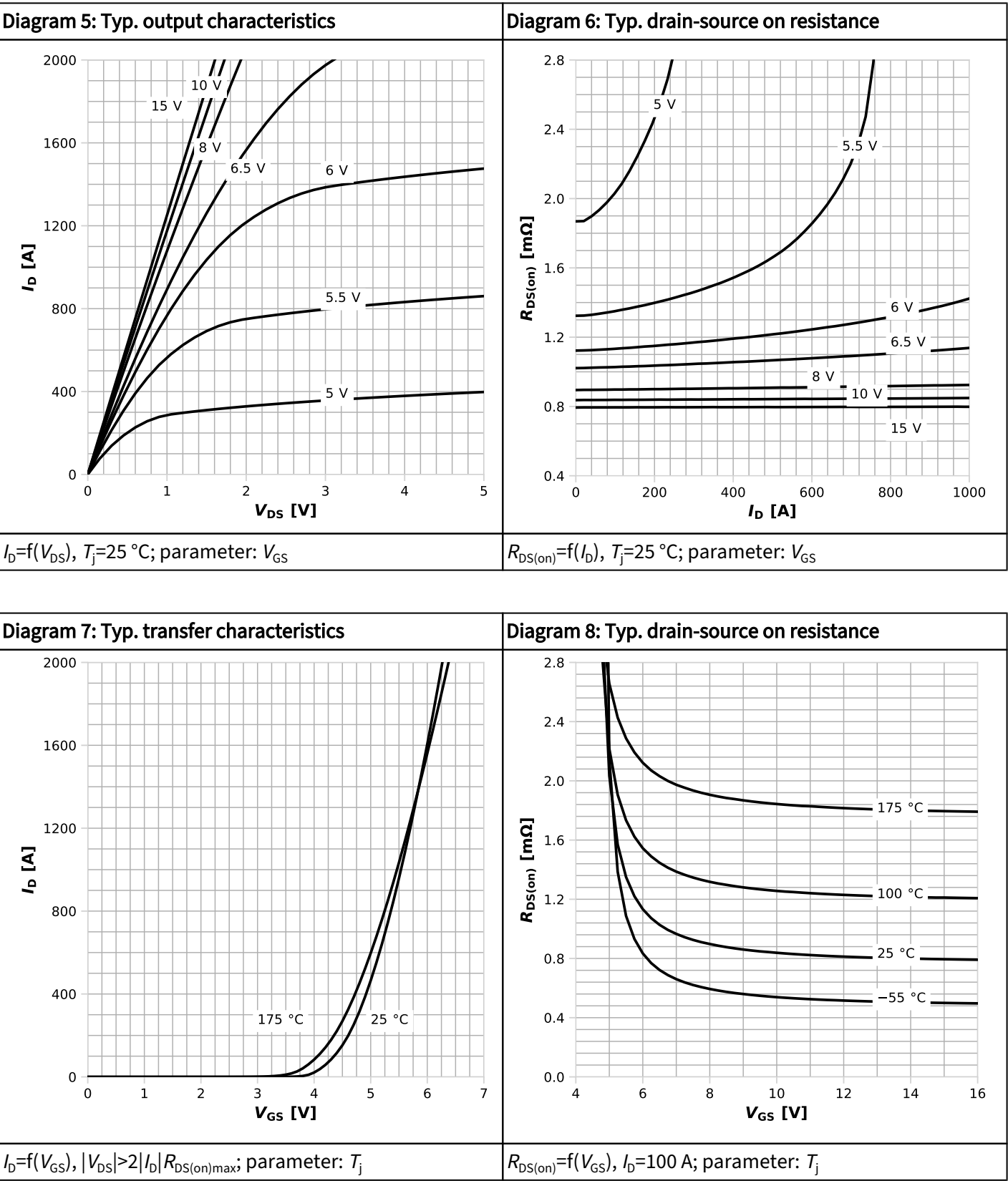
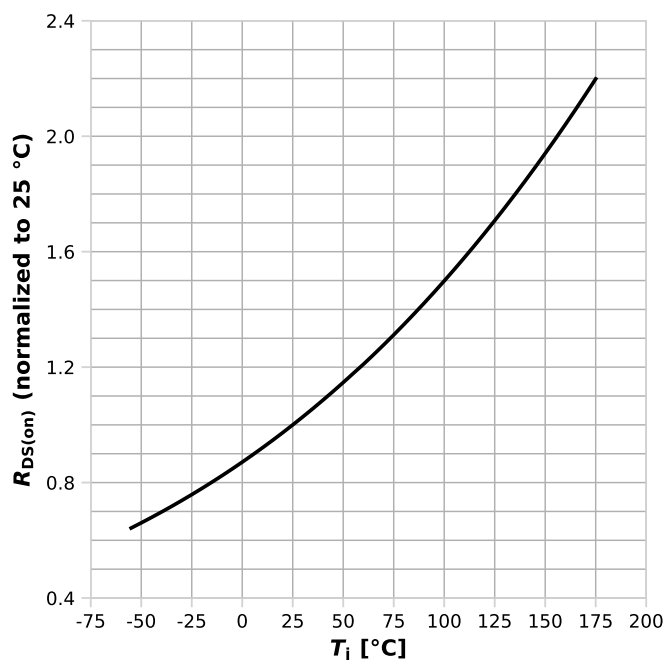
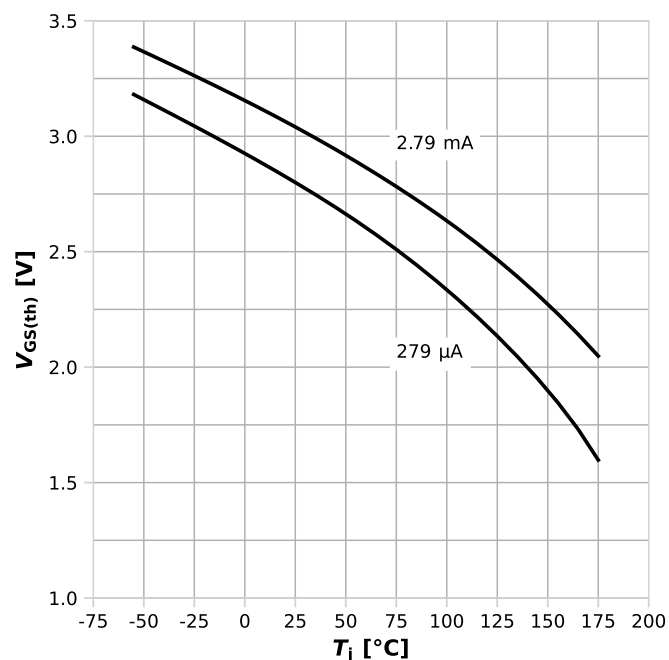


Diagram 9: Normalized drain-source on resistance



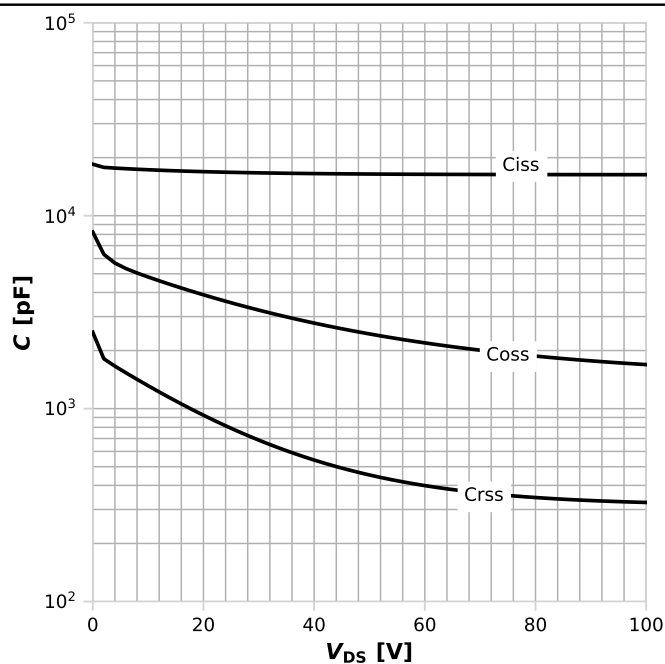
$$R_{DS(on)} = f(T_j), I_D = 100 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



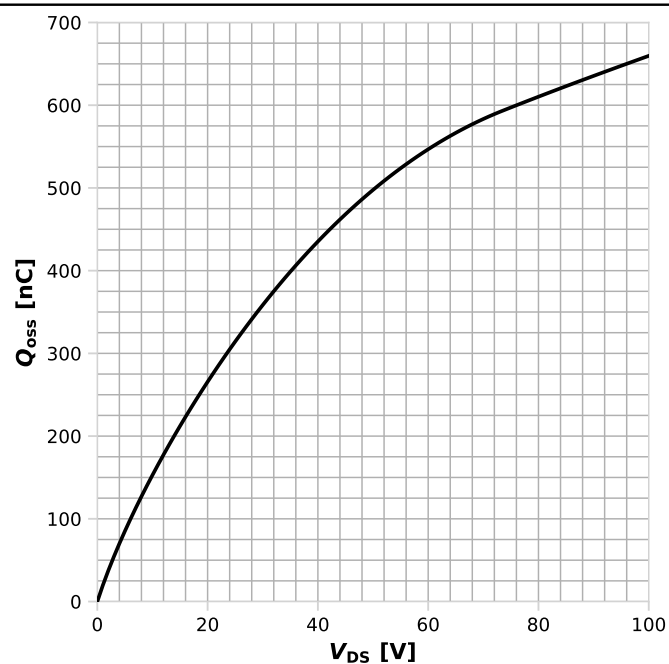
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



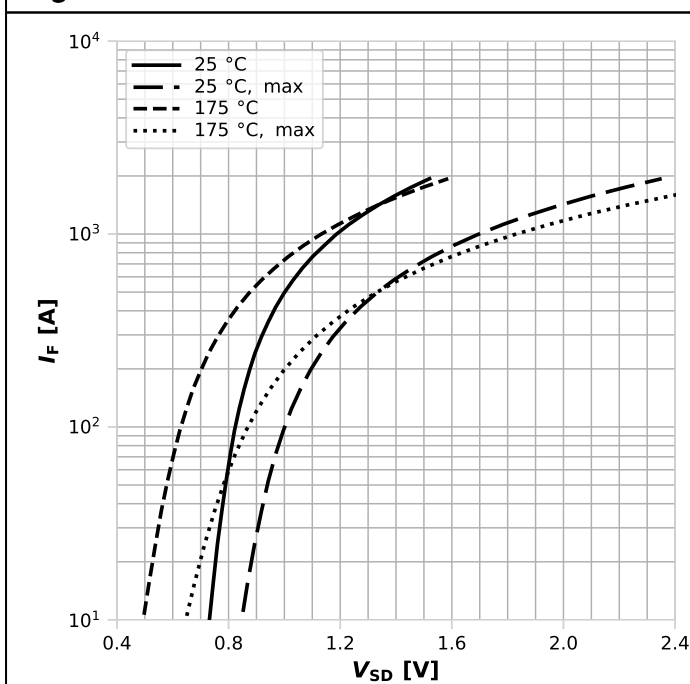
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Typ. output charge



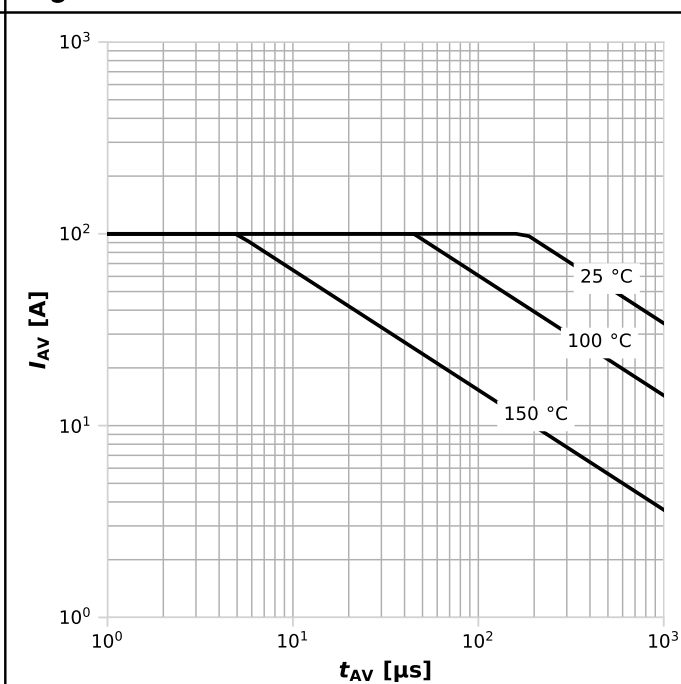
$$Q_{oss} = f(V_{DS}), V_{GS} = 0 \text{ V}$$

Diagram 13: Forward characteristics of reverse diode



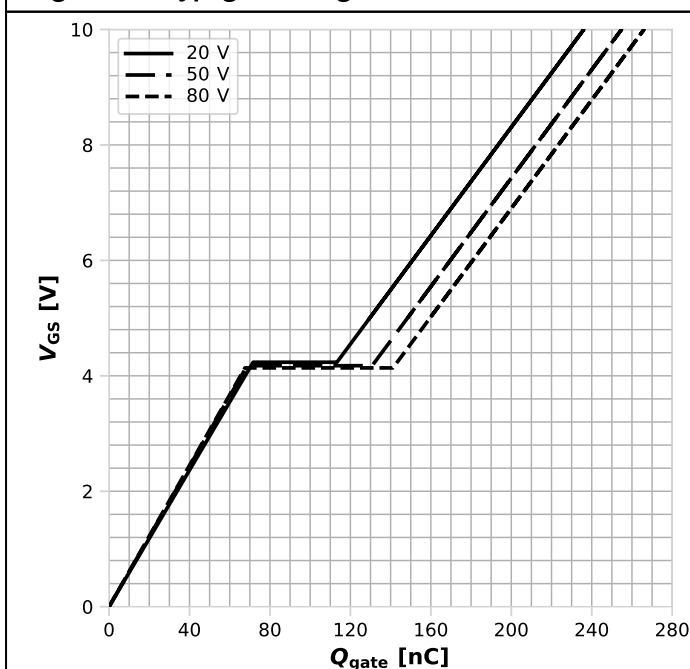
$I_F = f(V_{SD})$; parameter: T_j

Diagram 14: Avalanche characteristics



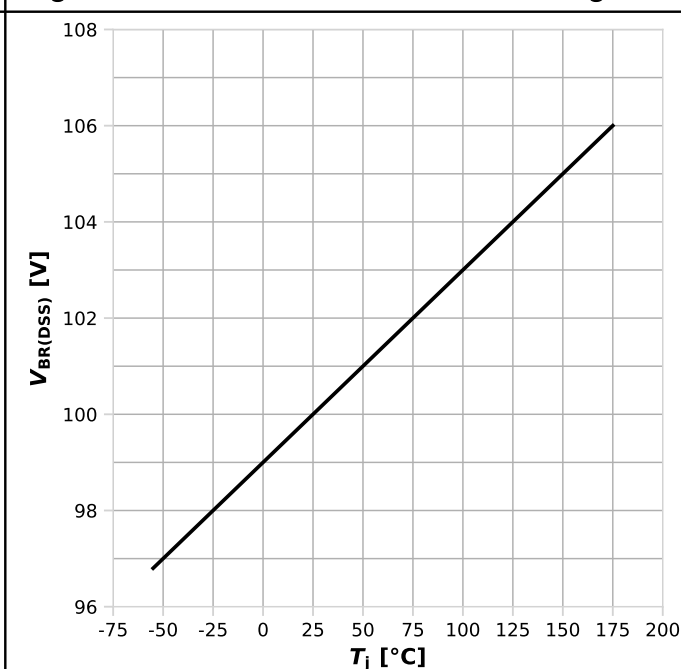
$I_{AS} = f(t_{AV})$; $R_{GS} = 25 \Omega$; parameter: $T_{j,start}$

Diagram 15: Typ. gate charge



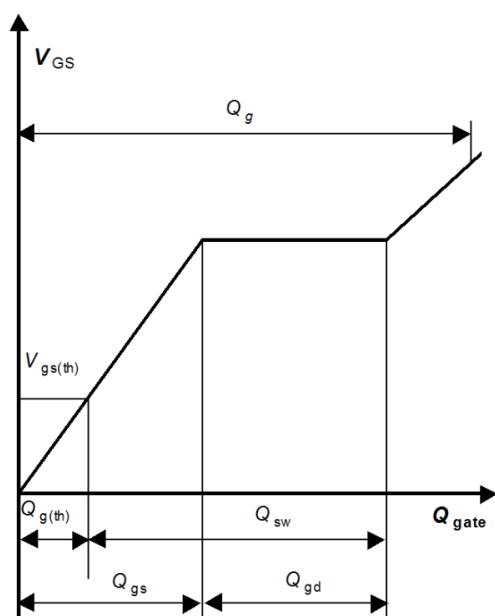
$V_{GS} = f(Q_{gate})$, $I_D = 50 \text{ A}$ pulsed, $T_j = 25 \text{ °C}$; parameter: V_{DD}

Diagram 16: Min. drain-source breakdown voltage

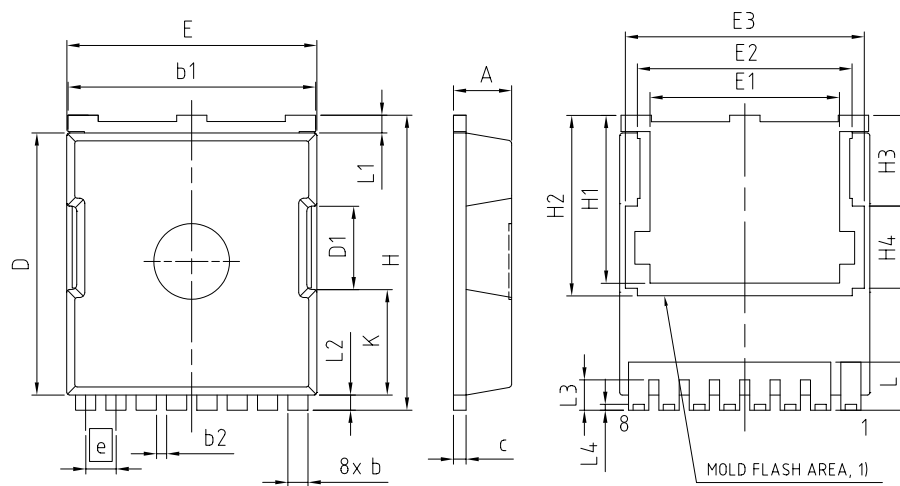


$V_{BR(DSS)} = f(T_j)$; $I_D = 1 \text{ mA}$

Gate charge waveforms

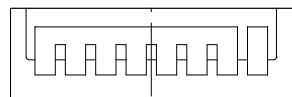


5 Package outlines



PACKAGE - GROUP NUMBER: PG-HSOF-8-U01		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.30	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	7.50
H3	3.59	
H4	3.26	
N	8	
K	4.03	4.33
L	1.60	2.10
L1	0.50	0.90
L2	0.45	0.75
L3	1.00	1.30
L4	0.13	0.33

5:1



OPTIONAL LEAD FORM:
WITHOUT LTI OPTION

1) PATIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

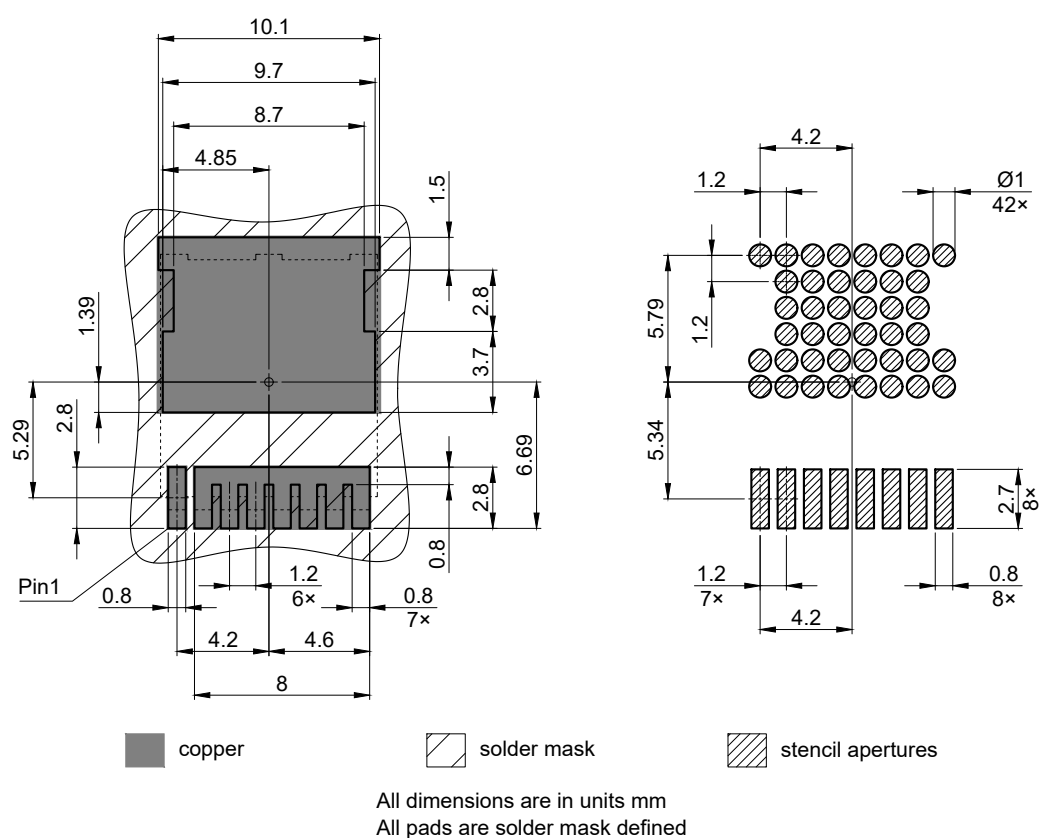
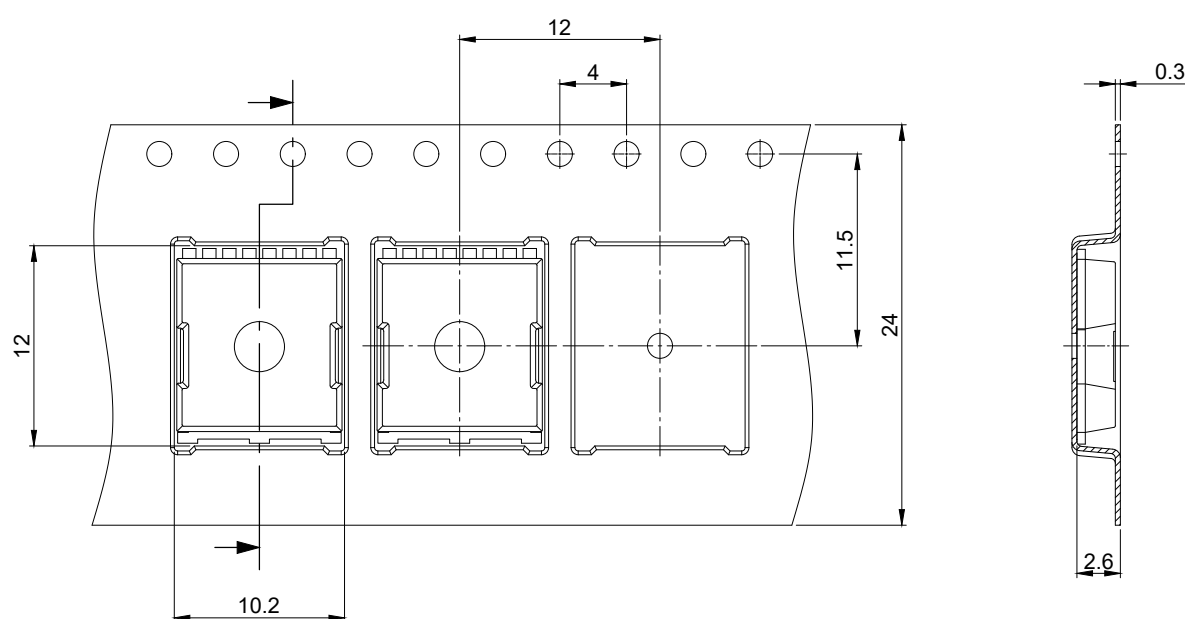


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm



Revision history

IPT009N10NM8

Revision 2025-12-10, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-12-10	Release of final version

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