To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC4570GR-9LG

ULTRA LOW-NOISE, WIDEBAND, DUAL OPERATIONAL AMPLIFIER

DESCRIPTION

The μPC4570GR-9LG is an ultra low-noise, wideband high slew-rate, dual operational amplifier. Input equivalent noise is three times better than the conventional 4558 type op-amps. The gain bandwidth products and the slew-rate are seven times better than 4558. In spite of fast AC performance, the μPC4570GR-9LG is extremely stable under voltage-follower circuit conditions. Supply current is also improved compared with conventional wideband op-amps. The μPC4570GR-9LG is an excellent choice for pre-amplifiers and active filters in audio, instrumentation, and communication circuits.

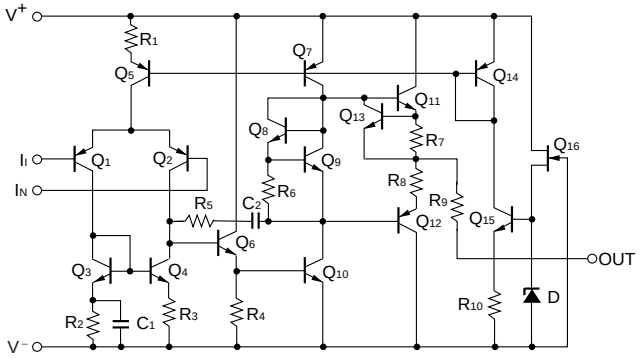
FEATURES

- Ultra low noise : e_n = 4.5 nV/$\sqrt{Hz}$
- High slew rate : 7 V/μs
- High gain bandwidth product : GBW = 15 MHz at 100 kHz
- Internal frequency compensation

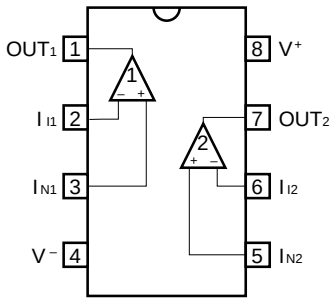
ORDERING INFORMATION

Part Number	Package
μPC4570GR-9LG-A	8-pin plastic TSSOP (5.72 mm (225))
μPC4570GR(5)-9LG-A	8-pin plastic TSSOP (5.72 mm (225))

EQUIVALENT CIRCUIT (1/2 Circuit)



PIN CONFIGURATION (Top View)



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Date Published November 2006 NS CP(N)
Printed in Japan

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Ratings	Unit
Voltage between V^+ and V^- Note1	$V^+ - V^-$	–0.3 to +36	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Note2	V_I	V^-–0.3 to V^+ +0.3	V
Output Voltage Note3	V_O	V^-–0.3 to V^+ +0.3	V
Power Dissipation Note4	P_T	440	mW
Output Short Circuit Duration Note5		10	sec
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Notes 1. Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

4. Power dissipation is specified with mounting on the glass epoxy printed wiring board as follows, and ambient temperature condition is 44°C or less.
Board size : 100 mm square Thickness : 1.6 mm Cupper area : 15% of mounting area (single side)
Thermal deleting factor is –5.5 mV/°C when operating ambient temperature is higher than 44°C.

5. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	$V^{\pm}$	±4		±16	V
Output Current	I_O			±10	mA
Source Resistance	R_S			50	kΩ
Capacitive Load (A_V = +1)	C_L			100	pF

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μPC4570GR-9LG

ELECTRICAL CHARACTERISTICS (T_A = 25°C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$		±0.3	±5	mV
Input Offset Current Note6	I_{IO}			±10	±100	nA
Input Bias Current Note6	I_B			100	400	nA
Large Signal Voltage Gain	A_V	$R_L \geq 2\ k\Omega$, V_O = ±10 V	30,000	300,000		
Supply Current Note7	I_{CC}	I_O = 0 A		5	8	mA
Common Mode Rejection Ratio	CMR		80	100		dB
Supply Voltage Rejection Ratio	SVR		80	100		dB
Output Voltage Swing	V_{om}	$R_L \geq 10\ k\Omega$	±12	±13.4		V
		$R_L \geq 2\ k\Omega$	±10	±12.8		V
Common Mode Input Voltage Range	V_{ICM}		±12	±14		V
Slew Rate	SR	$R_L \geq 2\ k\Omega$	5	7		V/μs
Gain Bandwidth Product	GBW	f_O = 100 kHz	10	15		MHz
Unity Gain Frequency	f_{unity}	open loop		7		MHz
Phase Margin	ϕ_{unity}	open loop		50		degree
Total Harmonic Distortion	THD	V_O = 3 $V_{r.m.s.}$, f = 20 Hz to 20 kHz (Figure1)		0.002		%
Input Equivalent Noise Voltage	V_n	RIAA (Figure2)		0.9		$\mu V_{r.m.s.}$
		FLAT+JIS A, R_S = 100 Ω (Figure3)		0.53	0.65	$\mu V_{r.m.s.}$
Input Equivalent Noise Voltage Density	e_n	f_O = 10 Hz, R_S = 100 Ω		5.5		$nV/\sqrt{Hz}$
		f_O = 1 kHz, R_S = 100 Ω		4.5		$nV/\sqrt{Hz}$
Input Equivalent Noise Current Density	i_n	f_O = 1 kHz		0.7		$pA/\sqrt{Hz}$
Channel Separation		f = 20 Hz to 20 kHz		120		dB

Notes 6. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

7. This current flows irrespective of the existence of use.

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μPC4570GR(5)-9LG

ELECTRICAL CHARACTERISTICS (T_A = 25°C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$		±0.3	±1	mV
Input Offset Current Note6	I_{IO}			±10	±50	nA
Input Bias Current Note6	I_B			100	200	nA
Large Signal Voltage Gain	A_V	$R_L \geq 2\ k\Omega$, V_O = ±10 V	50,000	300,000		
Supply Current Note7	I_{CC}	I_O = 0 A		5	7	mA
Common Mode Rejection Ratio	CMR		85	100		dB
Supply Voltage Rejection Ratio	SVR		85	100		dB
Output Voltage Swing	V_{om}	$R_L \geq 10\ k\Omega$	±13	±13.4		V
		$R_L \geq 2\ k\Omega$	±12	±12.8		V
Common Mode Input Voltage Range	V_{ICM}		±13.5	±14		V
Slew Rate	SR	$R_L \geq 2\ k\Omega$	5	7		V/μs
Gain Bandwidth Product	GBW	f_O = 100 kHz	10	15		MHz
Unity Gain Frequency	f_{unity}	open loop		7		MHz
Phase Margin	ϕ_{unity}	open loop		50		degree
Total Harmonic Distortion	THD	V_O = 3 $V_{r.m.s.}$, f = 20 Hz to 20 kHz (Figure1)		0.002		%
Input Equivalent Noise Voltage	V_n	RIAA (Figure2)		0.9		$\mu V_{r.m.s.}$
		FLAT+JIS A, R_S = 100 Ω (Figure3)		0.53	0.65	$\mu V_{r.m.s.}$
Input Equivalent Noise Voltage Density	e_n	f_O = 10 Hz, R_S = 100 Ω		5.5		$nV/\sqrt{Hz}$
		f_O = 1 kHz, R_S = 100 Ω		4.5		$nV/\sqrt{Hz}$
Input Equivalent Noise Current Density	i_n	f_O = 1 kHz		0.7		$pA/\sqrt{Hz}$
Channel Separation		f = 20 Hz to 20 kHz		120		dB

Notes 6. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

7. This current flows irrespective of the existence of use.

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MEASUREMENT CIRCUIT

Figure1 Total Harmonic Distortion Measurement Circuit

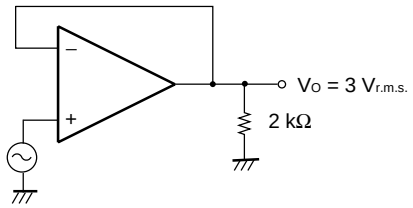


Figure2 Noise Measurement Circuit (RIAA)

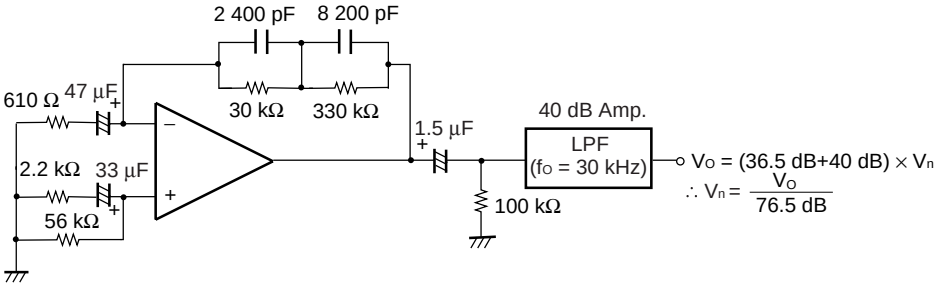
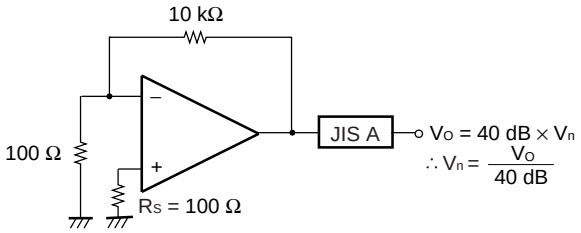


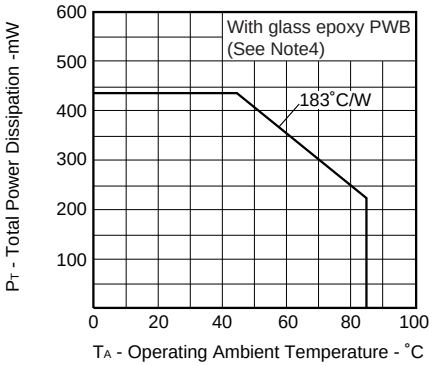
Figure3 Noise Measurement Circuit (FLAT+JIS A)



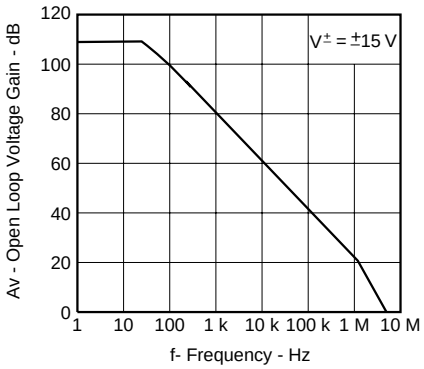
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TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, TYP.)

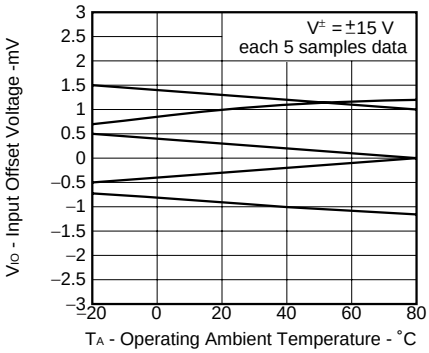
POWER DISSIPATION



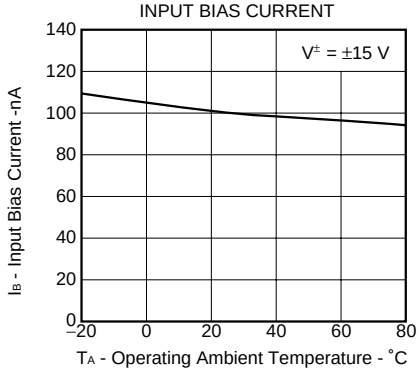
OPEN LOOP FREQUENCY RESPONSE



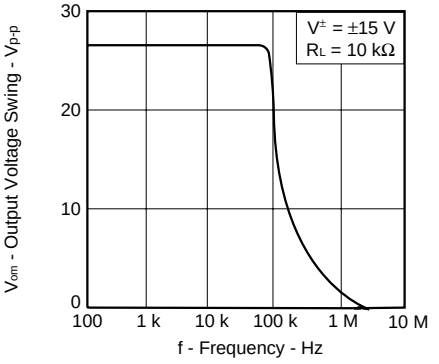
INPUT OFFSET VOLTAGE



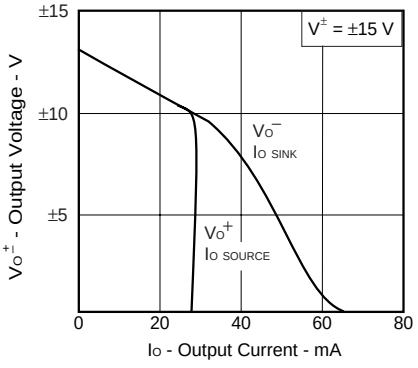
INPUT BIAS CURRENT



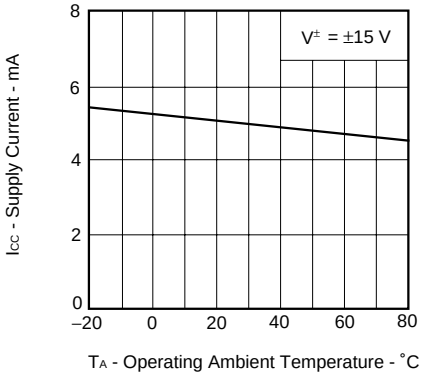
LARGE SIGNAL FREQUENCY RESPONSE



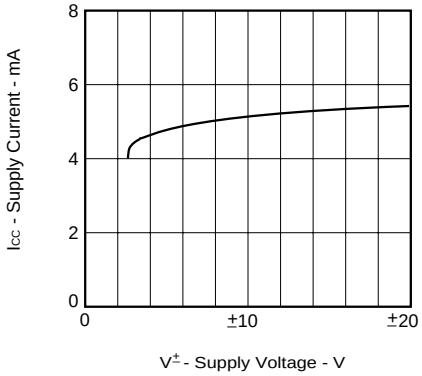
OUTPUT CURRENT LIMIT



SUPPLY CURRENT

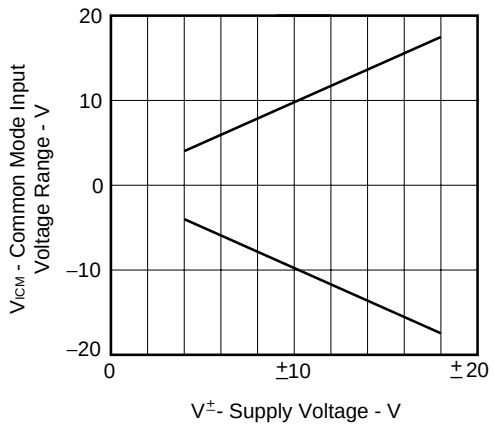


SUPPLY CURRENT

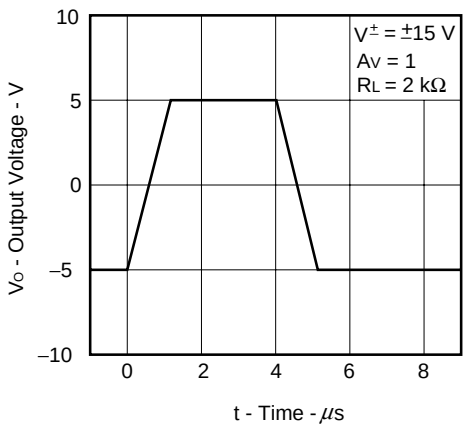


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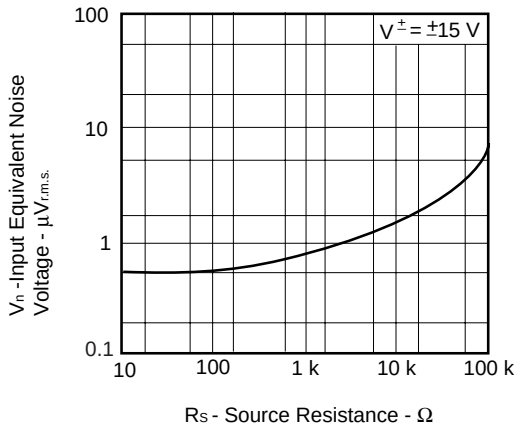
COMMON MODE INPUT VOLTAGE RANGE



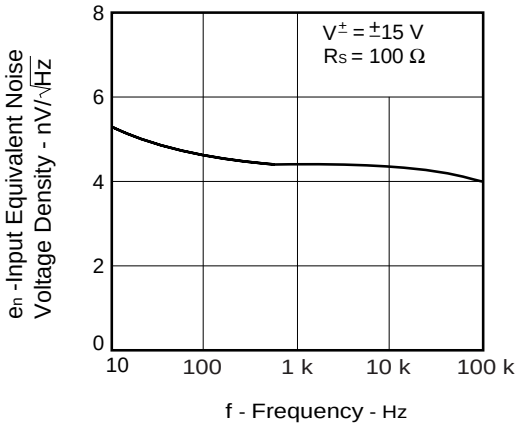
VOLTAGE FOLLOWER PULSE RESPONSE



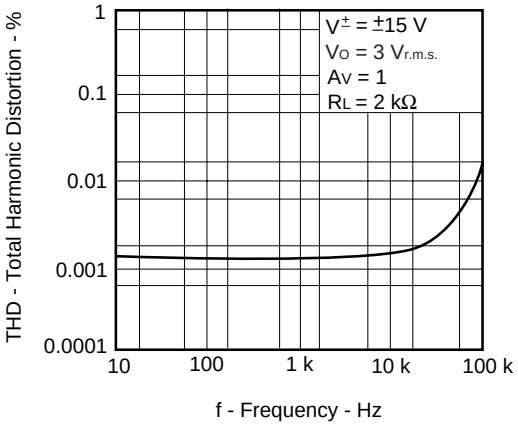
INPUT EQUIVALENT NOISE VOLTAGE (FLAT+JIS A)



INPUT EQUIVALENT NOISE VOLTAGE DENSITY



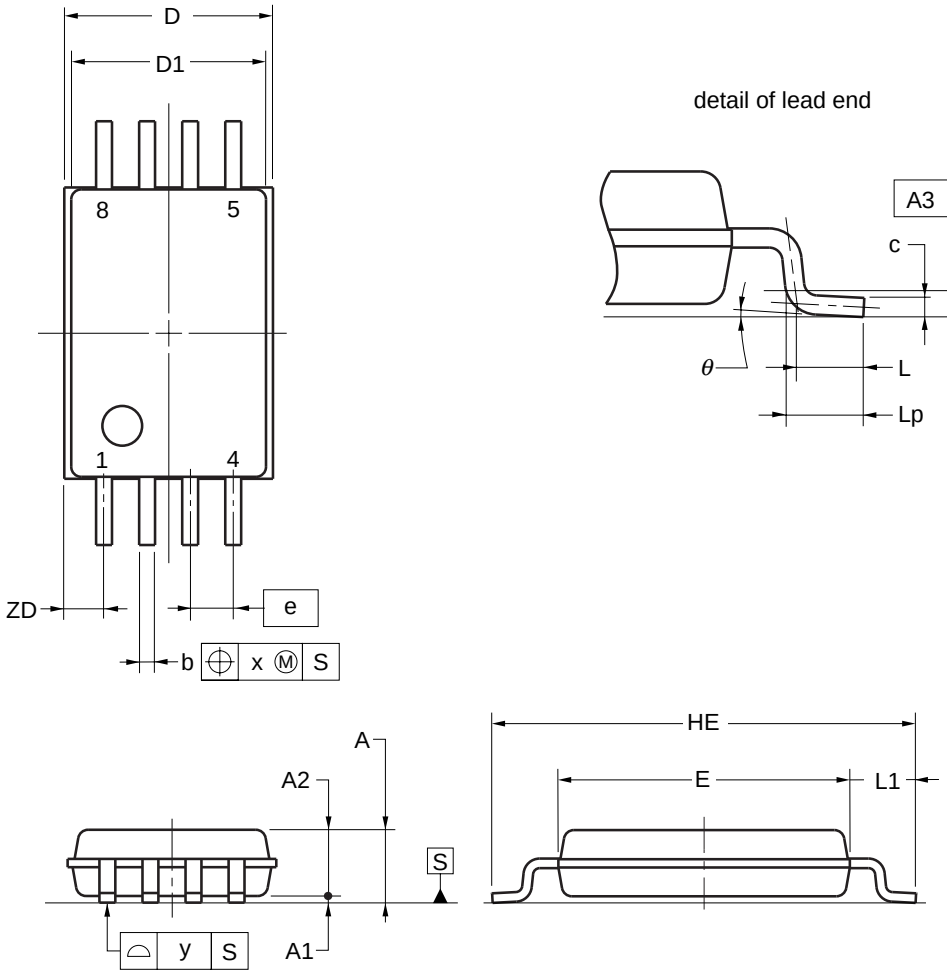
TOTAL HARMONIC DISTORTION



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PACKAGE DRAWING (Unit: mm)

8-PIN PLASTIC TSSOP (5.72mm (225))



(UNIT:mm)

ITEM	DIMENSIONS
D	3.15±0.15
D1	3.00±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	$0.24^{+0.06}_{-0.05}$
c	0.145±0.055
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.10
y	0.10
ZD	0.60

P8GR-65-9LG

NOTE
Each lead centerline is located within 0.10mm of its true position at maximum material condition.

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RECOMMENDED SOLDERING CONDITIONS

The μPC4570GR-9LG should be soldered and mounted under the following recommended conditions.

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For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 260°C or below (Package surface temperature), Reflow time: 60 seconds or less (at 220°C or higher), Maximum number of reflow processes: 3 time.	IR60-00-3
Wave Soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120°C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (Per each side of the device).	P350

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

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