

NCP458R, NCP459

4 A Single Load Switch for Low Voltage Rail

The NCP458R and NCP459 are power load switch with very low R_{on} NMOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, thanks to a best in class current consumption optimization with NMOS structure, leakage currents are drastically decreased. Offering optimized leakages isolation on the ICs connected on the battery.

Output discharge path is proposed, in the NCP459 version, to eliminate residual voltages on the external components connected on output pin.

Reverse voltage protection, from OUT to IN is offered in the NCP458R version.

Proposed in wide input voltage range from 0.75 V to 5.5 V, and a very small CSP8 $1 \times 2 \text{ mm}^2$.

Features

- 0.75 V – 5.5 V Operating Range
- 11 m Ω N-MOSFET
- Vbias Rail Input
- DC Current up to 4 A
- Output Auto-Discharge Option
- Reverse Blocking Option
- Active High EN Pin
- CSP8, $1 \times 2 \text{ mm}^2$, Pitch 0.5 mm

Typical Applications

- Notebooks
- Tablets
- Wireless
- Mobile Phones
- Digital Cameras



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MARKING DIAGRAM

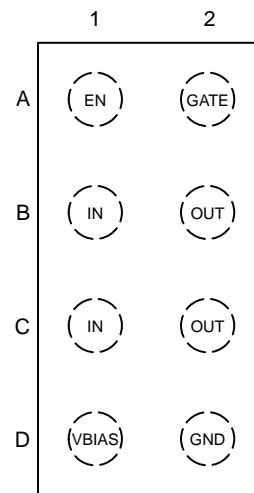


**WLCSP8
CASE 567HD**

XXXX
AYWW▪

A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

PINOUT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

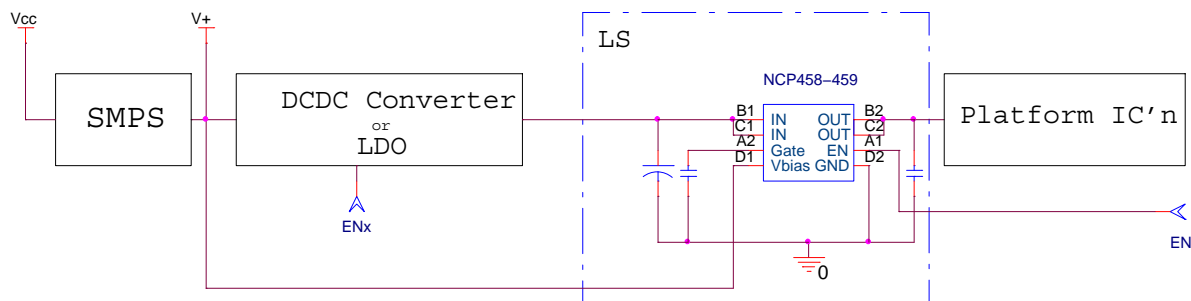


Figure 1. Typical Application Schematic

NCP458R, NCP459

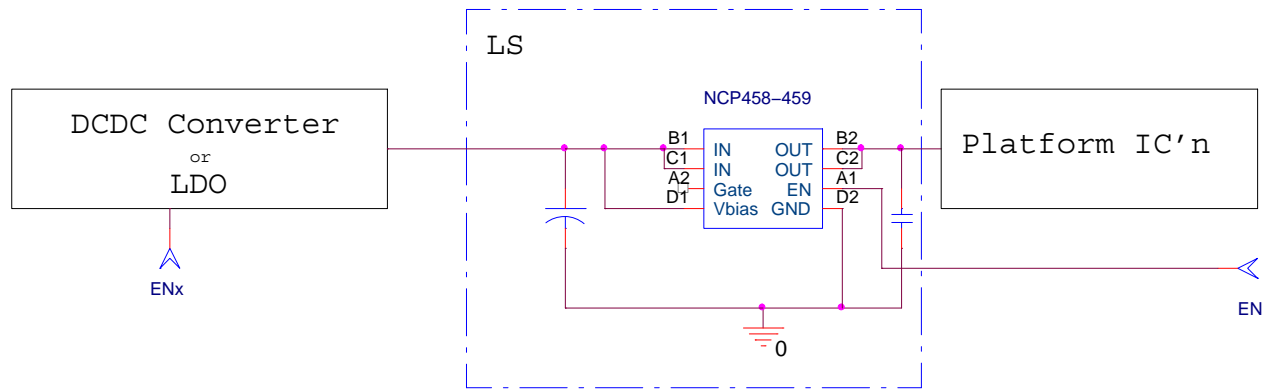


Figure 2. Application Schematic with Vbias Connected to IN and No Gate Delay

PIN FUNCTION DESCRIPTION

| Pin Name | Pin Number | Type | Description |
|----------|------------|-------|--|
| EN | A1 | INPUT | Enable input, logic high turns on power switch . |
| IN | B1, C1 | POWER | Load-switch input pin. |
| VBIAS | D1 | POWER | External supply voltage input. |
| GATE | A2 | INPUT | OUT pin slew rate control (t_{rise}). |
| OUT | B2, C2 | POWER | Load-switch output pin. |
| GND | D2 | POWER | Ground connection. |

NCP458R, NCP459

BLOCK DIAGRAMS

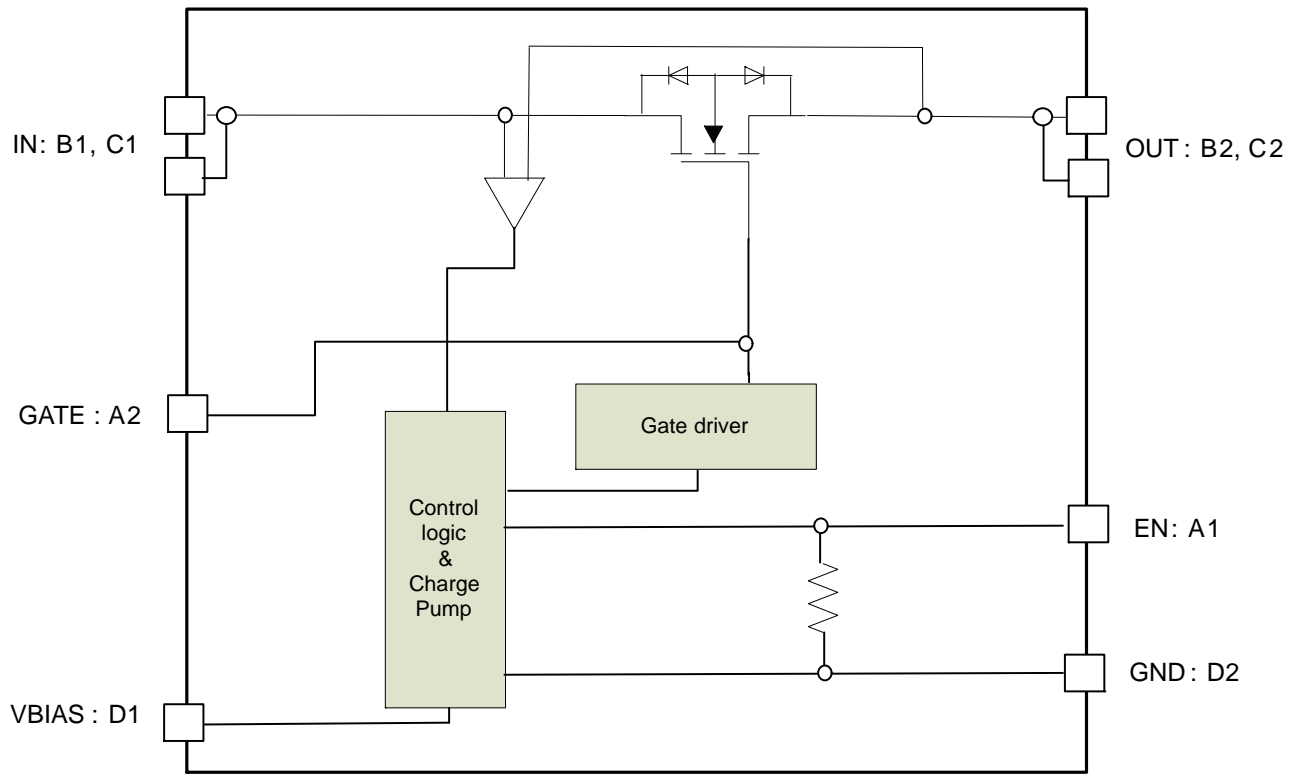


Figure 3. NCP458R Block Diagram

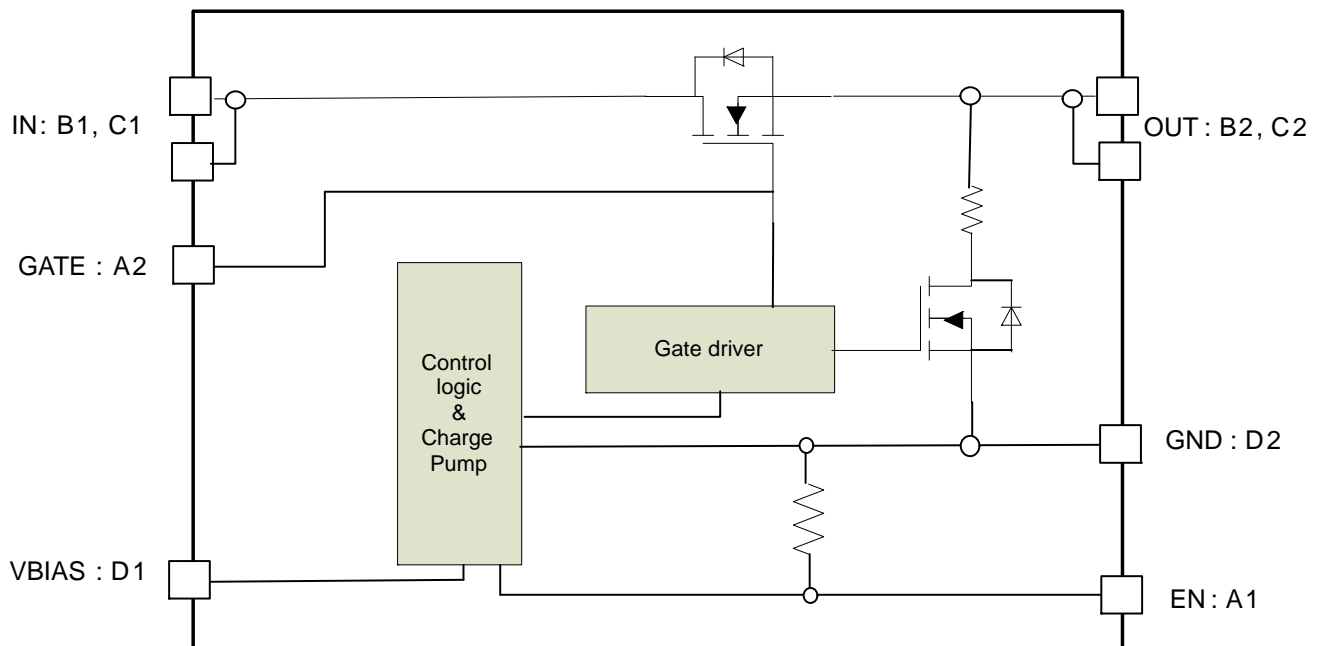


Figure 4. NCP459 Block Diagram

NCP458R, NCP459

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|---|--------------|------|
| IN, OUT, EN, VBIAS, GATE Pins: (Note 1) | $V_{EN}, V_{IN}, V_{OUT}, V_{BIAS}, V_{GATE}$ | -0.3 to +6.5 | V |
| From IN to OUT Pins: Input/Output (Note 1) NCP459 | V_{IN}, V_{OUT} | 0 to + 6.5 | V |
| From IN to OUT Pins: Input/Output (Note 1) NCP458R | V_{IN}, V_{OUT} | ±6.5 | V |
| Human Body Model (HBM) ESD Rating are (Note 2) | ESD HBM | 2000 | V |
| Machine Model (MM) ESD Rating are (Note 2) | ESD MM | 200 | V |
| Latch-up protection (Note 3) – Pins IN, OUT, EN, VBIAS and GATE | LU | 100 | mA |
| Maximum Junction Temperature | T_J | -40 to + 125 | °C |
| Storage Temperature Range | T_{STG} | -40 to + 150 | °C |
| Moisture Sensitivity (Note 4) | MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- According to JEDEC standard JESD22-A108.
- This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114 for all pins.
Machine Model (MM) ±250 V per JEDEC standard: JESD22-A115 for all pins.
- Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.

OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--|---------------|------|-------|------|------|
| V_{IN} | Operational Power Supply | | 0.75 | | 5.5 | V |
| V_{EN} | Enable Voltage | | 0 | | 5.5 | V |
| V_{BIAS} | Bias voltage ($V_{BIAS} \geq$ best of V_{IN}, V_{OUT}) | | 1.2 | | 5.5 | V |
| T_A | Ambient Temperature Range | | - 40 | 25 | + 85 | °C |
| C_{IN} | Decoupling input capacitor | | 100 | | | nF |
| C_{OUT} | Decoupling output capacitor | | 100 | | | nF |
| $R_{\theta JA}$ | Thermal Resistance Junction to Air | CSP8 (Note 5) | | 90 | | °C/W |
| I_{OUT} | DC current | | | 4 | 4.5 | A |
| | AC current 1 ms @ 217 Hz | | | | 5 | A |
| | AC current 100 μ s spike | | | | 15 | A |
| P_D | Power Dissipation Rating (Note 6) | | | 0.315 | | W |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
- The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

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ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} between 0.75 V and 5.5 V, and V_{BIAS} between 1.2 V and 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.3\text{ V}$ and $V_{BIAS} = 5\text{ V}$ (Unless otherwise noted).

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---------------------|---|--|------------------------|-----|-----|-----|------|
| POWER SWITCH | | | | | | | |
| R _{DS(on)} | Static drain–source on–state resistance for each rail | V _{IN} = V _{BIAS} = 5.5 V | T _A = 25°C | | 11 | 20 | mΩ |
| | | | T _J = 125°C | | | 24 | |
| | | V _{IN} = V _{BIAS} = 3.3 V | T _A = 25°C | | 11 | 20 | |
| | | | T _J = 125°C | | | 24 | |
| | | V _{IN} = V _{BIAS} = 1.8 V | T _A = 25°C | | 12 | 20 | |
| | | | T _J = 125°C | | | 24 | |
| | | V _{IN} = V _{BIAS} = 1.5 V | T _A = 25°C | | 13 | 20 | |
| | | | T _J = 125°C | | | 24 | |
| | | V _{IN} = V _{BIAS} = 1.2 V | T _A = 25°C | | 13 | 20 | |
| | | | T _J = 125°C | | | 24 | |
| | | V _{IN} = 1.0 V V _{BIAS} = 1.2 V | T _A = 25°C | | 14 | 24 | |
| | | | T _J = 125°C | | | 30 | |
| | | V _{IN} = 0.8 V V _{BIAS} = 1.2 V | T _A = 25°C | | 17 | 30 | |
| | | | T _J = 125°C | | | 35 | |
| R _{DIS} | Output discharge path | | EN = low, NCP459 | | 230 | 300 | Ω |

TIMINGS

| | | | | | | | |
|------------------|--|--|------------------------|---------------------|------|-----|----|
| T _R | Output rise time From 10% to 90% of V _{OUT} | V _{IN} = 5 V C _{LOAD} = 1 μF, R _{LOAD} = 25 Ω | No cap on GATE pin | | 0.26 | | ms |
| | | | Gate capacitor = 1 nF | | 1.5 | | |
| | | | Gate capacitor = 10 nF | | 15 | | |
| T _{en} | Enable time From En V _{ih} to 10% of V _{OUT} | | Without Cgate | | 10 | | μs |
| | | | With 1 nF on Gate | | 60 | | μs |
| T _F | Fall Time. From 90% to 10% of V _{OUT} | | | | 50 | | μs |
| T _{dis} | Disable time | | | From EN to 90% Vout | | 75 | |
| T _R | Output rise time From 10% to 90% of V _{OUT} | V _{IN} = 3.3 V C _{LOAD} = 1 μF, R _{LOAD} = 25 Ω | No cap on GATE pin | | 0.25 | 0.5 | ms |
| | | | Gate capacitor = 1 nF | | 1 | | |
| | | | Gate capacitor = 10 nF | | 10 | | |
| T _{en} | Enable time From En V _{ih} to 10% of V _{OUT} | | Without Cgate, NCP459 | | 20 | 50 | μs |
| | | | Without Cgate, NCP458R | | 90 | 150 | μs |
| T _F | Output fall time From 90% to 10% of V _{OUT} | | With 1 nF on Gate | | 114 | | μs |
| | | | | | 60 | 120 | μs |
| T _R | Output rise time From 10% to 90% of V _{OUT} | V _{IN} = 1.8 V C _{LOAD} = 1 μF, R _{LOAD} = 25 Ω | No cap on GATE pin | | 0.12 | | ms |
| | | | Gate capacitor = 1 nF | | 0.6 | | |
| | | | Gate capacitor = 10 nF | | 5.5 | | |
| T _{en} | Enable time From En V _{ih} to 10% of V _{OUT} | | Without Cgate | | 15 | | μs |
| | | | With 1 nF on Gate | | 85 | | μs |
| T _F | Output fall time From 90% to 10% of V _{OUT} | | | | 35 | | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

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ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} between 0.75 V and 5.5 V, and V_{BIAS} between 1.2 V and 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.3\text{ V}$ and $V_{BIAS} = 5\text{ V}$ (Unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

TIMINGS

| | | | | | | |
|----------|---|---|------------------------|--|------|---------------|
| T_R | Output rise time From 10% to 90% of V_{OUT} | $V_{IN} = 1\text{ V}$ $C_{LOAD} = 1\text{ }\mu\text{F}$, $R_{LOAD} = 25\text{ }\Omega$ | No cap on GATE pin | | 0.01 | ms |
| | | | Gate capacitor = 1 nF | | 1 | |
| | | | Gate capacitor = 10 nF | | 13 | |
| T_{en} | Enable time From En V_{ih} to 10% of V_{OUT} | $V_{IN} = 1\text{ V}$ $C_{LOAD} = 1\text{ }\mu\text{F}$, $R_{LOAD} = 25\text{ }\Omega$ | Without C_{gate} | | 10 | μs |
| | | | With 1 nF on Gate | | 0.4 | ms |
| T_F | Output fall time | | | | 20 | μs |

Logic

| | | | | | | |
|----------|--------------------------|--|-----|--|-----|-----------|
| V_{IH} | High-level input voltage | | 0.9 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.4 | V |
| R_{EN} | Pull down resistor | | 3 | | 7 | $M\Omega$ |

REVERSE CURRENT BLOCKING

| | | | | | | |
|-----------------|----------------------------------|-----------------------------------|--|-----|--|---------------|
| V_{rev_thr} | Reverse threshold | $V_{OUT} - V_{IN}$ | | 45 | | mV |
| V_{rev_hyst} | Reverse threshold hysteresis | | | 60 | | mV |
| T_{rev} | Reverse comparator response time | $V_{OUT} - V_{in} > V_{rev_thr}$ | | 2.5 | | μs |

QUIESCENT CURRENT- NCP458R

| | | | | | | |
|-----------------|------------------------------|---|--|------|-----|---------------|
| I_{VBIAS} | V_{BIAS} Quiescent current | $V_{BIAS} = 3.3\text{ V}$, EN = high | | 1.5 | 6 | μA |
| I_{INQ} | IN Quiescent current | EN = high | | 0.01 | 0.3 | μA |
| I_{STBIN} | Standby current IN | EN = low, IN standby current, $V_{IN} = 3.3\text{ V}$, without discharge path. | | 0.01 | 0.3 | μA |
| $I_{STDVbias}$ | Standby current V_{BIAS} | $V_{BIAS} = 3.3\text{ V}$ EN = low | | 0.4 | 1.5 | μA |
| I_{out_leak} | Output leakage current | IN connected to GND, $V_{OUT} = 5\text{ V}$ | | 0.01 | 0.5 | μA |

QUIESCENT CURRENT - NCP459

| | | | | | | |
|----------------|------------------------------|--|--|------|-----|---------------|
| I_{VBIAS} | V_{BIAS} Quiescent current | $V_{BIAS} = 3.3\text{ V}$, EN = high | | 1.3 | 5 | μA |
| I_{INQ} | IN Quiescent current | EN = high | | 0.01 | 0.3 | μA |
| I_{STBIN} | Standby current IN | EN = low, IN standby current, $V_{IN} = 3.3\text{ V}$, with discharge path. NCP459. | | 0.01 | 0.3 | μA |
| $I_{STDVbias}$ | Standby current V_{BIAS} | $V_{BIAS} = 3.3\text{ V}$ EN = low | | 0.4 | 1.5 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

NCP458R, NCP459

TIMINGS

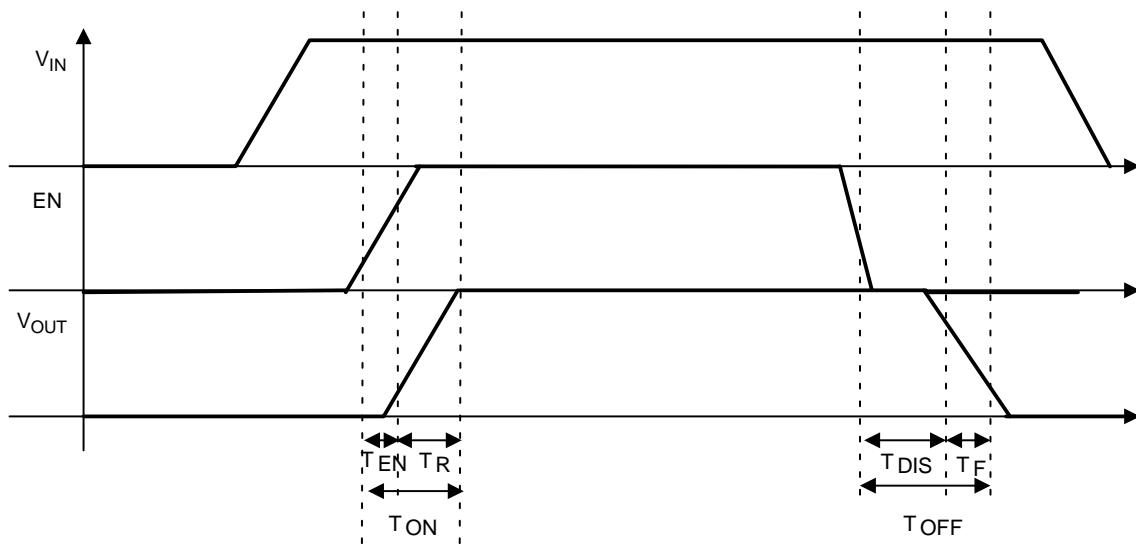


Figure 5. Enable, Rise and Fall Time

TYPICAL CHARACTERISTICS

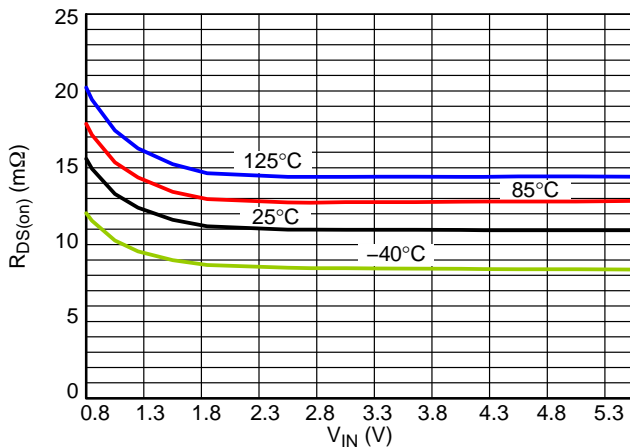


Figure 6. $R_{DS(on)}$ (m Ω) vs V_{IN} (V), Over Temperature Range

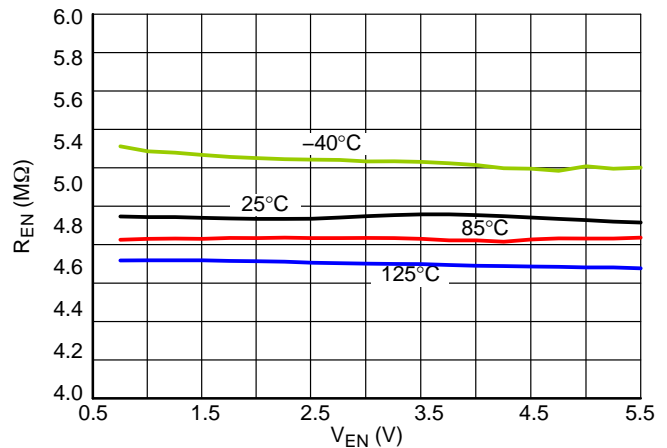


Figure 7. Pull Down Resistor (M Ω) vs V_{EN} (V), Over Temperature Range

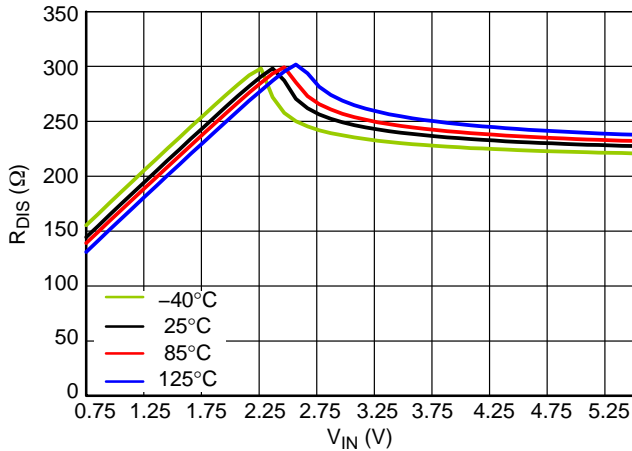


Figure 8. Discharge Resistor (Ω) vs V_{IN} (V), Over Temperature Range

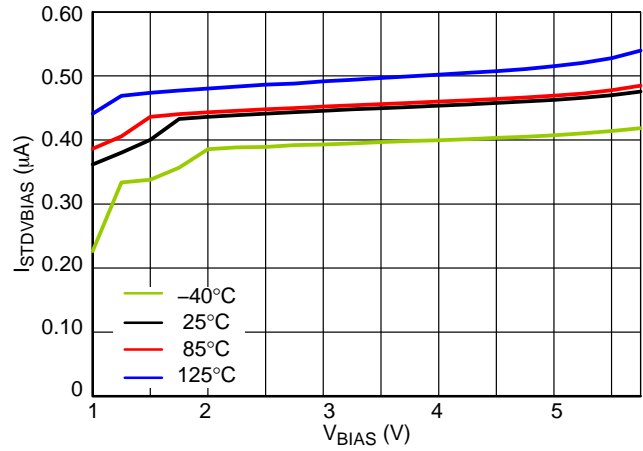


Figure 9. NCP458R Standby Current (μ A) vs V_{BIAS} (V), Over Temperature Range

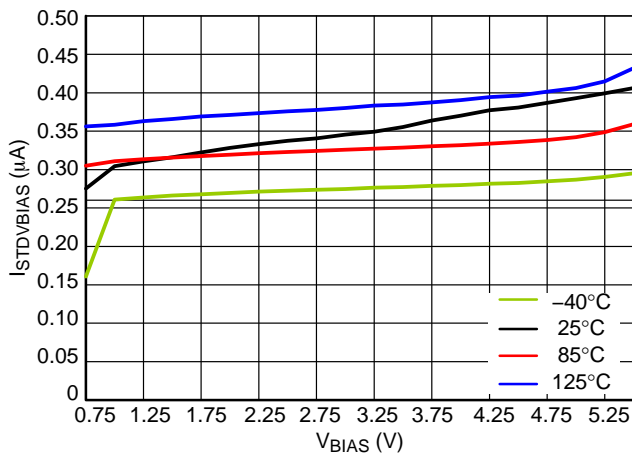


Figure 10. NCP459 Standby Current (μ A) vs V_{BIAS} (V), Over Temperature Range

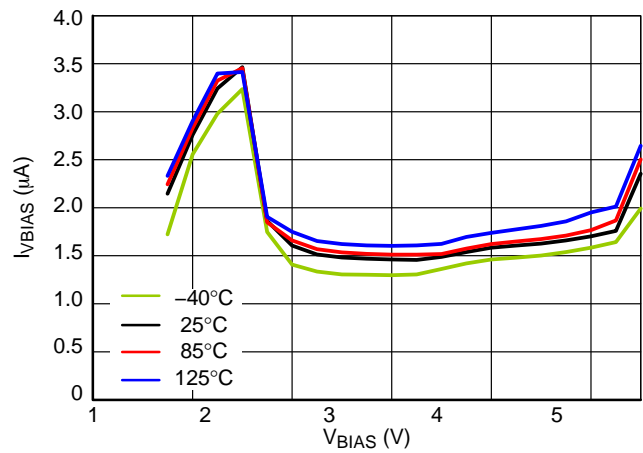


Figure 11. NCP458R Quiescent Current (μ A) vs V_{BIAS} (V), Over Temperature Range

NCP458R, NCP459

TYPICAL CHARACTERISTICS

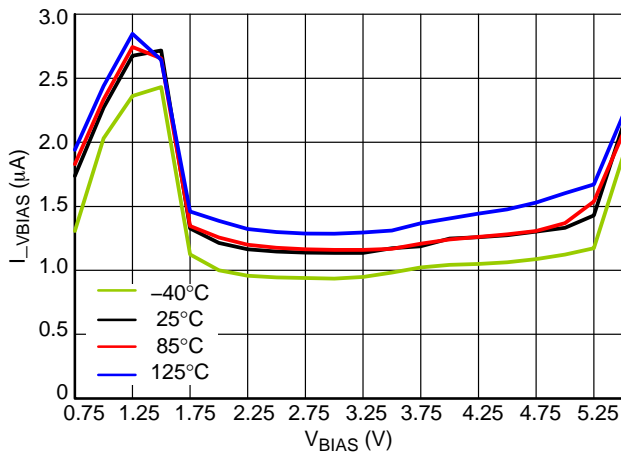


Figure 12. NCP459 Quiescent Current (μA) vs V_{BIAS} (V), Over Temperature Range

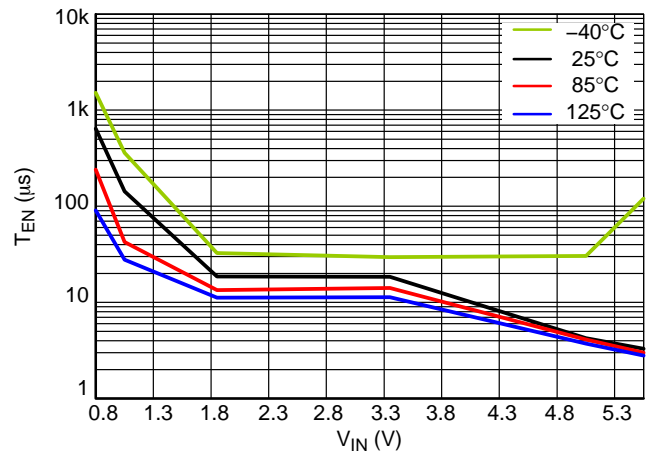


Figure 13. Enable Time (μs) vs V_{IN} (V), Over Temperature Range (without C_{gate})

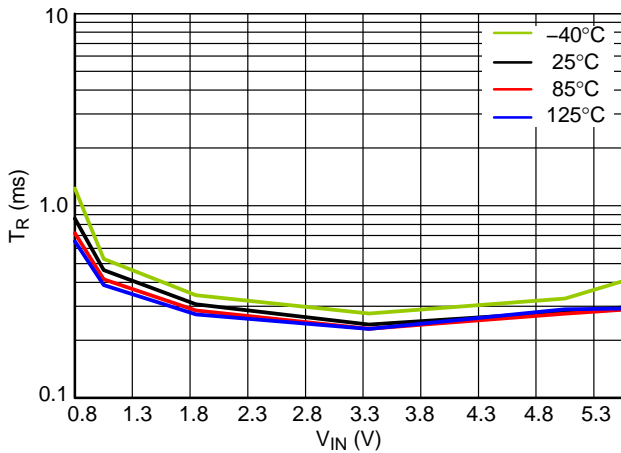


Figure 14. Rise Time (ms) vs V_{IN} (V), Over Temperature Range (without C_{gate})

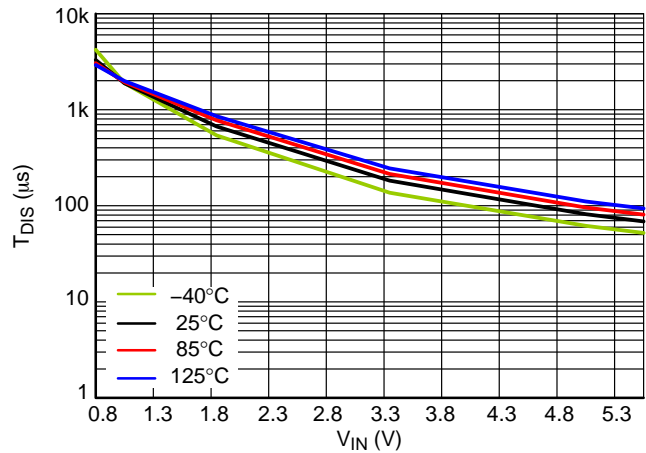


Figure 15. Disable Time (μs) vs V_{IN} (V), Over Temperature Range
 V_{BIAS} and V_{IN} Tied Together

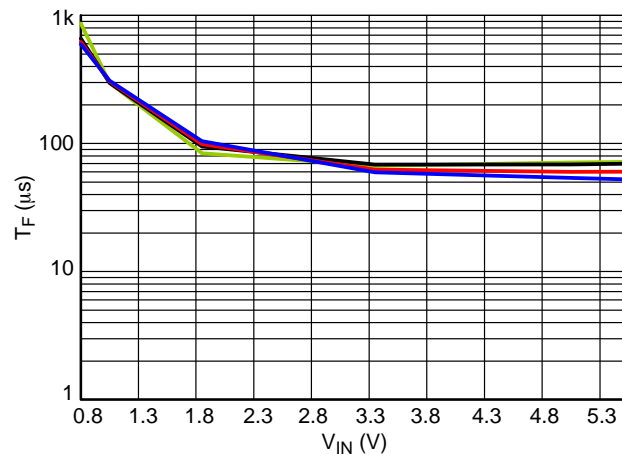


Figure 16. Fall Time (μs) vs V_{IN} (V), Over Temperature Range
 V_{BIAS} and V_{IN} Tied Together
 $R_{\text{load}} = 25 \Omega$

FUNCTIONAL DESCRIPTION

Overview

The NCP458R and NCP459 are high side N channel MOSFET power distribution switch designed to isolate ICs connected on the battery or DCDC supplies in order to save energy. The part can be used with a wide range of supply from 0.75 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing NMOS switch off.

The IN/OUT path is activated with a minimum of $V_{BIAS\ min}$, $V_{in\ min}$ and EN forced to high level.

Auto Discharge (Optional – NCP459)

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level.

In order to limit the current across the internal discharge Nmosfet, the typical value is set at R_{DIS} value.

Vbias Rail

The core of the IC is supplied thanks to Vbias supply rail (common +5 V, 3.3 V, 1.8 V, 1.2 V). Indeed, no current consumption is used on IN pin, allowing to improve power saving of the rail that must be isolated by the power switch.

If Vbias rail is not available or used, Vbias pin and Vin pin can be connected together as close as possible the DUT. A minimum of 1.2 V is necessary to control the IC.

Output rise time – Gate control

The NMOS is control with internal charge pump and driver. A minimum gate slew rate is internally set to avoid huge inrush current when EN is set from low to high. The default gate slew rate depends on Vin level. The higher Vin level, the longer rise time.

In addition, an external capacitor can be connected between Gate pin and GND in order to slow down the gate rising. See electrical table for more details.

Cin and Cout Capacitors

100 nF external capacitors must be connected as close as possible the DUT for noise immunity and better stability. In case of input hot plug (input voltage connected with fast slew rate – few μs – it's strongly recommended to avoid big capacitor connected on the input. That allows to avoid input over voltage transients.

Reverse Blocking Control (Optional NCP458R)

A reverse blocking control circuitry is embedded to eliminate leakages from OUT to IN in case of $V_{out} > V_{in}$.

A comparator measures the dropout voltage on the switch between OUT and IN and turn off the NMOS if this voltage exceeds specified reverse voltage.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times (I_{OUT})^2 \quad (\text{eq. 1})$$

| | |
|--|--|
| P_D | = Power dissipation (W) |
| $R_{DS(on)}$ | = Power MOSFET on resistance (Ω) |
| I_{OUT} | = Output current (A) |
| $T_J = P_D \times R_{\theta JA} + T_A$ | (eq. 2) |
| T_J | = Junction temperature ($^{\circ}\text{C}$) |
| $R_{\theta JA}$ | = Package thermal resistance ($^{\circ}\text{C}/\text{W}$) |
| T_A | = Ambient temperature ($^{\circ}\text{C}$) |

Demoboard

The NCP458R and NCP459 integrate a 4 A rated NMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon.

The package is a CSP and due to the low thermal resistance of the silicon, all the balls can be used to improved power dissipation. Indeed, even if the power crosses the IN / OUT pins only, all the balls around this power area should be connected to the larger PCB area.

In the below PCB example (application demonstration board), all the PCB areas connected to 6 balls are enlarged. In addition vias are connected to bottom side with exactly same form factor of the other PCB side.

Additional improvements can be done also by using more copper thickness and the thinner epoxy as possible.

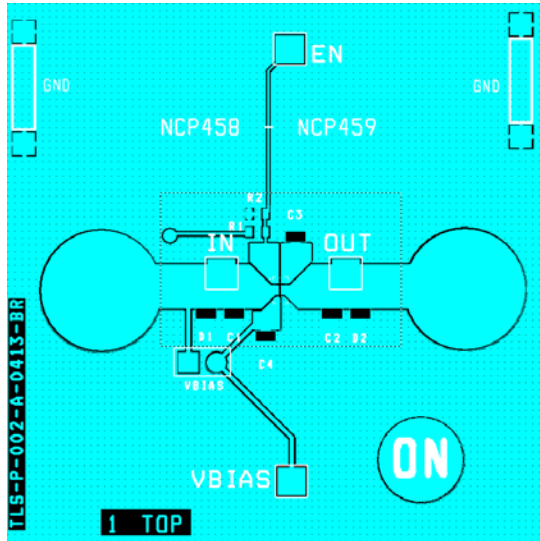


Figure 17. Demonstration Board (top view)

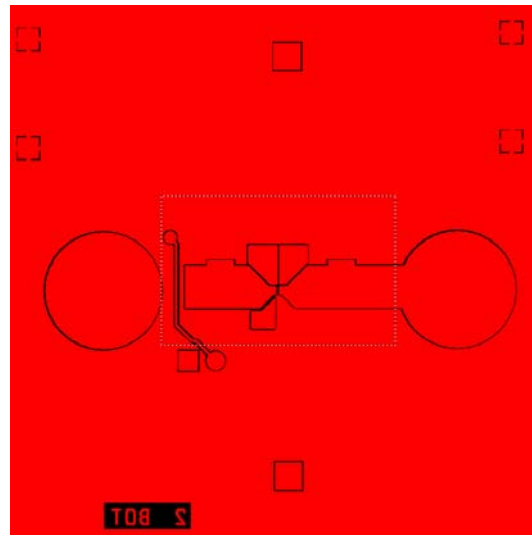


Figure 18. Demonstration Board (bottom view)

NCP458R, NCP459

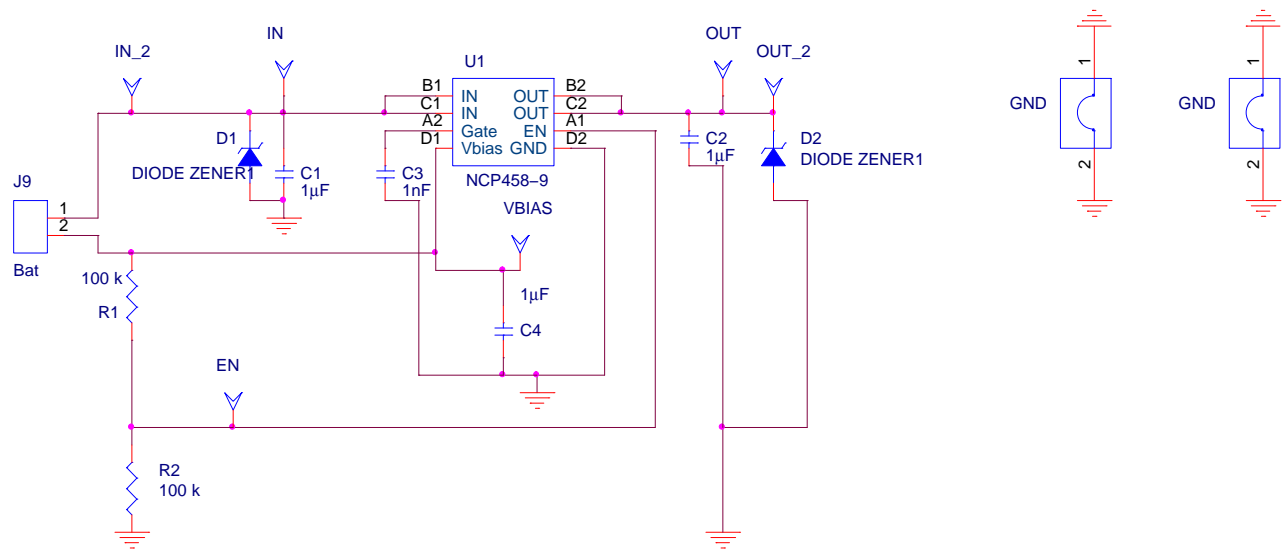


Figure 19. Demonstration Board Schematic

BILL OF MATERIAL TABLE

| Quantity | Reference schem | Part description | Part number | Manufacturer |
|----------|------------------------|-------------------------|-------------------------|------------------|
| 2 | IN, OUT | Socket, 4mm, metal, PK5 | B010 | HIRSCHMANN |
| 4 | IN_2, OUT_2, VBIAS, EN | HEADER200 | 2.54 mm, 77313-101-06LF | FC |
| 1 | J9 (Bat) | HEADER200-2 | 2.54 mm, 77313-101-06LF | FC |
| 3 | C1, C2, C4 | 1uF | GRM155R70J105KA12# | Murata |
| 1 | C3 | 1nF, Not mounted | GRM188R60J102ME47# | Murata |
| 1 | D1, D2 | TVS | ESD9x | ON Semiconductor |
| 2 | GND2,GND | GND JUMPER | D3082F05 | Harvin |
| 2 | R2, R3 | Resistor 100k 0603 | MC 0.063 0603 1% 100K | MULTICOMP |
| 1 | U1 | Load switch | NCP458 - 459 | ON Semiconductor |

ORDERING INFORMATION

| Device | Options | Marking | Package | Shipping† |
|---------------|---|-----------|--------------------------|------------------|
| NCP458RFCT2G | Reverse Voltage Protection | 458RdYWW | WLCSP 1 x 2 mm (Pb-Free) | 3000 Tape / Reel |
| NCP458RFCCT2G | Reverse Voltage Protection, Die Coating | 458RCdYWW | WLCSP 1 x 2 mm (Pb-Free) | 3000 Tape / Reel |
| NCP459FCT2G | Discharge Path | 459dYWW | WLCSP 1 x 2 mm (Pb-Free) | 3000 Tape / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

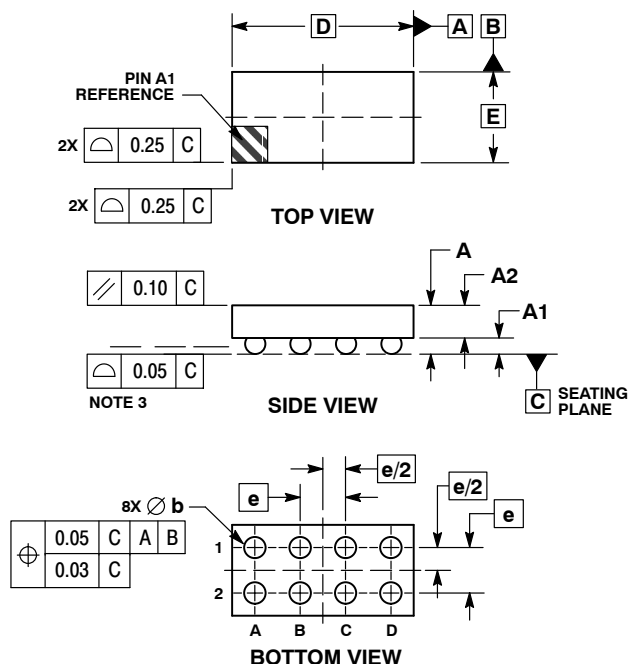
ON Semiconductor®



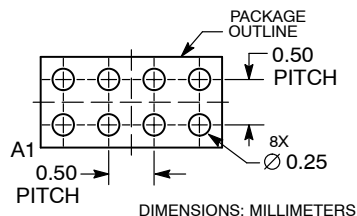
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WLCSP8, 2.0x1.0
CASE 567HD
ISSUE O

DATE 26 APR 2013



RECOMMENDED SOLDERING FOOTPRINT*



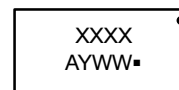
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | --- | 0.66 |
| A1 | 0.21 | 0.27 |
| A2 | 0.36 | REF |
| b | 0.29 | 0.34 |
| D | 2.00 | BSC |
| E | 1.00 | BSC |
| e | 0.50 | BSC |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|-----------------|--|
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