μPD720210

ASSP (Four-port USB3.0 Hub Controller)

R19DS0070EJ0600
Rev.6.00
Jul 11.25

Description

The μPD720210 is a USB 3.0 hub controller that complies with the Universal Serial Bus (USB) Specification Revision 3.0 and operates at up to 5 Gbps. The device incorporates Renesas' market proven design expertise in USB 3.0 interface technologies and market proven USB 3.0 hub core. The device is fully compatible with all prior versions of USB spec and 100% compatible with Renesas' industry standard USB 3.0 host controller.

The μPD720210 can be configured with 2, 3, or 4 downstream ports at all data rates. It supports for up to four downstream ports allows system designers to easily add up to four USB 3.0 ports to their systems.

The μPD720210 incorporates Renesas' low-power technologies and supports all mainstream battery charging specifications.

The μPD720210 integrates several commonly required external components and USB termination resistors, making it ideally suited for applications with limited PCB space. It is available in a small, low-pin count, 76-pin, 9mmx9mm QFN package with simple pin assignment for PCB layout. All USB signal traces can be routed directly to the connector pins using one layer of the PCB.

Features

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0
  - Supports Low-Speed (1.5 Mbps), Full-Speed (12 Mbps), Hi-Speed (480 Mbps), and Super-Speed (5 Gbps)
  - Transports all USB compliant data transfer types as follows; Control / Bulk / Interrupt / Isochronous transfer
  - Supports USB 3.0 link power management (U0/U1/U2/U3)
  - Supports USB 2.0 link power management (LPM: L0/L1/L2/L3)
- Supports Energy Star and EuP specifications for low-power PC peripheral system
- Supports all VBUS control options
  - Individual or global over-current detection
  - Individual or ganged power control
- Supports USB 3.0/2.0 Compound (non-removable) devices by I/O pin configuration
- Supports clock output (24/12 MHz) for Compound (non-removal) device on downstream ports
- Supports USB Battery Charging Specification Revision 1.2 (DCP, and CDP mode) and other portable devices(China Mobile Phone, EU Mobile Phone, and Apple iOS products, etc)
- 5.0 V power supply
  - On chip LDO for 3.3 V from 5 V input and Switching Regulator for 1.05 V from 5 V input
- System clock: 24 MHz crystal or Oscillator
- Supports SPI ROM for optional firmware and parameter data
- Provides SUSPEND status output
- Self/Bus-Powered modes can be set by pin strapping
- Operating Temperature range
  - 0°C to 70°C

Application Block Diagram

Figure 1 Schematic example of a bus-powered stand-alone hub.

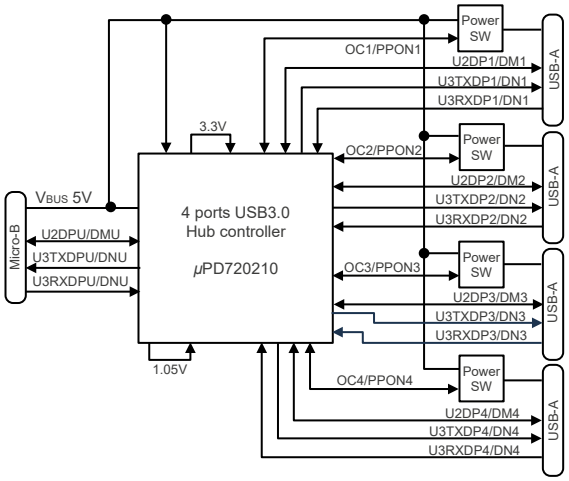


Figure 2 Schematic example of a Self-powered standalone hub.

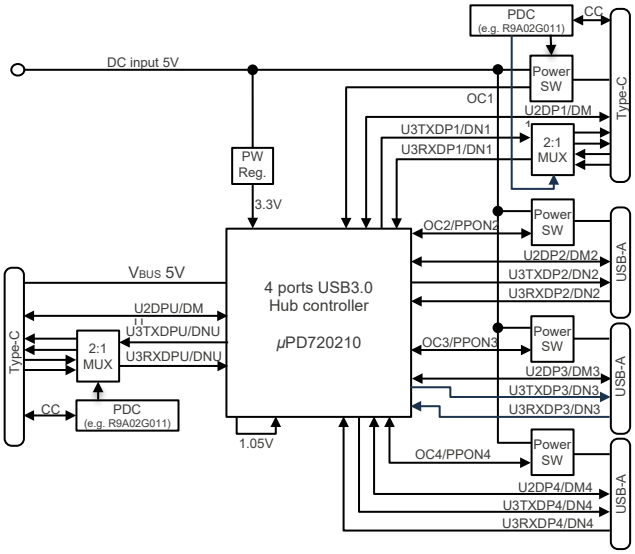


Figure 3 Schematic example of a USB3.0 hub on server/PC system.

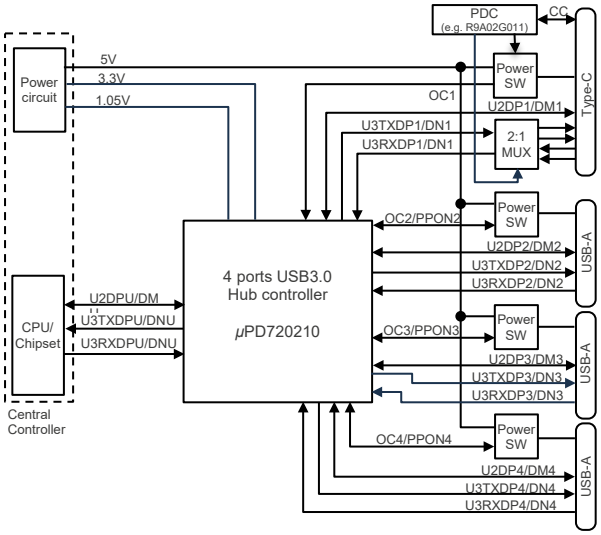
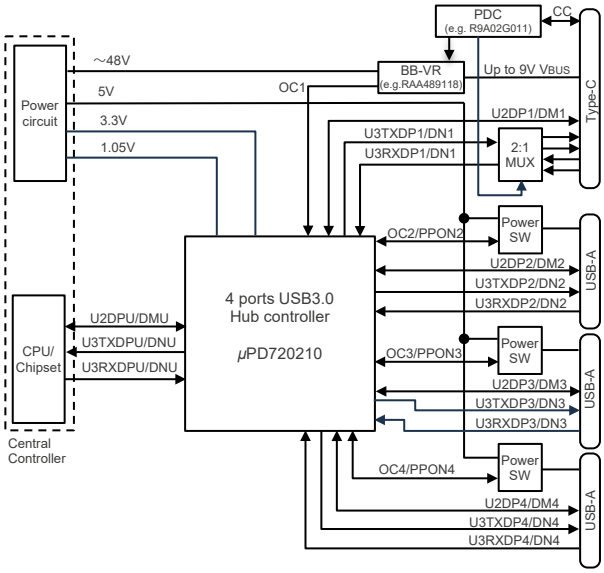


Figure 4 Schematic example of a USB3.0 hub with Power Delivery on server/PC system.



These schematics are conceptual only. Please refer to the User's manual and reference schematics for actual circuit configuration.

Contents

List of Figures

List of Tables

1. Overview

1.1 Applications

Standalone Hub, Monitor-Hub, Docking Station, Integrated Hub, etc.

1.2 Ordering Information

Part Number	Package	Packing form	Operating Temperature	Remark
*µ*PD720210K8-BAF-A	76-pin QFN (9 × 9)	Fraction (any vacancy in the tray and any free space in the carton)	0 to +70°C	Lead-free product
*µ*PD720210K8-BAF-M1-A		Full Carton (tray and Carton is packed with every product)		

1.3 Block Diagram

Figure 1-1. *µ*PD720210 Block Diagram

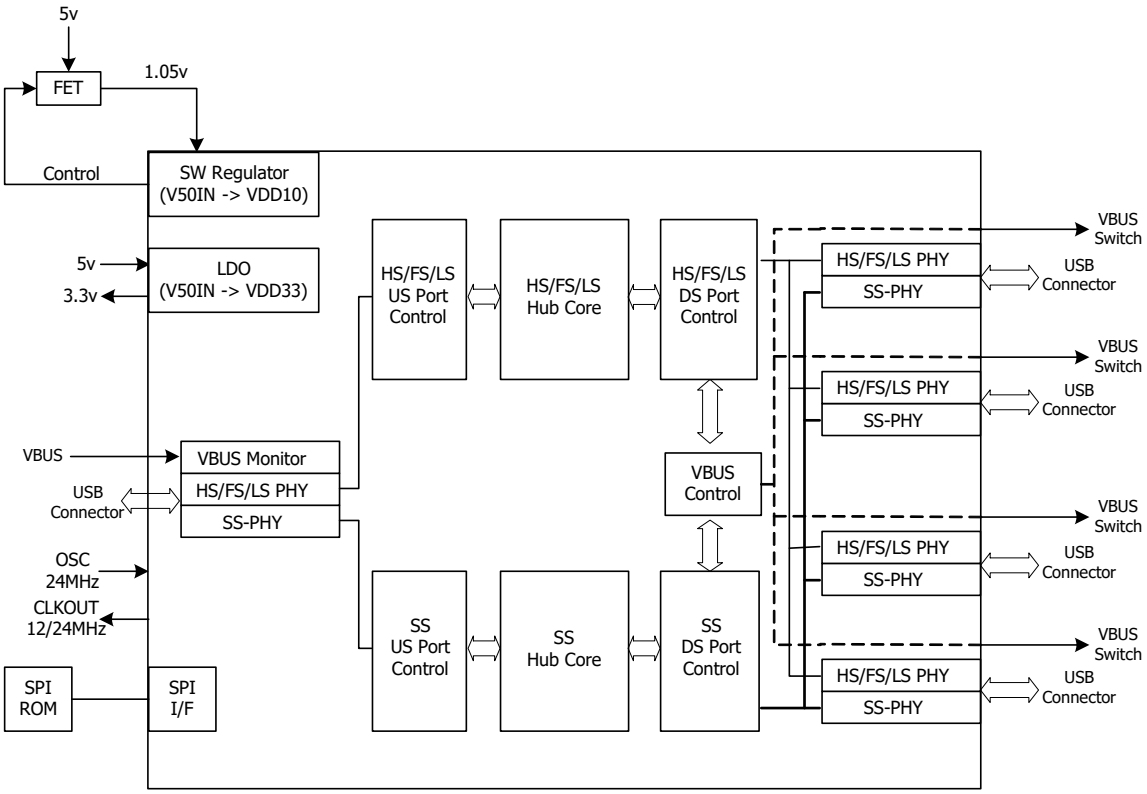


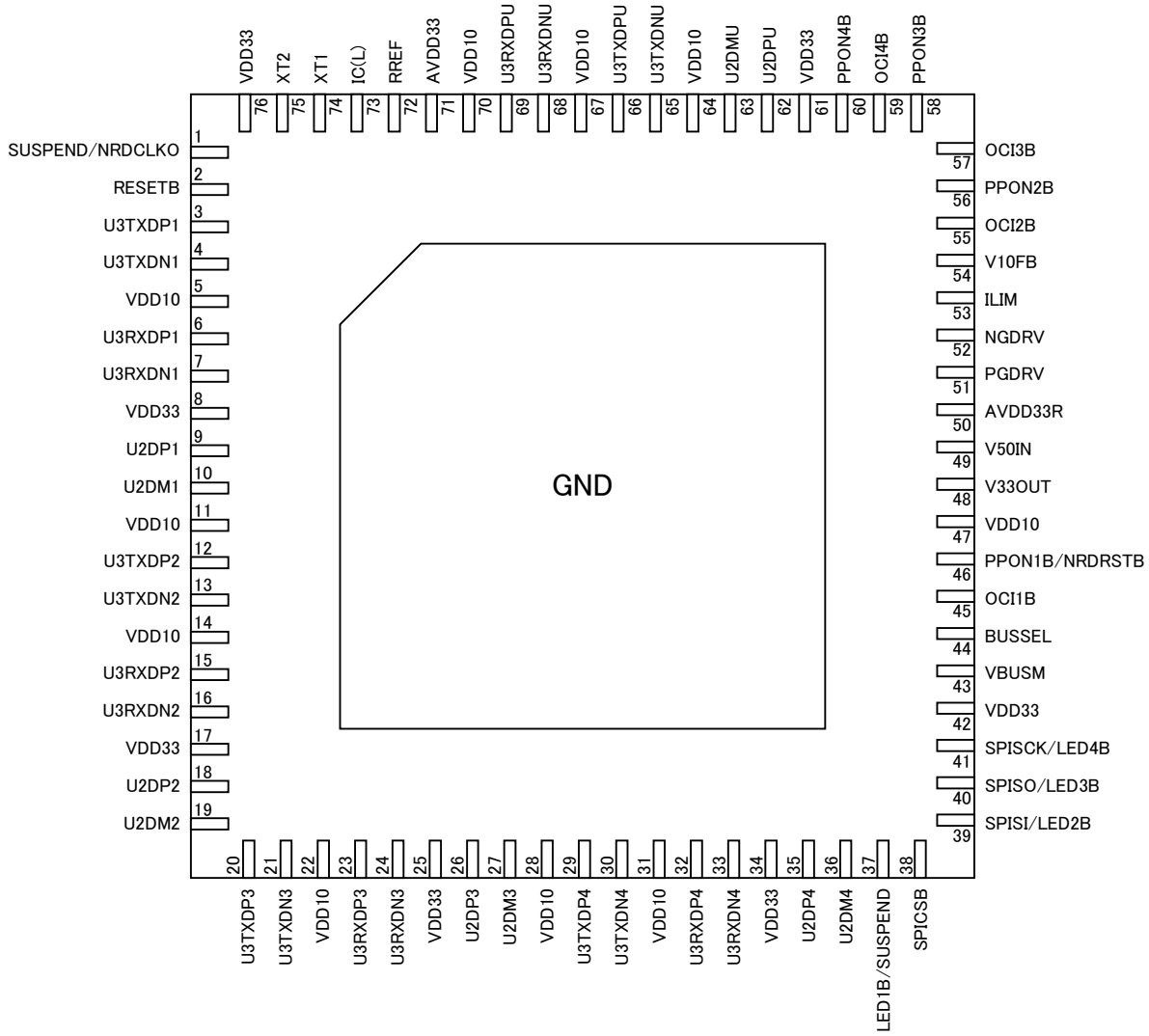
Table 1-1. Terminology

Block Name	Description
SS PHY	SuperSpeed transceiver
HS/FS/LS PHY	High-/Full-/Low-speed transceiver
VBUS Monitor	Monitors the VBUS voltage level of the upstream port.
SS US Port Control	Upstream port control logic for SuperSpeed
HS/FS/LS US Port Control	Upstream port control logic for High-/Full-/Low-speed
SS Hub Core	Central control logic for SS-Hub.
HS/FS/LS Hub Core	Central control logic for HS/FS/LS-Hub.
SS DS Port Control	Downstream port control logic for SuperSpeed
HS/FS/LS DS Port Control	Downstream port control logic for HS/FS/LS
VBUS Control	Controls all the external port power switches
SPI Interface	Connected to external serial ROM which can hold the optional firmware and hub settings
SW-Regulator	Switching regulator control logic to output 1.05 V power from 5 V input, utilizing the external transistor
LDO	Integrated Low Drop Out regulator to output 3.3 V power from 5 V input.

1.4 Pin Configuration

- **76-pin QFN (9 × 9)**
  *µ*PD720210K8-BAF-A / *µ*PD720210K8-BAF-M1-A

Figure 1-2. Pin Configuration of *µ*PD720210 (Top View)



2. Pin Function

This section describes each pin function.

Strapping information in the tables shows the pin can be used to configure the functional settings of this controller when the pin is pulled up/down, as detected at the end of chip reset. See *µ*PD720210 User's Manual (R19UH0093) for detail.

2.1 Power Supply

Table 2-1. Power Supply

Pin Name	Pin No.	I/O Type	Function
VDD10	5, 11, 14, 22, 28, 31, 47, 64, 67, 70	Power	1.05 V power supply for Core Logic
VDD33	8, 17, 25, 34, 42, 61, 76	Power	3.3 V power supply for IO buffer
AVDD33	71	Power	3.3 V power supply for Analog circuit
V50IN	49	Power	LDO Regulator 5 V Input Refer to Section 7.8, 7.9, 7.10 and 7.11 of User's Manual (Document# R19UH0093) in more detail.
V33OUT	48	Power	LDO 3.3 V Output Refer to Section 7.8, 7.9, 7.10 and 7.11 of User's Manual (Document# R19UH0093) in more detail.
AVDD33R	50	Power	SW Regulator 3.3 V Input
NGDRV	52	-	SW Regulator Nch FET Control Note
PGDRV	51	-	SW Regulator Pch FET Control Note
ILIM	53	-	SW Regulator Current Sense
V10FB	54	-	SW Regulator Output Monitor

Note: See Section 3.10 for important information about the selection of FET.

2.2 Analog Signal

Table 2-2. Analog Signal

Pin Name	Pin No.	I/O Type	Function
RREF	72	-	Reference Voltage Input for USB 2.0 RREF must be connected to a 1.6 kΩ resistor with a tolerance of +/- 1%. It is strongly recommended to use a single resistor for 1.6 kΩ, versus the combined resistance with multiple resistors to achieve this value and tolerance.

2.3 System Clock

Table 2-3. System Clock

Pin Name	Pin No.	I/O Type	Function
XT1	74	IN	External Oscillator Input Connect to 24 MHz crystal. This pin can be a 3.3 V Oscillator input as well.
XT2	75	OUT	External Oscillator Output Connect to 24 MHz crystal When using single-ended clock input to XT1, this pin should be left open.

2.4 System Interface Signal

Table 2-4. System Interface Signals

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Type</th><th>Active Level</th><th>Function</th></tr>
<tr><td>SUSPEND/NRDCLKO</td><td>1</td><td>OUT</td><td>High/NA</td><td>SUSPEND Output or CLKOUT depending on pin strap setting of SPICSB and OCI1B.
SUSPEND is Suspend state output.
1: in suspend state
0: not in suspend state
[Note]
SUSPEND/NRDCLKO output level is Hi-z till this pin function is configured as SUSPEND output or clock output for non-removable device
<table>
<tr><th>SPICSB</th><th>OCI1B</th><th>Pin Function</th></tr>
<tr><td rowspan="2">Low</td><td>Low</td><td>NRDCLKO</td></tr>
<tr><td>High</td><td>SUSPEND</td></tr>
<tr><td>High</td><td>X</td><td>Depends on Serial ROM setting</td></tr>
</table></td></tr>
<tr><td>VBUSM</td><td>43</td><td>IN</td><td>High</td><td>Upstream Port VBUS Monitor
Divide VBUS to 3.3V and connect to VBUSM</td></tr>
<tr><td>BUSSEL</td><td>44</td><td>IN</td><td>N/A</td><td>Power Mode Select Input
0: Bus-power setting
1: Self-power setting</td></tr>
<tr><td>LED1B/SUSPEND</td><td>37</td><td>OUT</td><td>Low</td><td>When the external ROM is used (SPICSB is high) and SUSPEND function is enabled in the ROM Writing Tool, LED1B/SUSPEND is used as SUSPEND function. If the SUSPEND function is not enabled, this pin is not functional (Hi-Z).
[Function]
Suspend state is shown by the following pin level.
1: in suspend state
0: not in suspend state
<table>
<tr><th>SPICSB</th><th>SPISCK/ LED4B</th><th>SPISO/ LED3B</th><th>SPISI/ LED2B</th><th>LED1B/ SUSPEND</th><th>Pin Function</th></tr>
<tr><td>Low</td><td colspan="3">Others</td><td>High</td><td>Reserved (Hi-Z)</td></tr>
<tr><td>Low</td><td>X</td><td>X</td><td>X</td><td>Low</td><td>Reserved (Hi-Z)</td></tr>
<tr><td>High</td><td>X</td><td>X</td><td>X</td><td>X</td><td>SUSPEND or Hi-Z</td></tr>
</table>
[Pin strapping option]
This pin is used for pin strap option to select the below functions. Refer to μPD720210 User's Manual (R19UH0093) for the following setting
- Battery Charging mode (Refer to Section 5.1.5)
- Address length of external ROM (Refer to Section 5.1.7)</td></tr>
<tr><td>RESETB</td><td>2</td><td>IN</td><td>Low</td><td>Chip Reset Input</td></tr>
</table>

2.5 USB Port Control Signal

Table 2-5. USB Port Control Signals

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Type</th><th>Active Level</th><th>Function</th></tr>
<tr><td>OCI1B</td><td>45</td><td>IN</td><td>Low</td><td>[Function]
Over Current Input
0: Over-current condition is detected.
1: Non over-current condition is detected.
[Pin strapping option]
<table><tr><td>OCI1B</td><td>Pin Function</td></tr><tr><td>High</td><td>Removable device setting and Over current input.</td></tr><tr><td>Low</td><td>Non-Removable setting.</td></tr></table>This pin is used to select non-removable setting.</td></tr>
<tr><td>OCI2B, OCI3B, OCI4B</td><td>55, 57, 59</td><td>IN</td><td>Low</td><td>[Function]
Over Current Input
0: Over-current condition is detected.
1: Non over-current condition is detected.
[Pin strapping option]
<table><tr><td>OCIXB</td><td>Pin Function</td></tr><tr><td>High</td><td>Removable device setting and Over Current Input.</td></tr><tr><td>Low</td><td>Non-Removable setting.</td></tr></table>This pin is used to select non-removable setting.</td></tr>
<tr><td>PPON1B/NRDRSTB</td><td>46</td><td>I/O</td><td>Low</td><td>[Function]
Port Power Control or NRDRSTB (Non-Removable Device Reset) depending on pin strap setting of this pin.
<table><tr><td>PPON1B/NRDRSTB</td><td>Pin Function</td></tr><tr><td>High</td><td>PPON1B</td></tr><tr><td>Low</td><td>NRDRSTB</td></tr></table>PPON1B is a Port Power Control signal
0: Power supply for VBUS is on.
1: Power supply for VBUS is off.
NRDRSTB is a reset signal for Non-Removable device.</td></tr>
<tr><td>PPON2B</td><td>56</td><td>I/O</td><td>Low</td><td>[Function]
This pin is a Port Power Control signal.
0: Power supply for VBUS is on.
1: Power supply for VBUS is off.
[Pin strapping option]
This pin is used for pin strapping option:
Gang/Individual Power Control of all ports.
<table><tr><td>PPON2B</td><td>Gang/Individual Mode</td></tr><tr><td>High</td><td>Individual</td></tr><tr><td>Low</td><td>Gang</td></tr></table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Type</th><th>Active Level</th><th>Function</th></tr>
<tr><td>PPON3B, PPON4B</td><td>58, 60</td><td>I/O</td><td>Low</td><td>[Function]
These pins are a Port Power Control signal.
0: Power supply for VBUS is on.
1: Power supply for VBUS is off.

[Pin strapping option]
These pins are used for pin strapping options to select Number of ports.
<table>
<tr><th>PPON4B</th><th>PPON3B</th><th>Number of ports</th></tr>
<tr><td>Low</td><td>Low</td><td>2 ports setting
Port 3 & 4 are not used.</td></tr>
<tr><td>Low</td><td>High</td><td>3 ports setting
Port 4 is not used</td></tr>
<tr><td>High</td><td>Low</td><td>Prohibit setting</td></tr>
<tr><td>High</td><td>High</td><td>All ports are used</td></tr>
</table>
</td></tr>
</table>

2.6 USB Data Signal

Table 2-6. USB Data Signals

Pin Name	Pin No.	I/O Type	Function
U3TXDN1, U3TXDN2, U3TXDN3, U3TXDN4	4, 13, 21, 30	OUT	USB 3.0 Downstream Transmit data D- signal for SuperSpeed
U3TXDNU	65	OUT	USB 3.0 Upstream Transmit data D- signal for SuperSpeed
U3TXDP1, U3TXDP2, U3TXDP3, U3TXDP4	3, 12, 20, 29	OUT	USB 3.0 Downstream Transmit data D+ signal for SuperSpeed
U3TXDPU	66	OUT	USB 3.0 Upstream Transmit data D+ signal for SuperSpeed
U3RXDN1, U3RXDN2, U3RXDN3, U3RXDN4	7, 16, 24, 33	IN	USB 3.0 Downstream Receive data D- signal for SuperSpeed
U3RXDNU	68	IN	USB 3.0 Upstream Receive data D- signal for SuperSpeed
U3RXDP1, U3RXDP2, U3RXDP3, U3RXDP4	6, 15, 23, 32	IN	USB 3.0 Downstream Receive data D+ signal for SuperSpeed
U3RXDPU	69	IN	USB 3.0 Upstream Receive data D+ signal for SuperSpeed
U2DM1, U2DM2, U2DM3, U2DM4	10, 19, 27, 36	I/O	USB 2.0 Downstream D- signal for High-/Full-/Low-speed
U2DMU	63	I/O	USB 2.0 Upstream D- signal for High-/Full-/Low-speed
U2DP1, U2DP2, U2DP3, U2DP4	9, 18, 26, 35	I/O	USB 2.0 Downstream D+ signal for High-/Full-/Low-speed
U2DPU	62	I/O	USB 2.0 Upstream D+ signal for High-/Full-/Low-speed

2.7 SPI Interface

Table 2-7. SPI Interface

Pin Name	Pin No.	I/O Type	Active Level	Function
SPISCK/LED4B	41	I/O	N/A	[Function] External serial ROM Clock Output depending on pin strap setting. [Pin strapping option] This pin is used for pin strapping option to select the below functions. Refer to μPD720210 User's Manual (R19UH0093) for the following setting. - Battery Charging mode (Refer to Section 5.1.5)
SPICSB	38	I/O	Low	[Function] External serial ROM Chip Select [Pin strapping option] This pin is used for pin strap option to select the below functions. Refer to μPD720210 User's Manual (R19UH0093) for the following setting. - External SPI ROM (Refer to Section 5.1.1) - Address length of external ROM (Refer to Section 5.1.7)
SPISO/LED3B	40	I/O	N/A	[Function] External serial ROM Data Input (to be connected to Serial Data Output pin of the external ROM) depending on pin strap setting. [Pin strapping option] This pin is used for pin strap option to select the below functions. Refer to μPD720210 User's Manual (R19UH0093) for the following setting. - Battery Charging mode (Refer to Section 5.1.5) - Address length of external ROM (Refer to Section 5.1.7)
SPISI/LED2B	39	I/O	N/A	[Function] External serial ROM Data Output (to be connected to Serial Data input pin of the external ROM) depending on pin strap setting. [Pin strapping option] This pin is used for pin strap option to select the below functions. Refer to μPD720210 User's Manual (R19UH0093) for the following setting. - Battery Charging mode (Refer to Section 5.1.5) - Address length of external ROM (Refer to Section 5.1.7)

2.8 Test Pin

Table 2-8. Test Pin

Pin Name	Pin No.	I/O Type	Active Level	Function
IC(L)	73	IN	High	IC(L) pin to be connected to GND

3. Electrical Specifications

3.1 Buffer List

- 3.3 V input buffer

  IC(L)

- 3.3 V input Schmitt buffer

  RESETB, OCI2B, OCI3B, OCI4B

- 3.3 V I_{OLH} = 4 mA output buffer

  SUSPEND/NRDCLKO, SPICSB, PPON1B/NRDRSTB, PPON2B, PPON3B, PPON4B

- 3.3 V I_{OLH} = 12 mA output buffer

  LED1B/SUSPEND, SPISI/LED2B, SPISCK/LED4B

- 3.3 V I_{OL} = 12 mA bi-directional buffer

  SPISO/LED3B

- 3.3 V input Schmitt buffer (5 V tolerant)

  VBUSM, BUSSEL, OCI1B

- 3.3 V oscillator interface

  XT1, XT2

- USB Classic interface

  U2DP(4:1, U), U2DM(4:1, U)

- USB SuperSpeed Serdes (Serializer-Deserializer)

  U3TXDP(4:1, U), U3TXDN(4:1, U), U3RXDP(4:1, U), U3RXDN(4:1, U)

- LDO Interface

  V33OUT, V50IN

- Switching Regulator Interface

  AVDD33R, PGDRV, NGDRV, ILIM, V10FB

3.2 Terminology

Table 3-1. Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, AV_{DD33}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a VDD pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into output pin.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Table 3-2. Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD10}, AV_{DD33}	Indicates the voltage range for normal logic operations occur when GND = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Input rise time	T_{ri}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device rises from 10% to 90%.
Input fall time	T_{fi}	Indicates the limit value for the time period when an input voltage applied to the input pins of the device falls from 90% to 10%.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.

Table 3-3. Term Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied whena 3-state output has high impedance.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.

3.3 Absolute Maximum Ratings

Table 3-4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Units
Power supply voltage	V_{DD33}, AV_{DD33}		−0.5 to +4.6	V
	V_{DD10}		−0.5 to +1.4	V
	V50IN		5.5	V
Input voltage, 3.3 V buffer	V_I	$V_I < V_{DD33}$ + 0.5 V	−0.5 to +4.6	V
Output voltage, 3.3 V buffer	V_O	$V_O < V_{DD33}$ + 0.5 V	−0.5 to +4.6	V
USB3.0 differential signals	V_I/V_O	$V_I/V_O < V_{DD10}$ + 0.5 V	−0.5 to +1.4	V
Input voltage, 5 V tolerant buffer	V_I	$V_I < V_{DD33}$ + 2.5 V	−0.5 to +6.6	V
Output current	I_O	4 mA Type	8	mA
	I_O	12 mA Type	24	mA
Storage temperature	T_{stg}		−65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

3.4 Recommended Operating Ranges

Table 3-5. Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating voltage With external power source	V_{DD33}, AV_{DD33}		3.0	3.3	3.6	V
	V_{DD10}		0.9975	1.05	1.1025	V
Operating voltage With on-chip Regulators	V50IN		4.75	5.0	5.25	V
Available Current for external components (3.3 V) **Note**	V33OUT				30	mA
High-level input voltage	V_{IH}		2.0		V_{DD33}+0.3	V
Low-level input voltage	V_{IL}		−0.3		+0.8	V
Input rise time	T_{ri}	Normal Buffer Schmitt Buffer	0 0		200 10	ns ms
Input fall time	T_{fi}	Normal Buffer Schmitt Buffer	0 0		200 10	ns ms
Operating ambient temperature	T_A		0		+70	°C

3.5 DC Characteristics

Table 3-6. DC Characteristics (V_{DD33} = 3.3 V ± 10%, V_{DD10} = 1.05 V ± 5%, T_A = 0 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Units
Off-state output current	I_{OZ}	V_I = V_{DD33} or GND		±10	μA
Input leakage current	I_I	V_I = V_{DD33} or GND		±10	μA
Low-level output voltage	V_{OL}	I_{OL} = 0 mA		0.1	V
High-level output voltage	V_{OH}	I_{OH} = 0 mA	V_{DD33}–0.1		V

Table 3-7. USB Interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z_{HSDRV}		40.5	49.5	Ω
Input Levels for Low-/Full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	|(D+) – (D–)|	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/Full-speed:					
High-level output voltage	V_{OH}	RL of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	RL of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		–50	+500	mV
High-speed differential input signaling level	See Figure 3-4.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		–10	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		–10	+10	mV
Chirp J level (differential signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V_{CHIRPK}		–900	–500	mV

Figure 3-1. Differential Input Sensitivity Range for Low-/Full-speed

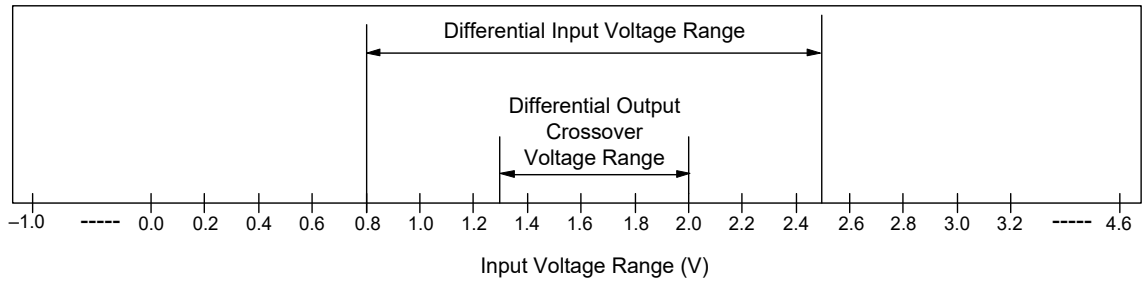


Figure 3-2. Full-speed Buffer VOH/IOH Characteristics for High-speed Capable Transceiver

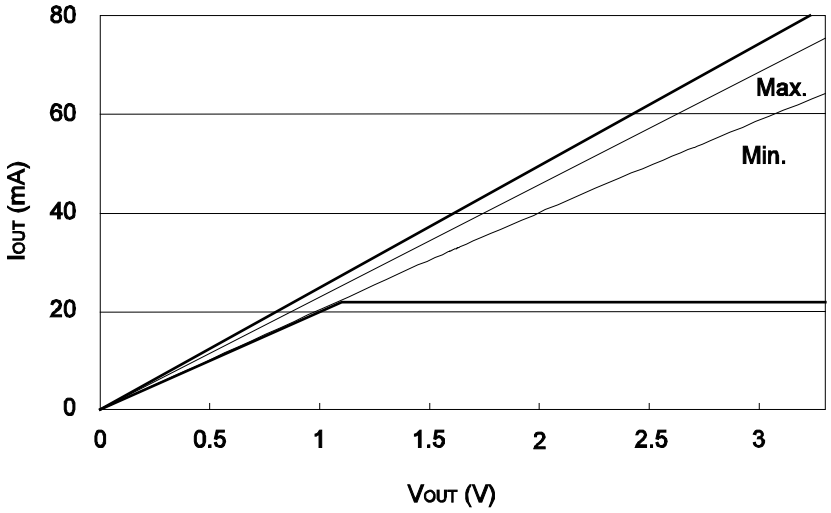


Figure 3-3. Full-speed Buffer VOL/IOL Characteristics for High-speed Capable Transceiver

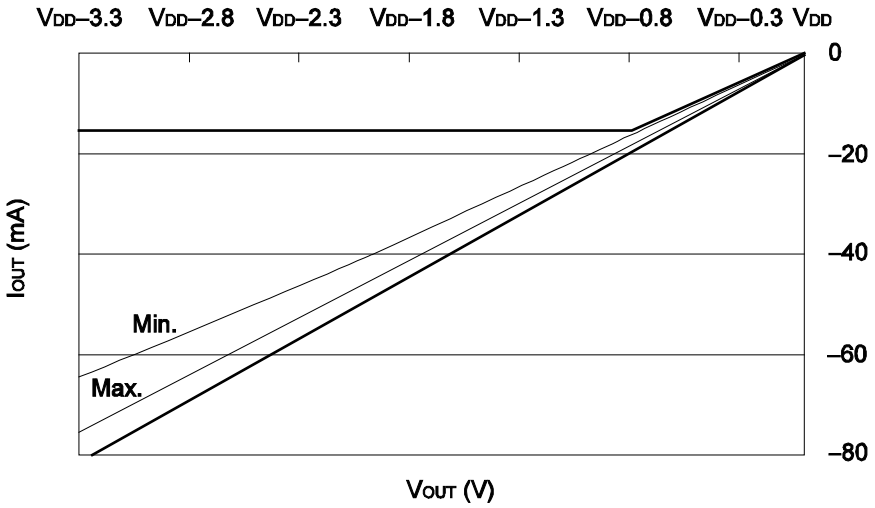


Figure 3-4. Receiver Sensitivity for Transceiver at DP/DM

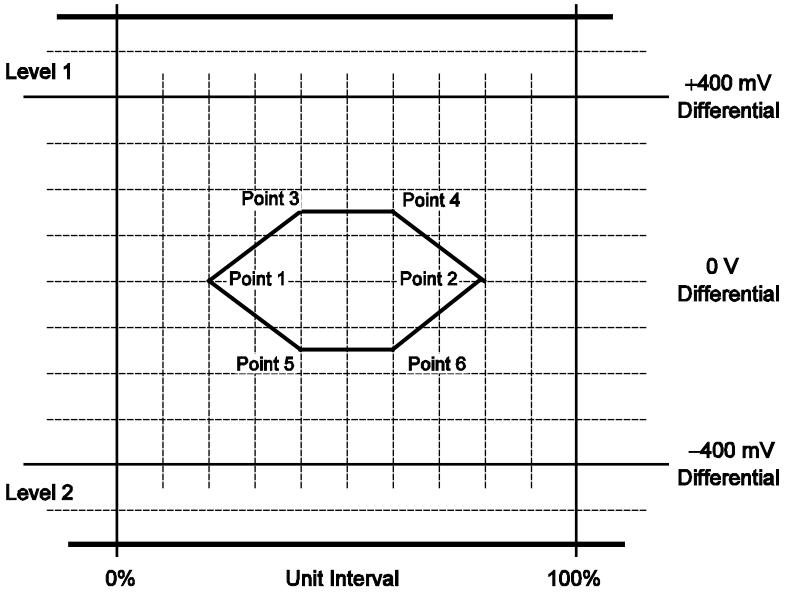


Figure 3-5. Receiver Measurement Fixtures

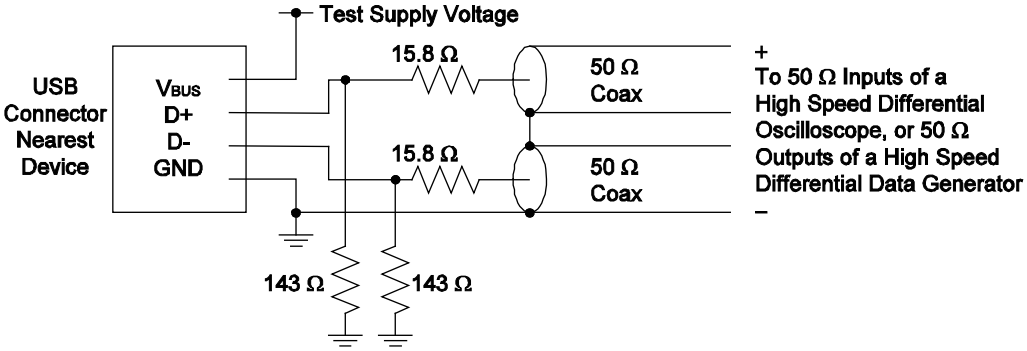


Table 3-8. Cut-off Current of On-chip Regulators

Parameter	Symbol	Condition	Min.	Max.	Units
Cut-off current of on-chip Regulator (1.05 V)	$I_{cutoff1}$	-	1.4	1.8	A
Cut-off current of on-chip Regulator (3.3 V)	$I_{cutoff3}$	-	0.8	1.2	A

3.6 Pin Capacitance

Table 3-9. Pin Capacitance

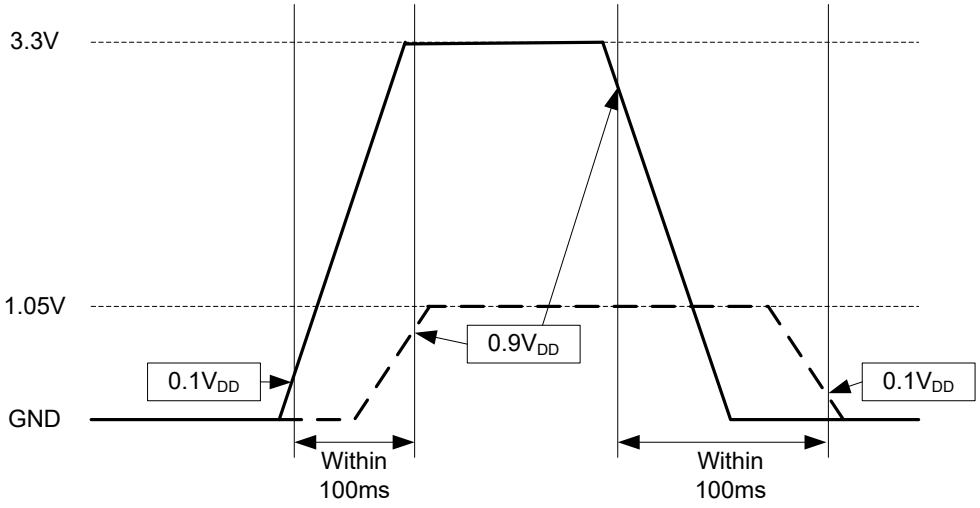
Parameter	Symbol	Condition	Min.	Max.	Units
System Interface Pins capacitance	C_{sys}			5	pF
USB Port Control Pins capacitance	C_{Por}			5	pF
SPI Interface Pins capacitance	C_{SPI}			5	pF

3.7 Sequence for Turning On or Off Power

When the external power source for 1.05 V and 3.3 V power is used, it is recommended that the time difference between the start of power-supply rise (3.3 V or 1.05 V) and the point where both power supplies are stabilized should be within 100 ms, regardless of the order of power sequence. A voltage of $0.1V_{DD}$ has to be raised to $0.9V_{DD}$ within the specified time.

When the on-chip LDO and the switching regulator are used, this timing is controlled by the internal circuit as defined here.

Figure 3-6. Order of Power Sequence



3.8 AC Characteristics

3.8.1 System Clock

Table 3-10. System Clock (XT1/XT2) Ratings (V_{DD33} = 3.3 V ± 10%, V_{DD10} = 1.05 V ± 5%, T_A = 0 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Clock frequency	F_{CLK}	Crystal	−100 ppm	24	+100 ppm	MHz
Clock duty cycle	T_{DUTY}		40	50	60	%

Remark Required accuracy of crystal or oscillator block includes initial frequency accuracy, the spread of Crystal capacitor loading, supply voltage, temperature and aging, etc.

3.8.2 Reset and Clock Timing

Table 3-11. Power On Reset (RESETB) Timings

Parameter	Symbol	Condition	Min.	Max.	Units
Power on reset time	T_{PONRST}	See **Figure 3-7**.	10		ms

Remarks 1. No order in power-on V_{DD33}, AV_{DD33}, and V_{DD10}.

2. All power sources should be stable within 100 ms from the earliest turned on power sources.

3. RESETB shall be de-asserted after all power sources and the system clock become stable.

Figure 3-7. Power On Reset Timing

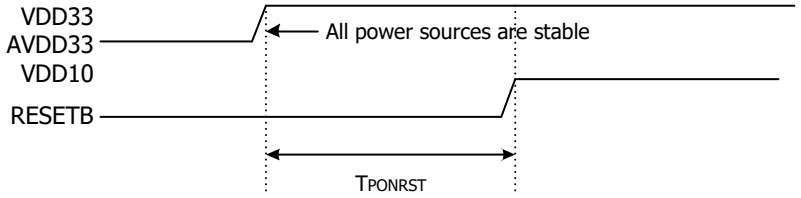


Table 3-12. NRDRST Output and CLKOUT Signal Timing

Parameter	Symbol	Condition	Min.	Max.	Units
Clock out timing after Reset out ends	$T_{RSTtoCLK}$	See Figure 3-8.		300	μs
Reset timing for Non-Removable Device after Clock out starts	$T_{CLKtoRSTE}$	See Figure 3-8.		30	ms

Figure 3-8. NRDRST Output and CLKOUT Signal Timing

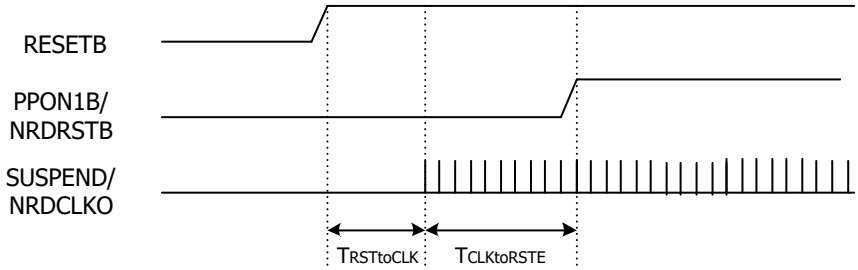


Table 3-13, **Figure 3-9** shows the stopping timing of clock output of SUSPNED/NRDCLKO pin. There are three cases for the timing. To stop the clock output, a setting of ROM Writing Tool is needed. Refer to *µ*PD720210 User's Manual (R19UH0093) in more detail.

Case 1: Non-removable device on Port 1 is a USB 2.0 device.
After a USB 2.0 non-removable device of Port1 transitions to suspend state and the wait time of "$T_{U2CLKOFF}$" is satisfied, the clock output stops.

Case 2: Non-removable device on Port 1 is a USB 3.0 device except USB 3.0 hub.
After a USB 3.0 non-removable device of Port1 transitions to suspend state and the wait time of "$T_{U3CLKOFF}$" is satisfied, the clock output stops.

Case 3: Non-removable device on Port 1 is a USB 3.0 hub.
After a USB 3.0 non-removable hub of Port1 transitions to suspend state and the wait time of "$T_{U2CLKOFF}$" and "$T_{U3CLKOFF}$" is satisfied, the clock output stops.

Table 3-13. NRDCLKO Clock Output Stop Timing

Parameter	Symbol	Condition	Min.	Max.	Units
Wait time of stopping Clock Output after Non-Removable USB 2.0 Device transitions to Suspend state **Note1**	$T_{U2CLKOFF}$	See Figure 3-9.		50	ms
Wait time of stopping Clock Output after Non-Removable USB 3.0 Device transitions to Suspend state **Note2**	$T_{U3CLKOFF}$	See Figure 3-9.		50	ms

Notes 1. If USB 2.0 Port 1 detects any resume signal during this wait time, *µ*PD720210 doesn't stop the clock output for non-removable device.
2. If USB 3.0 Port 1 detects U3exit during this wait time, *µ*PD720210 doesn't stop the clock output for non-removable device.

Figure 3-9. NRDCLKO Clock Output Stop Timing

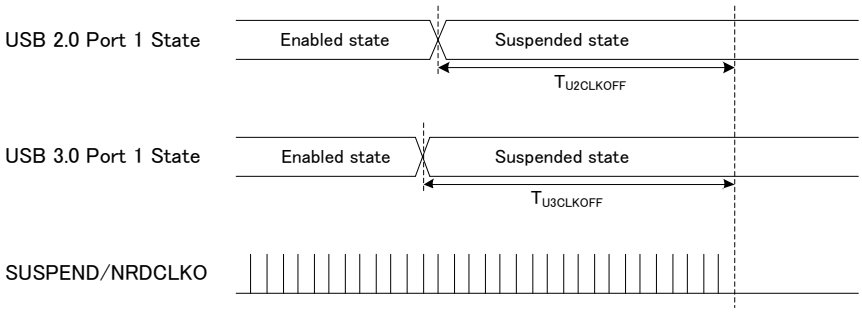


Table 3-14, Figure 3-10, Figure 3-11, and Figure 3-12 shows the starting timing of clock output of SUSPNED/NRDCLKO pin after stopping the clock output. There are three cases for the timing.

Case 1: Non-removable device on Port 1 is a USB 2.0 device.
If "$T_{CLKONbyU2R}$" or "$T_{CLKONbyU2T}$" or "$T_{CLKONbyU2Sta}$" is satisfied, the clock output is initiated.

Case 2: Non-removable device on Port 1 is a USB 3.0 device except USB 3.0 hub.
If "$T_{CLKONbyU3R}$" or "$T_{CLKONbyU3T}$" is satisfied, the clock output is initiated.

Case 3: Non-removable device on Port 1 is a USB 3.0 hub.
If "$T_{CLKONbyU2R}$" or "$T_{CLKONbyU2T}$" or "$T_{CLKONbyU2Sta}$" or "$T_{CLKONbyU3R}$" or "$T_{CLKONbyU3T}$" is satisfied, the clock output is initiated.

Table 3-14. NRDCLKO Clock Output Start Timing

Parameter	Symbol	Condition	Min.	Max.	Units
Clock Output Start timing after sending resume signal or detecting resume signal on the USB2.0 side of Port 1.	$T_{CLKONbyU2R}$	See Figure 3-10.		1	ms
Clock Output Start timing after transition to non-suspend state on the USB2.0 side of Port 1.	$T_{CLKONbyU2T}$	See Figure 3-10.		1	ms
Clock Output Start timing after transition to non-suspend state on the USB 2.0 side of the upstream port.	$T_{CLKONbyU2Sta}$	See Figure 3-11.		1	ms
Clock Output Start timing after sending U3exit or detecting U3exit on the USB3.0 side of Port 1	$T_{CLKONbyU3R}$	See Figure 3-12.		1	ms
Clock Output Start timing after transitioning to non-suspend state on the USB3.0 side of Port 1	$T_{CLKONbyU3T}$	See Figure 3-12.		1	ms

Figure 3-10. NRDCLKO Clock Output Start Timing by Resuming USB 2.0 Port 1

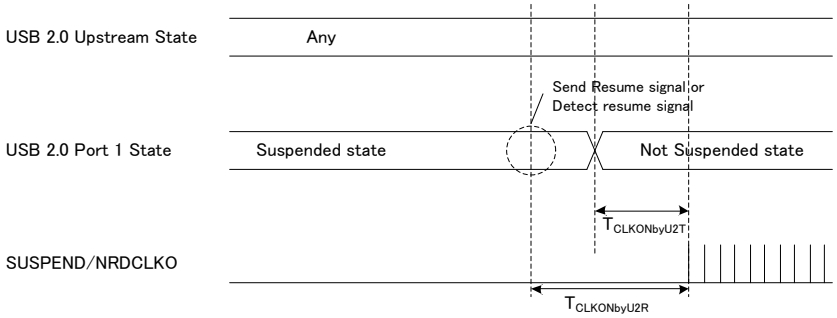


Figure 3-11. NRDCLKO Clock Output Initiate Timing by USB 2.0 Upstream State Transition

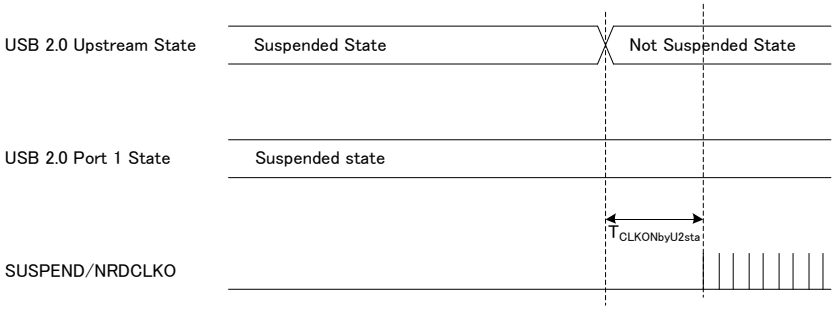
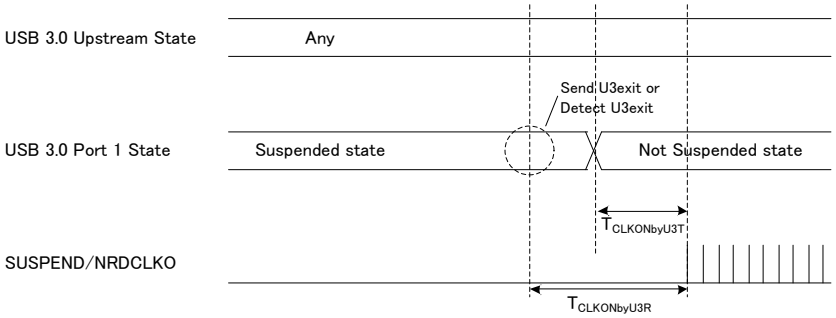


Figure 3-12. NRDCLKO Clock Output Initiate Timing by Resuming USB 3.0 Port 1



3.8.3 USB3.0 SuperSpeed Interface – Differential Transmitter (TX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Table 3-15. Transmitter Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Differential p-p Tx voltage swing	$V_{TX-DIFF-PP}$	0.8	1.2	V
Tx de-emphasis	$V_{TX-DE-RATIO}$	3.0	4.0	dB
DC differential impedance	$R_{TX-DIFF-DC}$	72	120	Ω
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		0.6	V
AC Coupling Capacitor	$C_{AC-COUPLING}$	75	200	nF
Maximum slew rate	$t_{CDR-SLEW-MAX}$		10	ms/s

Table 3-16. Transmitter Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Deterministic min pulse	$t_{MIN-PULSE-Dj}$	0.96		UI
Tx min pulse	$t_{MIN-PULSE-Tj}$	0.90		UI
Transmitter Eye	t_{TX-EYE}	0.625		UI
Tx deterministic jitter	$t_{TX-DJ-DD}$		0.205	UI
Tx input capacitance for return loss	$C_{TX-PARASITIC}$		1.25	pf
Transmitter DC common mode impedance	R_{TX-DC}	18	30	Ω
Transmitter short-circuit current limit	$I_{TX-SHORT}$		60	mA
Transmitter DC common-mode voltage	$V_{TX-DC-CM}$	0	2.2	V
Tx AC common mode voltage	$V_{TX-CM-AC-PP-ACTIVE}$		100	mVp-p
Absolute DC Common Mode Voltage between U1 and U0	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$		200	mV
Electrical Idle Differential Peak- Peak Output voltage	$V_{TX-IDLE-DIFF-AC-pp}$	0	10	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	0	10	mV

3.8.4 USB3.0 SuperSpeed Interface – Differential Receiver (RX) Specifications

(Refer to Universal Serial Bus 3.0 Specification Revision 1.0 for more information)

Table 3-17. Receiver Normative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Unit Interval	UI	199.94	200.06	ps
Receiver DC common mode impedance	R_{RX-DC}	18	30	Ω
DC differential impedance	$R_{RX-DIFF-DC}$	72	120	Ω
DC Input CM Input Impedance for V>0 during Reset of Power down	$Z_{RX-HIGH-IMP-DC-POS}$	25k		Ω
LFPS Detect Threshold	$V_{RX-LFPS-DET-DIFF-p-p}$	100	300	mV

Table 3-18. Receiver Informative Electrical Parameters

Parameter	Symbol	Min	Max	Units
Differential Rx peak-to-peak voltage	$V_{RX-DIFF-PP-POST-EQ}$	30		mV
Max Rx inherent timing error	T_{RX-Tj}		0.45	UI
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD}$		0.285	UI
Rx input capacitance for return loss	$C_{RX-PARASITIC}$		1.1	pF
Rx AC common mode voltage	$V_{RX-CM-AC-P}$		150	mVPeak
Rx AC common mode voltage during the U1 to U0 transition	$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$		200	mVPeak

3.8.5 USB2.0 Interface

Table 3-19. USB Interface (1 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Low-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{LR}	C_L = 200 pF to 600 pF	75	300	ns
Fall time (90% to 10%)	t_{LF}	C_L = 200 pF to 600 pF	75	300	ns
Differential rise and fall time matching	t_{LRFM}	(t_{LR}/t_{LF}) **Note**	80	125	%
Low-speed data rate	$t_{LDRATHS}$	Average bit rate	1.49925	1.50075	Mbps
Downstream facing port source jitter total (including frequency tolerance) (**Figure 3-19**):					
To next transition	t_{DDJ1}		−25	+25	ns
For paired transitions	t_{DDJ2}		−14	+14	ns
Downstream facing port differential receiver jitter total (including frequency tolerance) (**Figure 3-19**):					
To next transition	t_{UJR1}		−152	+152	ns
For paired transitions	t_{UJR2}		−200	+200	ns
Source SE0 interval of EOP (**Figure 3-18**)	t_{LEOPT}		1.25	1.5	μs
Receiver SE0 interval of EOP (**Figure 3-18**)	t_{LEOPR}		670		ns
Width of SE0 interval during differential transition	t_{LST}			210	ns
Hub differential data delay (**Figure 3-15**)	t_{LHDD}			300	ns
Hub differential driver jitter (including cable) (**Figure 3-15**):					
Downstream facing port					
To next transition	t_{LDHJ1}		−45	+45	ns
For paired transitions	t_{LDHJ2}		−15	+15	ns
Upstream facing port					
To next transition	t_{LUHJ1}		−45	+45	ns
For paired transitions	t_{LUHJ2}		−45	+45	ns
Data bit width distortion after SOP (**Figure 3-15**)	t_{LSOP}		−60	+60	ns
Hub EOP delay relative to t_{HDD} (**Figure 3-16**)	t_{LEOPD}		0	200	ns
Hub EOP output width skew (**Figure 3-16**)	t_{LHESK}		−300	+300	ns
Full-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% to 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms

Note: Excluding the first transition from the Idle state.

Table 3-20. USB Interface (2 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Electrical Characteristics (Continued)					
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (**Figure 3-17**): To next transition For paired transitions	 t_{DJ1} t_{DJ2}	**Note**	 –3.5 –4.0	 +3.5 +4.0	 ns ns
Source jitter for differential transition to SE0 transition (**Figure 3-18**)	t_{FDEOP}		–2	+5	ns
Receiver jitter (**Figure 3-19**): To Next Transition For Paired Transitions	 t_{JR1} t_{JR2}		 –18.5 –9	 +18.5 +9	 ns ns
Source SE0 interval of EOP (**Figure 3-18**)	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP (**Figure 3-18**)	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns
Hub differential data delay (**Figure 3-15**) (with cable) (without cable)	 t_{HDD1} t_{HDD2}			 70 44	 ns ns
Hub differential driver jitter (including cable) (**Figure 3-15**): To next transition For paired transitions	 t_{HDJ1} t_{HDJ2}		 –3 –1	 +3 +1	 ns ns
Data bit width distortion after SOP (**Figure 3-15**)	t_{FSOP}		–5	+5	ns
Hub EOP delay relative to t_{HDD} (**Figure 3-16**)	t_{FEOPD}		0	15	ns
Hub EOP output width skew (**Figure 3-16**)	t_{FHESK}		–15	+15	ns
High-speed Electrical Characteristics					
Rise time (10% to 90%)	t_{HSR}		500		ps
Fall time (90% to 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure 3-13**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 High-speed	Bit times
Data source jitter	See **Figure 3-13**.				
Receiver jitter tolerance	See **Figure 3-4**.				
Hub data delay (without cable)	t_{HSHDD}			36 High-speed+4 ns	Bit times
Hub data jitter	See **Figure 3-4**, **Figure 3-13**.				
Hub delay variation range	t_{HSHDV}			5 High-speed	Bit times

Note: Excluding the first transition from the Idle state.

Table 3-21. USB Interface (3 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings					
Time to detect a downstream facing port connect event (**Figure 3-21**): Awake hub Suspended hub	t_{DCNN}		 2.5 2.5	 2000 12000	 μs μs
Time to detect a disconnect event at a hub's downstream facing port (**Figure 3-20**)	t_{DDIS}		2.0	2.5	μs
Duration of driving resume to a downstream port (only from a controlling hub)	t_{DRSMDN}		20		ms
Time from detecting downstream resume to rebroadcast	t_{URSM}			1.0	ms
Duration of driving reset to a downstream facing port	t_{DRST}	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	t_{URLK}		2.5	100	μs
Time to detect a long SE0 from upstream	t_{URLSE0}		2.5	10000	μs
Duration of repeating SE0 upstream (for Low-/Full-speed repeater)	t_{URPSE0}			23	FS Bit times
Inter-packet delay (for High-speed) of packets traveling in same direction	$t_{HSIPDSD}$		88		Bit times
Inter-packet delay (for High-speed) of packets traveling in opposite direction	$t_{HSIPDOD}$		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for High-speed	$t_{HSRSPIPD1}$			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	t_{FILT}		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	t_{WTDCH}			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	t_{DCHBIT}		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t_{DCHSE0}		100	500	μs
Period of idle bus before device can initiate resume	t_{WTRSM}		5		ms
Duration of driving resume upstream	t_{DRSMUP}		1	15	ms

Table 3-22. USB Interface (4 of 4)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Hub Event Timings (Continued)					
Time to detect a reset from upstream for non High-speed capable devices	t_{DETRST}		2.5	10000	μs
Inter-packet delay for Full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response with detachable cable for Full-speed	$t_{RSPIPD1}$			6.5	Bit times
SetAddress() completion time	$t_{DSETADDR}$			50	ms
Time to complete standard request with no data	$t_{DRQCMPLTND}$			50	ms
Time to deliver first and subsequent (except last) data for standard request	$t_{DRETDATA1}$			500	ms
Time to deliver last data for standard request	$t_{DRETDATAN}$			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the High-speed detection handshake	$t_{FILTSE0}$		2.5		μs
Time a hub operating in non-suspended Full-speed will wait after start of SE0 on upstream before beginning the High-speed detection handshake	$t_{WTRSTFS}$		2.5	3000	ms
Time a hub operating in High-speed will wait after start of SE0 on upstream before reverting to Full-speed	t_{WTREV}		3.0	3.125	ms
Time a hub will wait after reverting to Full-speed before sampling the bus state on upstream and beginning the High-speed will wait after start of SE0 on upstream before reverting to Full-speed	$t_{WTRSTHS}$		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t_{UCH}		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t_{UCHEND}			7.0	ms
Time between detection of downstream chip and entering High-speed state	t_{WTHS}			500	μs
Time after end of upstream Chirp at which hub reverts to Full-speed default state if no downstream Chirp is detected	t_{WTFS}		1.0	2.5	ms

Figure 3-13. Transmit Waveform for Transceiver at DP/DM

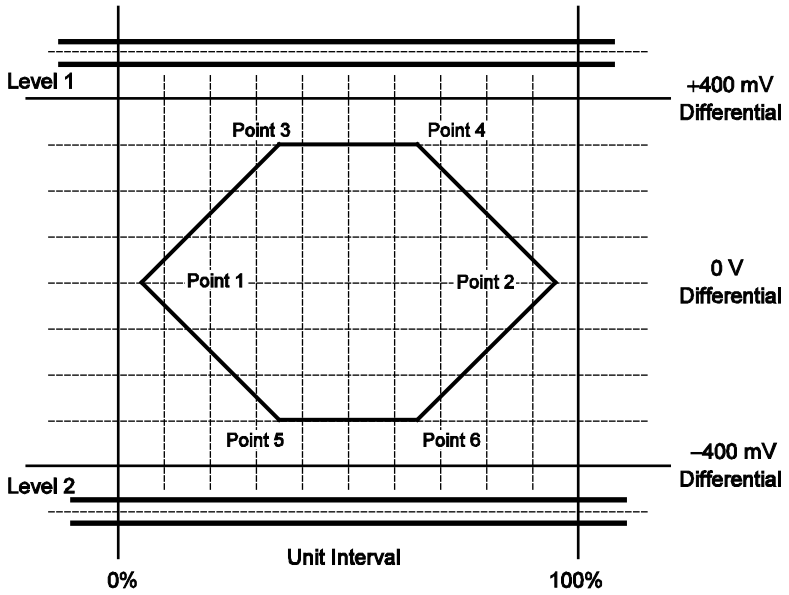


Figure 3-14. Transmitter Measurement Fixtures

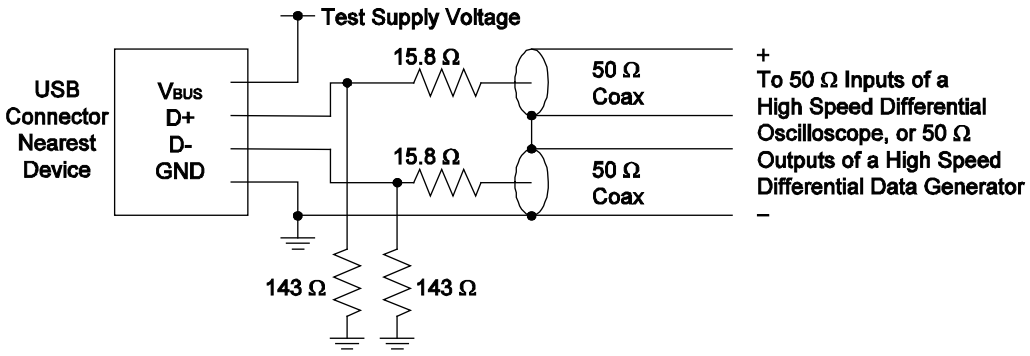
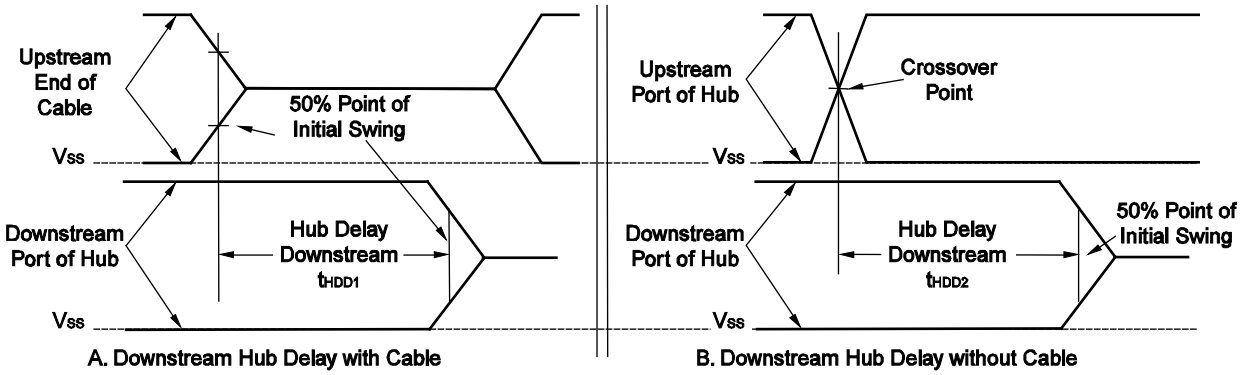
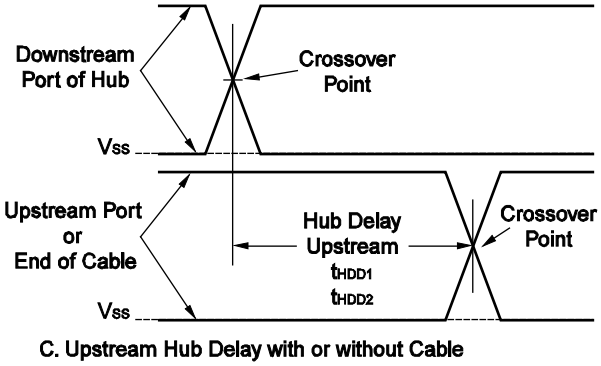
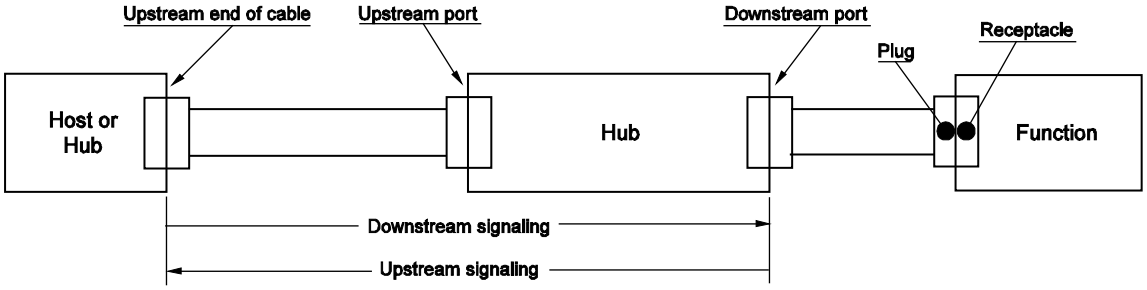


Figure 3-15. Hub Differential Delay, Differential Jitter, and SOP Distortion





C. Upstream Hub Delay with or without Cable



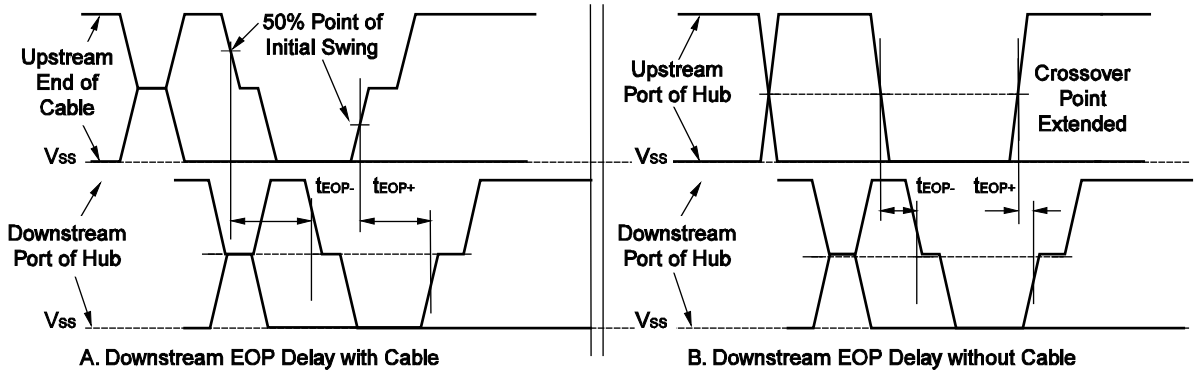
D. Measurement Points

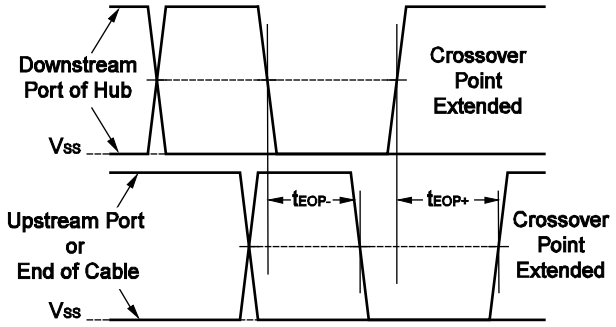
Hub Differential Jitter:
$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K)$ or $t_{HDDx}(K) - t_{HDDx}(J)$ Consecutive Transitions
$t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J)$ or $t_{HDDx}(K) - t_{HDDx}(K)$ Paired Transitions

Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):
$t_{FSOP} = t_{HDDx}$(next J) – t_{HDDx}(SOP)

Low-speed timings are determined in the same way for:
t_{LHDD}, t_{LDHJ1}, t_{LDJH2}, t_{LUHJ1}, t_{LUJH2}, and t_{LSOP}

Figure 3-16. Hub EOP Delay and EOP Skew





EOP Delay:
$t_{FEOPD} = t_{EOPy} - t_{HDDx}$
(t_{EOPy} means that this equation applies to t_{EOP-} and t_{EOP+})

EOP Skew:
$t_{FHESK} = t_{EOP+} - t_{EOP-}$

Low-speed timings are determined in the same way for:
t_{LEOPD} and t_{LHESK}

Figure 3-17. USB Differential Data Jitter for Low-/Full-speed

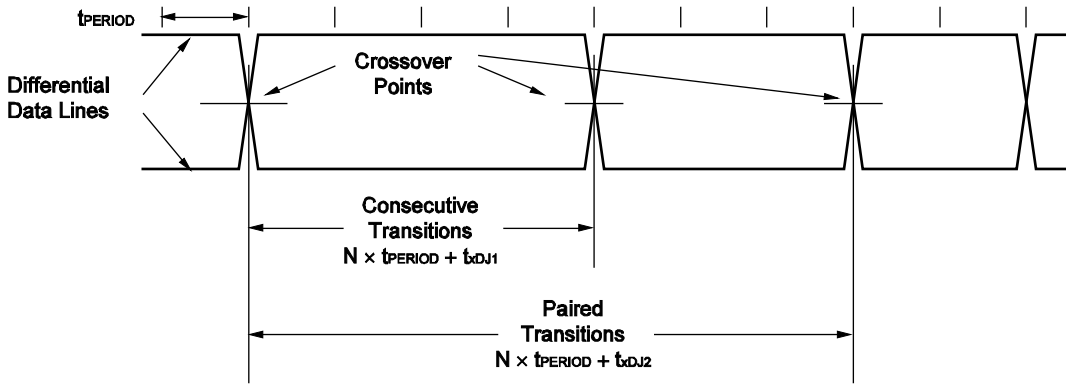


Figure 3-18. USB Differential-to-EOP Transition Skew and EOP Width for Low-/Full-speed

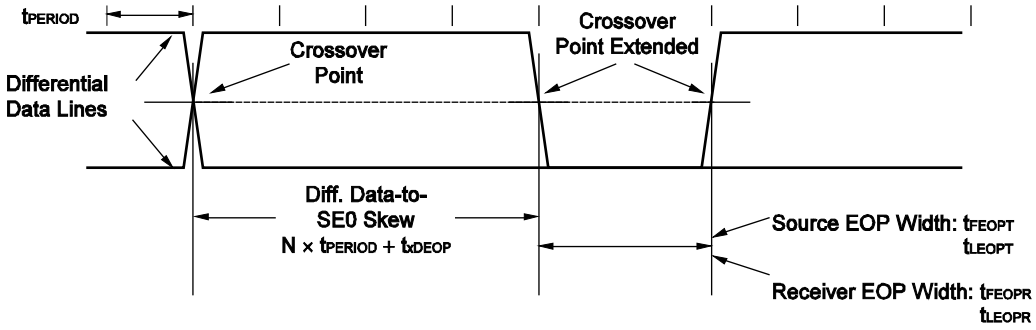


Figure 3-19. USB Receiver Jitter Tolerance for Low-/Full-speed

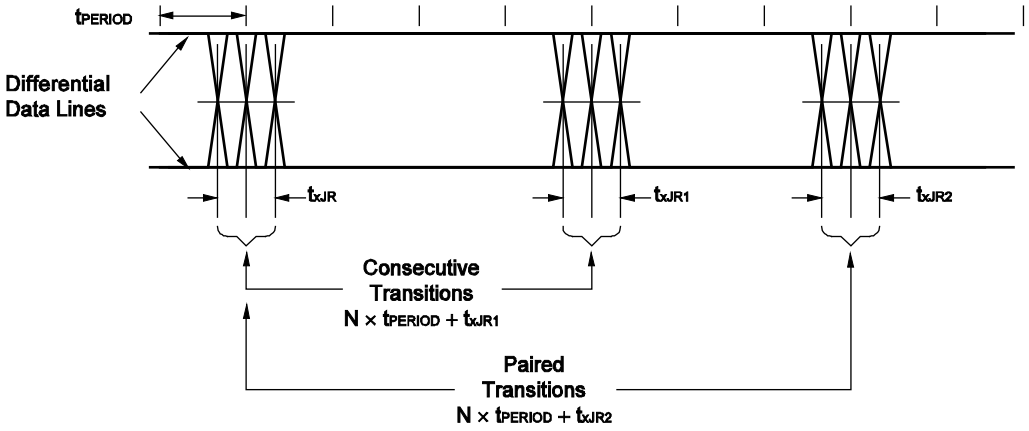


Figure 3-20. Low-/Full-speed Disconnect Detection

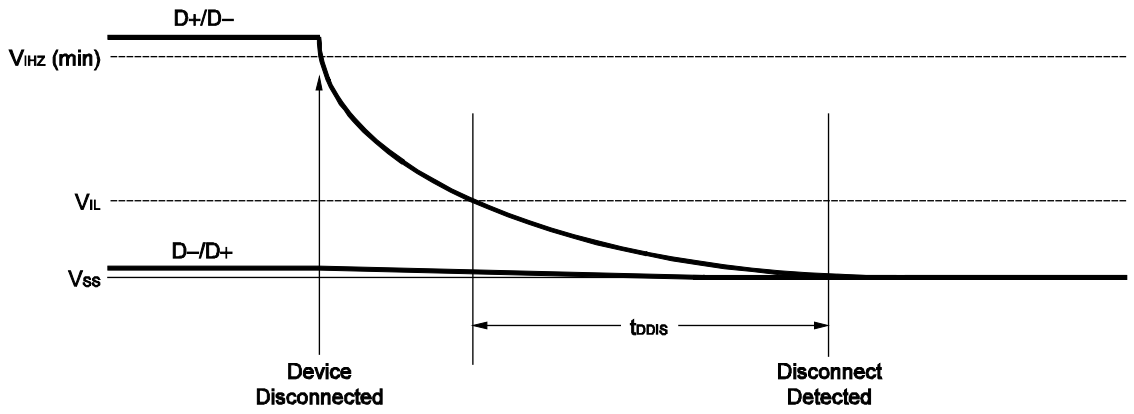
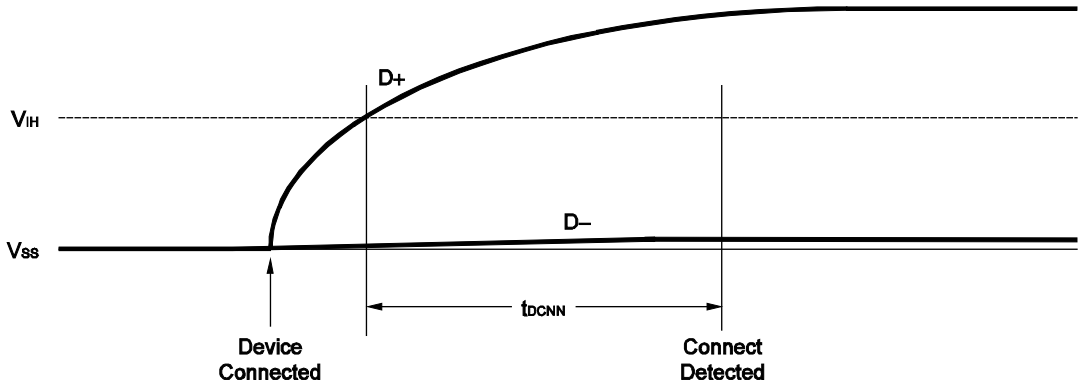


Figure 3-21. Full-/High-speed Device Connect Detection

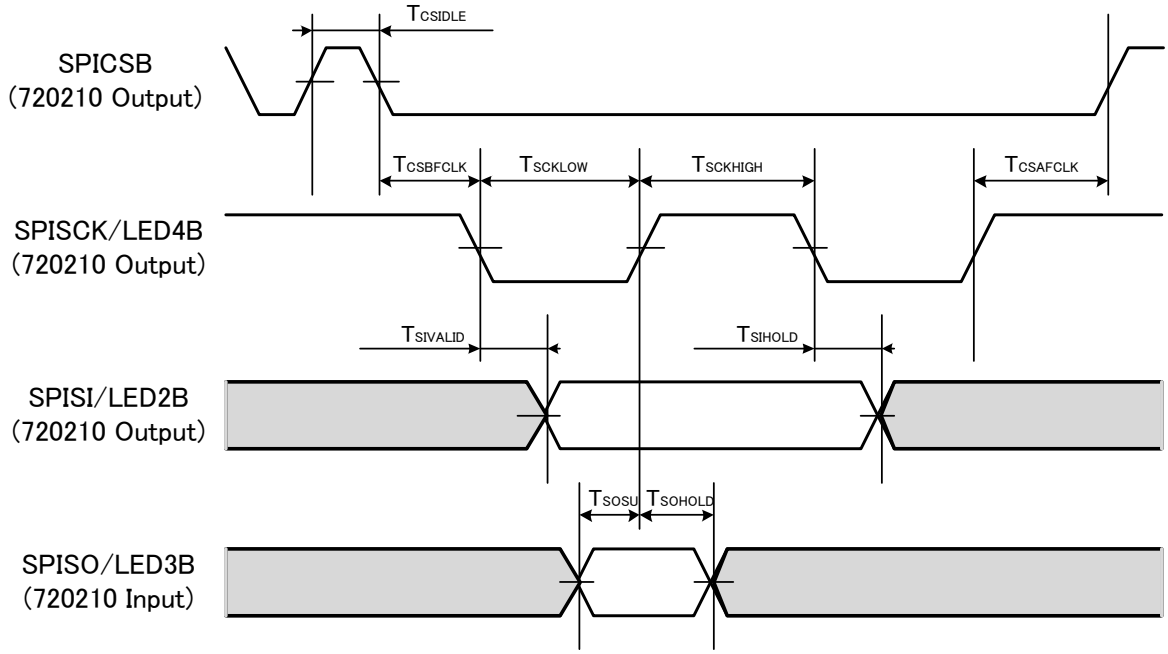


3.8.6 SPI Type Serial ROM Interface

Table 3-23. SPI Type Serial ROM Interface Signals Timing (SPI Mode 0)

Parameter	Symbol	Min.	Max.	Units
SPISCK/LED4B Clock Frequency		-	2.0	MHz
Chip Select idle time	T_{CSIDEL}	500	-	ns
Chip Select assertion time before clock	$T_{CSBFCLK}$	250	-	ns
Chip Select deassertion time after clock	$T_{CSAFCLK}$	250	-	ns
Clock pulses width Low	T_{SCKLOW}	250	-	ns
Clock pulses width High	$T_{SCKHIGH}$	250	-	ns
SPISI/LED2B validate time from SPISCK/LED4B falling edge	$T_{SIVALID}$	-	10	ns
SPISI/LED2B hold time from SPISCK/LED4B falling edge	T_{SIHOLD}	-10	10	ns
SPISO/LED3B setup time to SPISCK/LED4B rising edge	T_{SOSU}	5	-	ns
SPISO/LED3B hold time from SPISCK/LED4B rising edge	T_{SOHOLD}	5	-	ns

Figure 3-22. SPI Type Serial ROM Signal Timing



3.9 Power Consumption

Table 3-24. Power Consumption of μPD720210 (without on-chip regulators operating)

Parameter	Device connection	Condition	VDD10 line	VDD33 line	AVDD33 line	Units
Power Consumption	No host connection	Hub is not connected to host controller.	4.4	0.1	0.1	mA
	Suspend	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub goes into U3 state.	13.4	0.3	1.5	mA
	1 device	Hub is connected to host controller both with SuperSpeed and HighSpeed. Only one device is connected on the port.				
		Low-speed data transfer on the port.	28.3	23.0	11.8	mA
		Full-speed data transfer on the port.	30.5	24.8	12.3	mA
		High-speed data transfer on the port.	32.1	54.4	10.9	mA
		SuperSpeed transfer on the port. **Note**	288.1	1.8	11.0	mA
	2 devices	Hub is connected to host controller both with SuperSpeed and HighSpeed. Two devices are connected on the ports.				
		High-speed data transfer on the both ports.	34.3	73.2	11.1	mA
		SuperSpeed transfer on the both ports. **Note**	403.1	1.8	11.0	mA
	3 devices	Hub is connected to host controller both with SuperSpeed and HighSpeed. Three devices are connected on the ports.				
		High-speed data transfer on the three ports.	36.6	91.9	11.3	mA
		SuperSpeed transfer on the three ports. **Note**	518.1	1.8	11.0	mA
	4 devices	Hub is connected to host controller both with SuperSpeed and HighSpeed . Four devices are connected on the ports.				
		High-speed data transfer on the four ports.	38.3	110.7	11.6	mA
		SuperSpeed transfer on the four ports. **Note**	633.0	1.8	11.0	mA
	4 SS hubs with SS and HS devices	Hub is connected to host controller both with SuperSpeed and HighSpeed . Four SuperSpeed hubs are connected on all ports under SS and HS data transfer.	658.4	103.5	20.8	mA

Typical condition (T_A = 25°C, V_{DD33} = 3.3 V, V_{DD10} = 1.05 V)

Note: U1/U2 is enabled in this condition.

Table 3-25. Power Consumption of μPD720210 (with on-chip regulators operating)

Parameter	Device connection	Condition	Total Power **Note2**	Units
Power Consumption	No host connection	Hub is not connected to host controller.	26.3	mW
	Suspend	Hub is connected to host controller both with SuperSpeed and HighSpeed, hub goes into U3 state.	54.8	mW
	1 device	Hub is connected to host controller both with SuperSpeed and HighSpeed. Only one device is connected on the port.		
		Low-speed data transfer on the port.	235.5	mW
		Full-speed data transfer on the port.	245.1	mW
		High-speed data transfer on the port.	390.7	mW
		SuperSpeed transfer on the port. **Note1**	523.3	mW
	2 devices	Hub is connected to host controller both with SuperSpeed and HighSpeed. Two devices are connected on the ports.		
		High-speed data transfer on the both ports.	488.4	mW
		SuperSpeed transfer on the both ports. **Note1**	732.5	mW
	3 devices	Hub is connected to host controller both with SuperSpeed and HighSpeed. Three devices are connected on the ports.		
		High-speed data transfer on the three ports.	586.1	mW
		SuperSpeed transfer on the three ports. **Note1**	920.8	mW
	4 devices	Hub is connected to host controller both with SuperSpeed and HighSpeed . Four devices are connected on the ports.		
		High-speed data transfer on the four ports.	683.9	mW
		SuperSpeed transfer on the four ports. **Note1**	1169.5	mW
	4 SS hubs with SS and HS devices	Hub is connected to host controller both with SuperSpeed and HighSpeed . Four SuperSpeed hubs are connected on all ports under SS and HS data transfer.	1765.6	mW

Typical condition (T_A = 25°C, V_{DD33} = 3.3 V, V_{DD10} = 1.05 V)

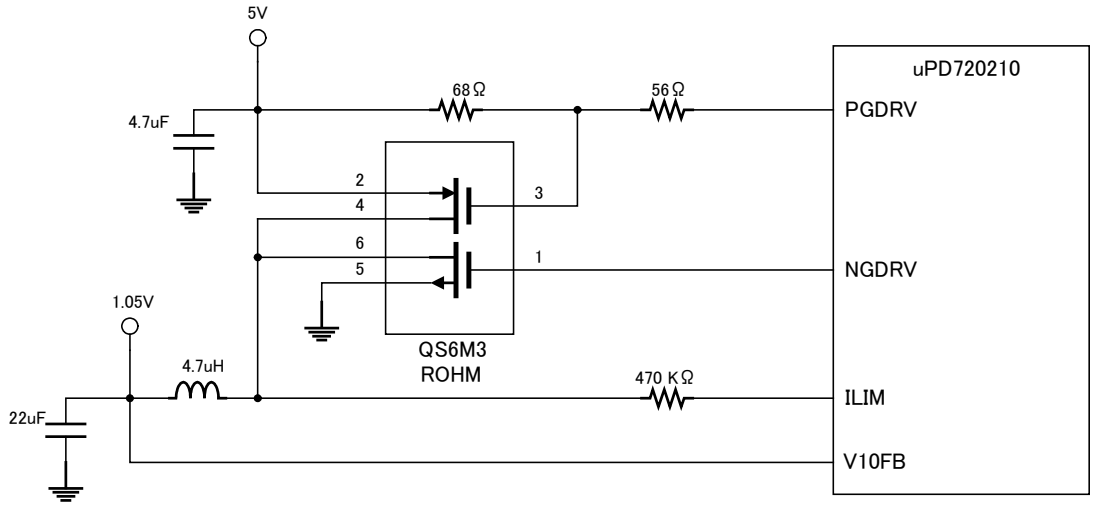
Notes 1. U1/U2 is enabled in this condition.

2. The values on this page do NOT represent the chip's pure power consumption. The values include power loss by external components, too.

Remark: Input voltage for on-chip regulators is 5 V.

3.10 Recommended FET for Internal Switching Regulator (5 V → 1.05 V)

Figure 3-23. Internal Switching Regulator Connection



It is necessary to use the correct Field Effect Transistor (FET) for the part of this switching regulator. The requirements for this FET are as follows.

1) Pch Vt: <2.5 V
2) P-ch gate capacitance (Ciss): <270 pF
3) Switching Period (On Time: Td+Tr, OffTime: Td+Tf) Nch<30 ns, Pch<65 ns
4) P-N One package, Single Die
5) Maximum Power Dissipation (Pd): >1.5 W
6) Drain Current (Id): Continuous >1.5 A
7) On Resistance (Rds): <170 mOHM (Vgs = 4.5 V)

Remarks 1. Recommended part for FET is QS6M3 (ROHM). Renesas is unaware of any other acceptable alternative device to the identified FET.
When QS6M3 (ROHM) is EOL (End of life), replacement part is QS6M4 (ROHM).
QS6M3 and QS6M4 are not pin compatible.

2. The 4.7 μH inductor should have DC resistance of 180 mΩ. Milli-Ohm resistor can be added to make 180 mΩ, if the inductor has less resistance.

Important:

Please note that there is no known acceptable alternate device for the ROHM QS6M3 and QS6M4 transistor noted in the μPD720210 User's Manual (R19UH0093), as shown in the excerpt above. The reason is that this transistor carries the main load current for the 1.05 V power used by the μPD720210 and may become excessively hot if an alternate transistor type is used. The heating can be severe enough to cause discoloration of the circuit board and possible damage to the end product and property unless the specified transistor is used as shown.

The only alternative is to use an external 1.05 V switching regulator instead of the on-chip regulator, as shown in the μPD720210 User's Manual (R19UH0093), Section 7.11.

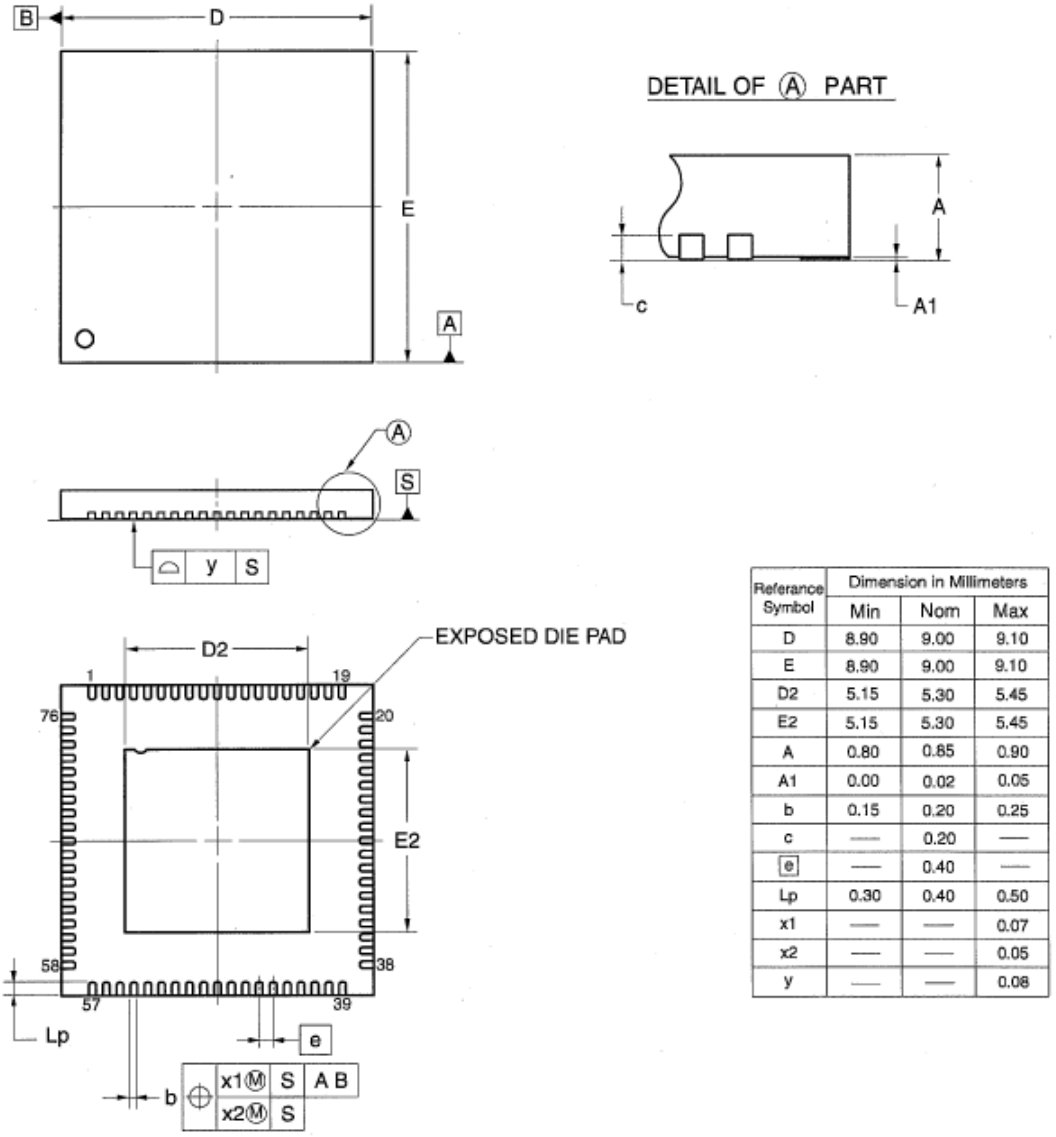
"Notwithstanding anything to the contrary, Renesas shall not be responsible for any loss or damage resulting from Customer's use or incorporation of any components, including any FET, used in the Customer's design, system or end product. Customer is solely responsible for any and all decisions concerning its design, the components used therein, its assembly and functionality."

4. Package Drawing

• *µ*PD720210K8-BAF-A / *µ*PD720210K8-BAF-M1-A

76-PIN QFN (9 x 9)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HVQFN76-9x9-0.40	PVQN0076LB-A	T76K8-40A-BAF	0.19



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	8.90	9.00	9.10
E	8.90	9.00	9.10
D2	5.15	5.30	5.45
E2	5.15	5.30	5.45
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	—	0.20	—
e	—	0.40	—
Lp	0.30	0.40	0.50
x1	—	—	0.07
x2	—	—	0.05
y	—	—	0.08

5. Recommended Soldering Conditions

The μPD720210 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact a Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Package Mount Manual

(https://www.renesas.com/en/document/oth/semiconductor-package-mount-manual)

• μPD720210K8-BAF-A / μPD720210K8-BAF-M1-A

76-pin QFN (9 x 9)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Peak package's surface temperature: 260°C, Reflow time: 60 seconds or less (220°C or higher), Maximum allowable number of reflow processes: 3, Exposure limit **Note**: 7 days (10 hours pre-backing is required at 125°C afterwards), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR60-107-3

Note: The Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

6. Revision History

Rev.	Date	Description	
		Page	Summary
0.10	Sep. 30, 2011	-	First Edition issued
0.11	Oct. 31, 2011	-	Pin Name changed. (U2DNx → U2DMx)
		-	Fig. 1-2 Changed. (names of Pin18 and Pin19)
0.12	Feb. 21, 2012	-	Part Number added
0.13	Feb. 22, 2012	-	Part Number updated
0.14	Mar. 16, 2012	-	Removed Package Drawing for future update
0.15	Apr. 26, 2012	3,5	Changed Block Diagram, Pin out, 1 V → 1.05 V
		6,35	Added Package Drawing
0.16	Aug. 31, 2012	1	Feature set updated
		6	LDO, RREF pin connection added
		7	LED description added
		9	LED description added
		12	LDO related values added
		15	LDO and Sw-Regulator's cut-off current values added
		16	Power sequence added
		18	Reset and Clock timing added
		30	Hub Parameter removed
		30	SPI interface timing added
		31	Power consumption added
		32	Power consumption added
		33	Package dimensions added
		34	Soldering conditions added
1.00	Sep. 26, 2012	-	Document promoted from Preliminary Data to full Data (Document No. R19DS0070)
1.01	Jan. 21, 2013	1	USB Logo, EuP support, and Apple products charging added
		6	Pin name change (V33IN → AVDD33R)
		6	Note for selection of FET added
		12	Ratings for USB3.0 differential signals added
		18	Typo rectified (PONRSTB → RESETB)
		33	Requirements for FET added
2.00	May. 26, 2014	-	Added the feature to section 1.1 Features
		-	Added the Operating Temperature to section 1.3 Ordering Information
		-	Modified the pin description in Section 2 PIN FUNCTION
		-	Modified the typo in section 3.1 Buffer List and all sections
		-	Delete Note description of Table 3-5
		-	Modified the parameter description of Table 3-12 NRDRST Output and CLKOUT Signal Timing.
		-	Added the description for clock output function in section 3.8.2 Reset and Clock Timing
		-	Modified the Figure 3-7 Power On Reset timing
		-	Modified the Min. value of Table 3-11 Power On Reset (RESETB) Timings (100 ms -> 10 ms)
		-	Modified the Figure 3-24 Internal Switching Regulator Connection
		-	Added the package information in Chapter 4

Rev.	Date	Description	
		Page	Summary
3.00	Nov. 25, 2014	-	Modified the feature to section 1.1 Features
		-	Modified the Function to section 2. Pin Function as below pins LED1B/SUSPEND SPISCK/LED4B SPICSB SPISO/LED3B SPISI/LED2B
		-	Modified to Table 3-9
		-	Modified typo of Section 3.8.2
		-	Modified to Section 3.10
4.00	Sep 16, 2015	29,30	Deleted the following parameters t_{SIGATT}, t_{ATTDB}, $t_{SUSAVGI}$, t_{RSMRCY}, t_{RSTRCY}
		35	Deleted Figure 3-22 “Power-on and Connection Events Timing”
		41	Modified the URL
5.00	Mar 08, 2024	-	Added new part number
		6	Updated the descriptions for V50IN/V33OUT pins in section 2.1
		-	Removed unnecessary cross reference.
6.00	Jul 11, 2025	1	Moved Section 1 Overview to Top Page Description and Section 1.1 Features to Top Page Features.
		2	Added Application Block Diagram to Top page.
		-	Added Contents, List of Figures, and List of Tables.
		7	Modified typo in Section 1.2.
		9	Modified description for SS-PHY, VBUS Control, and LDO in Table 1-1.
		11	Modified description in Chapter 2 and typos in Section 2.1.
		17	Modified description in Table 2-8.
		-	Unified section x.x to Section x.x.
		-	Changed some Style in Chapter 2.
		-	Modified the Document number referred.
		-	Added table numbers in Chapter 2.
		-	Added links to Chapter, Section, Figure, and Tables.
		-	Modified titles for Section 2.2, 2.4, 2.5, and 2.6.
		21	Modified the typo in Table 3-6.
		25	Modified the typo in Table 3-10.
		26	Modified the typo in Section 3.8.2.
		27	Modified the explanation for parameters in Table 3-14.
		31	Modified the typo in Table 3-20.
		39	Modified the typo in Table 3-23.
		44	Modified the URL in Chapter 5.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

Trademarks

USB Type-C® and USB-C® are trademarks of USB Implementers Forum. Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.