RClamp0544P
Low Capacitance RailClamp®
4-Line Surge and ESD Protection

PROTECTION PRODUCTS

Description

RailClamp® TVS arrays are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data lines from over-voltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

RClamp0544P has a maximum capacitance of only 0.22pF and extremely low insertion loss, which allows it to be used on high speed lines such as HDMI 2.1 and USB 3.2. Each device will protect four lines operating at 5 volts.

RClamp0544P is in a DFN 2.5 x 1.0 x 0.55mm 10-Lead package. The flow- through package design simplifies PCB layout.

Features

- Transient Protection to
  - IEC 61000-4-2 (ESD): ±20 kV (Air), ±8kV (Contact)
  - IEC 61000-4-4 (EFT): 40A (5/50ns)
  - IEC 61000-4-5 (Lightning): 6.5A (8/20µs)
- Protects four High-Speed Data Lines
- Package design optimized for high speed lines
- Working voltage: 5V
- Low clamping voltage
- Low maximum capacitance: 0.22pF
- Solid-State Silicon-Avalanche Technology

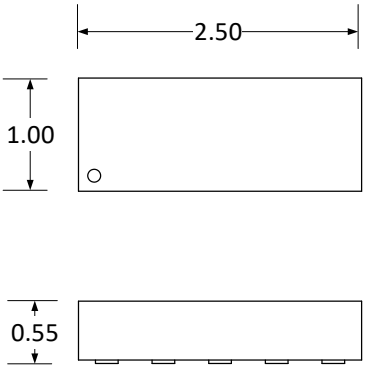
Mechanical Characteristics

- Package: DFN 2.5 x 1.0 x 0.55mm 10-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-Free
- Marking: Marking Code + Date Code
- Packaging: Tape and Reel

Applications

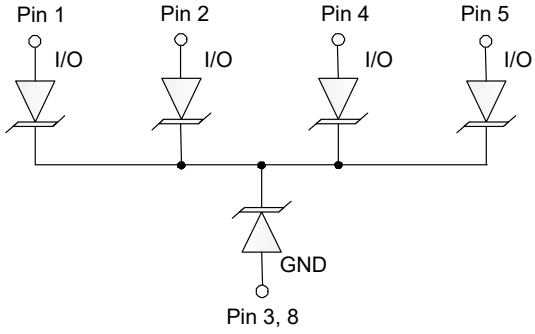
- HDMI 2.1/2.0
- USB 3.2 Gen 1/ Gen 2
- USB Type-C
- DisplayPort
- LVDS Interfaces

Nominal Dimension



Nominal Dimensions in mm

Functional Schematic



Device Schematic

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PP}	42	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	6.5	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(1)	V_{ESD}	±8 ±20	kV
Junction Temperature and Operating Temperature	T_J & T_{OP}	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to GND				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA, Any I/O pin to GND		5.5	7.7	10.0	V
Reverse Leakage Current	I_R	V_{RWM} = 5V			20	100	nA
Clamping Voltage (2)	V_C	I_{PP} = 6.5A, tp = 1.2/50µs (Voltage), 8/20µs (Current) Combination Waveform, R_S = 2 Ω			4.3	6.5	V
ESD Clamping Voltage(3)	V_C	tp = 0.2/100ns (TLP) Any I/O pin to GND	I_{PP} = 4A		3.2		V
			I_{PP} = 16A		5.5		
Dynamic Resistance(3),(4)	R_{DYN}	tp = 0.2/100ns (TLP)			0.19		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz, Any I/O pin to GND			0.19	0.22	pF

Notes:

(1) ESD gun return path connected to Ground Reference Plane (GRP)

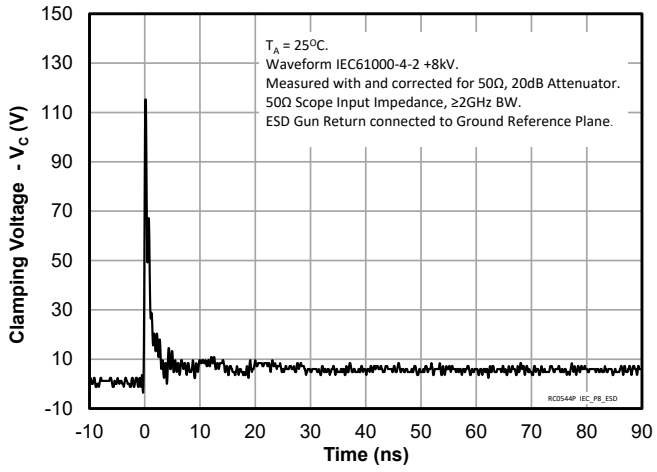
(2) Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, R_S = 2Ω. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

(3) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.

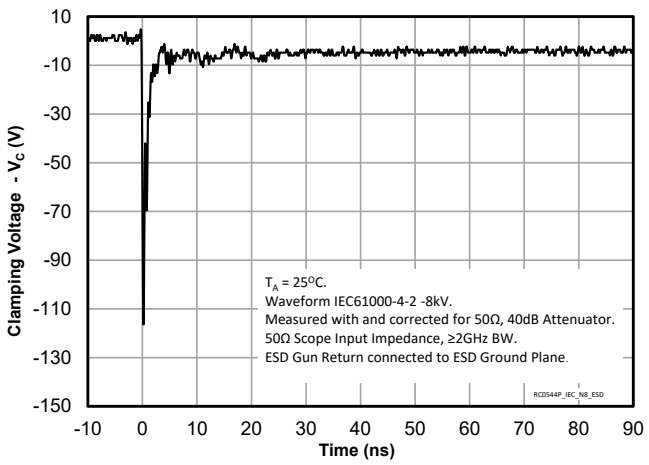
(4) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

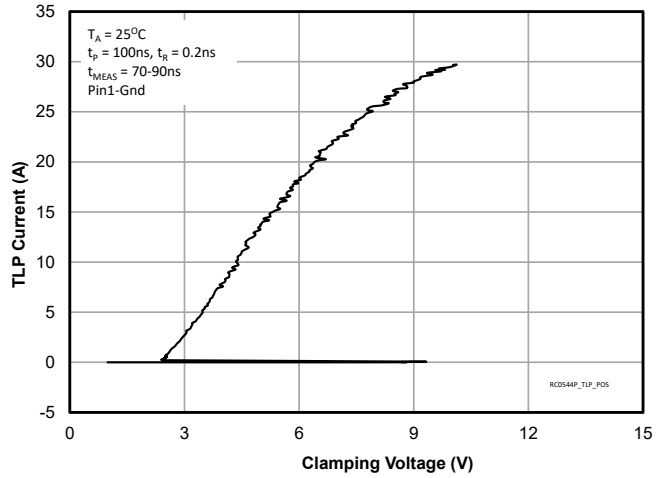
ESD Clamping (+8kV Contact per IEC 61000-4-2)



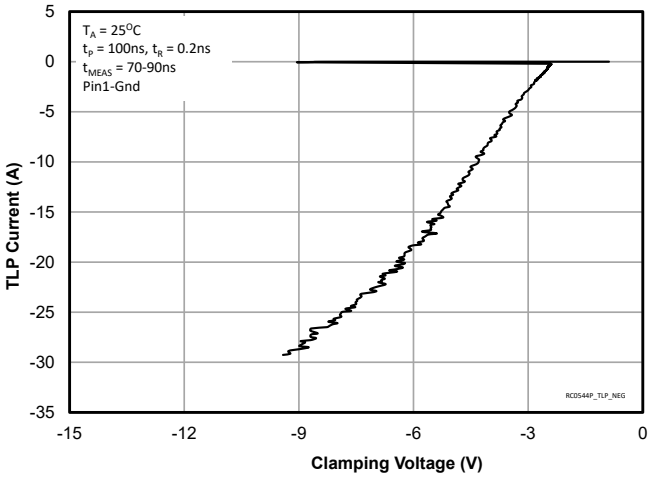
ESD Clamping (-8kV Contact per IEC 61000-4-2)



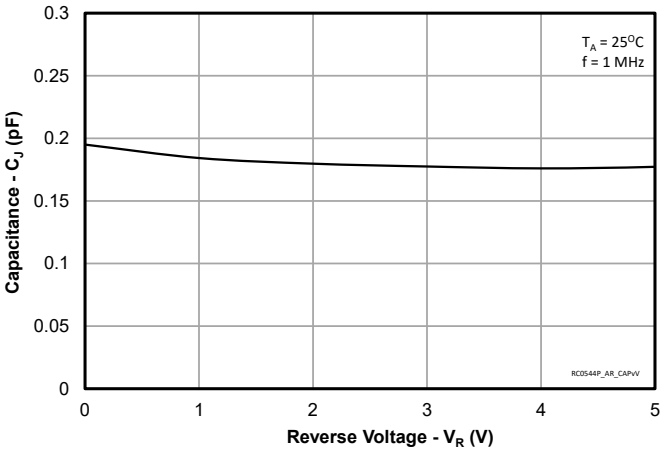
TLP Characteristic (Positive Pulse)



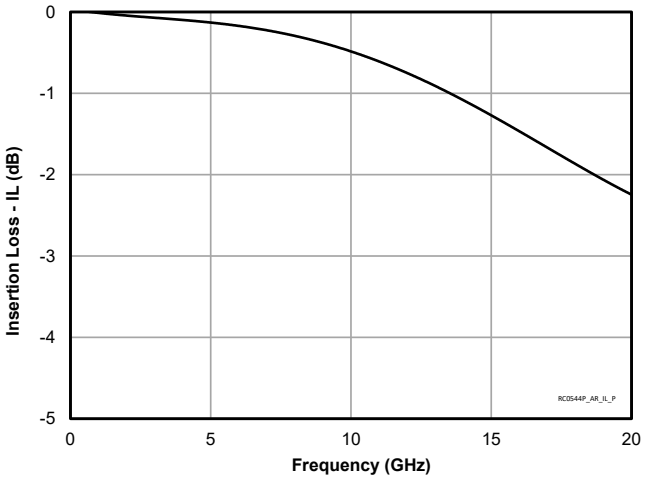
TLP Characteristic (Negative Pulse)



Capacitance vs. Reverse Voltage



Insertion Loss (Line to GND)



Applications Information

Layout Guidelines for Optimum ESD Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible. This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible. Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.

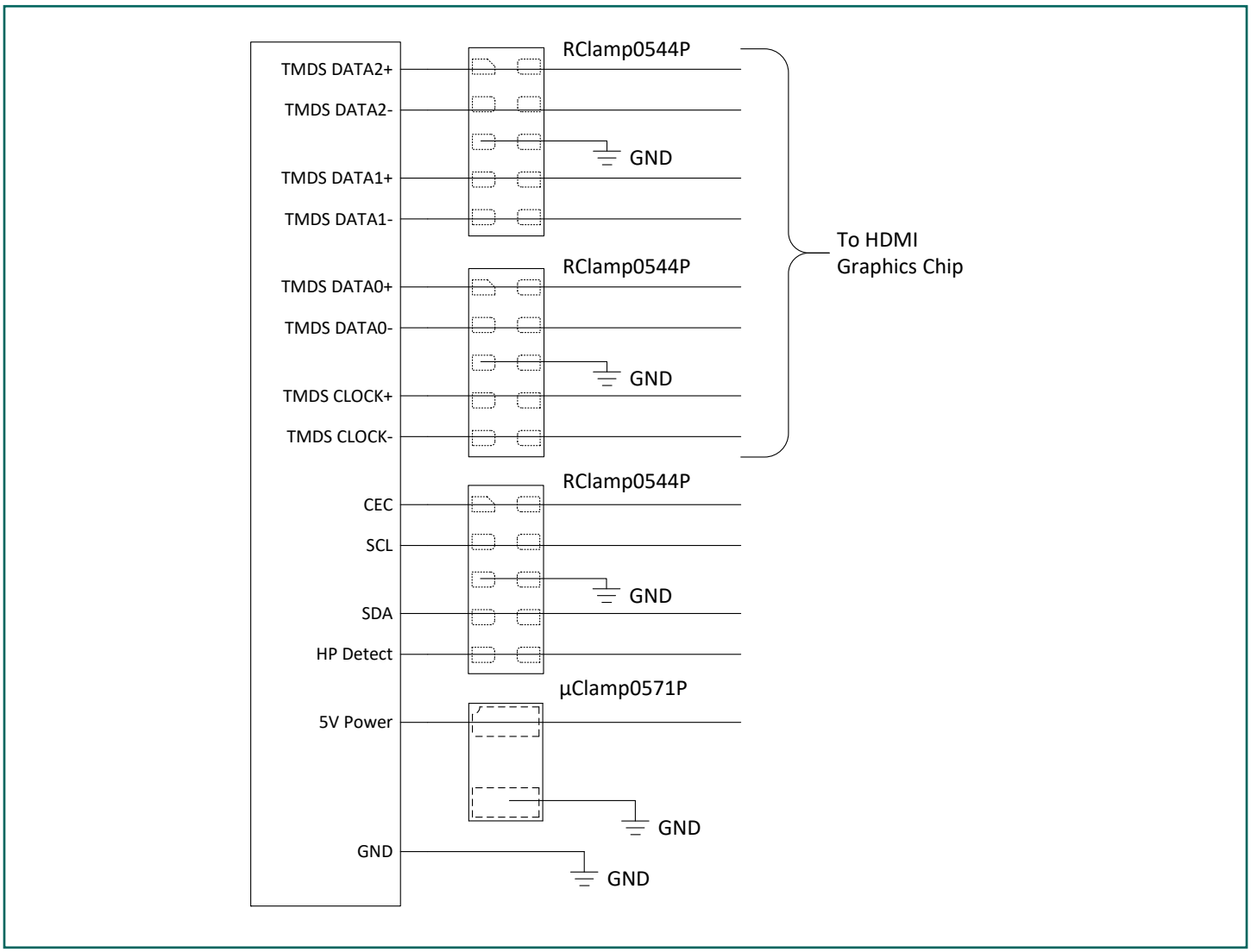


Figure 4. HDMI Application using RClamp0544P

Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 2. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm - 0.125mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. Due to the small aperture size, a solder paste with Type 4 or smaller particles is recommended. Assuming a 125um thick stencil, the aperture dimensions shown will yield an area ratio of 0.72 for the small pads and 1.25 for the large.

Recommended Stencil Design

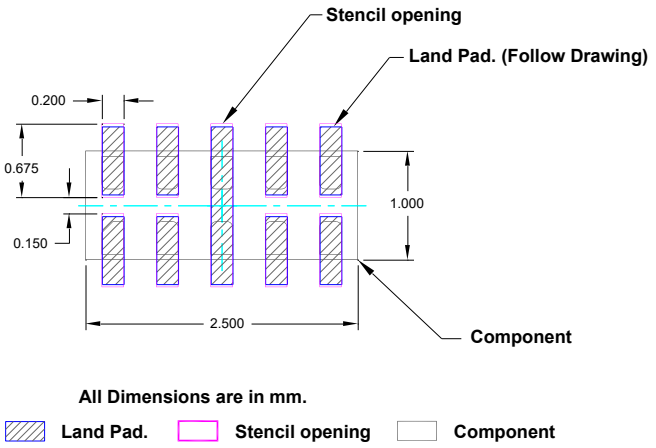
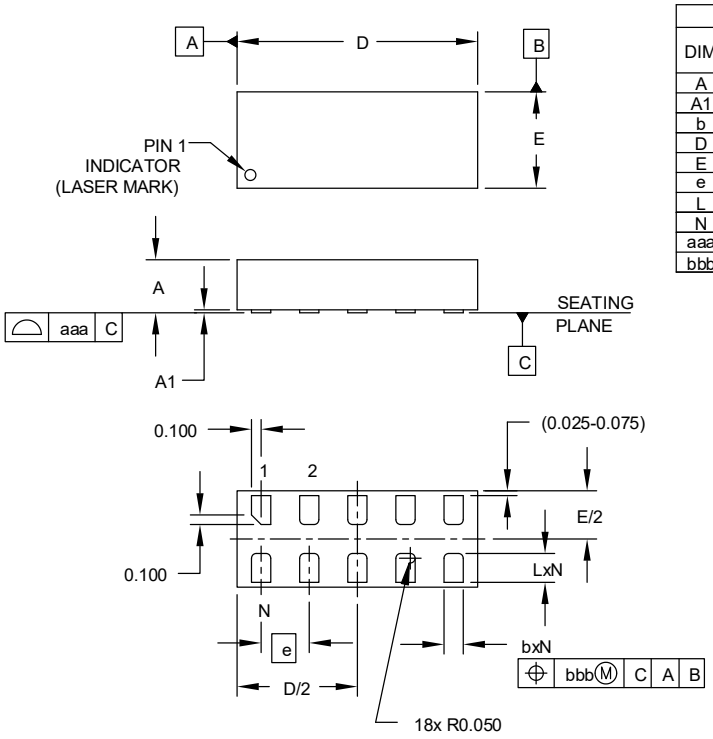


Table 2 - Recommended Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular
Solder Stencil Thickness	0.100mm (0.004") - 0.125mm (0.005")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - DFN 2.5 x 1.0 x 0.55mm 10-Lead

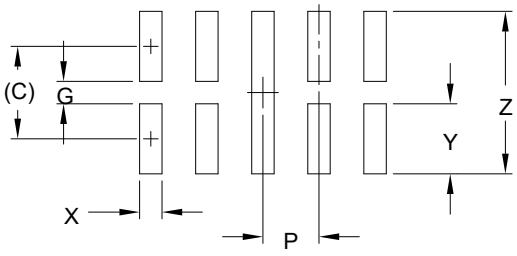


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.03	0.05
b	0.15	0.20	0.25
D	2.45	2.50	2.575
E	0.95	1.00	1.075
e	0.50 BSC		
L	0.25	0.30	0.35
N	10		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - DFN 2.5 x 1.0 x 0.55mm 10-Lead

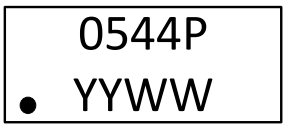


DIMENSIONS	
DIM	MILLIMETERS
C	(0.825)
G	0.20
P	0.50
X	0.20
Y	0.625
Z	1.45

NOTES:

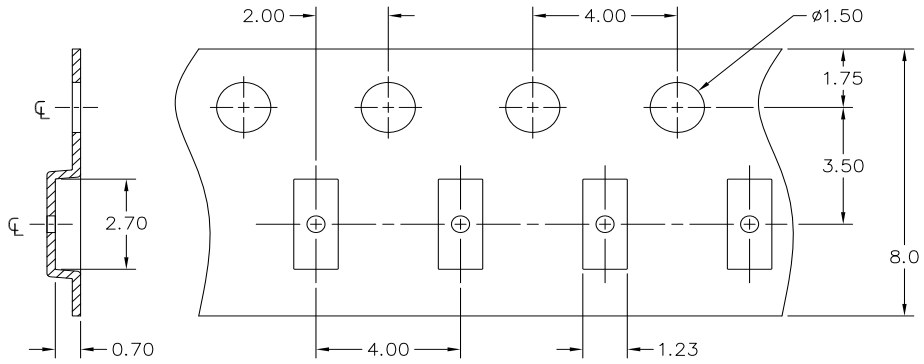
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

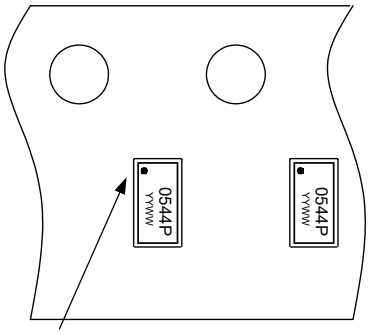


Notes: Dot indicates pin 1 location

Tape and Reel Specification (4mm Pitch)

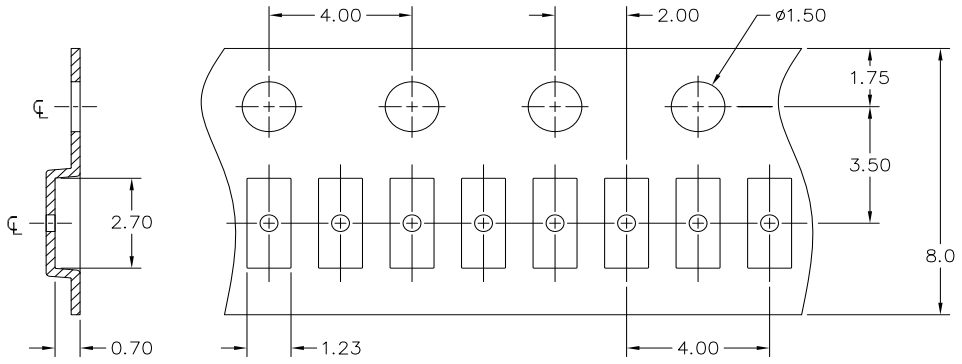


Note: All dimensions are nominal dimensions in mm.

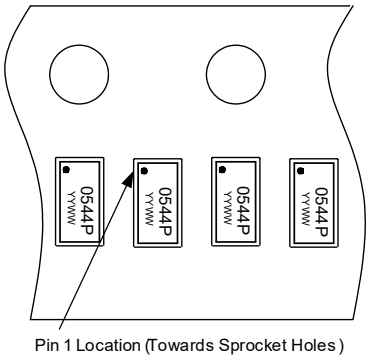


Pin 1 Location (Towards Sprocket Holes)

Tape and Reel Specification (2mm Pitch)



Note: All dimensions are nominal dimensions in mm.



Ordering Information

Part Number	Qty per Reel	Pocket Pitch	Reel Size
RClamp0544P.A	5,000	4mm	7″
RClamp0544P.N	10,000	2mm	7″
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