AP1010

18V 2ch H-Bridge Motor Driver IC

1. General Description

The AP1010 is a 2ch H-Bridge motor driver compatible with motor operating voltage 18V and can drive two DC motors or one stepping motor. The protection circuit has under voltage lockout circuit, thermal shutdown circuit, and overcurrent protection circuit, and overcurrent protection circuit can be disabled with the DIS OCP terminal. The package adopts a small 16-pin QFN package and contributes to downsize Printed Circuit Board.

2. Features

• Motor Operating Voltage Range	6.0V～18V (Control power supply is unnecessary)
• Maximum Output Current (DC)	0.7A @Ta=25°C
• H-Bridge On-Resistance	RON(TOP+BOT) = 1.1Ω @Ta=25°C
• Parallel Connection Possible	
• Under Voltage Lockout Circuit	
• Thermal Shutdown Circuit	
• Overcurrent Protection Circuit	Overcurrent protection circuit is disabled when DIS OCP terminal = “H”
• Operating Temperature Range	-30°C～85°C
• Package	16-pin QFN (3mm×3mm)

3. Table of Contents

4. Block Diagram

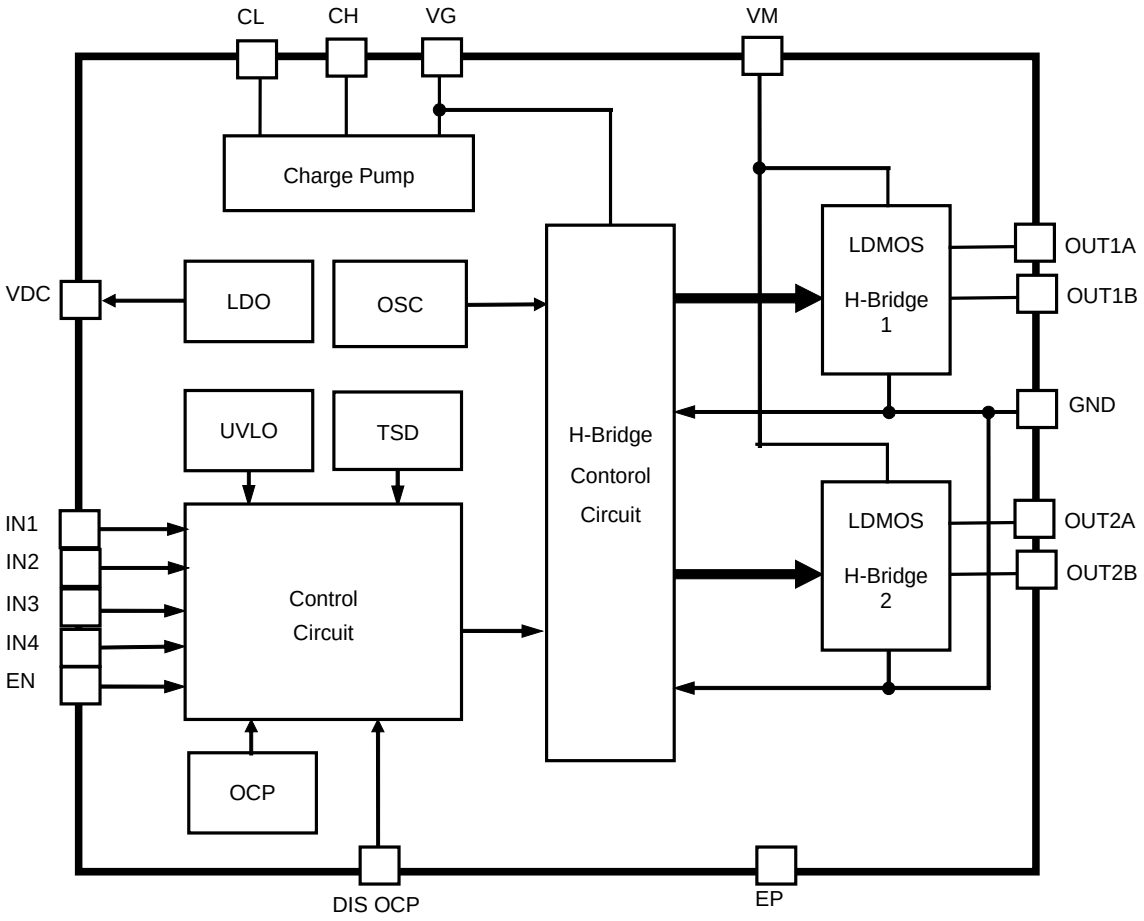
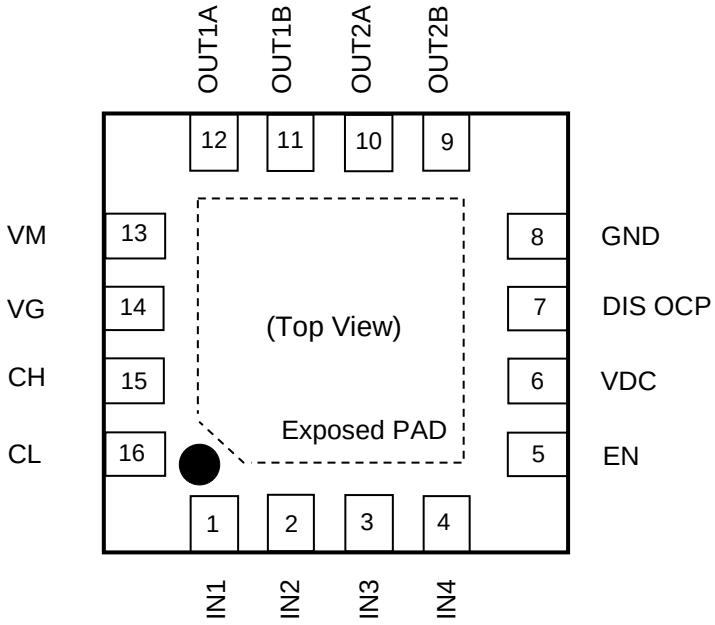


Figure 1. Block Diagram

5. Pin Configurations and Functions

5.1 Pin Configurations



5.2 Functions

Pin Number	Pin Name	I/O	Functions	Notes
1	IN1	I	Control Signal Input	Built-in 200kΩ Pull-down
2	IN2	I	Control Signal Input	Built-in 200kΩ Pull-down
3	IN3	I	Control Signal Input	Built-in 200kΩ Pull-down
4	IN4	I	Control Signal Input	Built-in 200kΩ Pull-down
5	EN	I	Enable Signal Input	Built-in 200kΩ Pull-down
6	VDC	O	Coupling terminal for internal power supply	Connect a 1.0 μF capacitor between VDC pin and GND.
7	DIS OCP	I	Over current protection function terminal	Built-in 200kΩ Pull-down
8	GND	P	Ground	
9	OUT2B	O	Motor Driver Output	
10	OUT2A	O	Motor Driver Output	
11	OUT1B	O	Motor Driver Output	
12	OUT1A	O	Motor Driver Output	
13	VM	P	Motor Power Supply	
14	VG	I/O	Connect Terminal for Stabilizing Capacitor.	
15	CH	I/O	Connect Terminal for Charge Pump Capacitor.	
16	CL	I/O	Connect Terminal for Charge Pump Capacitor.	
EP	EP	P	Ex-posed Pad	(Note 2)

Note 1. I(Input pin)、O(Output pin)、 P(Power pin)、I/O(Input/Output pin)
Note 2. Exposed PAD must be connected to GND.

6. Absolute maximum Ratings

Parameter	Symbol	min	max	Unit	Condition
Motor Operating Voltage	VM	-0.3	19	V	
Input Terminal Voltage 1 (IN1, IN2, IN3, IN4, EN)	Vterm1	-0.3	6.0	V	
Input Terminal Voltage 2 (DIS OCP)	Vterm2	-0.3	V_{DC}	V	
VM Level Terminal Voltage (OUTnA, OUTnB)	Vterm3	-0.3	VM	V	
CH, VG Terminal Voltage	Vterm4	-0.3	24	V	
VDC Terminal Voltage	VDC	-0.3	6.0	V	
CL Terminal Voltage	VCL	-0.3	V_{DC}	V	
Maximum Output Current	Iload	-	0.7	A	Ta=25°C, 1ch (Note 4)
		-	0.5	A	Ta=85°C, 1ch (Note 4)
			0.5	A/ch	Ta=25°C, 2ch simultaneously (Note 4)
		-	0.35	A/ch	Ta=85°C, 2ch simultaneously (Note 4)
Power Dissipation	PD	-	1.83	W	Ta=25°C (Note 4, Note 5)
Junction Temperature	Tj	-	150	°C	
Storage Temperature	Tstg	-40	150	°C	

Note 3. All voltages are for GND = 0V.
Note 4. For Power Dissipation, the output current rating may be limited by duty cycle, Ta, and PCB board heat sinking design.
Note 5. A 2-layer board is used. $R_{\theta JA}$ = 60°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

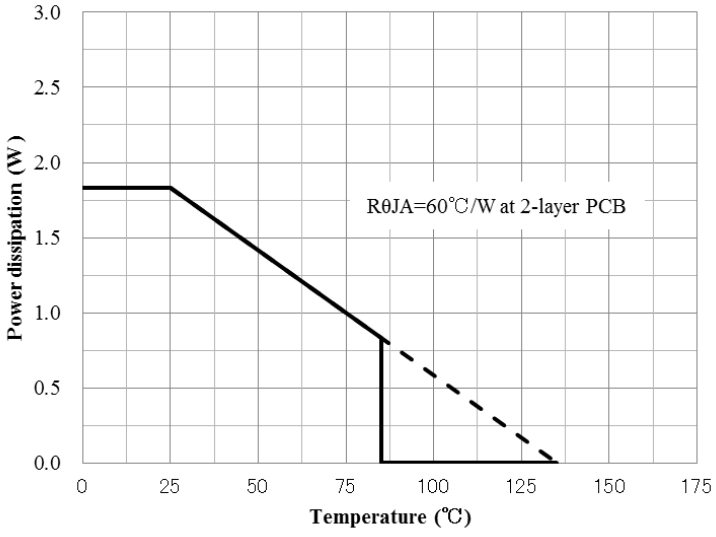


Figure 2. Maximum Power Dissipation

7. Recommended Operating Conditions

(Ta=25°C, unless otherwise specified.)

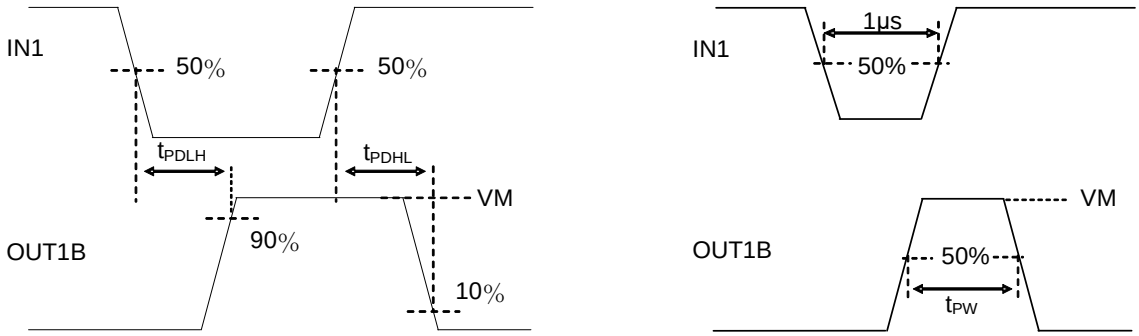
Parameter	Symbol	min	typ	max	Unit
Motor Operating Voltage	VM	6.0	12	18	V
Logic Terminal Voltage	VIO	0		5.5	V
Input Frequency Range	F_{in}	-	-	200	kHz
Operating Temperature Range	Ta	-30	-	85	°C

8. Electrical Charateristics

(Ta=25°C, VM=12V, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Quiescent Current						
VM Quiescent Current at the time of Power Save	I_{VMOFF}	IN=All "L", EN="L"	-	-	10	μA
VM Quiescent Current at the time of Operating	I_{VM}	IN1=IN3="H"/"L" 200kHz, IN2=IN4="L"/"H" 200kHz, EN="H", Open between OUTA and OUTB	-	1.8	3.0	mA
Charge Pump						
Charge Pump Voltage	VG	VG=VM+V_{DC}, Iload=0A	-	-	17	V
Charge Pump Rise Time	tVGON	EN="L"→"H", C_{VG}=0.1uF	-	0.6	3.0	ms
H-Bridge						
Driver on resistance (H-Bridge High+Low)	R_{ON}	$I_{load\ (1ch/2ch)}$ = 0.1A/0.1A	-	1.1	1.7	Ω
H-Bridge Driver Body diode forward voltage	V_F	I_F = 100mA	-	0.8	1.2	V
Delay Time						
Output Delay Time ("L"→"H")	t_{PDLH}	Connected to 1kΩ between OUTA and OUTB. (Figure 3)	-	-	1.0	μs
Output Delay Time ("H"→"L")	t_{PDHL}		-	-	1.0	μs
Output Pulse Width	t_{PW}	Connected to 1kΩ between OUTA and OUTB. Input Pulse Width : 1μs (Figure 3)	0.5	1.0	1.5	μs
Control Logic						
VDC Terminal Voltage	V_{DC}		4.2	4.65	5.0	V
Input High Level Voltage	V_{IH}		2.0	-	-	V
Input Low Level Voltage (EN)	V_{IL1}		-	-	0.4	V
Input Low Level Voltage (IN1, IN2, IN3, IN4, DIS OCP)	V_{IL2}		-	-	0.6	V
Input Pulse Rise Time	t_R		-	-	1.0	μs
Input Pulse Fall Time	t_F		-	-	1.0	μs
Pull-down resistance	R_{PD}		100	200	300	kΩ
Input Low Level Current	I_{IL}		-1.0	-	1.0	μA
Protection Circuit						
Under Voltage Detect Voltage	VM_{UV}		3.85	4.3	4.65	V
Thermal Shutdown Temperature (Note 7)	T_{TSD}		135	155	175	°C
Temperature Hysteresis (Note 7)	T_{TSDHYS}		-	30	-	°C
Overcurrent protection	I_{OCP}	DIS OCP="L"	1.3	2.6	3.9	A

Note 6. All above voltage is defined to GND=0V.
Note 7. Not tested under mass-production.



(a) Delay Time (IN2="H") (b) Pulse Width (IN2="H")

Figure 3. Timing Chart（Delay Time, Pulse Width）

9. Functional Descriptions

9.1 Operation Outline

Table 1. The relationship between input and output in each mode is as follows.

INPUT					OUTPUT				Mode
EN	IN1	IN2	IN3	IN4	OUT1A	OUT1B	OUT2A	OUT2B	
L	-	-	-	-	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Save(Note 8)
H	L	L	-	-	Hi-Z	Hi-Z	-	-	Standby
H	H	L	-	-	H	L	-	-	CW
H	L	H	-	-	L	H	-	-	CCW
H	H	H	-	-	L	L	-	-	Brake
H	-	-	L	L	-	-	Hi-Z	Hi-Z	Standby
H	-	-	H	L	-	-	H	L	CW
H	-	-	L	H	-	-	L	H	CCW
H	-	-	H	H	-	-	L	L	Brake

Note 8. Charge Pump Block and TSD, UVLO, OCP don't operate at the Power Save.
Note 9. After inputting "H" to the EN pin, input "H or L" to IN 1 - 4 pin.

9.2 Motor Driver Block Configuration

The Nch LDMOS FET is placed on both sides of the high side and the low side in the output stage, making it possible to apply a small package. Hi-side FET is driven by VG. VG = VM + V_{DC} is generated by the charge pump. Lo-side FET is driven by V_{DC}.

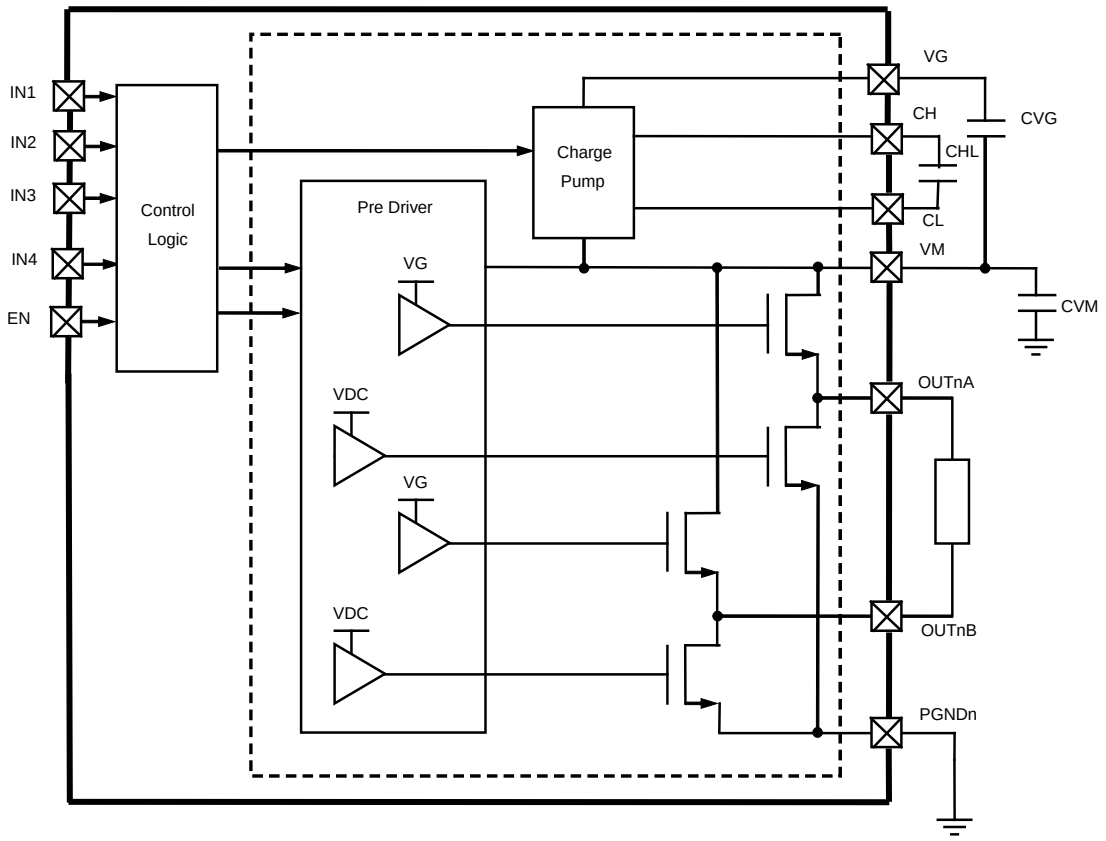


Figure 4. Driver Block Equivalent circuit

9.3 Protection Circuits

9.3.1 Under Voltage Lockout (UVLO)

If VM voltage is lower than 4.3V at the starting, the H-Bridge output is the Hi-Z.

9.3.2 Thermal Shutdown(TSD)

When the internal temperature of the IC reaches the specified temperature (T_{TSD}=155°C), and the H-Bridge driver outputs Hi-Z. When the internal temperature after the detection is lowered about 30°C (T_{TSDHYS}), the driver resumes operation.

Restart Temperature = T_{TSD} - T_{TSDHYS}

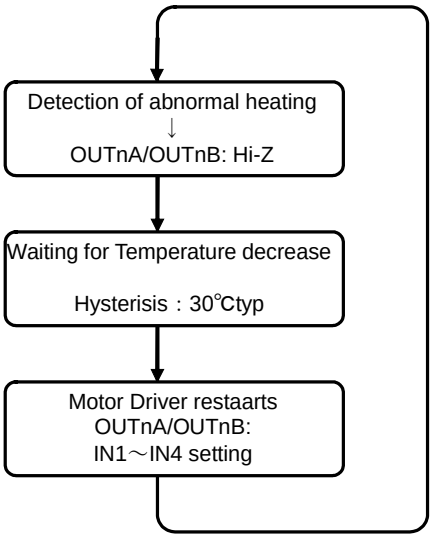


Figure 5. Detection of abnormal heating

9.3.3 Over current protection (OCP)

When the current of 2.6 A or more continues to flow to the H - Bridge driver for 10 µs, all H - Bridge driver outputs are set to Hi - Z, and automatically return after 200 ms.

Over current protection circuit can be used by setting the DIS OCP terminal to L level. When not using the overcurrent protection circuit, connect the DIS OCP terminal to the VDC terminal.

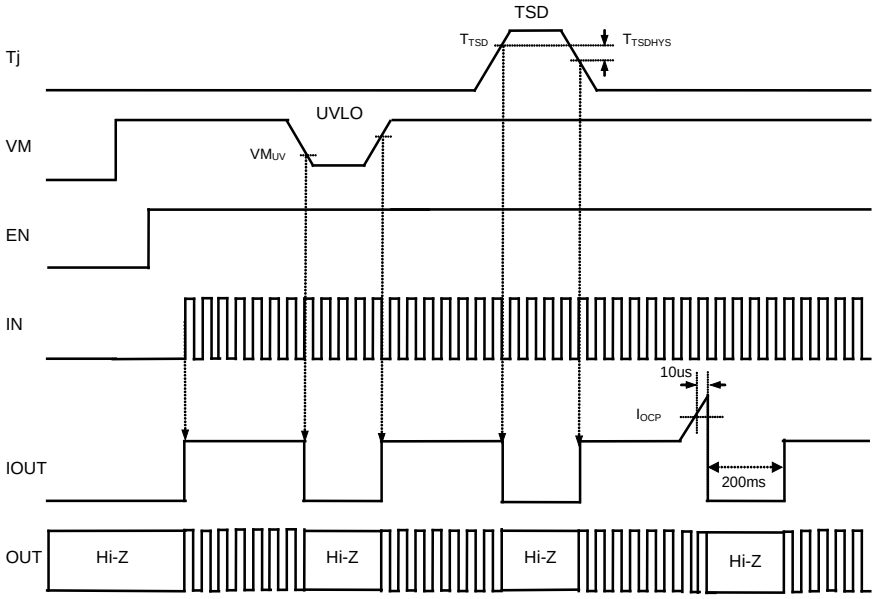
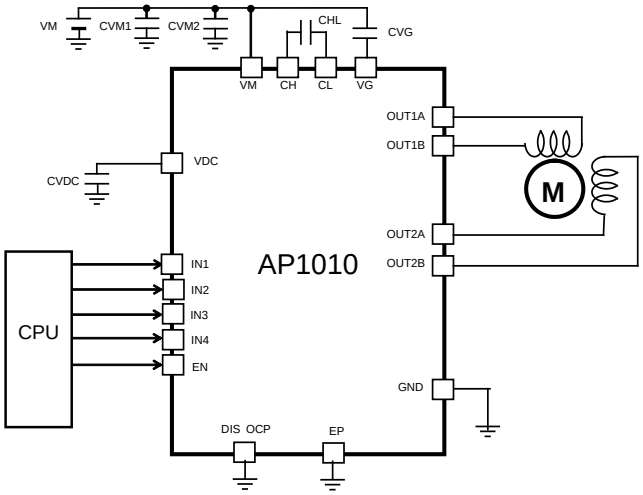


Figure 6. Protection Function Timing Chart

10. Recommended External Circuits

■ Driving Stepper Motor



■ Driving DC Motor

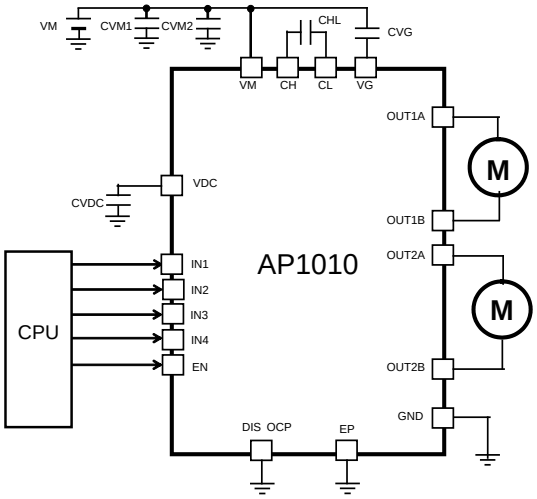


Figure 7. Recommended External Circuits

Table 2. Parts List

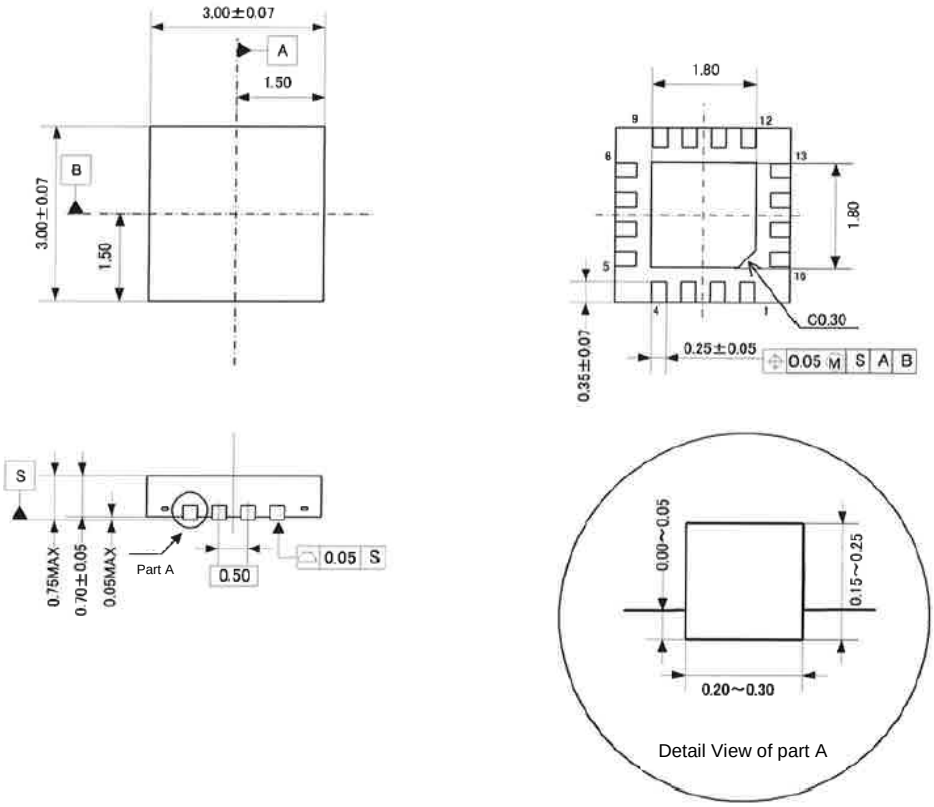
Items	Symbol	min	typ	max	Unit	Note
Motor driver power connection capacity(Decoupling capacitor)	CVM1	-	10	-	µF	(Note 10)
	CVM2	-	1	-	µF	
Charge pump capacity	CHL	0.047	0.1	0.22	µF	
	CVG	0.047	0.1	0.22	µF	
Internal power connection capacity (Decoupling capacitor)	CVDC	0.47	1.0	2.2	µF	

Note 10. Capacitance of CVM should be determined in consideration of the load current profile, the load capacitance, the line resistance and etc. of the actual system board.
Note 11. Please layout the large ground plane on the PCB.
Note 12. Please connect the exposed pad (heat sink) to the ground of the PCB.

11. Package

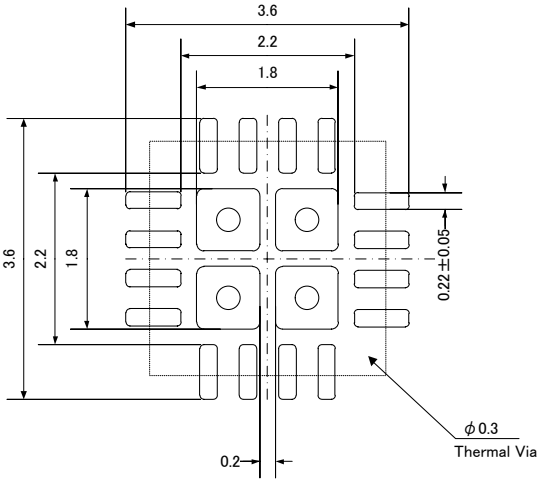
11.1 Outline Dimensions

・16-pin QFN (Unit : mm)



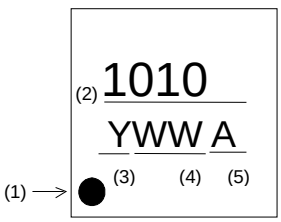
11.2 Recommended Land Pattern

・16-pin QFN (Unit : mm)



The optimum dimensions of the mount pad will vary depending on the substrate material, solder paste method, device accuracy, etc. In actual design, please optimize according to the situation.

11.3 Marking



(1) 1pin Indication
(2) Market No.
(3) Year code（last 1 digit）
(4) Week code
(5) Management code

12. Ordering Guide

AP1010AEN	-30°C～85°C	16-pin QFN

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
17/07/11	00	-	First Edition
17/11/01	01	5	Correction of mistake in Note 5. A 4-layer board is used.→A 2-layer board is used.

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