Intel® 810 Chipset Family: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH)

Specification Update

January 2001

Notice: The Intel® 82810/82810-DC100 GMCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290659-003

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	April 1999
-002	Added Specification Chages 1-7; Added Errata 1-16; Added Specification Clarifications 1-2, and Added Document Changes 1-4	November 1999
-003	Added Errata #17; Added Specification Clarification #3	January 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 810 Chipset: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) datasheet	290656-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® 82810/82810-DC100 behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® 82810/82810-DC100 GMCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	7120h/7121h 7122h/7123h	02h
A3	8086h	7120h/7121h 7122h/7123h	03h

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space. 7120h/7121h = 82810. 7122h/7123h = 82810-DC100. 7120h and 7122h = memory. 7121h and 7123h = graphics.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® 82810/82810-DC100 GMCH may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
A2	SL35K	FW82810DC100	Production GMCH (Display Cache 100)
A2	SL35X	FW82810	Production GMCH
A2	SL3KK	FW82810DC100	Remnants GMCH (Display Cache 100)
A2	SL3KL	FW82810	Remnants GMCH
A2	Q790	FW82810DC100	Anam Assembly, Folsom Test
A2	Q789	FW82810	Anam Assembly, Folsom Test
A3	SL3P6	FW82810DC100	Production GMCH (Display Cache 100)
A3	SL3P7	FW82810	Production GMCH
A3	SL3Q6	FW82810DC100	Remnants GMCH (Display Cache 100)
A3	SL3Q7	FW82810	Remnants GMCH
A3	Q859	FW82810DC100	Anam Assembly, Chandler Test
A3	Q862	FW82810	Anam Assembly, Chandler Test

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel® 82810/82810-DC100 GMCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Number	Steppings			SPECIFICATION CHANGES
	A2	A3		
1	X			Changed: IREF, Section 2.5(1)
2	X			Changed: SDRAMT Register Programming, Section 4.3.4(1)
3	X			Changed: Supported Processor Change
4	X			Changed: XOR Testability Changes and Corrections
5	X	X		Changed: Removed Pentium® II and Pentium® III Processor
6		X		Changed: Processor Support When Using the 82810/82810-DC100 GMCH A3 Stepping
7	X	X		Changed: 2D Graphics Refresh Rate

NOTES:

1. This specification change has been incorporated into the *Intel® 810 Chipset: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH)* datasheet, and has been removed from this document.

Number	Steppings			Plans	ERRATA
	A2	A3			
1	X	X		NoFix	CS Buffer Strength Bit
2	X	X		NoFix	Overlay TLB
3	X	X		NoFix on A2 Fix on A3	Blit Data Corruption
4	X	X		NoFix	Flat Panel Pixel Doubling Mode
5	X	X		NoFix	Anisotropic Texture Mapping
6	X	X		NoFix on A2 Fix on A3	Zero Length Partial Transaction
7	X	X		NoFix	HAB[7] Driven
8	X	X		NoFix	3D Texture Color/Chroma Key
9	X	X		Fixed	Data Decoded as Command during Low Priority to Interrupt Priority Ring Buffer Transition
10	X	X		NoFix	A3 Stepping LMD13 Strap
11	X	X		NoFix	Video Overlay Bandwidth
12	X	X		NoFix	Host Interface RCOMP
13	X	X		NoFix on A2 Fix on A3	Blit Hang
14	X	X		NoFix	AC97 Latency and Drop Out
15	X	X		NoFix	Asynchronous Queue Overflow
16	X	X		NoFix	PM_CS Power State Bits Accept Invalid States
17	X	X		NoFix	Asynchronous Screen Flip

Number	Steppings			SPECIFICATION CLARIFICATIONS
	A2	A3		
1	X			Changed: GMCH Graphics Controller Register Memory
2	X	X		Added: Video Overlay Support
3	X	X		Added: Resume from S3

Number	Steppings			DOCUMENTATION CHANGES
	A2	A3		
1	X			Changed: Intel® Dynamic Video Memory Technology, Section 4.4
2	X			Changed: Digital Video Output Signal/TV-Out Pins, Section 2.6; {CLKOUT[1:0]}
3	X	X		Changed: System Buffer Strength Control Register, Section 3.4.21; BUFF_SC 92h-93h Device 0 Register Description
4	X	X		Changed: Chapter 2, Signal Description; I/OD Definition Corrected

Specification Changes

1. Changed: IREF, Section 2.5

This specification change has been incorporated into the *Intel® 810 Chipset: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH)* datasheet, and has been removed from this document.

2. Changed: SDRAMT Register Programming, Section 4.3.4

This specification change has been incorporated into the *Intel® 810 Chipset: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH)* datasheet, and has been removed from this document.

3. Changed: Supported Processor Change

This specification change is invalid and has been removed from this document.

4. Changed: XOR Chain Pin Assignments

This specification change has been incorporated into the *Intel® 810 Chipset: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH)* datasheet, and has been removed from this document.

5. Changed: Removal of Pentium® II and Pentium® III Processor

This specification change is invalid and has been removed from this document.

6. Changed: Processor Support When Using the 82810/82810-DC100 GMCH A3 Stepping

Specification Changes #3 and #5 above are rescinded for the A3 stepping of the 82810/82810-DC100 GMCH. The 82810/82810-DC100 GMCH A3 stepping supports Intel® Pentium® II, Pentium® III and Celeron™ processors. Therefore, the following changes should be made:

Product Features List

Under Processor/Host Bus Support should read:

-Optimized for Intel Pentium II, Pentium III and Intel Celeron processors.

Host Interface, Section 1.3

First sentence should read:

The host interface of the GMCH is optimized to support the Intel Pentium II, Pentium III and Intel Celeron processors.

ChangeSystem Address Map, Section 4.1

The first sentence should read:

An Intel Pentium II, Pentium III or Intel Celeron processor system based on the GMCH, supports 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. (The P6 bus I/O addressability is 64 KB + 3).

Host Interface, Section 4.2

The first sentence should read:

The host interface of the GMCH is optimized to support the Intel Pentium II, Pentium III and Intel Celeron processors.

7. Changed: 2D Graphics Refresh Rate

On the Product Features List, 2D graphics bullet in the top right column, the first item is changed to read:

"— Up to 1600X1200 in 8-bit Color at 75 Hz Refresh"

Errata

1. CS Buffer Strength Bit

Problem: The GMCH chip select buffer strength bits in the GMCH BUFF_SC register (Device 0, offset 92-93h) bits 15:12 are as follows:

Bit	Description
15	**SCS[0]# Buffer Strength.** This field sets the buffer strength for the SCS[0] buffer. 0 = 3x 1 = 2x
14	**SCS[1]# Buffer Strength.** This field sets the buffer strength for the SCS[1] buffer. 0 = 3x 1 = 2x
13	**SCS[2]# Buffer Strength.** This field sets the buffer strength for the SCS[2] buffer. 0 = 3x 1 = 2x
12	**SCS[3]# Buffer Strength.** This field sets the buffer strength for the SCS[3] buffer. 0 = 3x 1 = 2x

Implication: BIOS must set the correct bits for the chip select buffer strengths. Buffer strengths work correctly otherwise.

Workaround: BIOS must set the correct bits as stated above for the chip select buffer strengths.

Status: BIOS workaround. No stepping Fix

2. Overlay TLB

Problem: The GMCH does not correctly determine when it is valid to throw away the old translations in the TBL and replace them with a new set of translations when the following conditions are met:
-Overlay is operating in 4:2:0 or 4:1:0 modes
-The overlay surface is read from linear memory
-An aligned 8 KB boundary falls in the middle of a scanline
-Either X-mirroring or Y-mirroring is activated

Implication: If the Conditions stated above are met the GMCH will display incorrect data on the screen resulting in some lines of color on the screen.

Workaround: Do not run overlay in 4:2:0 or 4:1:0 modes when the surface is in linear memory and either horizontal or vertical mirroring is turned on.

Status: No Stepping Fix

3. Blit Data Corruption

Problem: During a blit, the last QWord of data on a scan line will substitute the second to last QWord of data when clipping is enabled. This condition takes place when the last QWord of data is not full of pixel data.

Implication: Some of the scan lines will have the last 2 or 3 or 7 pixels, based on the color depth, corrupted. For 24bpp, up to the last 2 pixels can be corrupted, for 16bpp, up to the last 3 pixels can be corrupted and for 8bpp up to the last 7 pixels can be corrupted. This can result in up to 7 pixels being corrupted at the end of a scan line.

Workaround: None

Status: To be fixed in the A3 stepping

4. Flat Panel Pixel Doubling Mode

Problem: The flat panel display engine change cannot handle mode switches into a flat panel pixel doubling mode without being disabled first.

Implication: If an application changes to a pixel doubling mode the entire screen will display the border color.

Workaround: The work around requires the BIOS to detect a write to the pixel doubling bit (SR01[3]). When a write to this bit is detected, the flat panel engine must be disabled and restarted. This results in proper DCLK/FCLKOUT synchronization. Windows does not allow applications to write to registers that set pixel doubling modes. Legacy DOS applications that attempt to change the video mode to pixel doubling mode can still cause this issue to appear.

Status: BIOS workaround, No planned stepping fix.

5. Anisotropic Texture Mapping

Problem: Anisotropic logic with multiple textures uses the incorrect textel under certain conditions with color or chroma keying enabled. This issue takes place during texturing in the case of a multi-texture polygon, when the first texture is anisotropic and the second is not, and the first texture has color or chroma key on. In this case the kill bit for the last pixel of a 4X4 pixel span for the first texture can get lost and the pixel is displayed when it should not. This problem requires a unique set of conditions to appear. First, anisotropic logic must be turned on, which requires more video processing in the video hardware. Second, multiple textures must be applied to a single polygon.

Implication: This will cause a pixel to display incorrectly which may result in a sparkle on the screen.

Workaround: None

Status: No planned fix.

6. Zero Length Partial Transaction

Problem: A2 stepping of the Intel® 810 chipset does not support the MASKMOVQ instruction with non-aligned data on Intel® Pentium® III Processors. Impacts cycles to non-write combined AGP, memory mapped I/O, and PCI space. No impact on cycles to memory and write combined AGP space.

Implication: Results in data corruption that may lead to a system hang. No Intel® Pentium® III Processor support on Intel® 810 chipset platforms.

Workaround: None

Status: Intended to be fixed in the A3 stepping. See *Summary Table of Changes* for affected product(s) and steppings.

7. HAB[7] Driven

Problem: When the IOQ depth is set to one, a test mode, HAB[7] is driven to Vil until ADS# asserts on reset. When operating correctly the GMCH should float HAB[7] after two clock cycles following the deassertion of RESET#.

Implication: This problem does not affect the normal operation of Intel® 810 chipset platforms, which sets the IOQ depth at four. No contention on the host address bus results from this issue.

Workaround: Set the IOQ depth to four for normal operation. Do not set the IOQ depth to one, except for validation purposes.

Status: No planned fix.

8. 3D Texture Color/Chroma Key

Problem: A case exists where invalid data from the texture cache is included into the bilinear filter to determine the texture color for a pixel causing the shading for that pixel to be incorrect. This occurs when an indexed texture map has color or chroma key enabled and the filtering appears on a texture boundary. In this case one valid textel is keyed on and the other is keyed out. In this case the bilinear filtering uses two invalid textels in the cache that are past the texture boundary. If the valid textel that is keyed out lines up with an invalid texel that is keyed on, the valid texel, which is keyed out, is incorrectly replaced with the invalid textel before the bilinear filtering.

Implication: In this case a pixel may be shaded incorrectly on the edge of a texture.

Workaround: None.

Status: No planned fix.

9. Data Decoded As Command during Low Priority to Interrupt Priority Ring Buffer Transition

Problem: Data is decoded as a command packet if the low priority ring is executing non-pipelined state variable packets and the interrupt priority ring is enabled. This could happen anytime 3D is active and a stretch-blit (2D) operation is conducted through the interrupt ring.

Implication: The result could be a hang of the parser state machine or incorrect setting of the state variable in 3D. The only known application that uses the interrupt priority ring is the stretch-blit operation. Intel drivers associated with the 82810 do not use this process. This process is used by DVD software.

Workaround: Do not use non-pipelined state variable execution when the interrupt ring is enabled. DVD software writers are aware of this issue and can modify their DVD software to avoid this erratum. Please contact your DVD software provider to determine if this erratum has been addressed in their current DVD software and if a software patch is available for earlier versions of their DVD software.

Status: No planned silicon fix. Software fixes are already in place.

10. A3 Stepping LMD13 Strap

Problem: The 82810 GMCH A3 stepping did not implement an internal pull-down as required for reset startup strapping.

Implication: The GMCH A3 stepping may not work properly if LMD13 is floating at reset. The system may not boot if this pulldown resistor is not implemented.

Workaround: To compensate for any possible floating condition, add a weak pull-down resistor (10 KΩ–20 KΩ) to ground on the LMD13 signal of the GMCH A3 on the motherboard.

Status: No planned silicon fix. The Intel® 810 Chipset Design Guide Update, Rev 1.0, shows implementation of the required pull-down resistor on motherboards.

11. Video Overlay Bandwidth

Problem: Bandwidth limitations impact the use of graphics modes of 1152X864X24 @85Hz and at 1280X1024X24 at 85Hz with AVI or JPG video files.

Implication: Graphics corruption such as vertical stripes may appear while moving around an active AVI or JPG video overlay window.

Workaround: None identified. Using CAS latency 2 memory reduces the problem.

Status: No planned silicon fix.

12. Host Interface RCOMP

Problem: Depending upon system design and environmental factors, a violation of the host interface hold timing specification may occur. Root cause is a circuit (RCOMP) designed to dynamically adjust clock to out delay (Tco) and slew rate on host interface buffers that does not function.

Implication: If hold timing specifications are violated, data corruption may occur. This data corruption may also result in a system hang.

Workaround: A BIOS workaround is available to fix the Tco and Slew Rate at optimum values.

Status: No planned silicon fix.

13. Blit Hang

Problem: On back to back read modify writes with transparency enabled and the destination from the latest blits hits on the destination from one of the earlier blits, dead lock can occur in the graphics engine.

Implication: This issue can lead to system hangs using specific System Validation test software, but testing to date has not identified any real-world applications that cause this behavior. Operating systems tested were Win98 (315 applications), WinNT4 (74 applications), Win95 (92 applications), and Win2K (32 applications). Validation activity included the use of automated and manual testing of over 400 applications, stress test software, and benchmark software. Due to the specific sequencing of events necessary to create the failure, Intel and major OEMs were unable to recreate the problem during any testing described above.

Workaround: Allocate a separate surface that is 16 cache lines deep on a 4QW aligned boundary.

Status: Fixed in A3 silicon.

14. AC97 Latency and Drop Out

Problem: Cycles from the local cache fill up the command queue causing aperture cycles from the host to be starved. AC97 cycles are queued with a lower priority than the aperture cycles and can, therefore, experience underrun.

Implication: Latency or data drop out may occur in the completion of AC97 cycles. Audio cycles may not be synchronized with video. MODEM operation may drop out entirely during heavily loaded system operation. These effects may vary by application, user, OS in use, and system load.

Workaround: None identified.

Status: No planned silicon fix.

15. Asynchronous Queue Overflow

Problem: A specific heavily loaded system configuration and specific traffic causes the 82810 GMCH asynchronous queues to fill up, causing upbound I/O traffic to get blocked while waiting for an I/O transaction to complete.

If the following specific configuration and transaction sequence occurs, the system may hang:

1. A CPU memory write to the hub interface occurs,
2. AND a QWord misaligned CPU read to PCI or LPC occurs
3. AND any three of the following four interfaces are simultaneously active,
   (1) PHLD traffic from M-ISA or LPC to DRAM,
   (2) IDE BM traffic to DRAM,
   (3) PCI Master #1 read traffic from DRAM,
   (4) PCI Master #2 read traffic from DRAM,
4. AND sufficient system traffic exists to fill the asynchronous upbound and downbound queues in the GMCH.

Implication: If the specific configuration and transaction sequence shown above occurs, the system may hang.

Workaround: Disable PCI pre-fetching in the ICH. This may cause a 1%-2% performance hit on PCI initiated reads to DRAM only.

Status: No planned silicon fix. A software fix to disable PCI pre-fetching will be published.

16. PM_CS Power State Bits Accept Invalid States

Problem: PCI Power Management Control/Status Register (PM_CS), Device 1, address offset E0h-E1h, bits [1:0], accepts values representing power management states D1 and D2, which the hardware device does not support.

Implication: This is a violation of the PM 1.1 specification and causes the WHQL PC99A HCT9.x test to fail.

Workaround: None

Status: This issue will not be fixed in the 82810 GMCH. Intel is working with Microsoft* on a WHQL waiver for WHQL certification.

17. Asynchronous Screen Flip

Problem: When the Intel® 82810A2 or 82810A3 devices are configured for asynchronous screen flipping, under certain timing-dependent circumstances the display engine may temporarily read pixel data from a random memory location.

Implication: When changing display surfaces using the asynchronous screen flipping, subtle display corruption is seen in the form of short, somewhat random colored, horizontal lines along the left side of the screen.

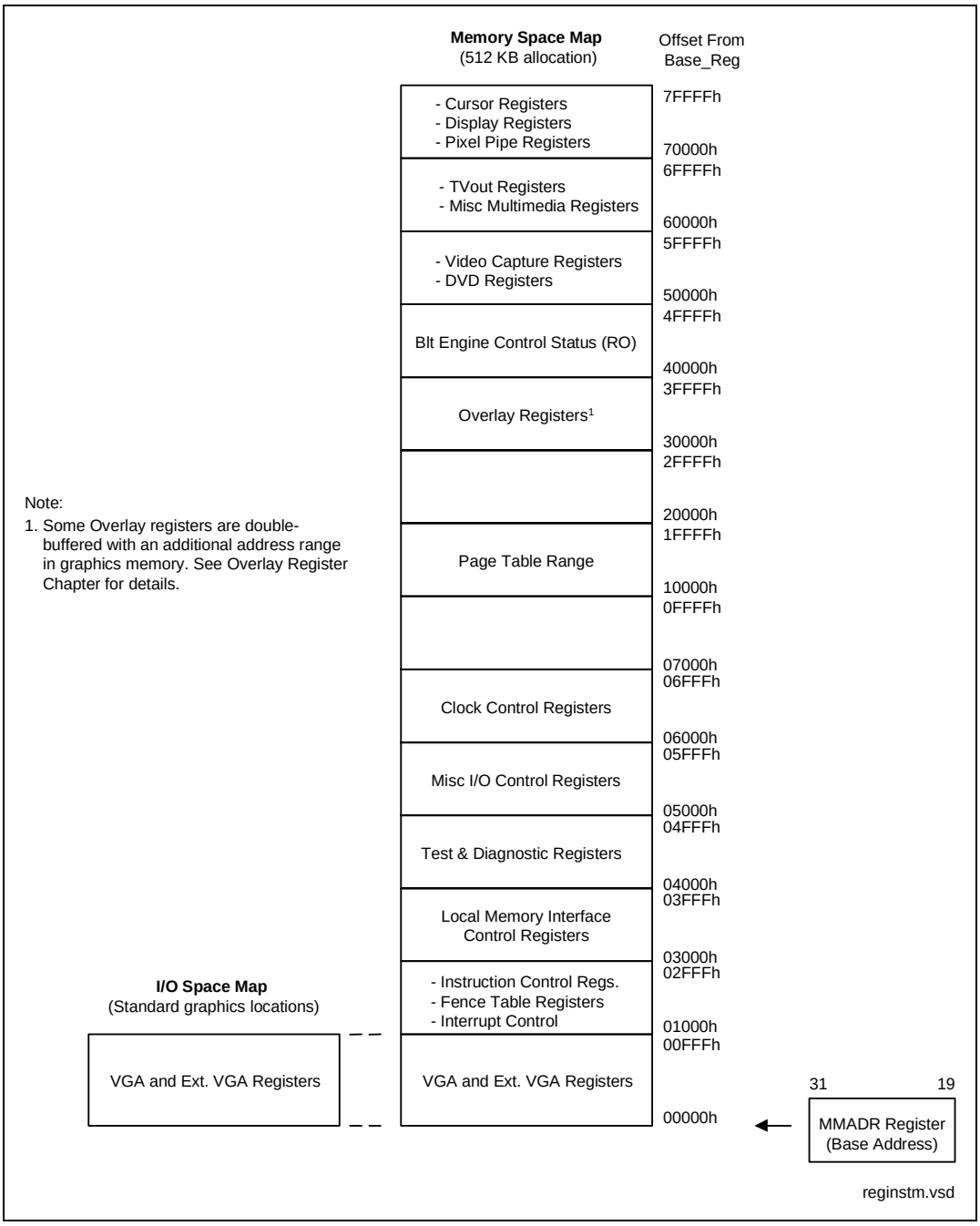
Workaround: Driver version 4.1.1 does, and future version will, disable asynchronous screen flipping for commonly used 3D resolutions.

Status: There are no plans to fix this erratum in silicon.

Specification Clarifications

1. Changed: GMCH Graphics Controller Register Memory

Figure 6 (*GMCH Graphics Register Memory Address Space*), Section 4.1.1.2, Extended Memory Area, is replaced with the figure below.



2. Added: Video Overlay Support

Reference Errata #11, Video Overlay Bandwidth Errata, in this document. In addition to Errata #11, the following clarification concerning video overlay support is provided:

Reference Section 4.6.11, *Display*, the following information is added:

Hardware bandwidth limitations define resolution when using video overlay. These limitations are established in the table below. The table below is added as Table 17a in the datasheet.

Table 17a. Overlay Modes Supported:

The table shows support for desktop modes and overlay.

D = Available Desktop Mode						
Y = Overlay Support						
Pixel Resolution	**Colors**	**60Hz**	**70Hz**	**72Hz**	**75Hz**	**85Hz**
640x480	256	D/Y	D/Y	D/Y	D/Y	D/Y
640x480	16 Bit	D/Y	D/Y	D/Y	D/Y	D/Y
640x480	24 Bit	D/Y	D/Y	D/Y	D/Y	D/Y
720x480	256	-	-	-	D/Y	D/Y
720x480	16 Bit	-	-	-	D/Y	D/Y
720x480	24 Bit	-	-	-	D/Y	D/Y
720x576	256	-	-	-	D/Y	D/Y
720x576	16 Bit	-	-	-	D/Y	D/Y
720x576	24 Bit	-	-	-	D/Y	D/Y
800x600	256	D/Y	D/Y	D/Y	D/Y	D/Y
800x600	16 Bit	D/Y	D/Y	D/Y	D/Y	D/Y
800x600	24 Bit	D/Y	D/Y	D/Y	D/Y	D/Y
1024x768	256	D/Y	D/Y	-	D/Y	D/Y
1024x768	16 Bit	D/Y	D/Y	-	D/Y	D*
1024x768	24 Bit	D/Y	D/Y	-	D/Y	D*
1152x864	256	D/Y	D/Y	D/Y	D/Y	D*
1152x864	16 Bit	D/Y	D/Y	D*	D*	D*
1152x864	24 Bit	D/Y	-	-	D*	D*
1280x1024	256	D/Y	D*	D*	D*	D*
1280x1024	16 Bit	D*	D*	D*	D	D
1280x1024	24 Bit	D*	D*	-	D	D
1600x1200	256	D*	D*	D*	D	-
*Overlay support modified in the 2.2 driver						

3. Added: ACPI Rev 1.0 - Support for Resume from S3 State, Section 4.9.2

The following information is added as Section 4.9.2:

4.9.2 ACPI Rev 1.0 - Support for Resume from S3 State

The 82810 chipset enters self-refresh upon entering S3 (Suspend to RAM). The normal sequence is that the GMCH sends a “Precharge All banks” to SDRAM and then issues an “Enter Self-Refresh” command prior to actually entering the S3 state. However, the GMCH may issue an "Open Bank" command between these two commands if the graphics portion is not correctly shut down prior to entering S3. The “Open Bank” command may adversely affect the memory interface in back-to-back repetitive S3-S0-S3-S0 testing activities.

There should be no request for access to the memory interface when entering S3. For CPU initiated transfers, the ICHx guarantees this since it asserts STPCLK#. For I/O based traffic such as PCI cards, all traffic should be stopped by the O/S, BIOS, and graphics driver combination.

Unified Memory Architecture such as that used in the 82810 chipset requires additional precautions since the graphics controller shares memory directly with system memory. All graphics initiated traffic needs to be stopped. The solution is to stop all graphics engines that request memory resources.

Software must disable all traffic generated by the GMCH graphics engines prior to entering S3. This includes display screen refresh (SR01 (I/O and memory offset address 3C5h (Index = 01h)), bit 5 = 1), Overlay (MMADR+68h), hardware cursor (Cursor Control Register, Memory Offset Address 70080h, bits 2:0 = 000), and the command streamer. The responsibility for this action can be in the O/S, in the system BIOS, or in the graphics driver.

The standard VGA mode only needs to disable the screen refresh since it doesn't start any other graphics traffic. Standard VGA drivers normally ensure this prior to entering S3 by setting the SR01 (I/O and memory offset address 3C5h (Index = 01h)), bit 5 = 1.

This page is intentionally left blank.

Documentation Change

1. Changed: Intel® Dynamic Video Memory Technology, Section 4.4

Section 4.4, *Intel® Dynamic Video Memory Technology*, the first paragraph should read as follows.
"The internal graphics device on both the 82810 and 82810-DC100 support Intel® Dynamic Video Memory Technology (D.V.M.T.). D.V.M.T. dynamically responds to application requirements by allocating the proper amount of display and texturing memory.
For more details refer to the document titled "*Intel® 810 Chipset: Great Performance for Value PCs*" available at http://developer.intel.com/design/chipsets/810/810white.htm

2. Changed: Digital Video Output Signal/TV-Out Pins, Section 2.6; {CLKOUT[1:0]}

Section 2.6, D*igital Video Output Signal/TV-Out Pins*, the CLKOUT[1:0] section should read LCD/TV Port Clock Out: These pins provide a differential pair reference clock that can run up to 85 MHz.

3. Changed: System Buffer Strength Control Register, Section 3.4.21; BUFF_SC 92h-93h Device 0 Register Description

The horizontal depiction of bits [15:8] is changed to show the correct bit [15:12] relationship to [SCS0#:SCS3#] as follows:

15	14	13	12	11 10	9 8
SCS0# Buffer Strength	SCS1# Buffer Strength	SCS2# Buffer Strength	SCS3# Buffer Strength	SMAA[7:4] Buffer Strength	SMAB[7:4]# Buffer Strength

4. Changed: Chapter 2, Signal Description; I/OD Definition Corrected

The signal description for the I/OD signals on page 19 is changed to read:

I/OD Input / Open Drain Output pin. This pin requires a pull-up to 3.3V.

This page is intentionally left blank.

This page is intentionally left blank.