Data sheet acquired from Harris Semiconductor
SCHS218C

February 1998 - Revised October 2003

CD74HC7046A, CD74HCT7046A

Phase-Locked Loop with VCO and Lock Detector

Features

- Center Frequency of 18MHz (Typ) at V_{CC} = 5V, Minimum Center Frequency of 12MHz at V_{CC} = 4.5V
- Choice of Two Phase Comparators
  - Exclusive-OR
  - Edge-Triggered JK Flip-Flop
- Excellent VCO Frequency Linearity
- VCO-Inhibit Control for ON/OFF Keying and for Low Standby Power Consumption
- Minimal Frequency Drift
- Zero Voltage Offset Due to Op-Amp Buffer
- Operating Power-Supply Voltage Range
  - VCO Section . . . . . 3V to 6V
  - Digital Section . . . . . 2V to 6V
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Applications

- FM Modulation and Demodulation
- Frequency Synthesis and Multiplication
- Frequency Discrimination
- Tone Decoding
- Data Synchronization and Conditioning
- Voltage-to-Frequency Conversion
- Motor-Speed Control
- Related Literature
  - AN8823, CMOS Phase-Locked-Loop Application Using the CD74HC/HCT7046A and CD74HC/HCT7046A

Description

The CD74HC7046A and CD74HCT7046A high-speed silicon-gate CMOS devices, specified in compliance with JEDEC Standard No. 7A, are phase-locked-loop (PLL) circuits that contain a linear voltage-controlled oscillator (VCO), two-phase comparators (PC1, PC2), and a lock detector. A signal input and a comparator input are common to each comparator. The lock detector gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (Gnd). For a frequency range of 100kHz to 10MHz, the lock detector capacitor should be 1000pF to 10pF, respectively.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 7046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

Ordering Information

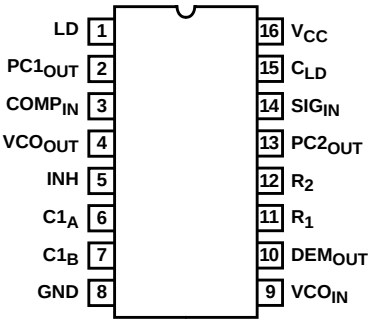
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE
CD74HC7046AE	-55 to 125	16 Ld PDIP
CD74HC7046AM	-55 to 125	16 Ld SOIC
CD74HC7046AMT	-55 to 125	16 Ld SOIC
CD74HC7046AM96	-55 to 125	16 Ld SOIC
CD74HCT7046AE	-55 to 125	16 Ld PDIP
CD74HCT7046AM	-55 to 125	16 Ld SOIC
CD74HCT7046AMT	-55 to 125	16 Ld SOIC
CD74HCT7046AM96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

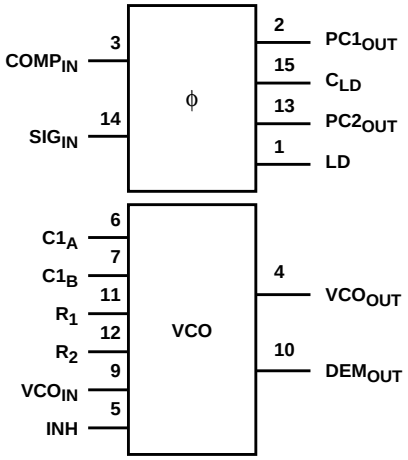
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Pinout

CD74HC7046A, CD74HCT7046A
(PDIP, SOIC)
TOP VIEW



Functional Diagram



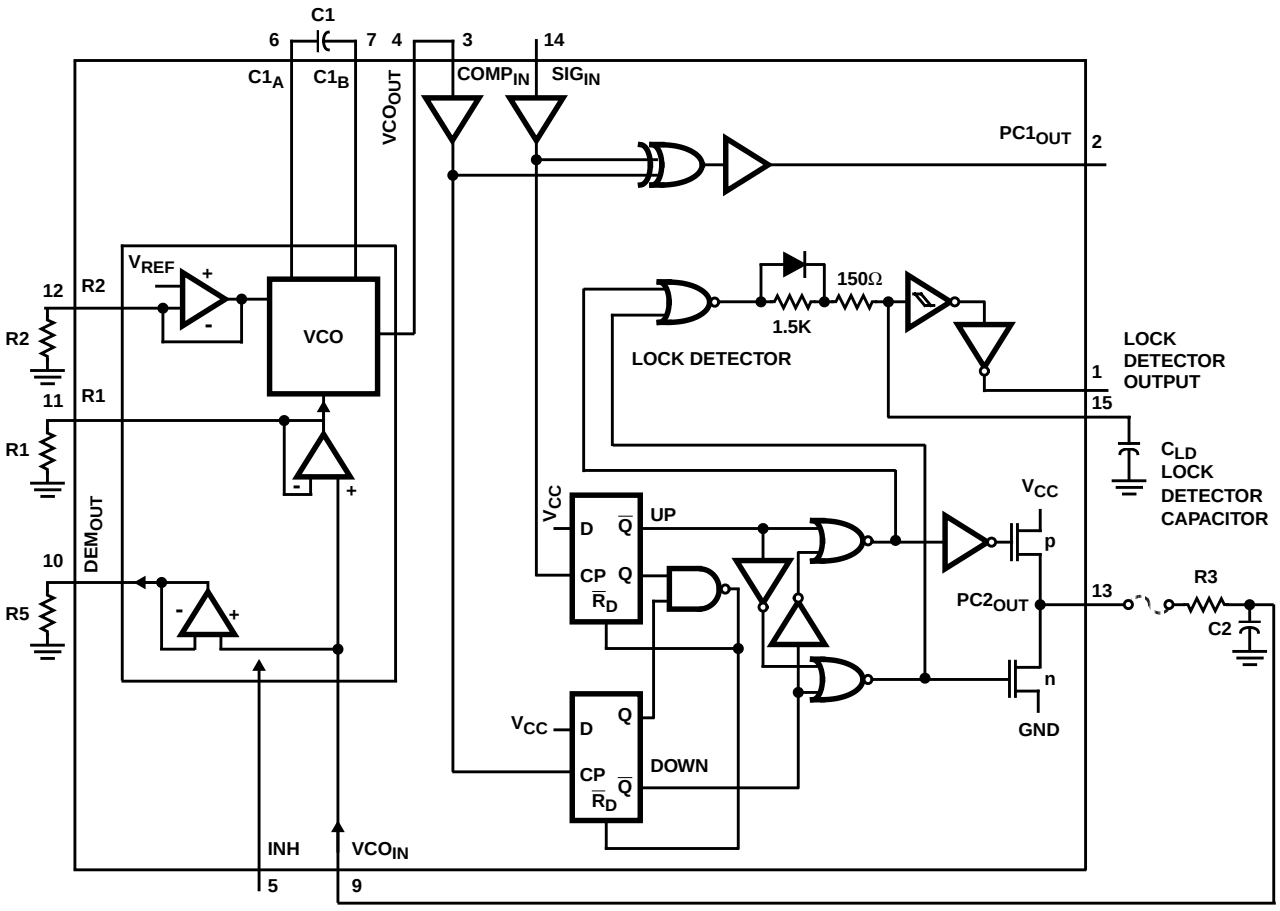


FIGURE 1. LOGIC DIAGRAM

Pin Descriptions

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	Lock Detector Output (Active High)
2	$PC1_{OUT}$	Phase Comparator 1 Output
3	$COMP_{IN}$	Comparator Input
4	VCO_{OUT}	VCO Output
5	INH	Inhibit Input
6	$C1_A$	Capacitor C1 Connection A
7	$C1_B$	Capacitor C1 Connection B
8	Gnd	Ground (0V)
9	VCO_{IN}	VCO Input
10	DEM_{OUT}	Demodulator Output
11	R_1	Resistor R1 Connection
12	R_2	Resistor R2 Connection
13	$PC2_{OUT}$	Phase Comparator 2 Output
14	SIG_{IN}	Signal Input
15	C_{LD}	Lock Detector Capacitor Input
16	V_{CC}	Positive Supply Voltage

General Description

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R1 and Gnd) or two external resistors R1 and R2 (between R1 and Gnd, and R2 and Gnd). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. See logic diagram, Figure 1.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to Gnd; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a specified duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO, while a HIGH level disables the VCO to minimize standby power consumption.

Phase Comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels, Capacitive coupling is required for signals with smaller swings.

Phase Comparator 1 (PC1)

This is an Exclusive-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Figure 2. The average of V_{DEM} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN}, and with this input the VCO oscillates at the center frequency (f_o). Typical waveforms for the PC1 loop locked at f_o shown in Figure 3.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock behavior even with very noisy input signals. Typical of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO center frequency.

Phase Comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIGIN and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a three-state output stage. The circuit functions as an up-down counter (Figure 1) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/4\pi)\ (\phi_{SIGN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The average output voltage from PC2, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Figure 4. Typical waveforms for the PC2 loop locked at f_o are shown in Figure 5.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held “ON” for a time corresponding to the phase differences (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held “ON”.

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held “ON” for most of the input signal cycle time, and for the remainder of the cycle both n-type and p-type drivers are “OFF” (three-state). If the SIG_{IN} fre-

quency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in three-state and the VCO input at pin 9 is a high impedance.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p-type and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN}, the VCO adjusts, via PC2, to its lowest frequency.

Lock Detector Theory of Operation

Detection of a locked condition is accomplished by a NOR gate and an envelope detector as shown in Figure 6. When the PLL is in Lock, the output of the NOR gate is High and the lock detector output (Pin 1) is at a constant high level. As the loop tracks the signal on Pin 14 (signal in), the NOR gate outputs pulses whose widths represent the phase differences between the VCO and the input signal. The time between pulses will be approximately equal to the time constant of the VCO center frequency. During the rise time of the pulse, the diode across the 1.5kΩ resistor is forward biased and the time constant in the path that charges the lock detector capacitor is T = (150Ω x C_{LD}).

During the fall time of the pulse the capacitor discharges through the 1.5kΩ and the 150Ω resistors and the channel resistance of the n-device of the NOR gate to ground (T = (1.5kΩ + 150Ω + Rn-channel) x C_{LD}).

The waveform preset at the capacitor resembles a sawtooth as shown in Figure 7. The lock detector capacitor value is determined by the VCO center frequency. The typical range of capacitor for a frequency of 10MHz is about 10pF and for a frequency of 100kHz is about 1000pF. The chart in Figure 8 can be used to select the proper lock detector capacitor value. As long as the loop remains locked and tracking, the level of the sawtooth will not go below the switching threshold of the Schmitt-trigger inverter. If the loop breaks lock, the width of the error pulse will be wide enough to allow the sawtooth waveform to go below threshold and a level change at the output of the Schmitt trigger will indicate a loss of lock, as shown in Figure 9. The lock detector capacitor also acts to filter out small glitches that can occur when the loop is either seeking or losing lock.

Note: When using phase comparator 1, the detector will only indicate a lock condition on the fundamental frequency and not on the harmonics, which PC1 will also lock on. If a detection of lock is needed over the harmonic locking range of PC1, then the lock detector output must be OR-ed with the output of PC1.

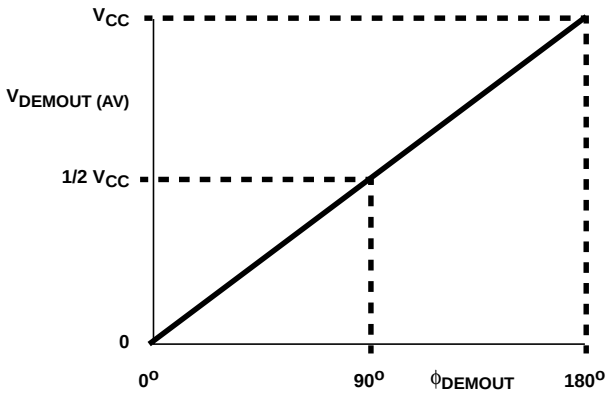


FIGURE 2. PHASE COMPARATOR 1: AVERAGE OUTPUT VOLTAGE vs INPUT PHASE DIFFERENCE: $V_{DEMOUT} = V_{PC1OUT} = (V_{CC}/\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$; $\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$

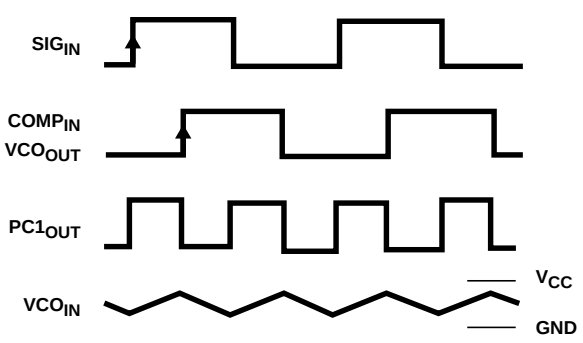


FIGURE 3. TYPICAL WAVEFORMS FOR PLL USING PHASE COMPARATOR 1, LOOP LOCKED AT f_o

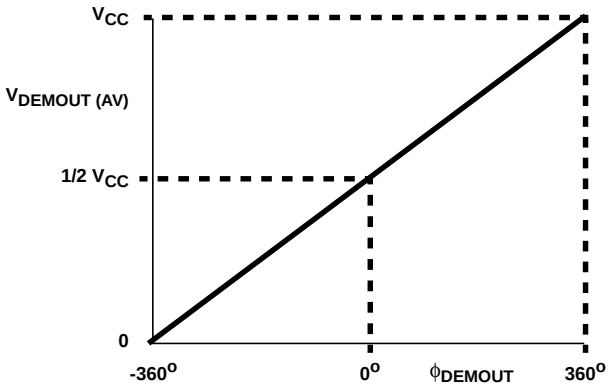


FIGURE 4. PHASE COMPARATOR 2: AVERAGE OUTPUT VOLTAGE vs INPUT PHASE DIFFERENCE: $V_{DEMOUT} = V_{PC2OUT} = (V_{CC}/\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$; $\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$

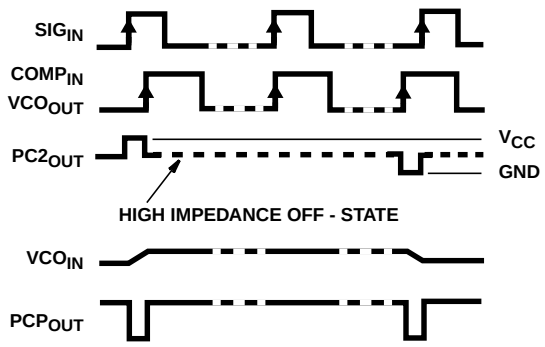


FIGURE 5. TYPICAL WAVEFORMS FOR PLL USING PHASE COMPARATOR 2, LOOP LOCKED AT f_o

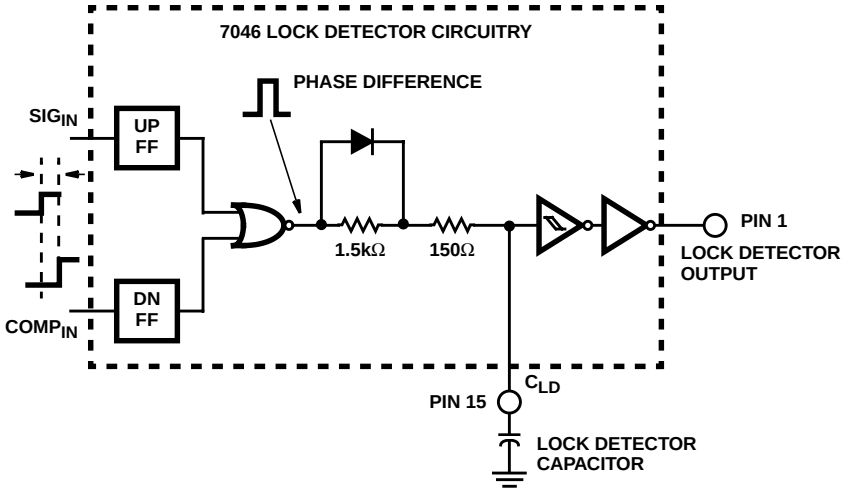


FIGURE 6. CD74HC/HCT7046A LOCK DETECTOR CIRCUIT

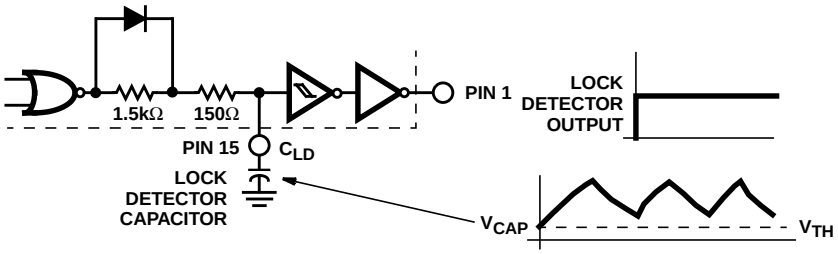


FIGURE 7. WAVEFORM PRESENT AT LOCK DETECTOR CAPACITOR WHEN IN LOCK

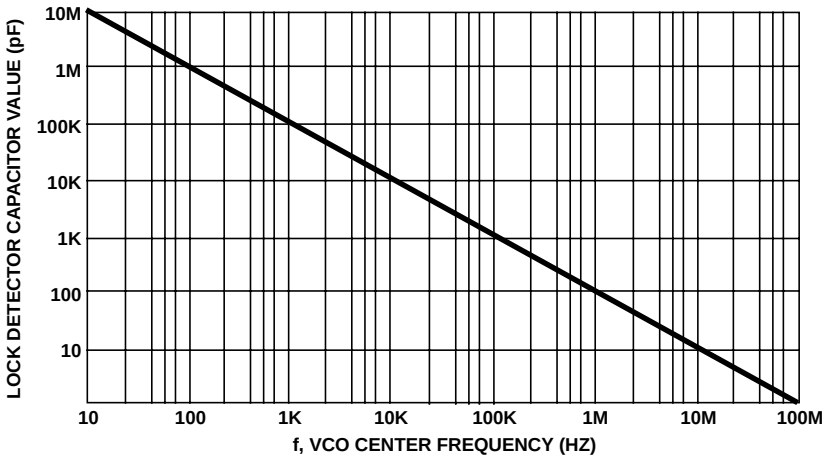


FIGURE 8. LOCK DETECTOR CAPACITOR SELECTION CHART

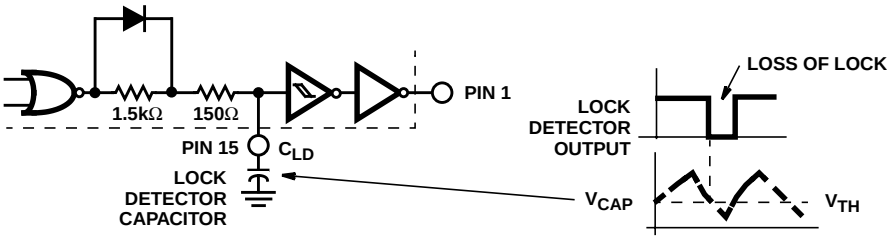


FIGURE 9. WAVEFORM PRESENT AT LOCK DETECTOR CAPACITOR WHEN UNLOCKED

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
E (PDIP) Package 67
M (SOIC) Package 73
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V . . . . . 500ns (Max)
6V . . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25^oC MIN	25^oC TYP	25^oC MAX	-40^oC TO 85^oC MIN	-40^oC TO 85^oC MAX	-55^oC TO 125^oC MIN	-55^oC TO 125^oC MAX	UNITS
HC TYPES												
VCO SECTION												
INH High Level Input Voltage	V_{IH}	-	-	3	2.1	-	-	2.1	-	2.1	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
INH Low Level Input Voltage	V_{IL}	-	-	3	-	-	0.9	-	0.9	-	0.9	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
VCO_{OUT} High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	3	2.9	-	-	2.9	-	2.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
VCO_{OUT} High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
VCO_{OUT} Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
VCO_{OUT} Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
C1A, C1B Low Level Output Voltage (Test Purposes Only)	V_{OL}	V_{IL} or V_{OL}	4	4.5	-	-	0.40	-	0.47	-	0.54	V
			5.2	6	-	-	0.40	-	0.47	-	0.54	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
INH VCO_{IN} Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
R1 Range (Note 2)	-	-	-	4.5	3	-	-	-	-	-	-	kΩ
R2 Range (Note 2)	-	-	-	4.5	3	-	-	-	-	-	-	kΩ
C1 Capacitance Range	-	-	-	3	-	-	No Limit	-	-	-	-	pF
				4.5	40	-		-	-	-	-	pF
				6	-	-		-	-	-	-	pF
VCO_{IN} Operating Voltage Range	-	Over the range specified for R1 for Linearity See Figure 8, and 35 - 38 (Note 3)		3	1.1	-	1.9	-	-	-	-	V
				4.5	1.1	-	3.2	-	-	-	-	V
				6	1.1	-	4.6	-	-	-	-	V
PHASE COMPARATOR SECTION												
SIG_{IN}, $COMP_{IN}$ DC Coupled High-Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
SIG_{IN}, $COMP_{IN}$ DC Coupled Low-Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
LD, PCn_{OUT} High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
				4.5	4.4	-	-	4.4	-	4.4	-	V
				6	5.9	-	-	5.9	-	5.9	-	V
LD, PCn_{OUT} High-Level Output Voltage TTL Loads	V_{OH}	V_{IL} or V_{IH}	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
LD, PCn_{OUT} Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
				4.5	-	-	0.1	-	0.1	-	0.1	V
				6	-	-	0.1	-	0.1	-	0.1	V
LD, PCn_{OUT} Low-Level Output Voltage TTL Loads	V_{OL}	V_{IL} or V_{IH}	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
SIG_{IN}, $COMP_{IN}$ Input Leakage Current	I_I	V_{CC} or GND	-	2	-	-	±3	-	±4	-	±5	µA
				3	-	-	±7	-	±9	-	±11	µA
				4.5	-	-	±18	-	±23	-	±29	µA
				6	-	-	±30	-	±38	-	±45	µA
$PC2_{OUT}$ Three-State Off-State Current	I_{OZ}	V_{IL} or V_{IH}	-	6	-	-	±0.5	-	±5	-	±10	µA
SIG_{IN}, $COMP_{IN}$ Input Resistance	R_I	V_I at Self-Bias Operation Point: ΔV_I = 0.5V, See Figure 8		3	-	800	-	-	-	-	-	kΩ
				4.5	-	250	-	-	-	-	-	kΩ
				6	-	150	-	-	-	-	-	kΩ
DEMODULATOR SECTION												
Resistor Range	R_S	at R_S > 300kΩ Leakage Current Can Influence V_{DEMOUT}		3	10	-	300	-	-	-	-	kΩ
				4.5	10	-	300	-	-	-	-	kΩ
				6	10	-	300	-	-	-	-	kΩ

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Offset Voltage VCO_{IN} to V_{DEM}	V_{OFF}	$V_I = V_{VCOIN} = \frac{V_{CC}}{2}$ Values taken over R_S Range See Figure 15		3	-	±30	-	-	-	-	-	mV
				4.5	-	±20	-	-	-	-	-	mV
				6	-	±10	-	-	-	-	-	mV
Dynamic Output Resistance at DEM_{OUT}	R_O	$V_{DEMOUT} = \frac{V_{CC}}{2}$		3	-	25	-	-	-	-	-	Ω
				4.5	-	25	-	-	-	-	-	Ω
				6	-	25	-	-	-	-	-	Ω
Quiescent Device Current	I_{CC}	Pins 3, 5 and 14 at V_{CC} Pin 9 at GND, I_I at Pins 3 and 14 to be excluded		6	-	-	8	-	80	-	160	µA
HCT TYPES												
VCO SECTION												
INH High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
INH Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
VCO_{OUT} High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
VCO_{OUT} High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
VCO_{OUT} Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
VCO_{OUT} Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
C1A, C1B Low Level Output Voltage (Test Purposes Only)	V_{OL}	V_{IH} or V_{IL}	4	4.5	-	-	0.40	-	0.47	-	0.54	V
INH VCO_{IN} Input Leakage Current	I_I	Any Voltage Between V_{CC} and GND		5.5	-		±0.1	-	±1	-	±1	µA
R1 Range (Note 2)	-	-	-	4.5	3	-	-	-	-	-	-	kΩ
R2 Range (Note 2)	-	-	-	4.5	3	-	-	-	-	-	-	kΩ
C1 Capacitance Range	-	-	-	4.5	40	-	No Limit	-	-	-	-	pF
VCO_{IN} Operating Voltage Range	-	Over the range specified for R1 for Linearity See Figure 8, and 35 - 38 (Note 3)		4.5	1.1	-	3.2	-	-	-	-	V
PHASE COMPARATOR SECTION												
SIG_{IN}, $COMP_{IN}$ DC Coupled High-Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	3.15	-	-	3.15	-	3.15	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
SIG_{IN}, $COMP_{IN}$ DC Coupled Low-Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	1.35	-	1.35	-	1.35	V
LD, PCn_{OUT} High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-	4.5	4.4	-	-	4.4	-	4.4	-	V
LD, PCn_{OUT} High-Level Output Voltage TTL Loads	V_{OH}	V_{IL} or V_{IH}	-	4.5	3.98	-	-	3.84	-	3.7	-	V
LD, PCn_{OUT} Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	-	4.5	-	-	0.1	-	0.1	-	0.1	V
LD, PCn_{OUT} Low-Level Output Voltage TTL Loads	V_{OL}	V_{IL} or V_{IH}	-	4.5	-	-	0.26	-	0.33	-	0.4	V
SIG_{IN}, $COMP_{IN}$ Input Leakage Current	I_I	Any Voltage Between V_{CC} and GND	-	5.5	-	-	±30		±38		±45	µA
$PC2_{OUT}$ Three-State Off-State Current	I_{OZ}	V_{IL} or V_{IH}	-	5.5	-	-	±0.5	±5	-	-	±10	µA
SIG_{IN}, $COMP_{IN}$ Input Resistance	R_I	V_I at Self-Bias Operation Point: ΔV, 0.5V, See Figure 8		4.5	-	250	-	-	-	-	-	kΩ
DEMODULATOR SECTION												
Resistor Range	R_S	at R_S > 300kΩ Leakage Current Can Influence V_{DEMOUT}		4.5	10	-	300	-	-	-	-	kΩ
Offset Voltage VCO_{IN} to V_{DEM}	V_{OFF}	$V_I = V_{VCOIN} = \frac{V_{CC}}{2}$ Values taken over R_S Range See Figure 15		4.5	-	±20	-	-	-	-	-	mV
Dynamic Output Resistance at DEM_{OUT}	R_O	$V_{DEMOUT} = \frac{V_{CC}}{2}$		4.5	-	25	-	-	-	-	-	Ω
Quiescent Device Current	I_{CC}	V_{CC} or GND	-	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 4)	V_{CC} -2.1 (Excluding Pin 5)	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

2. The value for R1 and R2 in parallel should exceed 2.7kΩ; R1 and R2 values above 300kΩ may contribute to frequency shift due to leakage currents.
3. The maximum operating voltage can be as high as V_{CC} -0.9V, however, this may result in an increased offset voltage.
4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
INH	1

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES											
PHASE COMPARATOR SECTION											
Propagation Delay SIG_{IN}, $COMP_{IN}$ to PC_{1OUT}	t_{PLH}, t_{PHL}		2	-	-	200	-	250	-	300	ns
			4.5	-	-	40	-	50	-	60	ns
			6	-	-	34	-	43	-	51	ns
Output Transition Time	t_{THL}, t_{TLH}		2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Enable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PZH}, t_{PZL}		2	-	-	280	-	350	-	420	ns
			4.5	-	-	56	-	70	-	84	ns
			6	-	-	48	-	60	-	71	ns
Output Disable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PHZ}, t_{PLZ}		2	-	-	325	-	405	-	490	ns
			4.5	-	-	65	-	81	-	98	ns
			6	-	-	55	-	69	-	83	ns
AC Coupled Input Sensitivity ($_{P-P}$) at SIG_{IN} or $COMP_{IN}$		$V_{I(P-P)}$	3	-	11	-	-	-	-	-	mV
			4.5	-	15	-	-	-	-	-	mV
			6	-	33	-	-	-	-	-	mV
VCO SECTION											
Frequency Stability with Temperature Change	$\frac{\Delta f}{\Delta T}$	R_1 = 100kΩ, R_2 = ∞	3	-	-	-	Typ 0.11		-	-	%/°C
			4.5	-	-	-			-	-	%/°C
			6	-	-	-			-	-	%/°C
Maximum Frequency	f_{MAX}	C_1 = 50pF, R_1 = 3.5kΩ, R_2 = ∞	3	-	-	-	-	-	-	-	MHz
			4.5	-	24	-	-	-	-	-	MHz
			6	-	-	-	-	-	-	-	MHz
		C_1 = 0pF, R_1 = 9.1kΩ, R_2 = ∞	3	-	-	-	-	-	-	-	MHz
			4.5	-	38	-	-	-	-	-	MHz
			6	-	-	-	-	-	-	-	MHz
Center Frequency	f_o	C_1 = 40pF, R_1 = 3kΩ, R_2 = ∞, VCO_{IN} = V_{CC}/2	3	7	10	-	-	-	-	-	MHz
			4.5	12	17	-	-	-	-	-	MHz
			6	14	21	-	-	-	-	-	MHz
Frequency Linearity	Δf_{VCO}	R_1 = 100kΩ, R_2 = ∞, C_1 = 100pF	3	-	-	-	-	-	-	-	%
			4.5	-	0.4	-	-	-	-	-	%
			6	-	-	-	-	-	-	-	%

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Offset Frequency		R_2 = 220kΩ, C_1 = 1nF	3	-	-	-	-	-	-	-	kHz
			4.5	-	400	-	-	-	-	-	kHz
			6	-	-	-	-	-	-	-	kHz
DEMODULATOR SECTION											
V_{OUT} vs f_{IN}		R_1 = 100kΩ, R_2 = ∞, C_1 = 100pF, R_5 = 10kΩ, R_3 = 100kΩ, C_2 = 100pF	3	-	-	-	-	-	-	-	mV/kHz
			4.5	-	330	-	-	-	-	-	mV/kHz
			6	-	-	-	-	-	-	-	mV/kHz
HCT TYPES											
PHASE COMPARATOR SECTION											
Propagation Delay SIG_{IN}, $COMP_{IN}$ to PC_{1OUT}	t_{PLH}, t_{PHL}		4.5	-	-	45	-	56	-	68	ns
Output Transition Time	t_{THL}, t_{TLH}		4.5	-	-	15	-	19	-	22	ns
Output Enable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PZH}, t_{PZL}		4.5	-	-	60	-	75	-	90	ns
Output Disable Time, SIG_{IN}, $COMP_{IN}$ to PCZ_{OUT}	t_{PHZ}, t_{PLZ}		4.5	-	-	70	-	86	-	105	ns
AC Coupled Input Sensitivity ($_{P-P}$) at SIG_{IN} or $COMP_{IN}$		$V_{I(P-P)}$	3	-	11	-	-	-	-	-	mV
			4.5	-	15	-	-	-	-	-	mV
			6	-	33	-	-	-	-	-	mV
VCO SECTION											
Frequency Stability with Temperature Change	$\frac{\Delta f}{\Delta T}$	R_1 = 100kΩ, R_2 = ∞	4.5	-	-	-	Typ 0.11		-	-	%/°C
Maximum Frequency	f_{MAX}	C_1 = 50pF, R_1 = 3.5kΩ, R_2 = ∞	4.5	-	24	-	-	-	-	-	MHz
		C_1 = 0pF, R_1 = 9.1kΩ, R_2 = ∞	4.5	-	38	-	-	-	-	-	MHz
Center Frequency	f_0	C_1 = 40pF, R_1 = 3kΩ, R_2 = ∞, VCO_{IN} = V_{CC}/2	4.5	12	17	-	-	-	-	-	MHz
Frequency Linearity	Δf_{VCO}	R_1 = 100kΩ, R_2 = ∞, C_1 = 100pF	4.5	-	0.4	-	-	-	-	-	%
Offset Frequency		R_2 = 220kΩ, C_1 = 1nF	4.5	-	400	-	-	-	-	-	kHz
DEMODULATOR SECTION											
V_{OUT} vs f_{IN}		R_1 = 100kΩ, R_2 = ∞, C_1 = 100pF, R_5 = 10kΩ, R_3 = 100kΩ, C_2 = 100pF	4.5	-	330	-	-	-	-	-	mV/kHz

Test Circuits and Waveforms

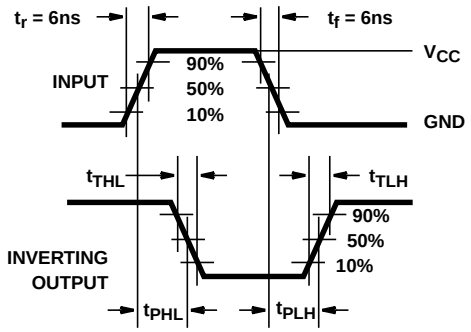


FIGURE 10. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

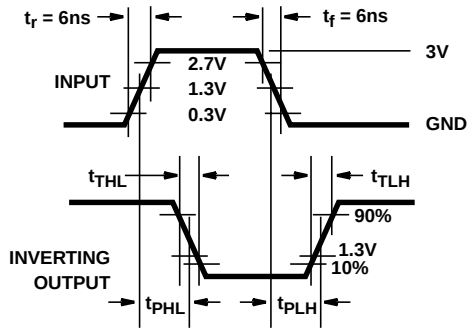


FIGURE 11. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Typical Performance Curves

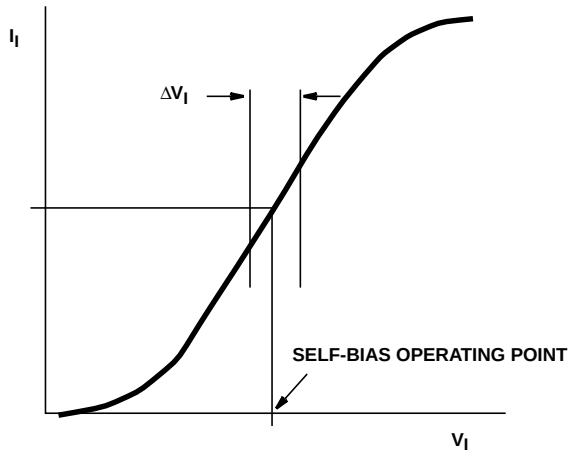


FIGURE 12. TYPICAL INPUT RESISTANCE CURVE AT SIG_{IN}, $COMP_{IN}$

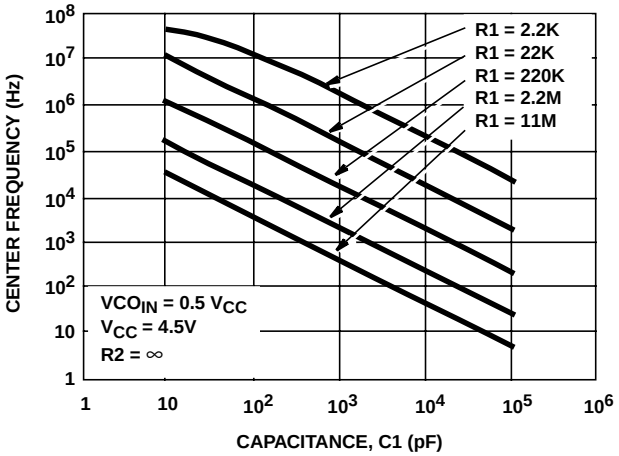


FIGURE 13. HC7046A TYPICAL CENTER FREQUENCY vs R1, C1

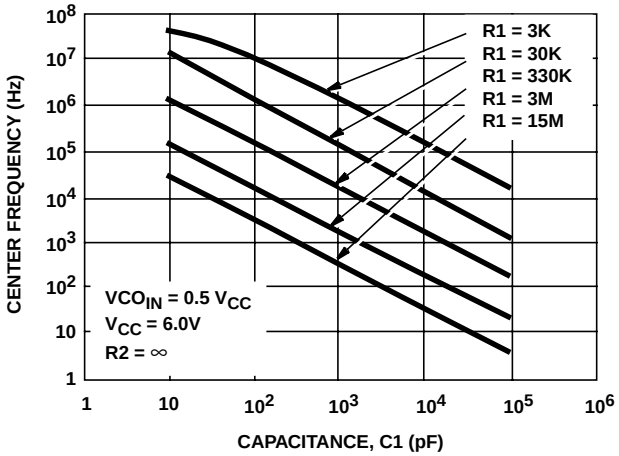


FIGURE 14. HC7046A TYPICAL CENTER FREQUENCY vs R1, C1

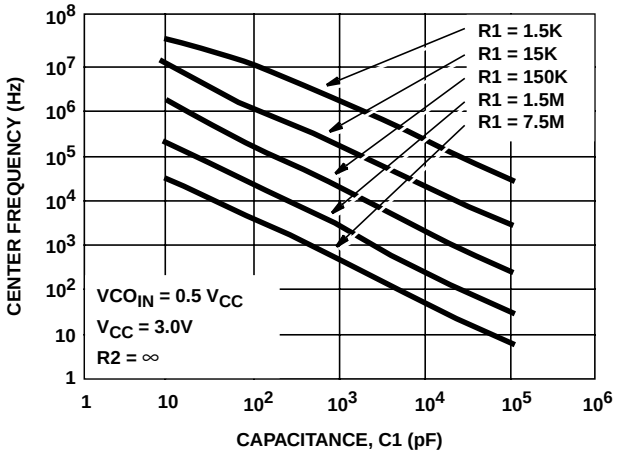


FIGURE 15. HC7046A TYPICAL CENTER FREQUENCY vs R1, C1

Typical Performance Curves (Continued)

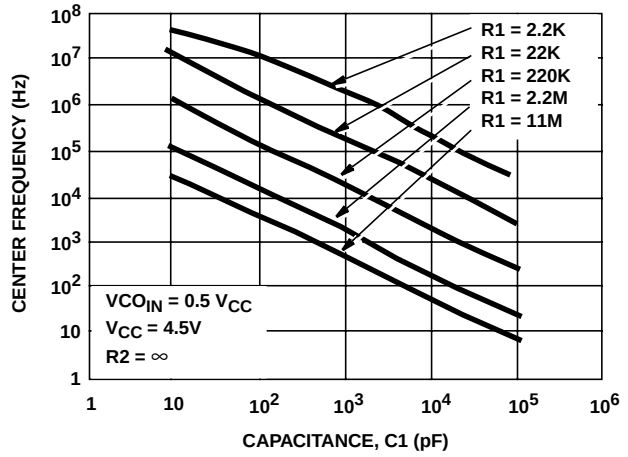


FIGURE 16. HCT7046A TYPICAL CENTER FREQUENCY vs R1, C1

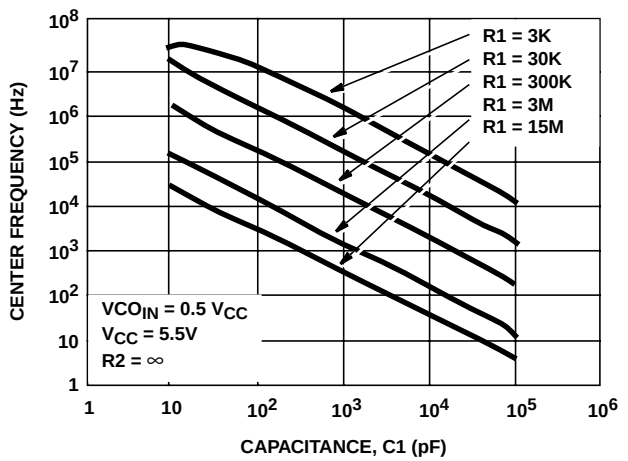


FIGURE 17. HCT7046A TYPICAL CENTER FREQUENCY vs R1, C1

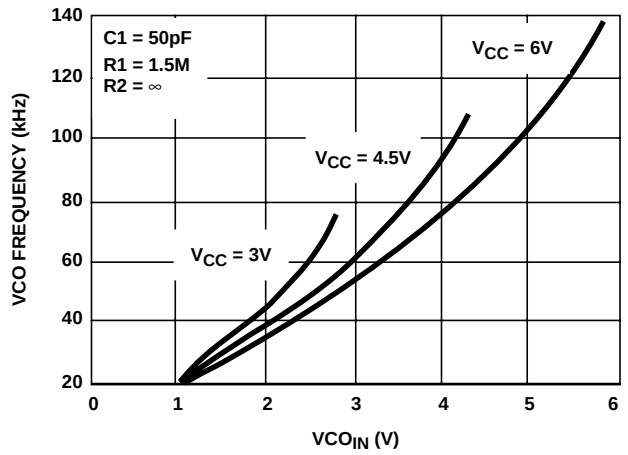


FIGURE 18. HC7046A TYPICAL VCO FREQUENCY vs VCO_{IN}

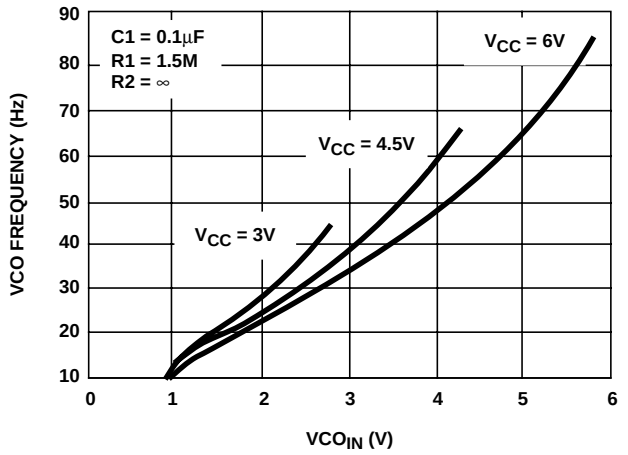


FIGURE 19. HC7046A TYPICAL VCO FREQUENCY vs VCO_{IN} ($R1 = 1.5M\Omega$, $C1 = 0.1\mu F$)

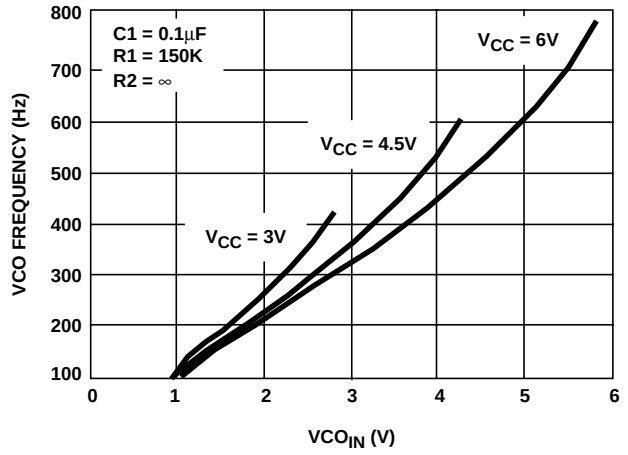


FIGURE 20. HC7046A TYPICAL VCO FREQUENCY vs VCO_{IN} ($R1 = 150k\Omega$, $C1 = 0.1\mu F$)

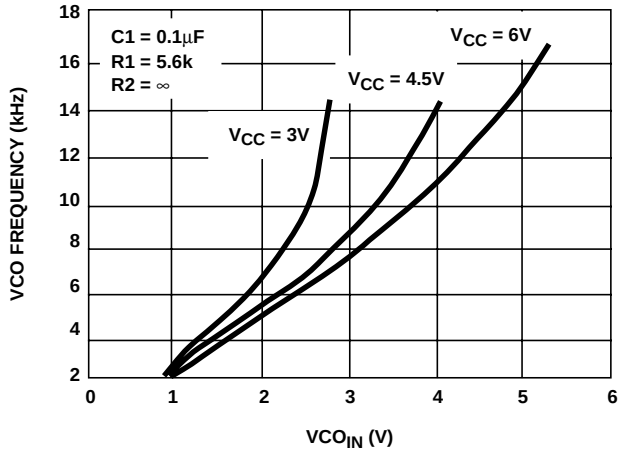


FIGURE 21. HC7046A TYPICAL VCO FREQUENCY vs VCO_{IN} ($R1 = 5.6k\Omega$, $C1 = 0.1\mu F$)

Typical Performance Curves (Continued)

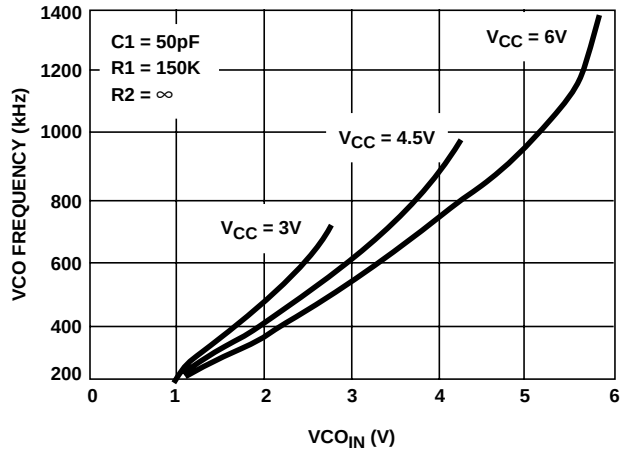


FIGURE 22. HC7046A TYPICAL VCO FREQUENCY vs VCO_{IN} ($R1 = 150k\Omega$, $C1 = 0.1\mu F$)

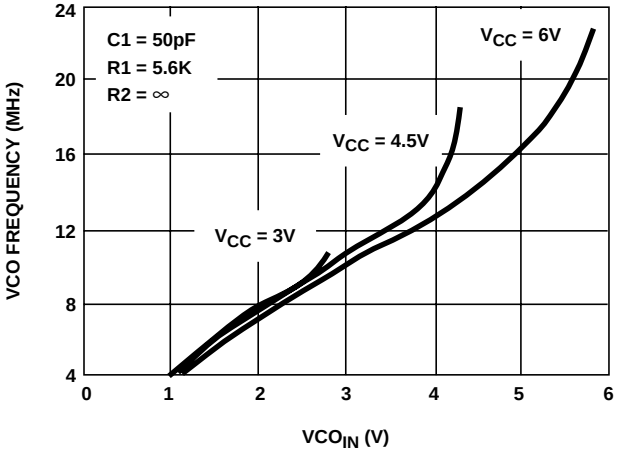


FIGURE 23. HC7046A TYPICAL VCO FREQUENCY vs VCO_{IN} ($R1 = 5.6k\Omega$, $C1 = 50pF$)

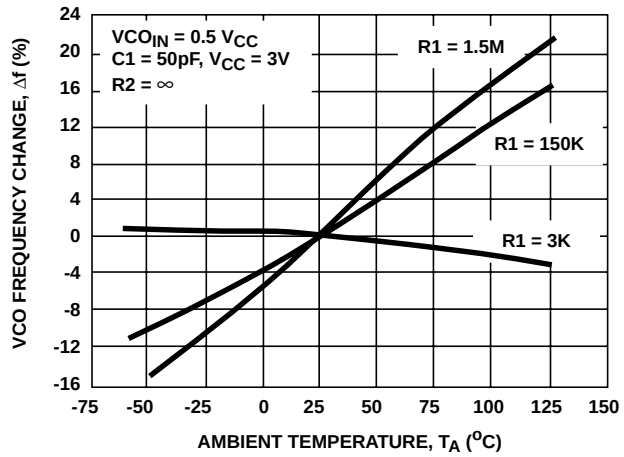


FIGURE 24. HC7046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1 (V_{CC} = 3V)

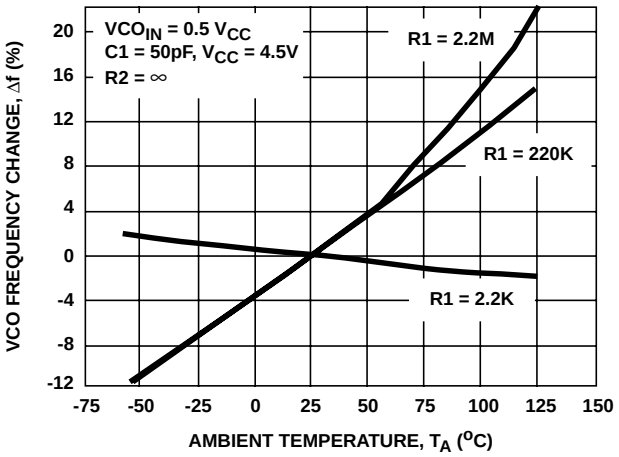


FIGURE 25. HC7046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1

Typical Performance Curves (Continued)

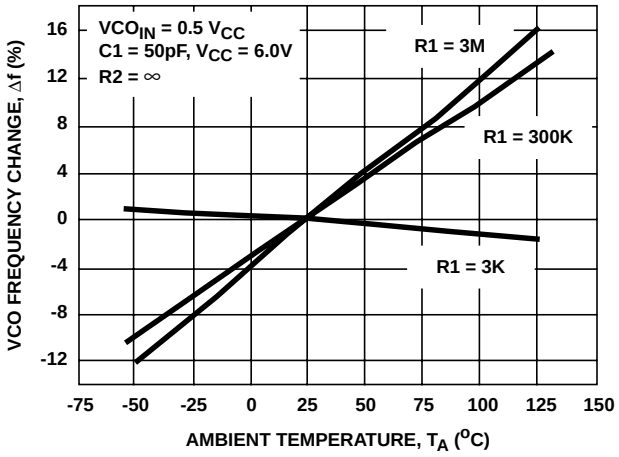


FIGURE 26. HC7046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1

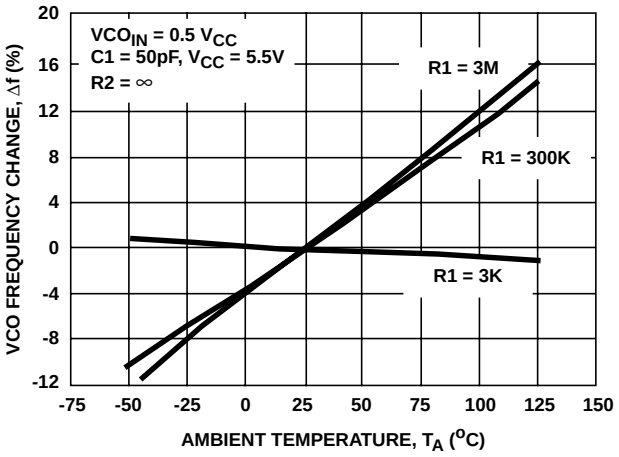


FIGURE 27. HCT7046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1

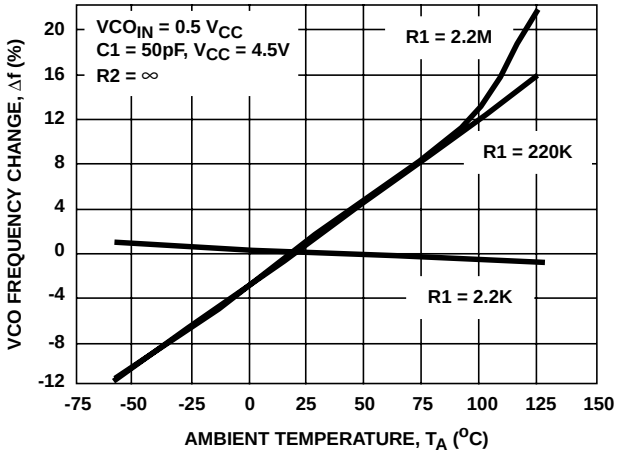


FIGURE 28. HC7046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1

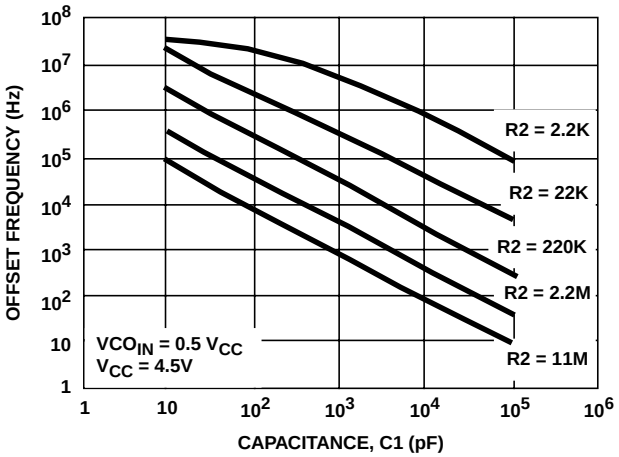


FIGURE 29. HC7046A OFFSET FREQUENCY vs R2, C1

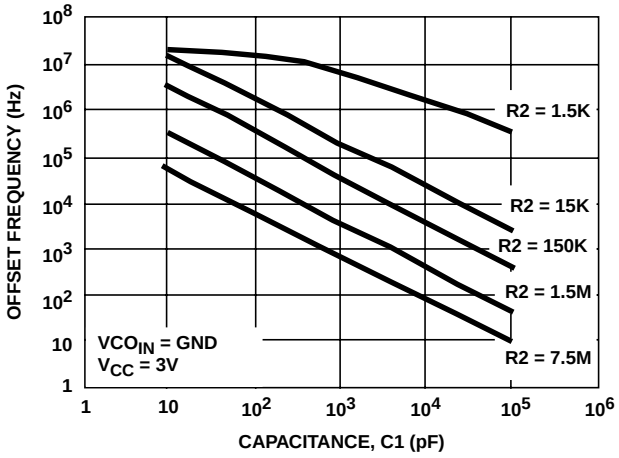


FIGURE 30. HC7046A OFFSET FREQUENCY vs R2, C1

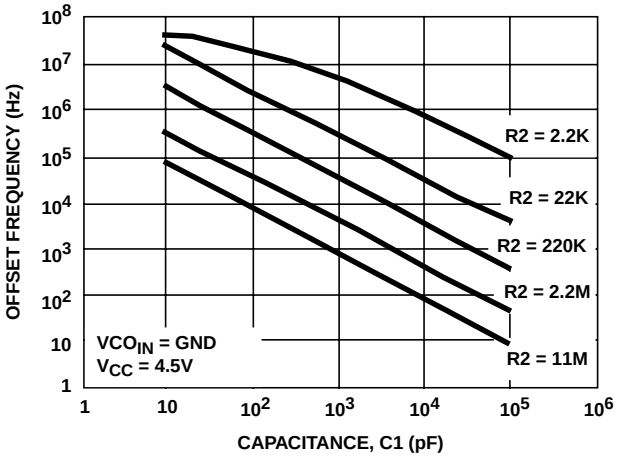


FIGURE 31. HCT7046A OFFSET FREQUENCY vs R2, C1

Typical Performance Curves (Continued)

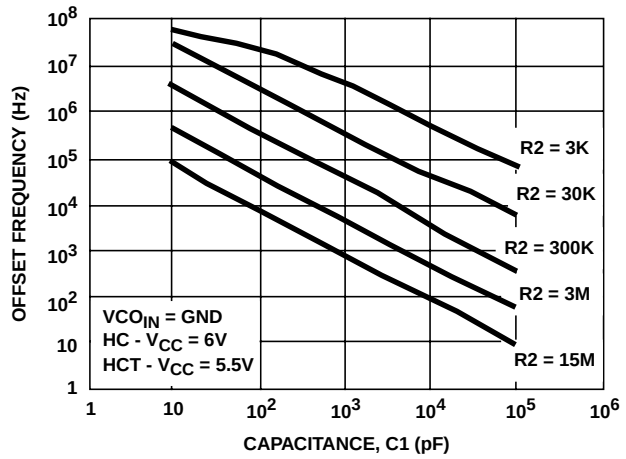


FIGURE 32. HC7046A AND HCT7046A OFFSET FREQUENCY vs R2, C1

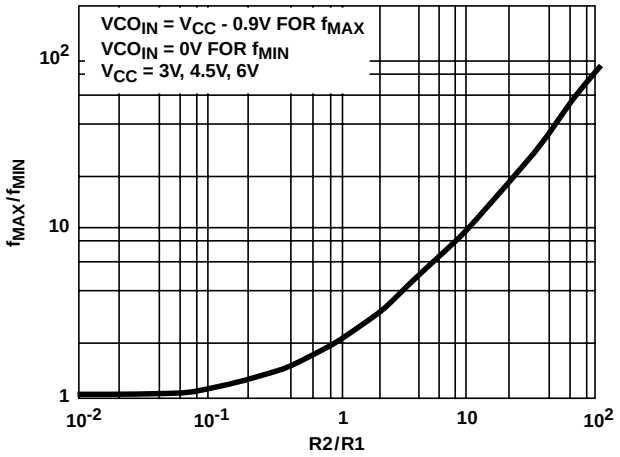


FIGURE 33. HC7046A f_{MIN}/f_{MAX} vs R2/R1

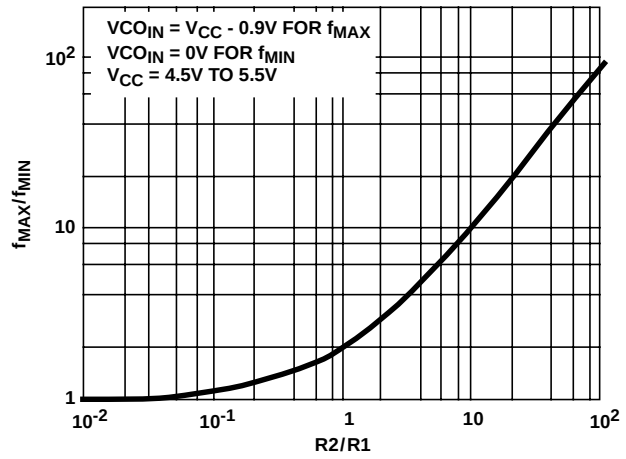


FIGURE 34. HCT7046A f_{MAX}/f_{MIN} vs R2/R1

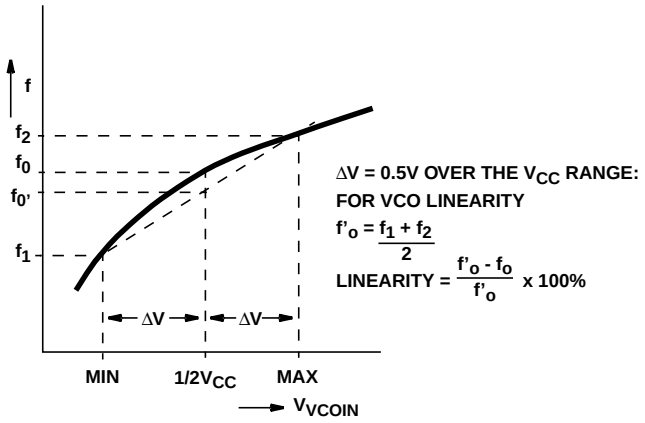


FIGURE 35. DEFINITION OF VCO FREQUENCY LINEARITY

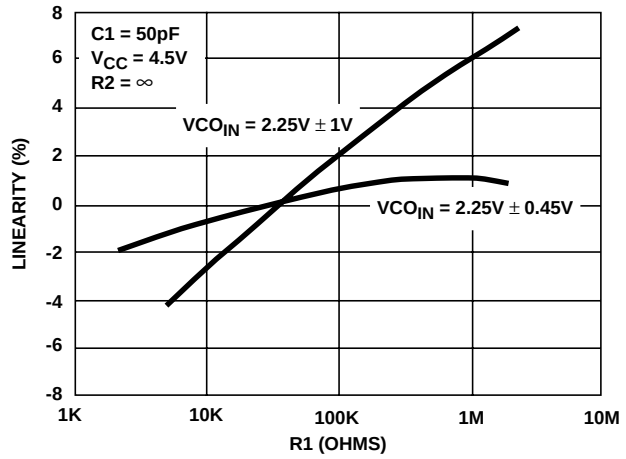


FIGURE 36. HC7046A VCO LINEARITY vs R1

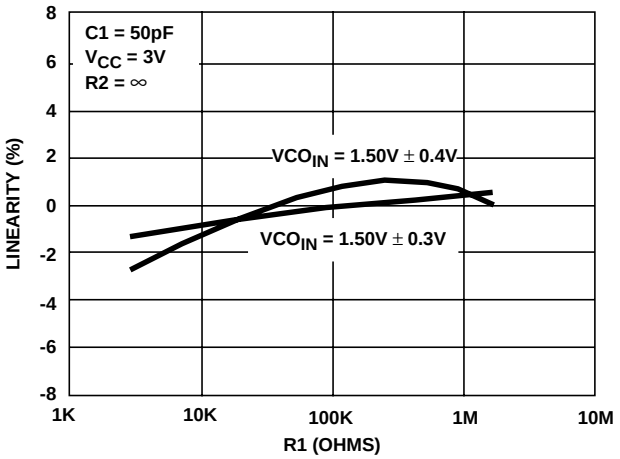


FIGURE 37. HC7046A VCO LINEARITY vs R1

Typical Performance Curves (Continued)

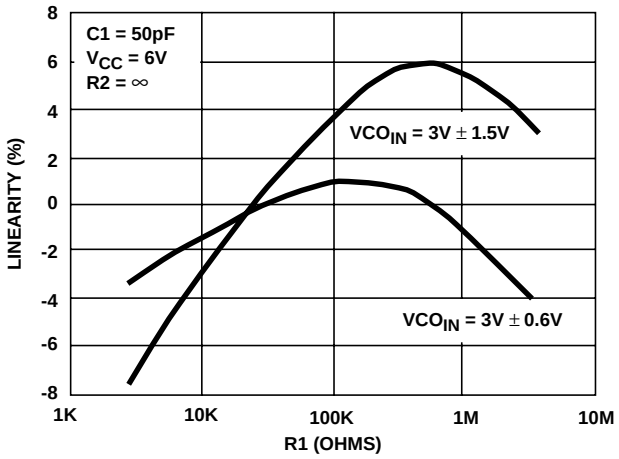


FIGURE 38. HC7046A VCO LINEARITY vs R1

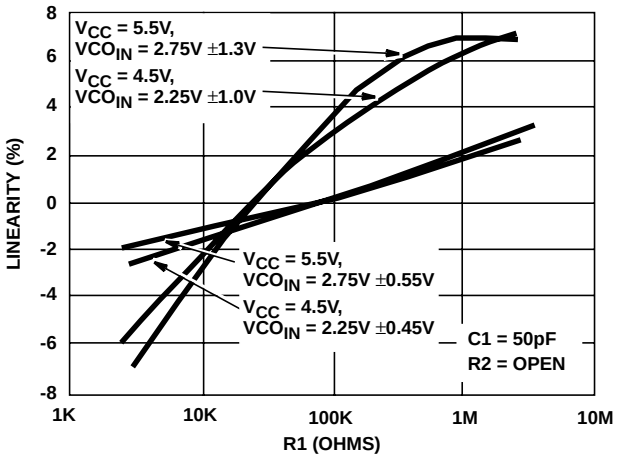


FIGURE 39. HCT7046A VCO LINEARITY vs R1

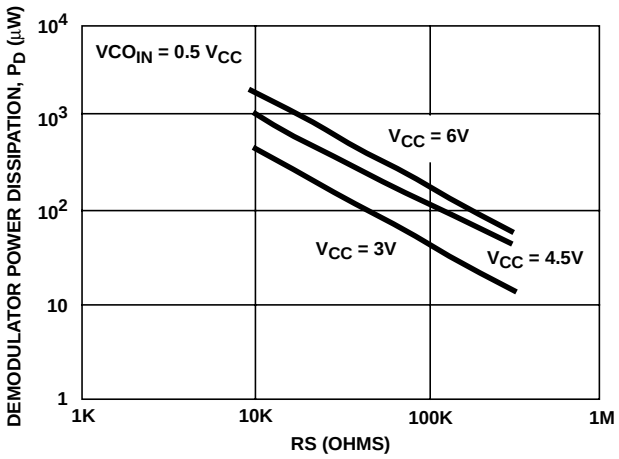


FIGURE 40. HC7046A DEMODULATOR POWER DISSIPATION vs RS (TYP)

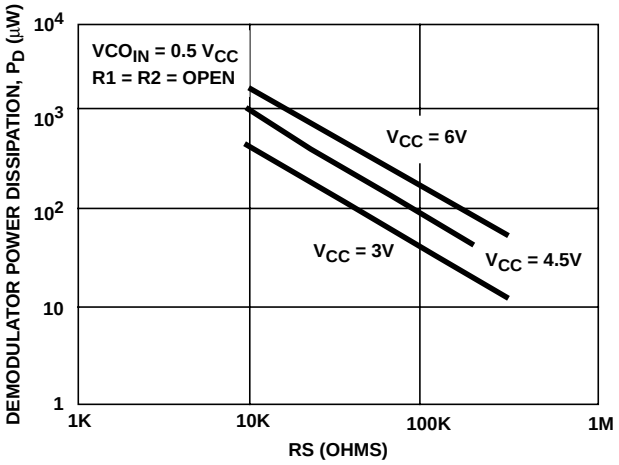


FIGURE 41. HCT7046A DEMODULATOR POWER DISSIPATION vs RS (TYP) (V_{CC} = 3V, 4.5V, 6V)

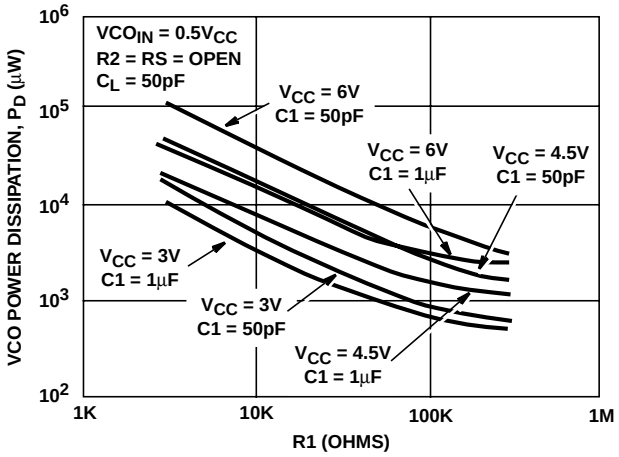


FIGURE 42. HC7046A VCO POWER DISSIPATION vs R1 (C1 = 50pF, 1µF)

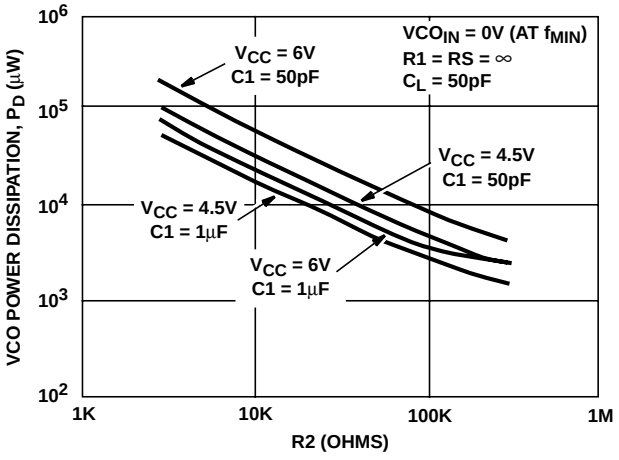


FIGURE 43. HCT7046A VCO POWER DISSIPATION vs R2 (C1 = 50pF, 1µF)

Typical Performance Curves (Continued)

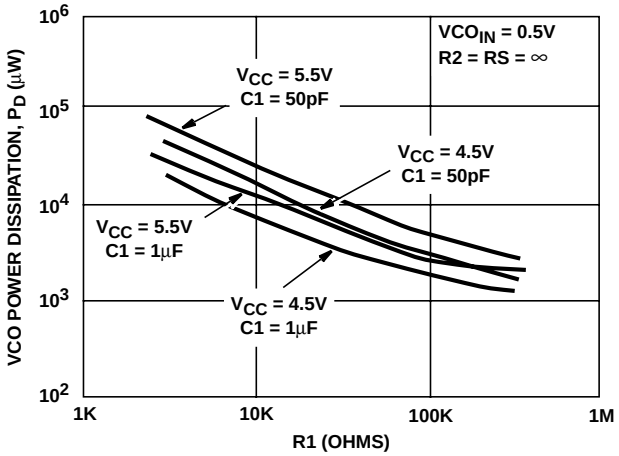


FIGURE 44. HCT7046A VCO POWER DISSIPATION vs R1 (C1 = 50pF, 1μF)

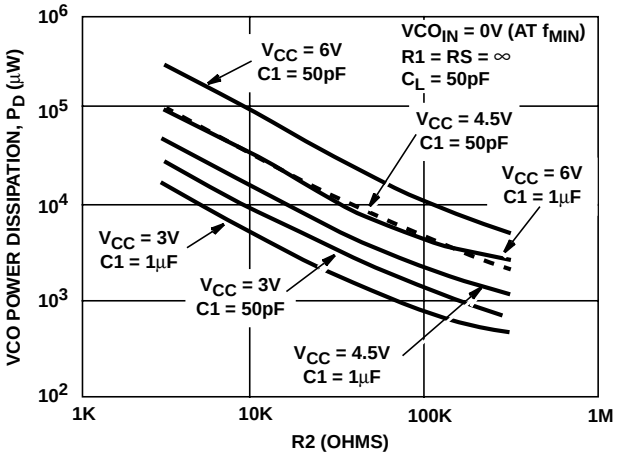


FIGURE 45. HC7046A VCO POWER DISSIPATION vs R2 (C1 = 50pF, 1μF)

HC/HCT7046A C_{PD}

CHIP SECTION	HC	HCT	UNIT
Comparator 1	48	50	pF
Comparator 2	39	48	pF
VCO	61	53	pF

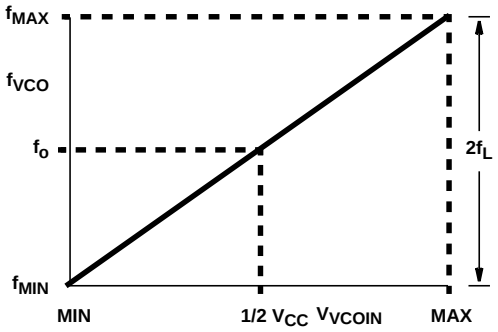
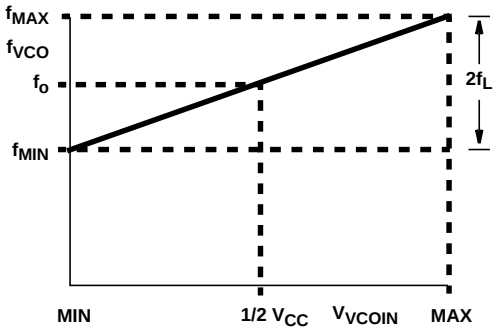
Application Information

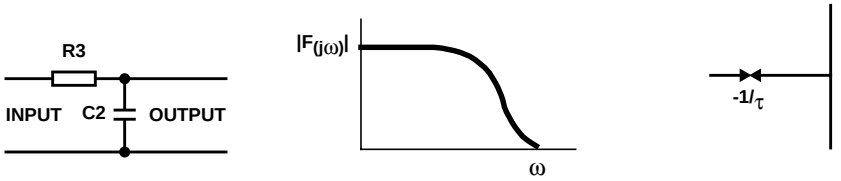
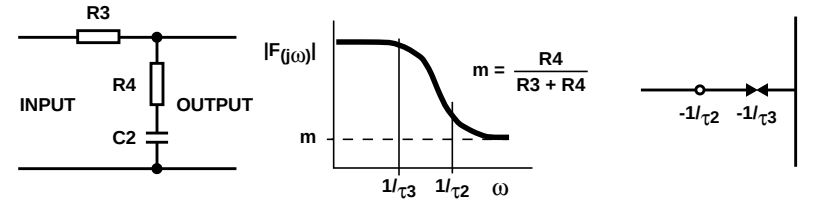
This information is a guide for the approximation of values of external components to be used with the CD74HC7046A and CD74HCT7046A in a phase-lock-loop system.

References should be made to Figures 13 through 23 and Figures 36 through 41 as indicated in the table.

Values of the selected components should be within the following ranges:

R1	> 3kΩ;
R2	> 3kΩ;
R1 || R2	parallel value > 2.7kΩ;
C1	greater than 40pF

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO Frequency Without Extra Offset ($R2 = \infty$)	PC1 or PC2	VCO Frequency Characteristic The characteristics of the VCO operation are shown in Figures 13 - 23.  **FIGURE 46. FREQUENCY CHARACTERISTIC OF VCO OPERATING WITHOUT OFFSET: f_o = CENTER FREQUENCY: $2f_L$ = FREQUENCY LOCK RANGE**
	PC1	Selection of R1 and C1 Given f_o, determine the values of R1 and C1 using Figures 13 - 17.
	PC2	Given f_{MAX} calculate f_o as $f_{MAX}/2$ and determine the values of R1 and C1 using Figures 13 - 17. To obtain $2f_L$: $2f_L \approx \frac{2(\Delta VCO_{IN})}{R1C1}$ where $0.9V < VCO_{IN} < V_{CC} - 0.9V$ is the range of ΔVCO_{IN}
VCO Frequency with Extra Offset ($R2 > 3k\Omega$)	PC1 or PC2	VCO Frequency Characteristic The characteristics of the VCO operation are shown in Figures 29 - 32.  **FIGURE 47. FREQUENCY CHARACTERISTIC OF VCO OPERATING WITH OFFSET: f_o = CENTER FREQUENCY: $2f_L$ = FREQUENCY LOCK RANGE**
	PC1 or PC2	Selection of R1, R2 and C1 Given f_o and f_L, offset frequency, f_{MIN}, may be calculated from $f_{MIN} \approx f_o - 1.6\ f_L$. Obtain the values of C1 and R2 by using Figures 29 - 32. Calculate the values of R1 from Figures 33 - 34.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL Conditions with No Signal at the SIG_{IN} Input	PC1	VCO adjusts to f_0 with $\phi_{DEMOUT} = 90^o$ and $V_{VCOIN} = 1/2\ V_{CC}$ (see Figure 2)
	PC2	VCO adjusts to f_{MIN} with $\phi_{DEMOUT} = -360^o$ and $V_{VCOIN} = 0V$ (see Figure 4)
PLL Frequency Capture Range	PC1 or PC2	Loop Filter Component Selection  **(A) τ1 = R3 x C2** **(B) AMPLITUDE CHARACTERISTIC** **(C) POLE-ZERO DIAGRAM** A small capture range ($2f_c$) is obtained if $\tau > 2f_c \approx (1/\pi)\ (2\pi f_L/\tau 1.)^{1/2}$ **FIGURE 48. SIMPLE LOOP FILTER FOR PLL WITHOUT OFFSET**
		 **(A) τ2 = R4 x C2; τ3 = (R3 + R4) x C2** **(B) AMPLITUDE CHARACTERISTIC** **(C) POLE-ZERO DIAGRAM** **FIGURE 49. SIMPLE LOOP FILTER FOR PLL WITH OFFSET**
PLL Locks on Harmonics at Center Frequency	PC1	Yes
	PC2	No
Noise Rejection at Signal Input	PC1	High
	PC2	Low
AC Ripple Content when PLL is Locked	PC1	$f_r = 2f_i$, large ripple content at $\phi_{DEMOUT} = 90^o$
	PC2	$f_r = f_i$, small ripple content at $\phi_{DEMOUT} = 0^o$

Lock Detector Circuit

The lock detector feature is very useful in data synchronization, motor speed control, and demodulation. By adjusting the value of the lock detector capacitor so that the lock output will change slightly before actually losing lock, the designer can create an “early warning” indication allowing corrective measures to be implemented. The reverse is also true, especially with motor speed controls, generators, and clutches that must be set up before actual lock occurs or disconnected during loss of lock.

When using phase comparator 1, the detector will only indicate a lock condition on the fundamental frequency and not on the harmonics, which PC1 will lock on.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC7046AE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC7046AE	Samples
CD74HC7046AM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC7046AM	Samples
CD74HC7046AM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC7046AM	Samples
CD74HC7046AMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC7046AM	Samples
CD74HCT7046AE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT7046AE	Samples
CD74HCT7046AEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT7046AE	Samples
CD74HCT7046AM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT7046AM	Samples
CD74HCT7046AM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT7046AM	Samples
CD74HCT7046AMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT7046AM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

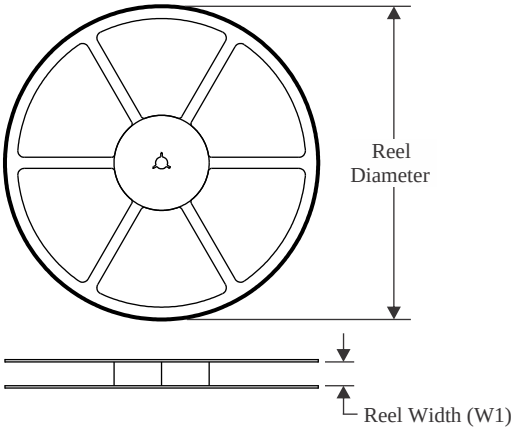
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

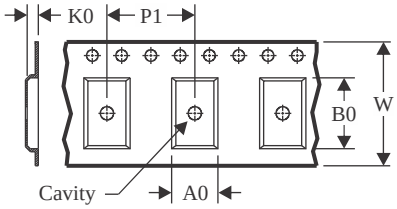
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

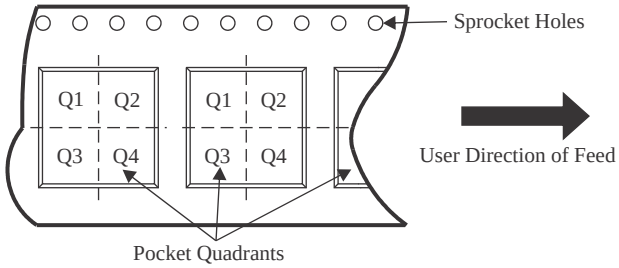


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

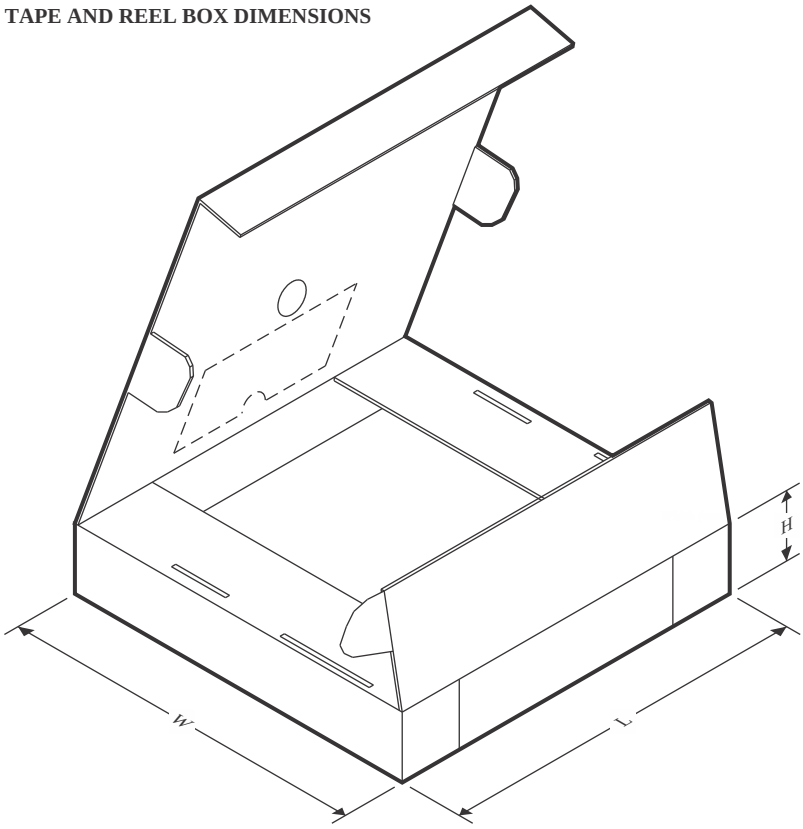
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC7046AM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT7046AM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

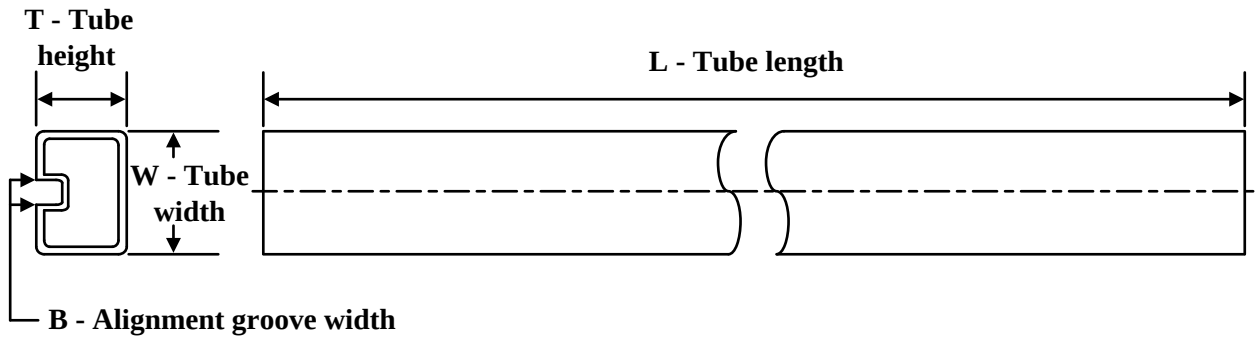
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC7046AM96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT7046AM96	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



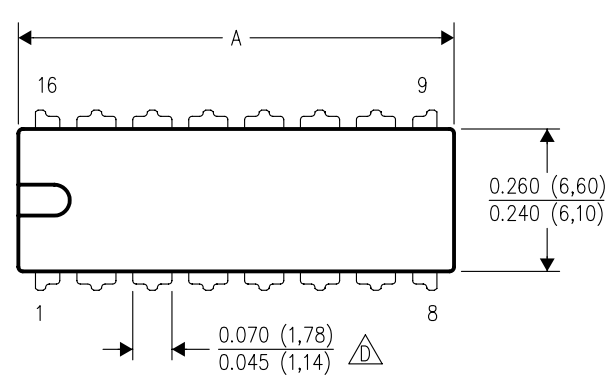
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC7046AE	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC7046AE	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC7046AM	D	SOIC	16	40	507	8	3940	4.32
CD74HCT7046AE	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT7046AE	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT7046AEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT7046AEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT7046AM	D	SOIC	16	40	507	8	3940	4.32

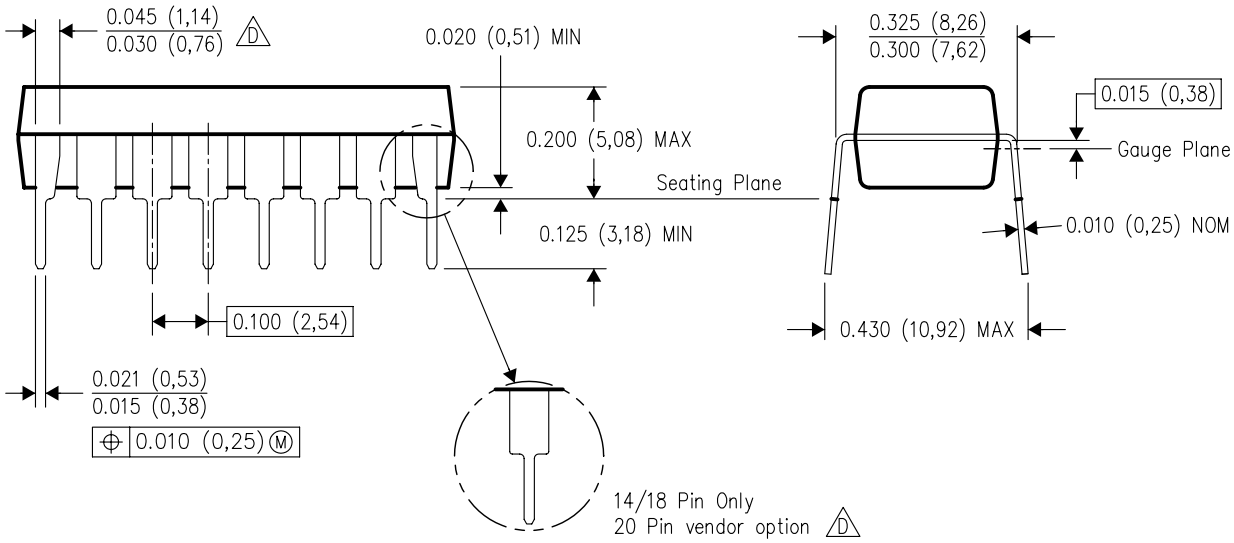
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



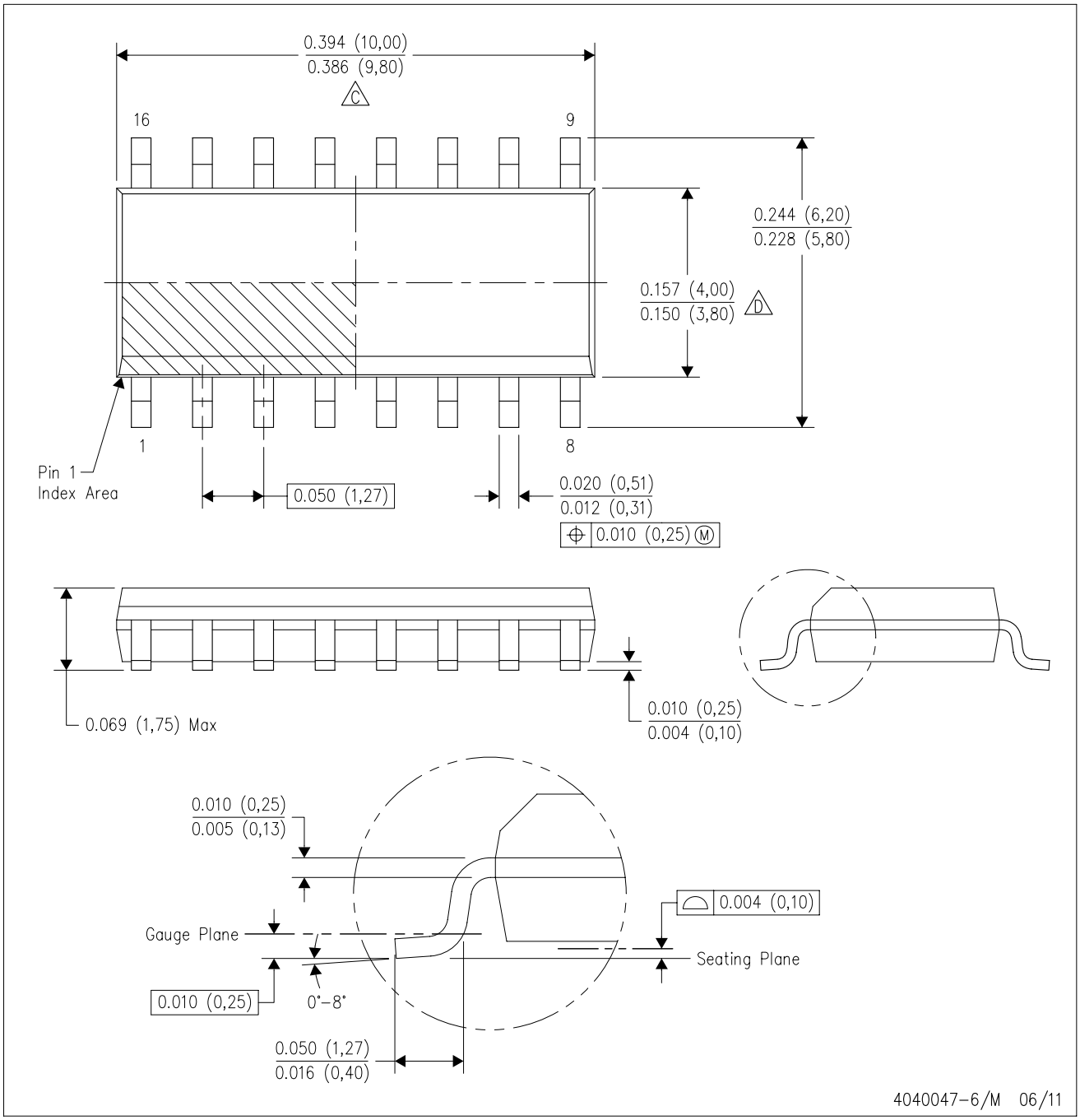
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

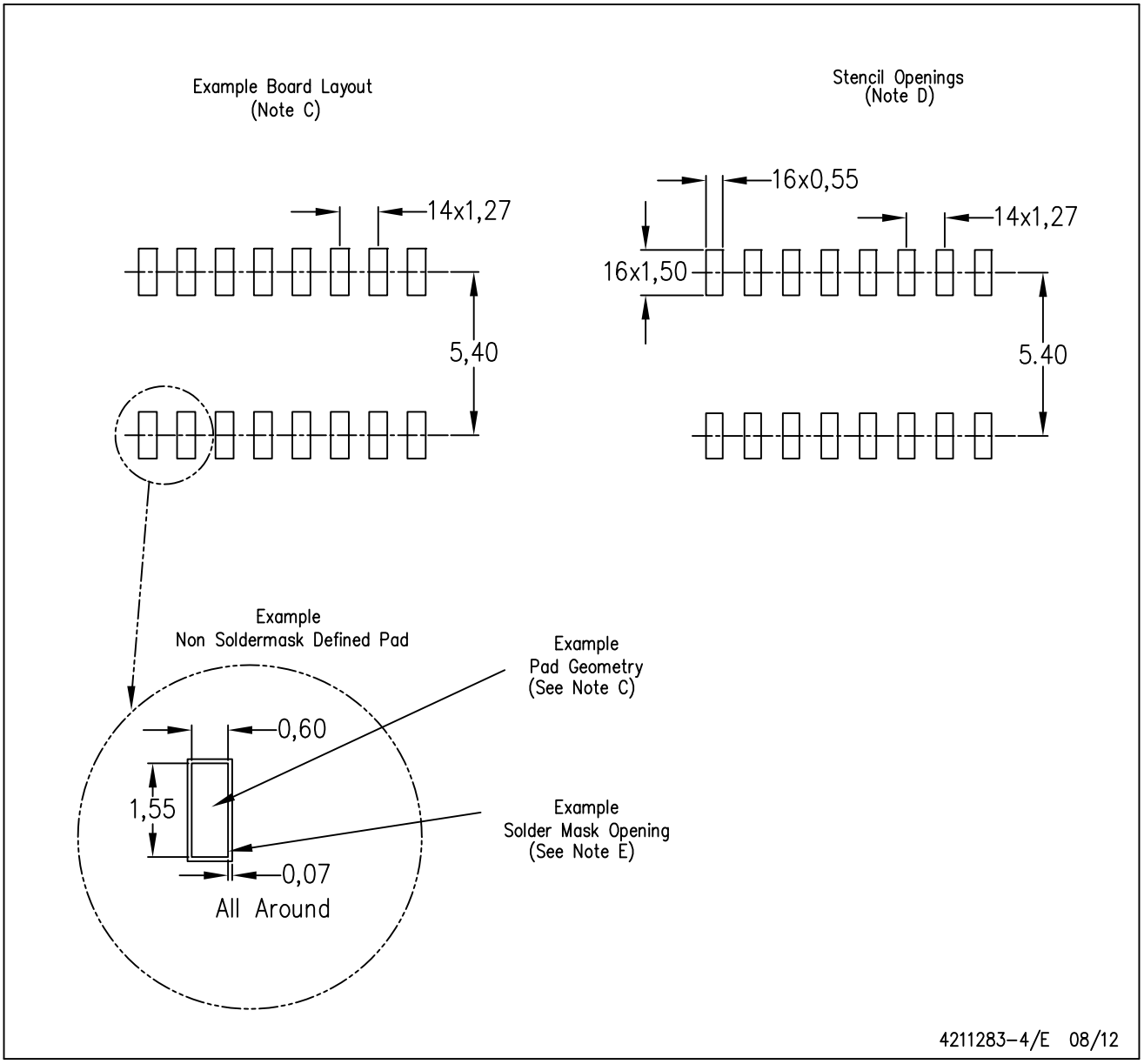
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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