CSI-2/DSI D-PHY Tx IP

User Guide

FPGA-IPUG-02080-2.2

July 2024

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AXI	Advance eXtensible Interface
CSI-2	Camera Serial Interface-2
DSI	Digital Serial Interface
EoTP	End of Transmission Packet
FPGA	Field-Programmable Gate Array
FSM	Finite State Machine
HS	High Speed
LMMI	Lattice Memory Mapped Interface
LP	Low Power

1. Introduction

1.1. Overview of the IP

The Lattice Semiconductor CSI-2/DSI D-PHY Transmitter IP Core converts data bytes from a requestor to either DSI or CSI-2 data format for Lattice Semiconductor CrossLink™-NX, Certus™-NX, CertusPro™-NX, MachXO5™-NX, and Lattice Avant™ family devices as indicated in the dark gray boxes in Figure 1.1.

The CSI-2/DSI D-PHY Transmitter Submodule IP is intended for applications that require a D-PHY transmitter in the FPGA logic.

This IP supports both high-speed (HS) and low power (LP) modes. The payload data uses the high-speed mode whereas the control and status information are sent in low power mode.

The number of D-PHY data lanes for data transmission is configurable. This IP supports 1, 2, 3, or 4 data lanes.

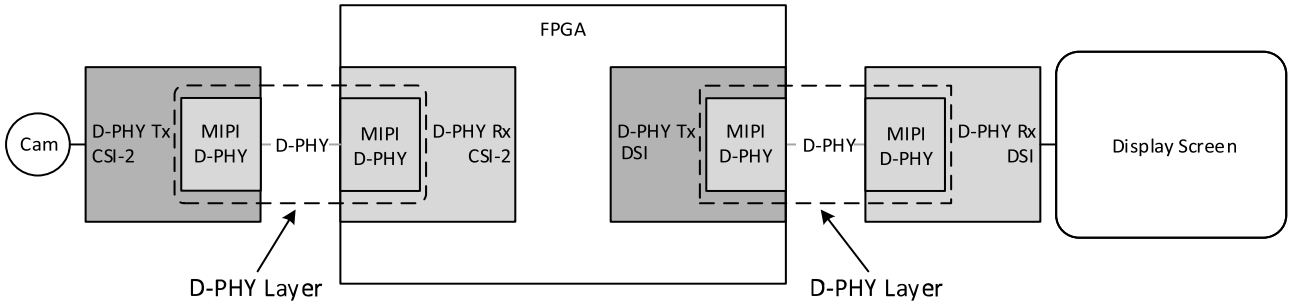

Figure 1.1. D-PHY Tx IP

1.2. Quick Facts

Table 1.1 presents a summary of the CSI-2/DSI DPHY Tx IP Core.

Table 1.1. CSI-2/DSI DPHY Tx IP Core Quick Facts

IP Requirements	Supported FPGA Families	Lattice Avant, MachXO5-NX, CrossLink-NX, CertusPro-NX, Certus-NX
Resource Utilization	Targeted Devices	LAV-AT-E/G/X30, LAV-AT-E/G/X50, LAV-AT-E/G/X70, LFMXO5-25, LFMXO5-55T, LFMXO5-100T, LIFCL-40, LIFCL-33, LIFCL-17, LFCPNX-100, LFCPNX-50, LFD2NX-40, LFD2NX-17
	Supported User Interfaces	LMMI /AXI4-Stream interface
	Resource	See the Resource Utilization section
Design Tool Support	Lattice Implementation	IP Core v1.0.x – Lattice Radiant™ software 2.0 IP Core v1.1.x – Lattice Radiant software 2.1 or later IP Core v1.2.x – Lattice Radiant software 3.0 IP Core v1.9.x for Nexus – Lattice Radiant software 2023.1 IP Core v1.9.x for Avant – Lattice Radiant software 2023.2 IP Core v2.0.x for Nexus – Lattice Radiant software 2024.1 IP Core v2.0.x for Avant – Lattice Radiant software 2024.1
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

1.3. Features

Key features of the CSI-2/DSI DPHY Tx IP include:

- Compliant with MIPI D-PHY v2.1, MIPI DSI v1.3, and MIPI CSI-2 v1.2 specifications.
- Supports 1, 2, 3, or 4 MIPI D-PHY data lanes.
- Supports DSI video modes.
- Supports low-power (LP) mode during vertical and horizontal blanking.
- Option for AXI4-stream interface.

1.3.1. Hard MIPI D-PHY Tx IP Core Features

- Maximum rate up to 2500 Mbps per lane available only in CrossLink-NX devices
- Supported gearing: 8x, 16x
- Option to use the dedicated D-PHY TX PLL or an external clock source
- Internal PLL configurable through LMMI bus
- Option to bypass the Control and Interface Logic (CIL)
- Reference frequency for the internal PLL from 24 MHz to 200 MHz
- Internal PLL output frequency from 80 MHz to 1250 MHz
- Hard D-PHY is supported only on Crosslink-NX devices
- Supports periodic deskew calibration

1.3.2. Soft MIPI D-PHY Tx IP Core Features

- Maximum rate up to 1500 Mbps per lane for Crosslink-NX, Certus-NX, and CertusPro-NX devices
- Maximum rate up to 1800 Mbps per lane for Avant devices
- Supported gearing: 8x
- External clock source
- Soft D-PHY is supported on Lattice Avant, Crosslink-NX, Certus-NX, and CertusPro-NX devices

1.4. Licensing and Ordering Information

An IP specific license string is required to enable full use of the CSI-2/DSI DPHY Tx IP in a complete, top-level design.

The IP can be fully evaluated through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP supports Lattice's IP hardware evaluation capabilities. You can create versions of the IP to operate in hardware for a limited time (approximately four hours) without requiring an IP license string. A license string is required to enable timing simulation and to generate a bitstream file that does not include the hardware evaluation timeout limitation.

For more information about pricing and availability of the CSI-2/DSI DPHY Tx IP, contact your local Lattice Sales Office.

1.4.1. Ordering Part Number

Table 1.2. Ordering Part Number

Device Family	Part Number	
	Single Machine Annual	Multi-Site Perpetual
CrossLink-NX	DPHY-TX-CNX-US	DPHY-TX-CNX-UT
Certus-NX	DPHY-TX-CTNX-US	DPHY-TX-CTNX-UT
CertusPro-NX	DPHY-TX-CPNX-US	DPHY-TX-CPNX-UT
Lattice Avant-E	DPHY-TX-AVE-US	DPHY-TX-AVE-UT
Lattice Avant-G	DPHY-TX-AVG-US	DPHY-TX-AVG-UT
Lattice Avant-X	DPHY-TX-AVX-US	DPHY-TX-AVX-UT
MachXO5-NX	DPHY-TX-XO5-US	DPHY-TX-XO5-UT
Bundled	MIPI-BNDL-US	MIPI-BNDL-UT

1.5. IP Validation Summary

Table 1.3 shows the validation status for the CSI-2/DSI DPHY Tx IP core. The ✓ mark indicates whether the IP has been validated for Simulation, Timing, or with Hardware.

Table 1.3. IP Validation Level

Device Family	IP Version	Validation Level		
		Simulation	Timing	Hardware
Lattice Nexus™	1.9.2	✓	✓	—
Lattice Avant™	1.9.2	✓	✓	—
Lattice Nexus	2.0.0	✓	✓	—
Lattice Avant	2.0.0	✓	✓	—

1.6. Minimum Device Requirements

Refer to the Resource Utilization section for the minimum required resource to instantiate this IP.

1.7. Naming Conventions

1.7.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.7.2. Signal Names

- _*n* are active low (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals
- _*io* are bidirectional signals

2. Functional Description

2.1. IP Architecture Overview

The CSI-2/DSI D-PHY Transmitter IP Core consists of the Global Operation Module, the D-PHY Tx Wrapper Module, an optional Packet Formatter Module, an optional AXI4 Stream Device Receiver, and an optional LMMI Target Module. Figure 2.1 shows the D-PHY Tx IP block with both LMMI Device and AXI4 Stream Device enabled. Figure 2.2 shows the D-PHY Tx IP block with AXI4 Stream Device enabled and LMMI Device disabled. Figure 2.3 shows the D-PHY Tx IP block with AXI4 Stream Device disabled and LMMI Device enabled. Figure 2.4 shows the D-PHY Tx IP block with both AXI4 Stream Device and LMMI Device disabled.

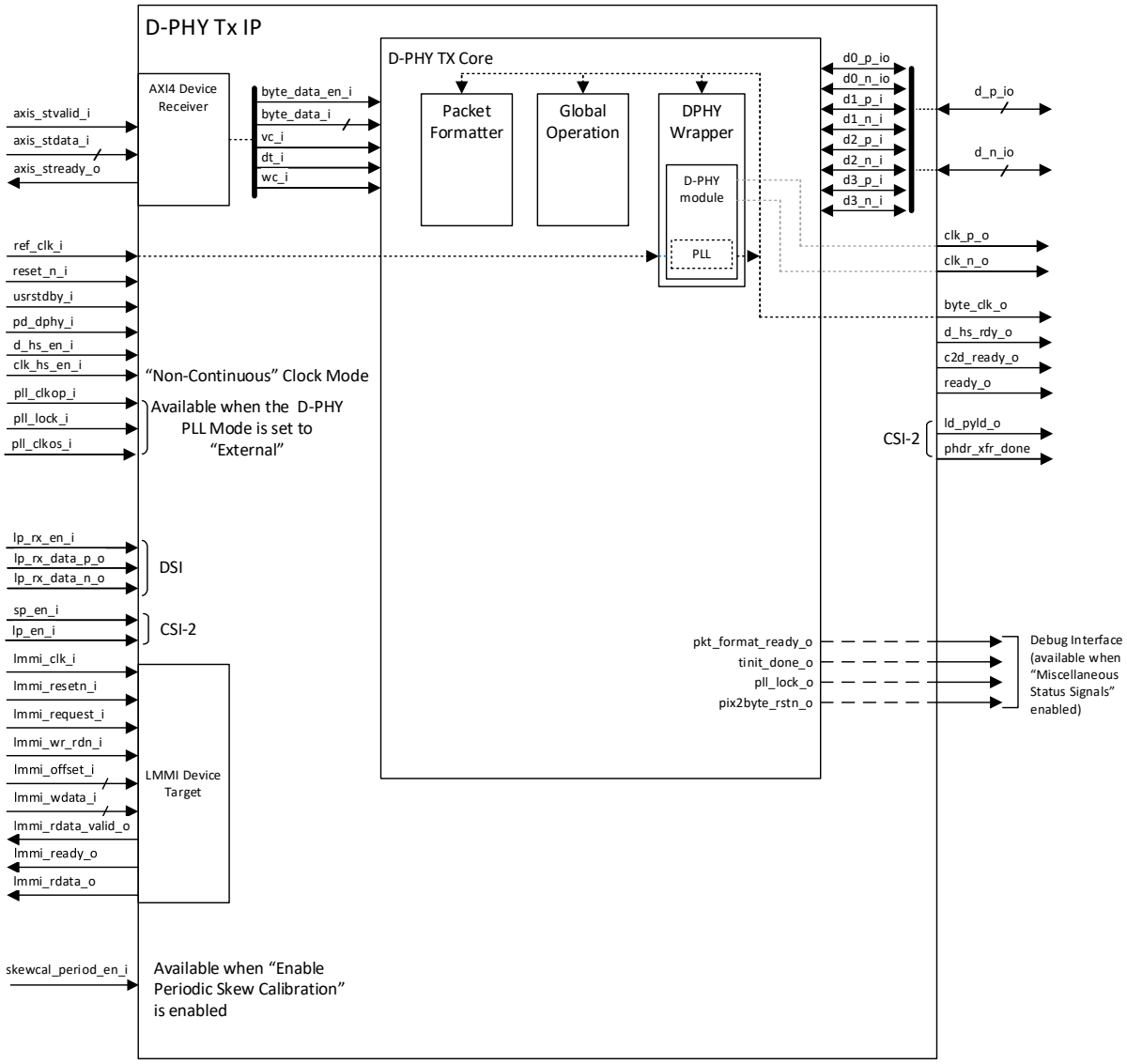

Figure 2.1. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Enabled

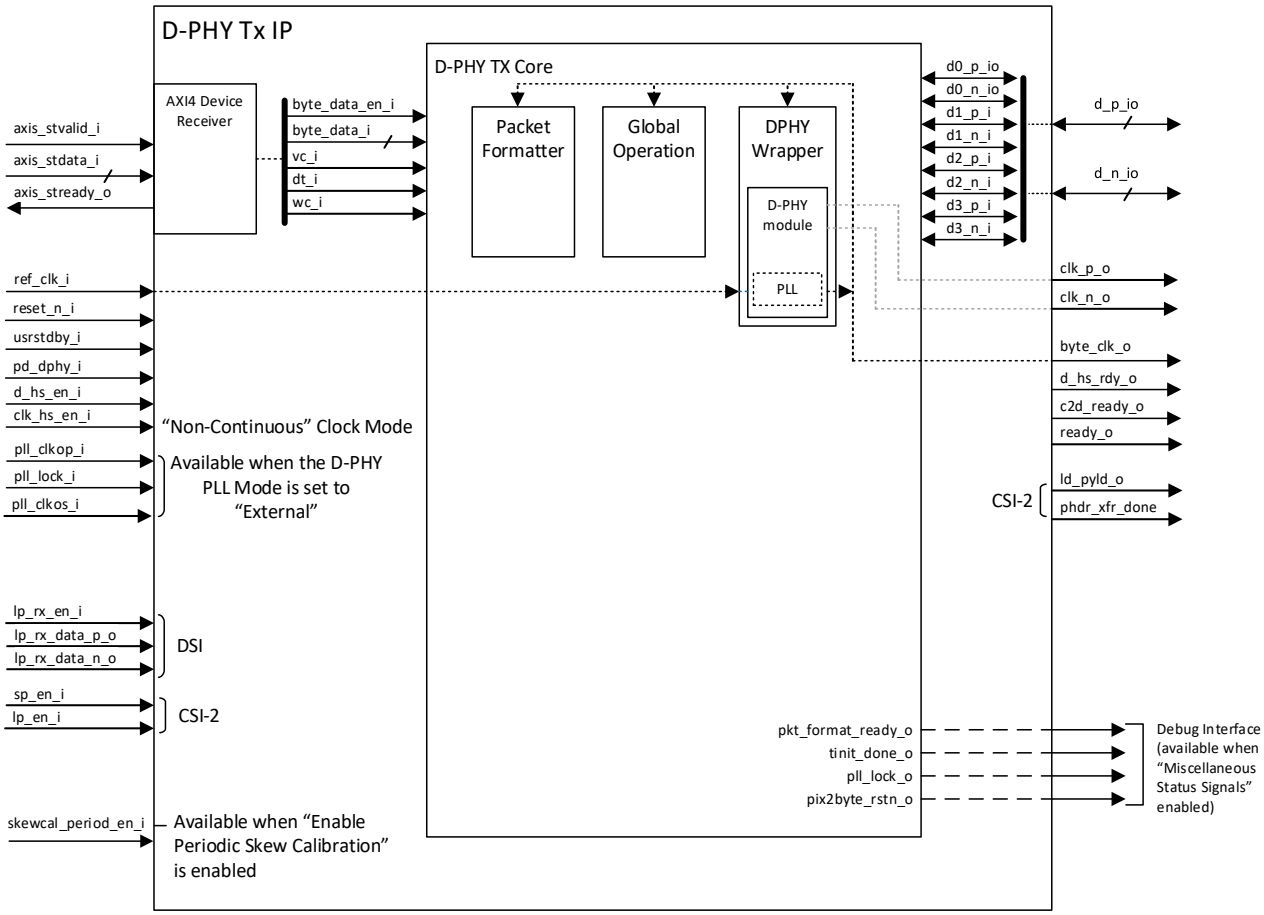

Figure 2.2. D-PHY Tx IP Block Diagram with AXI4-Stream Enabled and LMMI Disabled

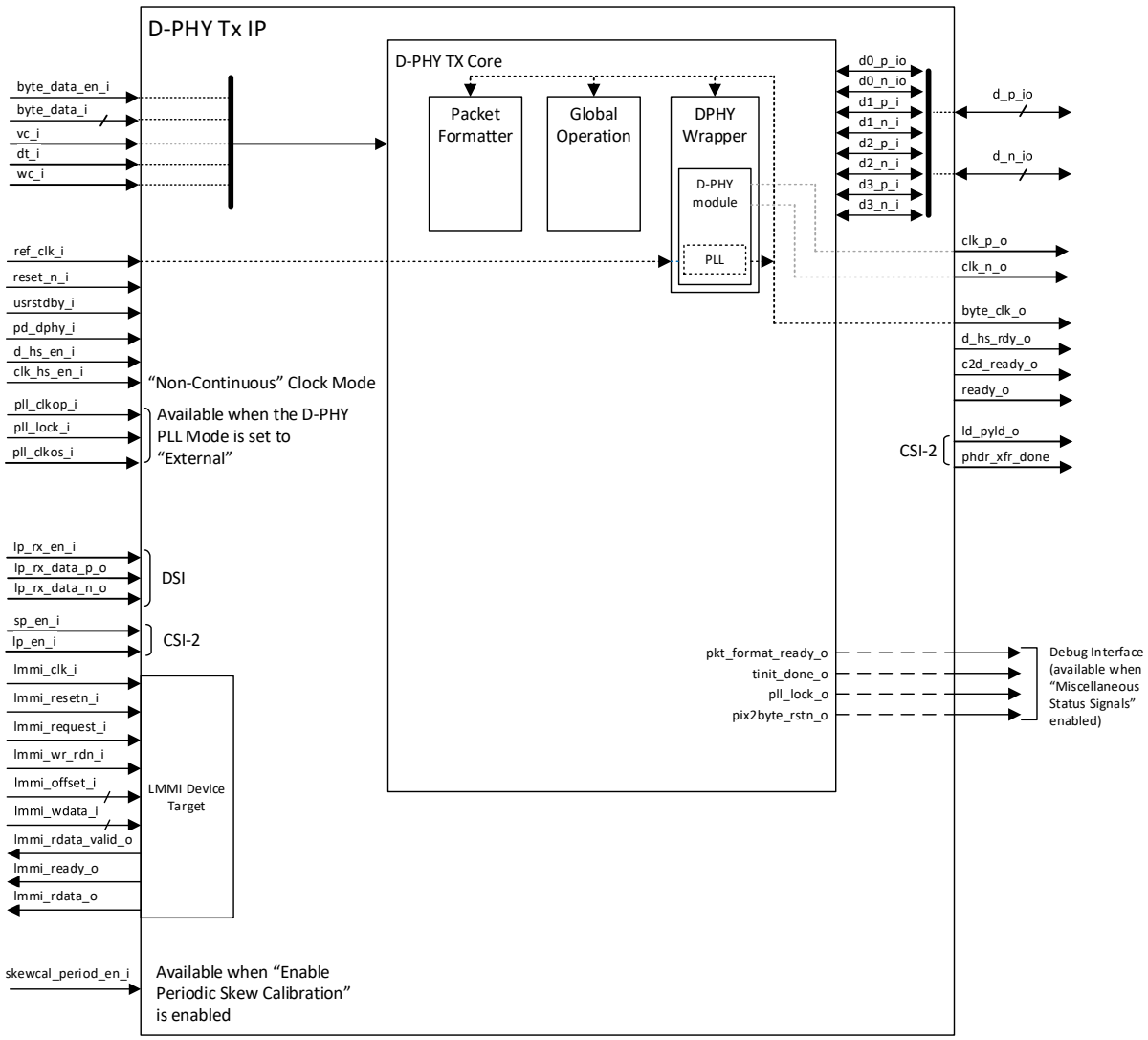

Figure 2.3. D-PHY Tx IP Block Diagram with AXI4-Stream Disabled and LMMI Enabled

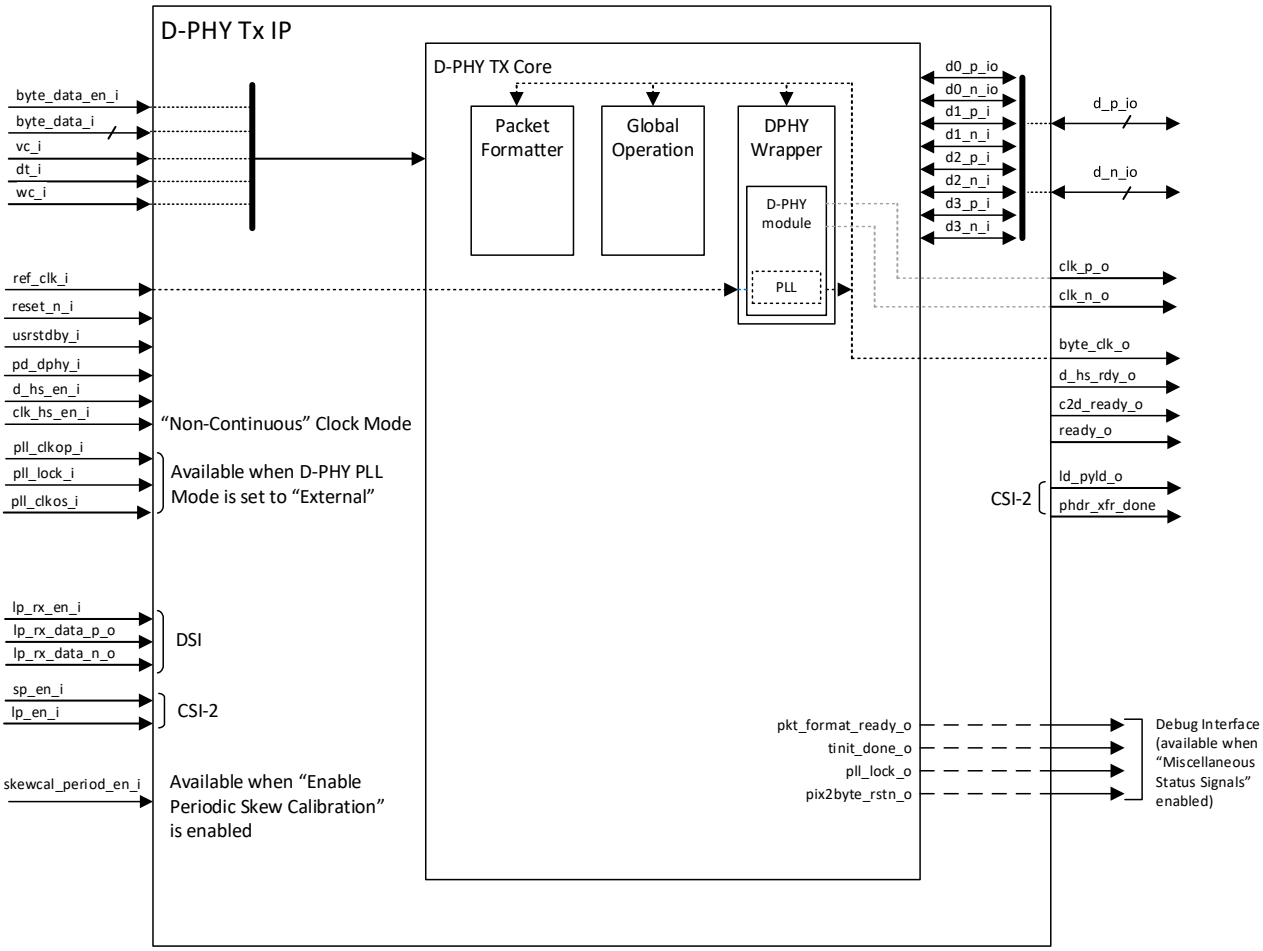

Figure 2.4. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Disabled

2.2. User Interfaces

Table 2.1 lists the available user interface and protocols used on the D-PHY Tx IP.

Table 2.1. User Interfaces and Supported Protocols

User Interface	Supported Protocols	Description
Control	LMMI	Configures the control registers of the D-PHY Tx IP, such as timing parameters.
Device Receiver	AXI4	Interface for receiving payload data (byte data or packet data with virtual channel, data type, and word count).

2.2.1. LMMI Device Target

The LMMI (Lattice Memory Mapped Interface) Device Target Module is used for configuring the control registers of the D-PHY Tx IP.

For more information on LMMI, see Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

If the LMMI bus is not enabled, the Hard D-PHY configuration registers take on the corresponding values based on the IP configuration set in the user interface. See the Register Description section for the list of the configuration registers.

An example of how the $T_{HS\text{-}TRAIL}$ timing parameter changes depending on u_PRG_HS_TRAIL[5:0] register is given in Table 2.2.

Table 2.2. High-Speed Trail Timer for Different Data Rates

Data Rate	Min (ns)	Max (ns)	u_PRG_HS_TRAIL [5:0]	THS-TRAIL (ns)
2.5 Gbps	61.6	109.8	011000	76.8
1.5 Gbps	62.67	113	001111	80
1.0 Gbps	64	117	001100	96
500 Mbps	68	129	000110	96
250 Mbps	79	153	000100	128
80 Mbps	110	255	000010	200

The other timing parameters can be changed by changing corresponding registers following the same logic.

2.2.2. AXI4-Stream Device Receiver

AXI4-Stream device receiver provides an interface for receiving payload data (byte data or packet data with virtual channel and cata type and word count). Figure 2.5 shows data format when AXI4-Stream is ON.

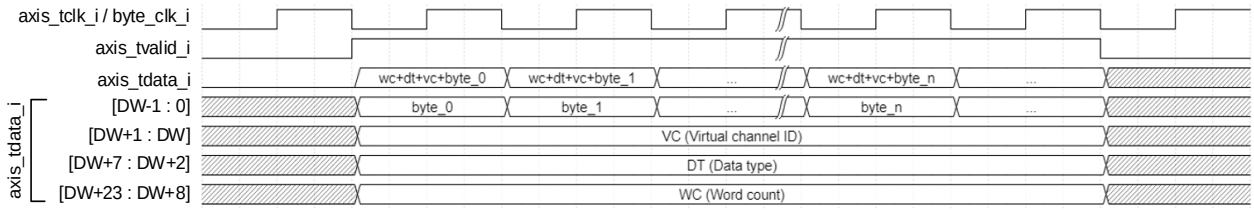

Figure 2.5. AXI4-Stream Enabled and LMMI Disabled Data Format and Packet Formatter Enabled

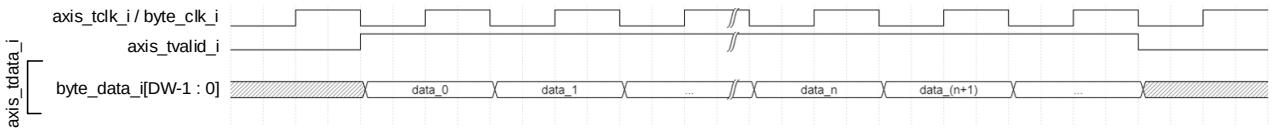

Figure 2.6. AXI4-Stream Enabled and Packet Formatter Disabled Data Format

If the AXI4-Stream device is not enabled, the following internal signals turn to top level input signals:

- byte_or_pkt_data_en_i
- byte_or_pkt_data_i […]
- vc_i
- dt_i
- wc_i

2.3. Wrapper Module

The D-PHY Tx Wrapper Module instantiates the PHY block. It may be configured to instantiate either a hardened D-PHY block or a soft logic implementation of the MIPI D-PHY.

Additional logic in the Wrapper Module is used to configure the connection between the PHY and the higher protocol layers.

2.3.1. Hard D-PHY Module

The Hard D-PHY block is available only in Crosslink-NX devices.

When the hardened block is used, a dedicated D-PHY PLL may be used to generate the byte clock and the high-speed clock for the D-PHY clock lanes. This PLL may be reconfigured by accessing the hard D-PHY registers through the LMMI bus. If the

LMMI is disabled, the PLL registers take on the value corresponding to the Reference Clock Frequency and the TX Line Rate per Lane attributes set in the user interface.

The hardened D-PHY block also has an option to use a clock source outside the Hard IP. This input clock pll_clkop_i is twice the D-PHY CLK lane and goes in directly to the hardened PHY.

2.3.2. Soft D-PHY Module

The D-PHY is implemented using the FPGA DDR elements. The D-PHY clock uses ECLK sync and clock divider elements. When *Enable Edge Clock Synchronizer and Divider == unchecked*, ports used to drive the DDR element are exposed as top-level ports of the IP. These ports are expected to be connected to the output of another D-PHY Tx instance which serves as the primary source of edge synchronizer and divider related clocks.

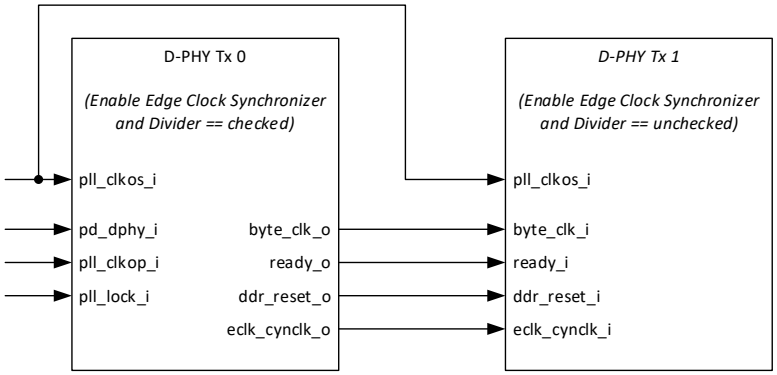

Figure 2.7. Sample Topology when Enable Edge Clock Synchronizer and Divider is Unchecked

This mode is useful when the design requires multiple Soft D-PHY Tx instances, but is constrained by the number of ECLK sync and clock divider elements. For example, multiple instances are required to be located on the same bank. However, this feature is only valid when all the D-PHY Tx instances are required to be run at the same bit rate per lane. In the example above, both data interfaces on the D-PHY Tx 0 and D-PHY Tx 1 are synchronized to the byte_clk_o of the D-PHY Tx 0.

For details on building the Soft MIPI D-PHY interfaces, refer to the following documents:

- Certus-NX High-Speed I/O Interface (FPGA-TN-02216)
- CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)

2.3.3. External PLL

The Soft D-PHY needs external clock sources pll_clkop_i and pll_clkos_i to produce the byte clock and to drive the D-PHY CLK lanes respectively. The pll_clkop_i goes into a clock divider to produce the output byte clock. The pll_clkos_i is 90-degree phase shifted from the pll_clkop_i. Both signals run at the desired D-PHY clock frequency.

2.3.4. Internal PLL

The hard D-PHY of CSI-2/DSI D-PHY Transmitter IP in CrossLink-NX devices contains its own PLL to generate the D-PHY clock lanes and the byte clock. The block diagram of the PLL is shown in Figure 2.8.

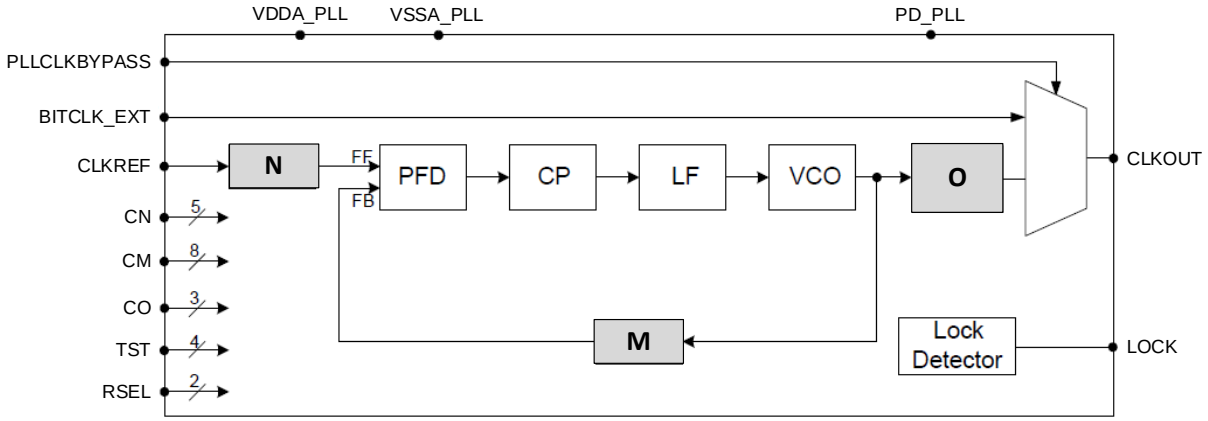

Figure 2.8. Internal PLL Block Diagram

The internal PLL multiplies the input frequency by (M/(N×O)), where N is the input divider, M is the feedback divider, and O is the output divider. The CLKOUT frequency is twice the D-PHY clock lane frequency.

The valid CLKREF of the D-PHY PLL, connected to the signal refclk_i, ranges from 24 MHz up to 200 MHz. Program the input divider, N, such that the frequency FF after the input divider is within 24 MHz and 50 MHz. The VCO output, which is also the input to the O divider, must be between 1250 MHz and 2500 MHz.

When PLL Mode is Internal, change the frequency by reconfiguring the LMMI control registers CM, CN, CO, and the protocol timing parameters. See Table 5.1. for details on register offsets and corresponding values.

Compute the data rate using this equation:

$$TX\ line\ rate = \left(\frac{CLKREF}{N}\right) \times \left(\frac{M}{O}\right)$$

To update the data rate without reprogramming the FPGA, follow these steps:

1. Set user standby input High. Keep it High at all times while registers CM, CN, and CO are written through LMMI write command.
2. Perform LMMI write command to the CM, CN, and CO register addresses with the values for the desired PLL frequency. See Table 5.2 and Table 5.3 for the conversion of the control registers CM, CN, and CO to the respective M, N, and O values.
3. Adjust the protocol timing registers for the new data rate.
4. Set user standby input to Low.
5. Wait for the pll_lock_o to assert.

2.4. Packet Formatter Module

The Packet Formatter Module includes the Packet Header and Packet Footer modules.

The Packet Header module generates the 32-bit header, including the ECC, for the DSI or the CSI-2 packet based on the input information. For CSI-2 configured IP which frame and line number information are not available, there is an internal line and frame counter logic that can be enabled through the IP user interface.

The Packet Footer module appends the CRC checksum at the end of the payload. This module also generates the End-of-Transmit packet (EoTP) for DSI when it is enabled.

2.5. Global Operation Module

The Global Operation Module contains the finite state machine (FSM) for controlling the HS and LP transitions for high-speed transmission. This module also contains counters for the D-PHY protocol timing requirements. These timing parameters are listed in Table 3.2.

Figure 2.9 shows the LP-to-HS transition flow diagram for data lanes.

Only the sequences from the Stop State to the high-speed state and vice versa are supported; the LP-request, escape mode and turnaround path are not supported.

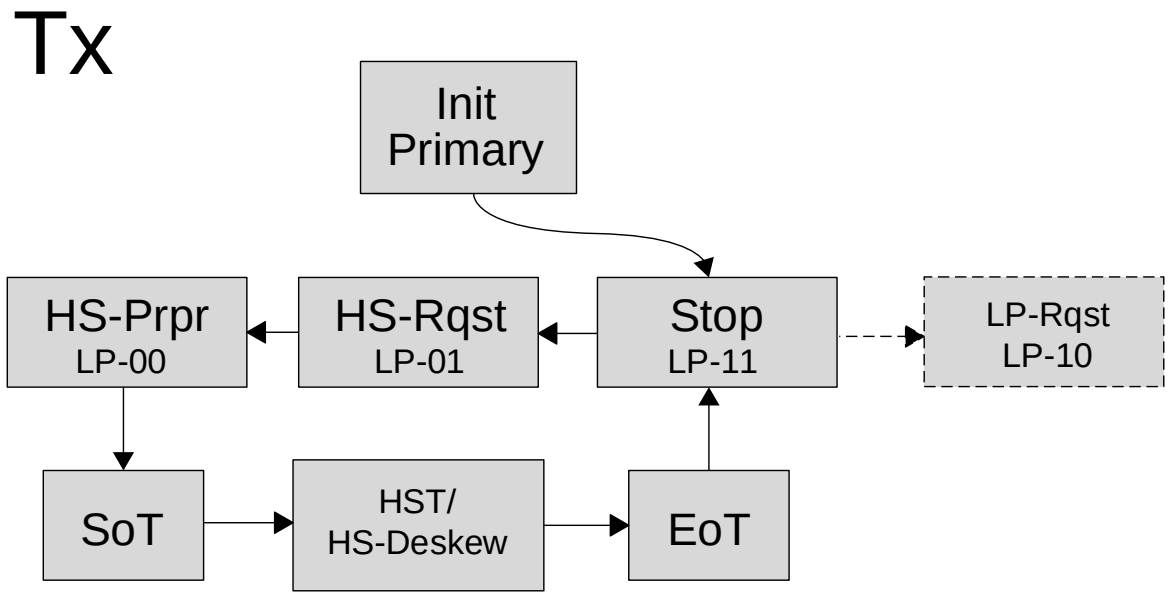

Figure 2.9. MIPI D-PHY Tx LP to HS Transition Flow Diagram on Data Lanes

During normal operation a data lane is either in control or in high-speed mode.

For sending payload data (the image data), the transmitter drives a particular sequence on data lanes to enter the receiver from the low power mode to high-speed mode.

As part of the initialization of D-PHY, initially all the lanes are held at LP11 state for a specified time. This LP11 state is also known as the Stop State. For sending the image data in high-speed, the transmitter drives the D-PHY lanes a particular LP sequence before the transmitter enters high-speed mode. The high-speed entry sequence (see Figure 2.10) consists of driving LP11->LP01->LP00 (LP->HS transition) on the lanes. On successful reception of this sequence, the high-speed receiver module enables its termination to receive the high-speed differential data.

After LP-to-HS transition, the transmitter sends HS Zeros (V(Dn)>V(Dp)) for a specified amount of time to make sure that the receiver is enabled properly before any payload data is transmitted. Internally, the FSM asserts the d_hs_rdy_o signal to indicate to the requestor that the tHS-ZERO counter threshold has been reached. The data lanes are in HS-00 state until the Global Operation Module receives the packet data from the Packet Formatter Module (or from the external requesting module, if the packet formatter is disabled).

Before the payload data of every HS burst on each lane, the transmitting D-PHY inserts a sync sequence (00011101). This sync sequence is used by the data lanes of the receiving D-PHY to establish synchronization with the high-speed payload data.

After every HS burst, the data lanes go to LP11 state. A single HS burst represents the image data corresponding to one of the horizontal lines of an image and the LP11 state in-between the HS bursts represents the blanking periods.

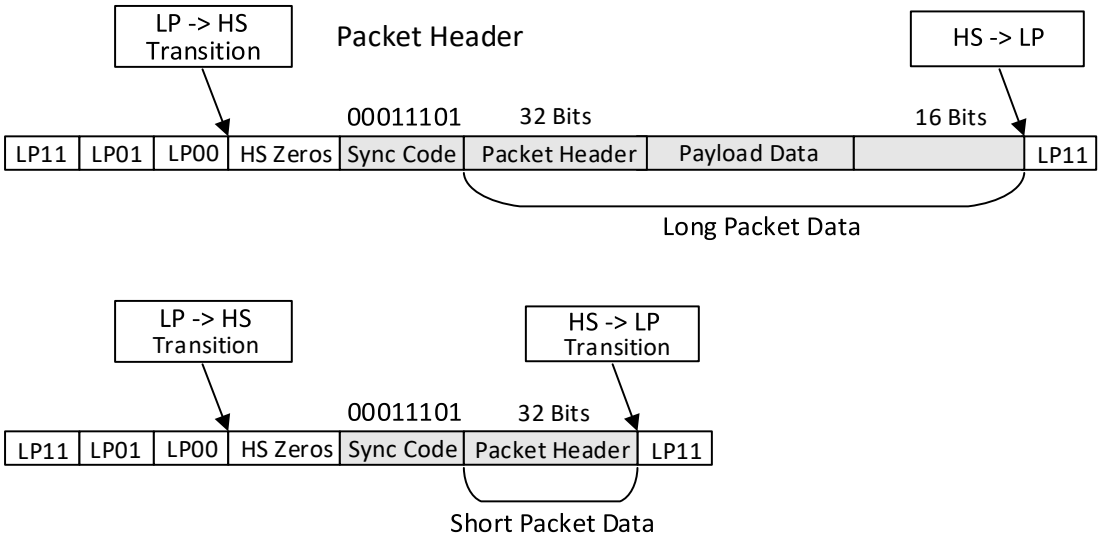

Figure 2.10. High-Speed Entry Sequence and Payload Data Transmission Cycle on Data Lanes

Receiver deskew is initiated by the Hard D-PHY when the data line rate is configured at greater than 1.5 Gbps. The transmitter sends a special deskew burst, as shown in Figure 2.11. When operating above 1.5 Gbps or changing to any rate above 1.5 Gbps, an initial deskew sequence is transmitted before high-speed data transmission in normal operation. Refer to the Initial Skew Calibration for Data Rates Above 1.5 Gbps section for timing details. When operating at or below 1.5 Gbps, the transmission of the initial deskew sequence is optional. Periodic deskew is optional irrespective of data rate.

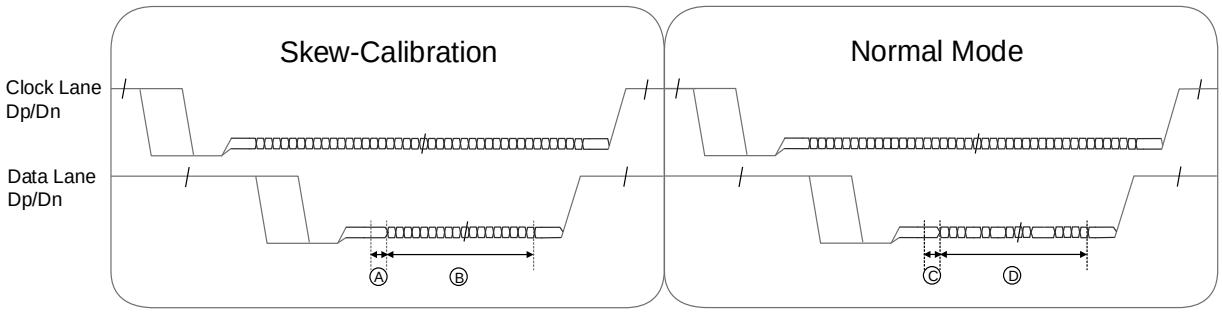

Figure 2.11. High-Speed Data Transmission in Skew Calibration

2.6. Timing Diagrams

In the configurations without the AXI4-Stream, the requestor waits for the c2d_ready_o signal to ensure the CSI-2/DSI D-PHY Transmitter IP is not busy from a previous transmit request, and that the data lanes (and also the clock lane, in the case of non-continuous clock mode) have completed the required tHS-EXIT.

The d_hs_rdy_o signal signifies the clock and data lanes have performed the LP-HS request sequence, including sending out the necessary tHS-ZERO and are in high-speed mode. The requestor can then send out the information of the packet to be transmitted, along with the payload. The c2d_ready_o signal goes back to high only after the completion of the tHS-EXIT.

The phdr_xfr_done_o indicates the Packet Header FSM has sent out the packet header and payload, including the CRC, to the Tx Global Operation module.

See the subsections below for more information on the required handshake timing.

2.6.1. Initial Skew Calibration for Data Rates Above 1.5 Gbps

D-PHY TX IP automatically drives initial skew calibration sequence after Initialization period is done (tinit_done_o = 1). c2d_ready_o remains de-asserted during initial skew calibration.

For non-continuous clock mode, c2d_ready_o goes back to high after the completion of tHS-EXIT for both clock and data lanes.

For continuous clock mode, c2d_ready_o goes back to high after the data lanes have completed tHS-EXIT.

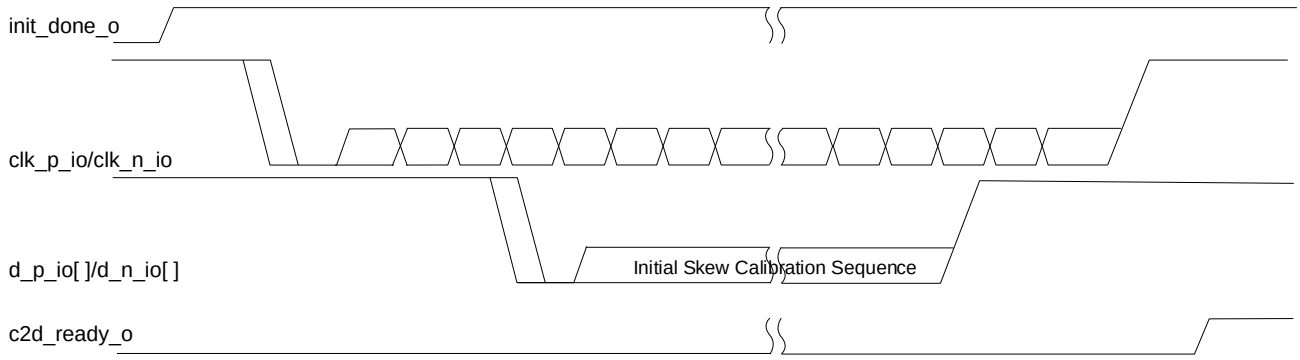

Figure 2.12. c2d_ready_o Timing for Non-Continuous D-PHY Clock Mode

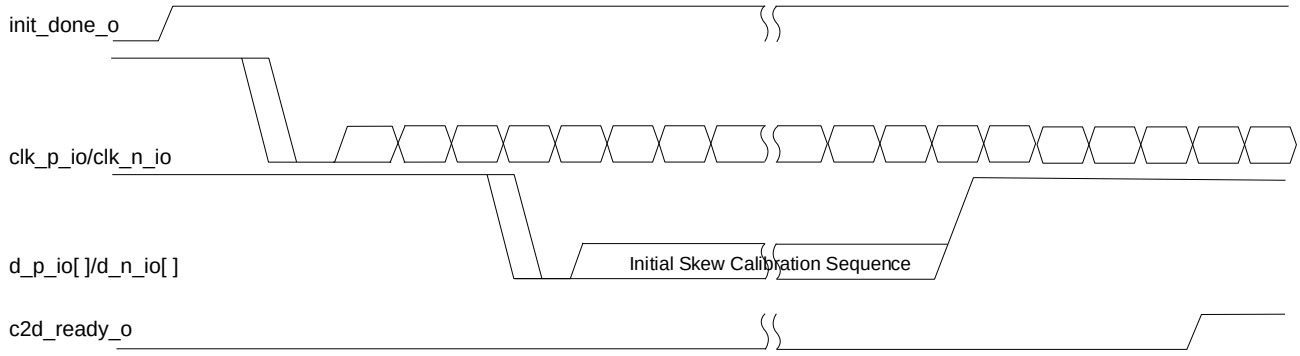

Figure 2.13. c2d_ready_o Timing for Continuous D-PHY Clock Mode

2.6.2. Packet Transmission in CSI-2/DSI Interfaces with Packet Formatter for Soft D-PHY and Hard D-PHY with Soft CIL (*CIL Bypass* is Checked)

When the protocol type selected is CSI-2, there is no internal buffer to save the incoming payload data before the creation of the header packet. The IP requires 3 cycles from the assertion of the ld_pyld_o to the arrival of the valid payload data. The ld_pyld_o asserts the next cycle after the detection of the lp_en_i.

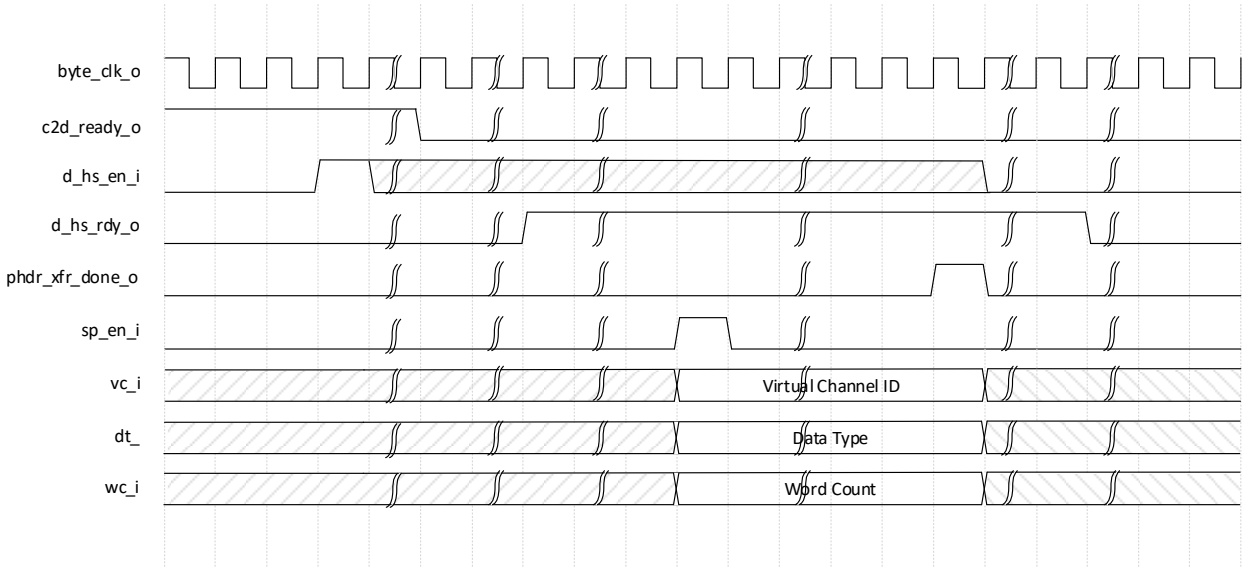

Figure 2.14. D-PHY Tx Input Bus for Short Packet Transmission in CSI-2/DSI Interfaces

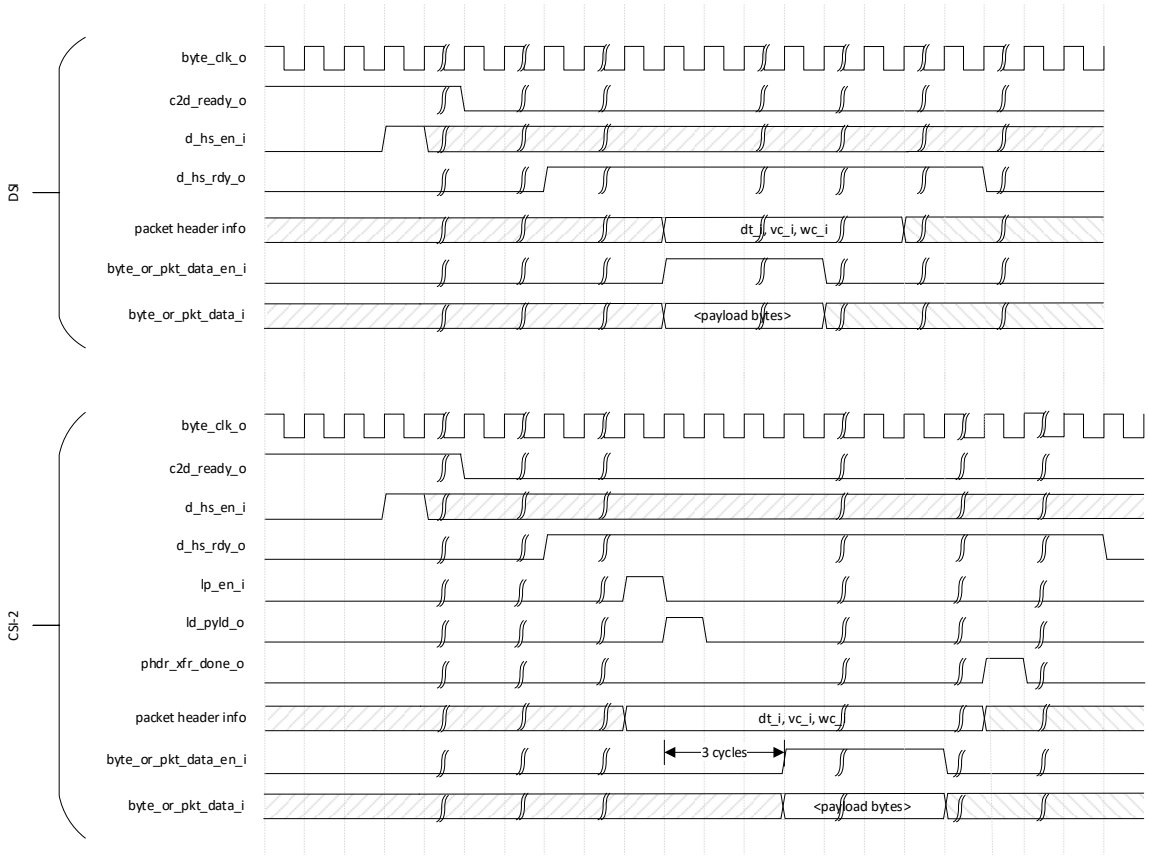

Figure 2.15. D-PHY Tx Input Bus for Long Packet Transmission in CSI-2/DSI Interface

2.6.3. Packet Transmission in CSI-2/DSI Interface with Packet Formatter for Hard D-PHY with Hardened CIL (*CIL Bypass* is Unchecked)

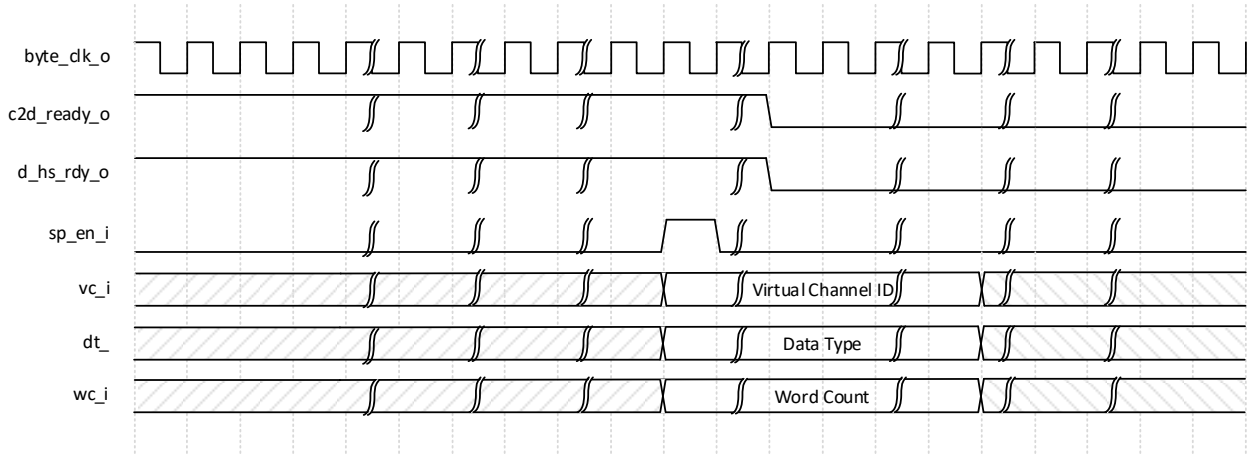

Figure 2.16. D-PHY Tx Input Bus for Short Packet Transmission in CSI-2/DSI Interfaces (*CIL Bypass* Unchecked)

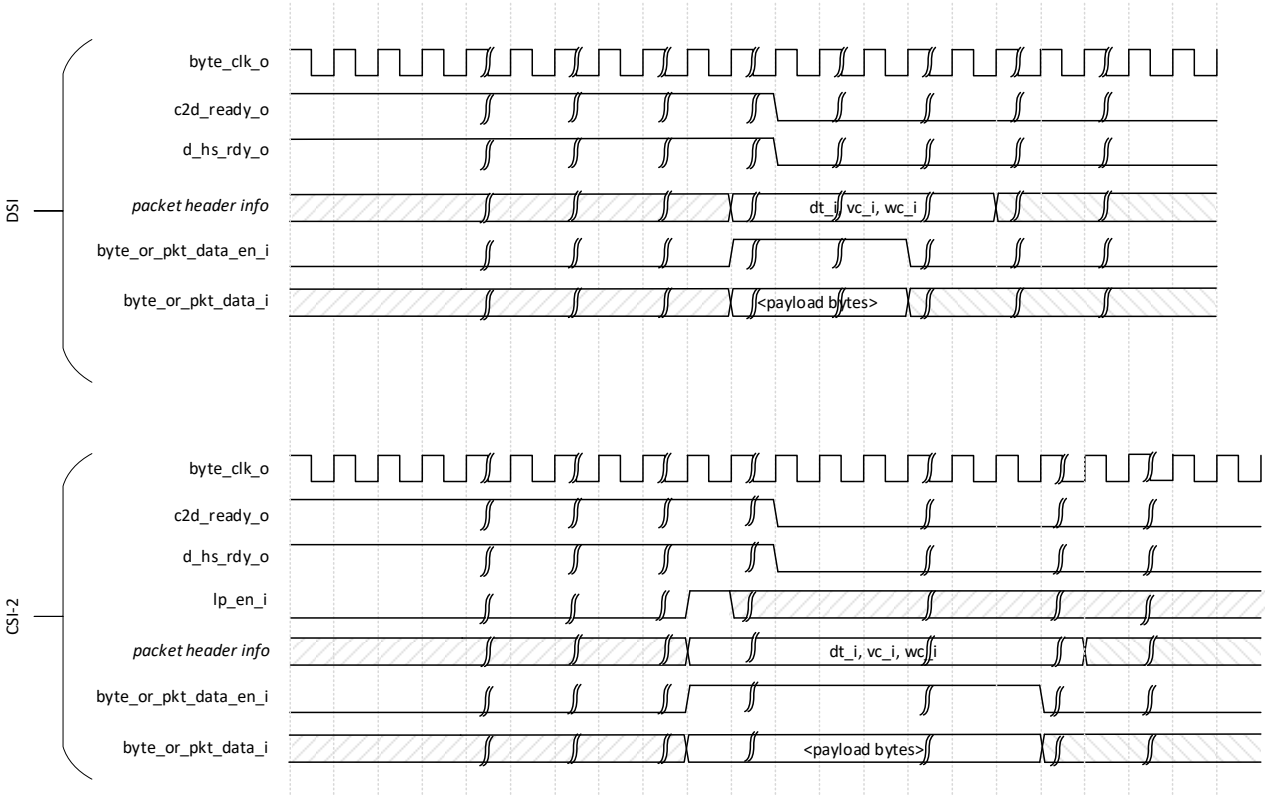

Figure 2.17. D-PHY Tx Input Bus for Long Packet Transmission in CSI-2/DSI Interface (*CIL Bypass* Unchecked)

2.6.4. Packet Transmission in CSI-2/DSI Interface without Packet Formatter

The Packet Formatter module appends the sync code before the packet header. If the packet formatter is disabled, the requestor interfaces directly to the Global Operations Control module, therefore the byte_or_pkt_data_i contains the sync code B8 for each lane. The Global Operations Control module is not aware of the boundary of the actual valid bits, therefore it cannot flip the last valid bit to create the trail. The last word is treated as pure trail bits, and is sent out to the

data lanes until the tHS-TRAIL is met. If *CIL Bypass* is unchecked, byte_or_pkt_data_en_i is unused and d_hs_en_i serves as data valid of byte_or_pkt_data_i. Sync code B8 and trail bytes are also not needed in the input stream.

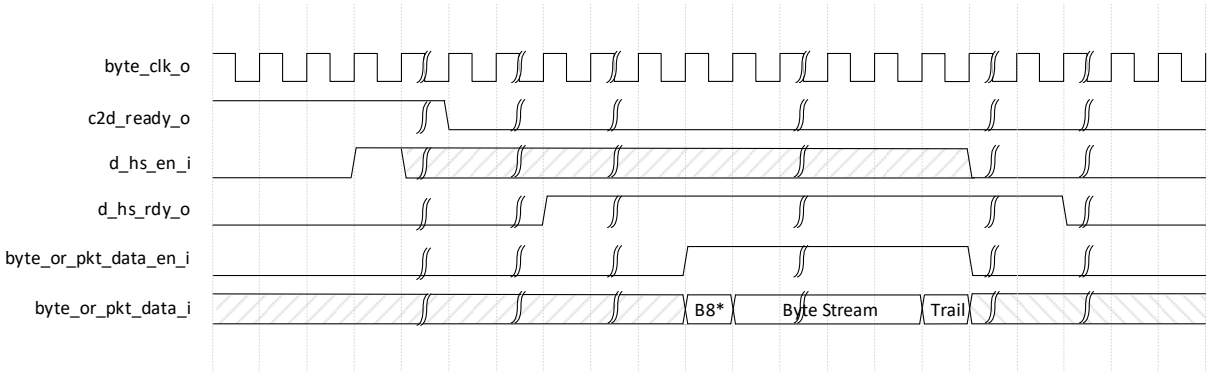

Figure 2.18. D-PHY Tx Input Bus for LP Transmission in CSI-2/DSI Interface without Packet Formatter (*D-PHY TX IP* = *Soft D-PHY* or *CIL Bypass* Checked)

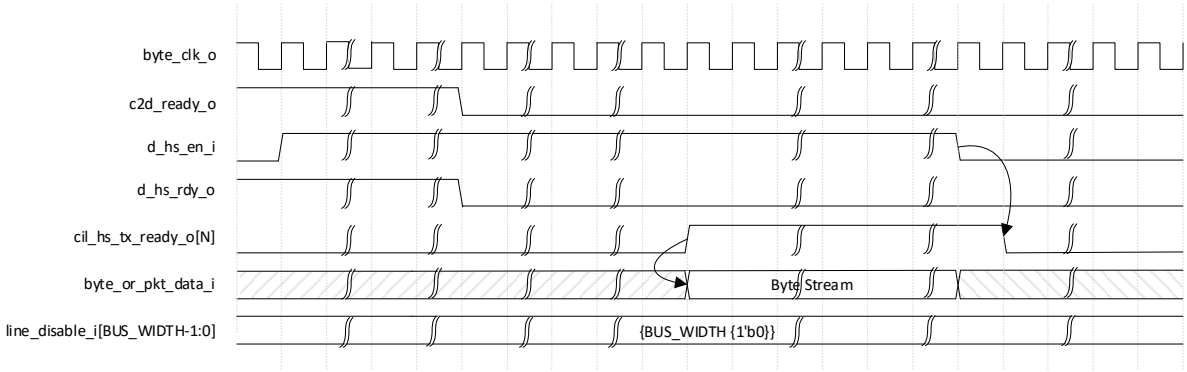

Figure 2.19. D-PHY Tx Input Bus for Transmission without Packet Formatter (*CIL Bypass* Unchecked)

If the number of valid bytes in the last cycle of byte_or_pkt_data_i does not align with the number of active D-PHY lanes, the corresponding tx_cil_word_valid_lane#_i and line_disable_i of the inactive lanes must be set accordingly. See the following figure for example.

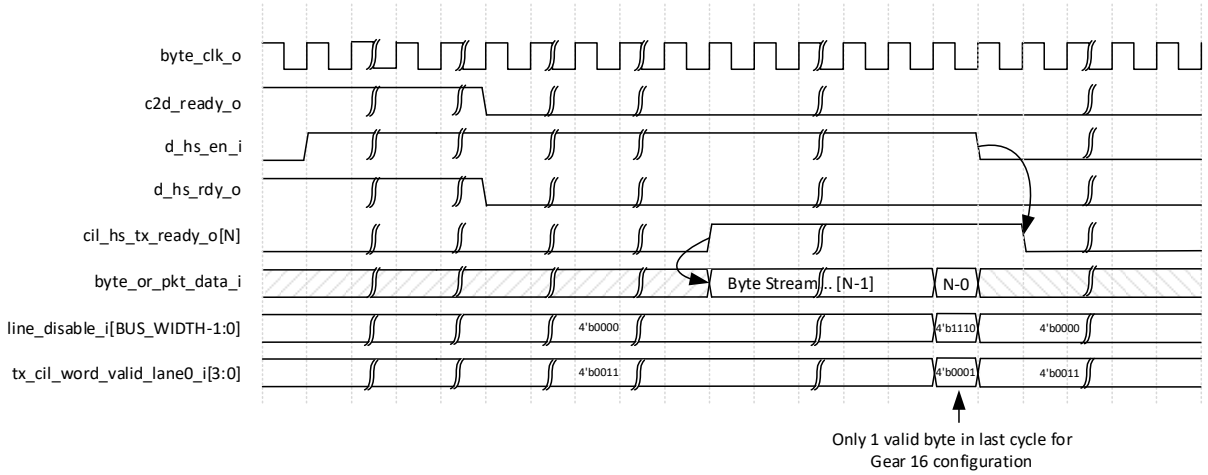

Figure 2.20. Example Configuration of Number of TX Lanes == 4, TX Gear == 16 with Unaligned Number of Bytes

2.6.5. Non-Continuous D-PHY Clock Mode

clk_hs_en_i triggers the IP to start HS entry sequence on the clock lane. When *D-PHY TX IP = Soft D-PHY* or *CIL Bypass* is checked, this is an active high pulse going to the Tx Global Operation and can be toggled together with d_hs_en_i. When *CIL Bypass* is unchecked, this signal must be asserted in the entire duration that clock is expected to be active.

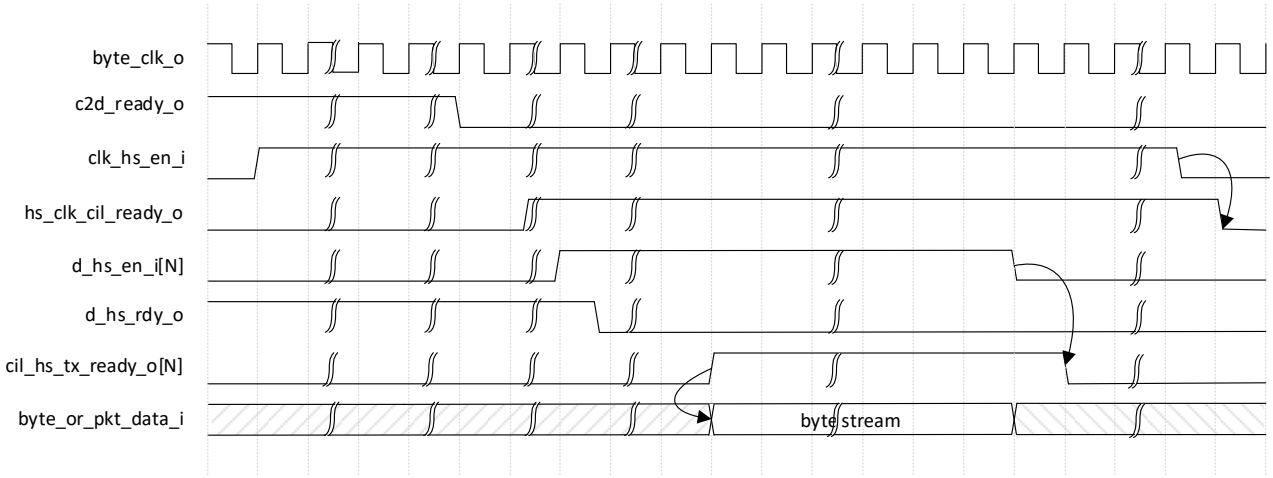

Figure 2.21. D-PHY Tx Input Bus for Non-Continuous Clock Mode with CIL Bypass Unchecked (without Packet Formatter)

2.6.6. Enable Periodic Skew Calibration

A low-to-high transition of skewcal_period_en_i initiates the periodic skew calibration. The signal, skewcal_period_en_i, is only available when the *Enable Periodic Skew Calibration* attribute is enabled. c2d_ready_o is high before initiating periodic skew calibration.

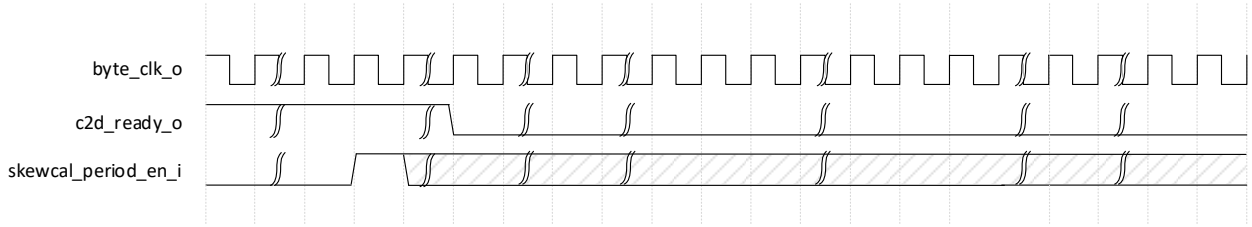

Figure 2.22. D-PHY Tx Input Bus to Enable Periodic Skew Calibration

2.6.7. CIL-Enabled Debug Ports

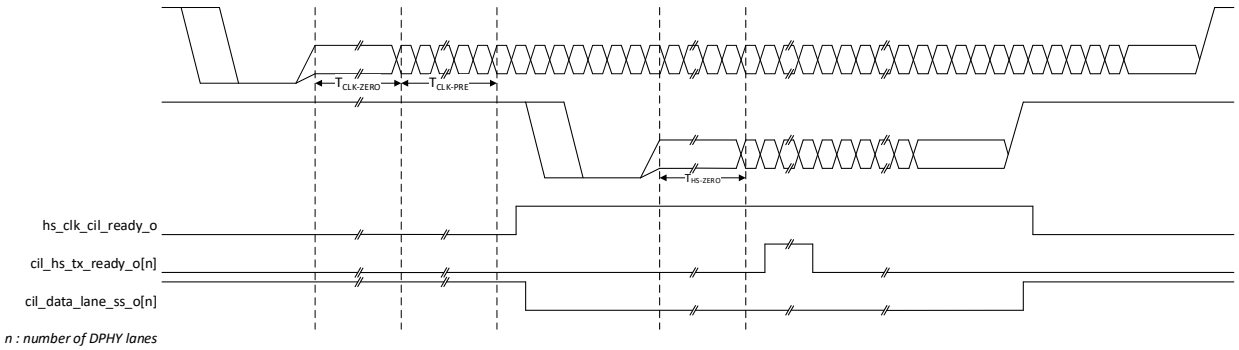

Figure 2.23. CIL-Enabled Debug Ports

2.6.8. Timing Configuration Registers

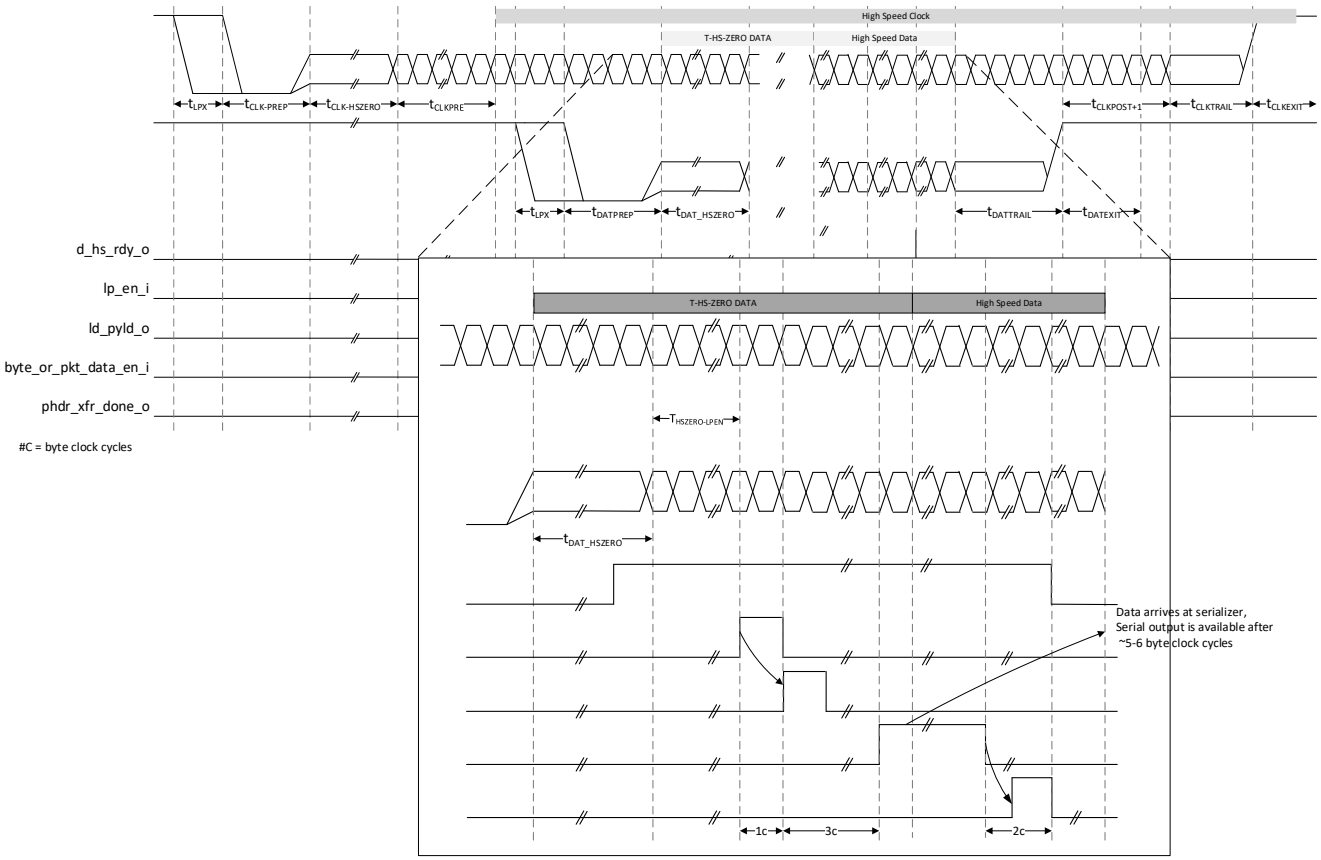

Figure 2.24. Timing Configuration Registers for Soft D-PHY or Hardened CIL Bypassed

2.6.9. Byte Data Arrangement

When in gear 16, the CSI-2/DSI D-PHY Transmitter IP has an option to take the parallel data arranged in sequential byte order, or in lane interleaved arrangement. This is configurable through the *Interleaved Input Data* attribute in the user interface, as shown in the following table. For gear 8, payload is always sequential.

Table 2.3. Interleaved versus Sequential Byte Data Input

byte_or_pkt_data_i	4-Lane		2-Lane		1-Lane	
	Interleaved	Sequential	Interleaved	Sequential	Interleaved	Sequential
[7:0]	Byte 0	Byte 0	Byte 0	Byte 0	Byte 0	Byte 0
[15:8]	Byte 4	Byte 1	Byte 2	Byte 1	Byte 1	Byte 1
[23:16]	Byte 1	Byte 2	Byte 1	Byte 2	—	—
[31:24]	Byte 5	Byte 3	Byte 3	Byte 3	—	—
[39:32]	Byte 2	Byte 4	—	—	—	—
[47:40]	Byte 6	Byte 5	—	—	—	—
[55:48]	Byte 3	Byte 6	—	—	—	—
[63:56]	Byte 7	Byte 7	—	—	—	—

Per lane distribution follows the ordinal number, depending on the number of active lanes. For example, in a 4-lane configuration with interleaved input data checked, Byte 0 to Byte 3 are distributed to Lane 0 to Lane 3 respectively. For gear 16 mode, the lane wraps around and Byte 4 to 7 are distributed to Lane 0 to Lane 3 respectively.

3. IP Parameter Description

The configurable attributes of the D-PHY Tx IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes[1]

Attribute	Selectable Values	Description
General Settings		
Transmitter		
TX Interface Type	DSI, **CSI-2**	DPHY-Tx Interface Type.
D-PHY TX IP	**Hard D-PHY**, Soft D-PHY	Implementation of the PHY layer of the D-PHY Tx. For Avant, Certus-NX, and CertusPro-NX devices, only *Soft D-PHY* is available.
Number of TX Lanes	1, 2, 3, **4**	Number of active D-PHY Tx data lanes. The 3-lane configuration is available only when *Bypass Packet Formatter* is checked.
TX Gear	**8**, 16	Gearing ratio between the ports in fabric and the high-speed I/O. *TX Gear = 16* is available only on *D-PHY TX IP = 'Hard D-PHY'*.
Interleaved Input Data	checked, **unchecked**	When this option is checked, the input parallel data is already interleaved across the lanes. See Table 2.3. Available only when *TX Gear = 16*.
CIL Bypass	**checked**, unchecked	When using *D-PHY TX IP = Hard D-PHY*, this option bypasses the built in Control Interface Logic of the Hard D-PHY.
Bypass Packet Formatter	checked, **unchecked**	Bypasses the Packet Formatter module. The data input to the IP is in packet format and the bytes are interleaved across the active data lanes.
Enable Frame Number Increment in Packet Formatter	checked, **unchecked**	Enables the Frame Number Increment in the Packet Formatter. Editable only if *Bypass Packet Formatter* is unchecked. When unchecked, information is derived from the wc_i input port.
Frame Number MAX Value Increment in Packet Formatter	**1**–255	Maximum frame number used in packet formatter. This option is editable only if *Enable Frame Number Increment in Packet Formatter* is checked.
Enable Line Number Increment in Packet Formatter	checked, **unchecked**	Enables the line number increment feature for the Packet Formatter. This option is editable only if *Bypass Packet Formatter* is unchecked. When unchecked, information is derived from the wc_i input port.
Extended Virtual Channel ID	checked, **unchecked**	Enables 4-bit instead of 2-bit Virtual Channel ID in CSI-2.
EoTp Enable	checked, **unchecked**	When checked, the IP appends an end-of-transmit packet at the end of a high-speed transmission. This option is enabled only if *TX Interface Type = DSI*.
Enable LMMI Interface	checked, **unchecked**	Enables the LMMI bus.
Enable AXI4-Stream Interface	checked, **unchecked**	Enables the AXI4-Stream bus.
Enable Periodic Skew Calibration	checked, **unchecked**	When this option is checked, there is an option to perform periodic skew calibration through the skewcal_period_en_i port. This option is available only when *D-PHY TX IP = Hard D-PHY*.
Clock		
Target TX Line Rate (Mbps per Lane)[2]	160–2500, **1000**	Maximum bandwidth per lane for TX Gear = 16.
	160–1500 or 160–1800, **1000**	Maximum bandwidth per lane for TX Gear = 8. Maximum line rate is 1800 Mbps for Avant devices and 1500 Mbps for other devices.

Attribute	Selectable Values	Description
Target TX Data Rate (Mbps)	160–10000, **4000**	Target total bandwidth of the D-PHY TX channel. Not editable. For information only.
Target TX D-PHY Clock Frequency (MHz)	80–1250, **500**	Target frequency of the D-PHY clock lane. Not editable. For information only.
Target TX Byte Clock Frequency (MHz)	10–225, **125**	Target operating frequency of the internal clock byte_clock_o. The value is (line_rate_per_lane / gearing). Not editable. For information only.
D-PHY Clock Mode	Continuous, **Non-continuous**	Determines the clock mode of the PHY layer. Continuous – if the clock lane is always in high speed mode. Non-continuous – the clock lane goes to low-power mode in between high-speed transactions.
D-PHY PLL Mode	**Internal**, External	Enables or disables the internal PLL when TX Interface = Hard D-PHY. For Soft D-PHY, only external PLL sources are supported.
Enable Edge Clock Synchronizer and Divider	**checked**, unchecked	Enables or disables the Edge Clock Synchronizer and Divider blocks when *D-PHY TX IP = Soft D-PHY.*
Reference Clock Frequency (MHz)	24–200, **100**	Operating frequency of the components interfaced with the fabric
Actual TX Data Rate (Mbps)	160–10000, **4000**	Actual D-PHY TX data rate based on the PLL settings and Reference Clock Frequency. Not editable. For information only.
Actual TX Line Rate (Mbps per Lane)	160–2500, **1000**	Actual data rate per lane based on the PLL settings and Reference Clock Frequency. Not editable. For information only.
Actual TX D-PHY Clock Frequency (MHz)	80–1250, **500**	Actual D-PHY TX clock frequency based on the PLL settings and Reference Clock Frequency. Not editable. For information only.
Actual TX Byte Clock Frequency (MHz)	10–187.5, **125**	Actual operating frequency of the internal clock byte_clock_o. The inputs to the IP is synchronized to this clock. Not editable. For information only.
Deviation from Target Data Rate	—, **0**	((target data rate – actual data rate) / target data rate), in percent.
Initialization		
tINIT Counter	checked, **unchecked**	Enables the initialization counter.
tINIT Value (Number of Byte Clock Cycles)	1–32768, **1000**	Maximum counter value; editable only if *tINIT Counter* is checked.
tinit Value in ns	Int, **0**	Equivalent value of *tINIT Value* in ns. Not editable. For information only.
Miscellaneous Signals		
Enable Miscellaneous Status Signals	checked, **unchecked**	Enables the other miscellaneous signals.

Notes:

1. The duration of the timing parameter is equal to the (byte clock period) × (attribute value).
2. The maximum data rate depends on the gear, device family, package, and speed grade of the device. Refer to the device data sheet for more information.

3.2. Protocol Timing Parameters

Table 3.2. Protocol Timing Parameters Attributes[1]

Attribute	Selectable Values	Description
Protocol Timing Parameters		
TX Global Operation Timing Parameters		
Customize TX Timing Parameter Values	checked, **unchecked**	Enables customization of the timing parameters.
t_LPX	1–255	Duration of any Low-Power state.
t_HS-PREPARE	1–255	Duration of the LP-00 Line state before the HS-0 Line state. When *CIL Bypass* is unchecked, the actual duration is based on u_PRG_HS_PREPARE.
t_HS_ZERO during skew calibration[2]	1–255	Duration when the data lanes are in HS-0 state before transmitting the sync sequence for HS skew calibration.
t_HS_ZERO[2]	1–255	Delay from the LP-00 State to the assertion of the d_hs_rdy_o signal. The actual HS-ZERO on the D-PHY data lanes depends on these three factors: • The delay between the d_hs_rdy_o assertion and the time the requestor sends the payload of a long packet. • The number of cycles the packet header (if enabled) can create the sync pattern and the 32-bit header. This varies with the number of lanes and gearing. • The serializer delay. The timing from parallel data input to the serialized output data differs between soft and hard D-PHY implementations. • When *CIL Bypass* is unchecked, the calculated value must be offset down by 5.
t_HS_TRAIL[2]	1–255	Duration of the flipped bit after the last payload data bit of an HS transmission burst.
t_HS_EXIT	1–255	Duration of the data LP-11 state following an HS transmission burst to the assertion of the c2d_ready_o signal when in continuous clock mode.
t_CLK-PREPARE	1–255	Duration of the LP-00 clock state immediately before the HS-0 clock state in the LP-to-HS sequence. When *CIL Bypass* is unchecked, the actual duration is based on uc_PRG_HS_PREPARE.
t_CLK-ZERO[2]	1–255	Duration of the clock HS-0 state prior to starting the actual toggling of the high-speed clock. When *CIL Bypass* is unchecked, the calculated value must be offset down by 4. Example: *D-PHY Gear* = 8 *D-PHY Clock Frequency (MHz)* = 480 MHz Frequency of byte_clk_o = 120 MHz byte_clk_o period = 8.336 ns Target clock HS-0 state duration = 262 ns t_CLK-ZERO = ceil((262/8.336) – 4) = 28
t_CLK-PRE	1–255	Duration of the HS clock prior to the start of the LP-to-HS sequence of the data lanes.
t_CLK_POST	1–255	Duration of the HS clock after the last associated Data Lane has transitioned to LP mode. The interval is defined as the period from the end of tHS-TRAIL to the beginning of tCLK-TRAIL.
t_CLK-TRAIL[2]	1–255	Duration of the HS-0 state after the last clock bit of an HS

Attribute	Selectable Values	Description
		transmission burst.
t_CLK-EXIT	1–255	Duration of the clock LP-11 state following an HS transmission burst to the assertion of the c2d_ready_o signal when in non-continuous clock mode.
t_SKEWCAL-INIT	2^{15} – 100 µs	Duration of initial Skew Calibration. Default value is close to 2^{15} UI.
t_SKEWCAL-PERIOD	2^{10} – 10 µs	Duration of periodic Skew Calibration. Default value is close to 2^{10} UI.

Notes:

1. The duration of the timing parameter is equal to the (byte clock period) × (attribute value), except for attributes marked with note 2.
2. When *CIL Bypass* is unchecked, regardless of the gear selected, the duration of the timing parameter is equal to the (8UI) × (attribute value).

The timing parameters are in number of byte clock cycles. This is computed automatically to ensure the design meets the required minimum and maximum timing ranges. The numbers set in the user interface and the actual duration in the D-PHY lanes might vary due to the serialization and register delays within the design.

4. Signal Description

This section describes the CSI-2/DSI D-PHY Tx IP ports.

4.1. D-PHY Tx

Table 4.1. D-PHY Tx Signal Description

Port Name	Direction	Mode/Configuration	Description
D-PHY Tx			
clk_p_io, clk_n_io	In/Out	—	MIPI D-PHY clock lane.
d_p_io[BUS_WIDTH[1]– 1:0], d_n_io[BUS_WIDTH[1] – 1:0]	In/Out	—	MIPI D-PHY data lanes.
ref_clk_i	In	—	If the PLL mode is internal, this clock is used as the reference clock for the internal PLL. The frequency must be between 24–200 MHz. If the PLL mode is external and the hardened CIL is enabled, this clock is used as the escape mode clock. If set as Soft PHY implementation and *Enable Edge Clock Synchronizer and Divider* is checked, this clock is used as a startup clock that clocks the gddr_sync module, which synchronizes the clock divider ECLKDIV and the DDR elements. This clock can be any low speed continuously running clock.
pll_clkop_i	In	DPHY PLL Mode – External or *Enable Edge Clock Synchronizer and Divider* – checked	External PLL clock source. For Hard PHY implementation, the frequency of this clock is twice that of the D-PHY clock lanes. For Soft PHY, the frequency of this clock is the same as the frequency of the D-PHY clock lanes.
pll_clkos_i	In	DPHY PLL Mode – External	90-degree phase shifted D-PHY clock. The pll_clkos_i is 90-degree phase shifted from the pll_clkop_i.
eclk_syncclk_o	Out	*Enable Edge Clock Synchronizer and Divider* – checked	Output clock of ECLKSYNC module and is only reset internally during DDR synchronization.
byte_clk_o	Out	D-PHY TX IP = *Hard D-PHY* or *Enable Edge Clock Synchronizer and Divider* – checked	Byte clock generated by D-PHY PLL if D-PHY TX IP = *Hard D-PHY* and ECLKDIV if D-PHY TX IP = *Soft D-PHY*. Default is 1'd0.
eclk_syncclk_i	In	D-PHY TX IP = *Soft D-PHY* *Enable Edge Clock Synchronizer and Divider* – unchecked	Drives the ECLK pin of DDR modules of data path. Must be generated by ECLKSYNC module (eclk_syncclk_o).
byte_clk_i	In	D-PHY TX IP = *Soft D-PHY* *Enable Edge Clock Synchronizer and Divider* – unchecked	Input byte clock. Drives the SCLK pin of DDR module used for data path. Must be generated by ECLKDIV module (byte_clk_o).
reset_n_i	In	—	Asynchronous active low system reset.
ddr_reset_i	In	D-PHY TX IP = *Soft D-PHY* *Enable Edge Clock Synchronizer and Divider* – unchecked	Drives the reset port of DDR modules. Must be generated by gddr_sync module (ddr_reset_o).

Port Name	Direction	Mode/Configuration	Description
pd_dphy_i	In	D-PHY TX IP = *Hard D-PHY* or *Enable Edge Clock Synchronizer and Divider* – checked	Active high powers down the D-PHY block, including the internal PLL if D-PHY TX IP = *Hard D-PHY*.
usrstdby_i	In	—	Active high puts the hard D-PHY block to standby mode.
pll_lock_i	In	DPHY PLL Mode – External	D-PHY PLL lock signal.
ready_i	In	D-PHY TX IP = *Soft D-PHY* *Enable Edge Clock Synchronizer and Divider* – unchecked	Indicates GDDR ready. Must be generated by gddr_sync module (ready_o).
clk_hs_en_i	In	DPHY Clock Mode – Non continuous	Enabled for non-continuous clock mode. This triggers the IP to start HS entry sequence on the clock lane. When D-PHY TX IP = *Soft D-PHY* or *CIL Bypass* is checked, this is an active high pulse going to the Tx Global Operation. When *CIL Bypass* is unchecked, this signal must be asserted in the entire duration that clock is expected to be active. See the Timing Diagrams section for details. This is unavailable if *CIL Bypass* and *Bypass Packet Formatter* are both unchecked.
d_hs_en_i	In	—	This triggers the IP to start HS entry sequence on the data lanes. If *CIL Bypass* is unchecked and *Bypass Packet Formatter* is checked, this also serves as data valid of byte_or_pkt_data_i. See the Timing Diagrams section for details. This is unavailable if *CIL Bypass* and *Bypass Packet Formatter* are both unchecked.
skewcal_period_en_i	In	*Enable Periodic Skew Calibration* = checked	Initiates periodic deskew calibration when set from low to high.
sp_en_i	In	*Bypass Packet Formatter* – unchecked	Short packet enable (frame or line packet). This high active pulse triggers the IP to transmit a CSI-2 or DSI short packet.
lp_en_i	In	Tx Interface Type – CSI-2 *Bypass Packet Formatter* – unchecked	This high active pulse triggers the packet formatter to prepare the 32-bit packet header for the CSI-2 long packet. The IP expects the payload to arrive 4 cycles after the assertion of the lp_en_i.
vcx_i[1:0]	In	AXI4-Stream disabled Extended Virtual Channel ID checked	2-bit virtual channel extension. This is the 2-bit MSB of a 4-bit virtual channel ID.
vc_i [1:0]	In	AXI4 Stream – disabled *Bypass Packet Formatter* – unchecked	2-bit virtual channel ID of the packet. This is used only when the Packet Formatter is enabled.
dt_i [5:0]	In	AXI4 Stream – disabled *Bypass Packet Formatter* – unchecked	CSI-2 or DSI 6-bit data type field. This is used only when the Packet Formatter is enabled.
wc_i [15:0]	In	AXI4 Stream – disabled *Bypass Packet Formatter* – unchecked	16-bit Word Count field. This denotes the number of bytes in the payload of a long packet. In a short packet, this contains a 2-byte data. This is used only when the Packet Formatter is enabled.
byte_or_pkt_data_i[DW^2 – 1:0]	In	AXI4 Stream – disabled	Byte data or packet data.
byte_or_pkt_data_en_i	In	AXI4 Stream – disabled	Indicates valid data on the byte_or_pkt_data_i bus. Not available if *CIL Bypass* is unchecked and *Bypass Packet Formatter* is checked.

Port Name	Direction	Mode/Configuration	Description
d_hs_rdy_o	Out	—	Active high signal to indicate data lane is ready for transmission. Default is 1'd1 when *CIL Bypass* – unchecked, else 1'd0.
c2d_ready_o	Out	—	Indicates that CMOS2DPHY is ready to receive data. When D-PHY TX IP is running at 1.5 Gbps and below, this signal asserts after Initialization period is done (tinit_done = 1). When D-PHY TX IP is running at more than 1.5 Gbps, this signal asserts when both initialization period and initial skew calibration period are done. Default is 1'd0.
ddr_reset_o	Out	*Enable Edge Clock Synchronizer and Divider* – checked	Output reset of gddr_sync module. Default is 1'd1.
ready_o	Out	D-PHY TX IP = *Hard D-PHY* or *Enable Edge Clock Synchronizer and Divider* – checked	Indicates PLL lock when D-PHY TX IP = *Hard D-PHY* or GDDR ready when D-PHY TX IP = *Soft D-PHY*. Default is 1'd0.
lp_rx_en_i	In	Tx Interface Type – DSI	Low Power Rx Enable signal.
lp_rx_data_p_o	Out	Tx Interface Type – DSI	Low Power Rx Positive data Default is 1'd1 when D-PHY TX IP = *Soft D-PHY*. Default is 1'b0 when D-PHY TX IP = *Hard D-PHY*.
lp_rx_data_n_o	Out	Tx Interface Type – DSI	Low Power Rx Negative data Default is 1'd1 when D-PHY TX IP = *Soft D-PHY*. Default is 1'b0 when D-PHY TX IP = *Hard D-PHY*.
phdr_xfr_done_o	Out	Tx Interface Type – CSI-2 *Bypass Packet Formatter* – unchecked	Single cycle pulse to indicate that the packet information, payload, and CRC are sent out to the Tx Global Operation (unavailable when *CIL Bypass* is unchecked). Default is 1'd0.
ld_pyld_o	Out	Tx Interface Type – CSI-2 *Bypass Packet Formatter* – unchecked	When high, the packet formatter is ready to receive data for packing (unavailable when *CIL Bypass* is unchecked). Default is 1'd0.
cil_hs_tx_ready_o[BUS_WIDTH[1] – 1:0]	Out	D-PHY TX IP = *Hard D-PHY* *CIL Bypass* – unchecked	Indicates DPHY is ready to send byte data. Default is {BUS_WIDTH[1]{1'd0}}.
cil_data_lane_ss_o[BUS_WIDTH[1] – 1:0]	Out	D-PHY TX IP = *Hard D-PHY* *CIL Bypass* – unchecked	Indicates data lane is in stop state. Default is {BUS_WIDTH[1]{1'd1}}.
hs_clk_cil_ready_o	Out	D-PHY TX IP = *Hard D-PHY* *Bypass Packet Formatter* – checked	Indicates DPHY high-speed clock is ready. Default is 1'd0.
tx_cil_word_valid_lane0_i[3]	In	D-PHY TX IP = *Hard D-PHY* *Bypass Packet Formatter* – checked	4-bit high-speed transmit word data valid. 0b0001 – 1 byte is valid in the corresponding clock cycle. 0b0011 – 2 bytes are valid in the corresponding clock cycle.
tx_cil_word_valid_lane1_i[3]	In	D-PHY TX IP = *Hard D-PHY* *Bypass Packet Formatter* – checked	4-bit high-speed transmit word data valid. 0b0001 – 1 byte is valid in the corresponding clock cycle. 0b0011 – 2 bytes are valid in the corresponding clock cycle.
tx_cil_word_valid_lane2_i[3]	In	D-PHY TX IP = *Hard D-PHY* *Bypass Packet Formatter* – checked	4-bit high-speed transmit word data valid. 0b0001 – 1 byte is valid in the corresponding clock cycle. 0b0011 – 2 bytes are valid in the corresponding clock cycle.

Port Name	Direction	Mode/Configuration	Description
tx_cil_word_valid_lane3_i[3]	In	D-PHY TX IP = *Hard D-PHY Bypass Packet Formatter* – checked	4-bit high-speed transmit word data valid. 0b0001 – 1 byte is valid in the corresponding clock cycle. 0b0011 – 2 bytes are valid in the corresponding clock cycle.
line_disable_i[3]	In	D-PHY TX IP = *Hard D-PHY Bypass Packet Formatter* – checked	D-PHY lane disable signal. Corresponding lane must be set to 1'b1 based on the expected active D-PHY lanes to be disabled. Bus width is dependent on BUS_WIDTH[1]. [0] – Lane 0 [1] – Lane 1 [2] – Lane 2 [3] – Lane 3 See the Timing Diagrams section for details.

Notes:

1. BUS_WIDTH – Number of D-PHY Lanes, 1 to 4 (available on the user interface)
2. DW – Byte or Packet Data Width
   DW = GEAR × NUM_TX_LANE
3. If the number of the last valid data byte (byte_or_pkt_data_i) is not a equal to the selected gear, for example, only 1 byte is valid in a gear 16 configuration, you need to properly set the corresponding tx_cil_word_valid_lane#_i and line_disable_i. Refer to Figure 2.20 for example.

4.2. LMMI Device Target

Table 4.2. LMMI Device Target Signal Description

Port Name	Direction	Mode/Configuration	Description
LMMI Device Target			
lmmi_clk_i	In	—	LMMI interface clock.
lmmi_resetn_i	In	—	Active low signal to reset the configuration registers.
lmmi_wdata_i[LDW[1] – 1:0]	In	—	Write data.
lmmi_wr_rdn_i	In	—	Write = HIGH, Read = LOW.
lmmi_offset_i[LOW[2] – 1:0]	In	—	Register offset, starting at offset 0.
lmmi_request_i	In	—	Start transaction.
lmmi_ready_o	Out	—	Ready to start a new transaction. Default is 1'd0.
lmmi_rdata_o[LDW[1] – 1:0]	Out	—	Read data. Default is 0x00 when there is no hard D-PHY enabled. When hard D-PHY is enabled, default value is based on lmmi_offset_i == 0x00.
lmmi_rdata_valid_o	Out	—	lmmi_rdata[3:0] contains valid data. Default is 1'd0.

Notes:

1. LDW – LMMI Data Width
   - If CIL_BYPASS is unchecked, then LDW = 4
   - Otherwise LDW = 8
2. LOW – LMMI Offset Width
   - If CIL_BYPASS is unchecked, then LOW = 5
   - Otherwise LOW = 7

4.3. AXI4-Stream Device Receiver

Table 4.3. AXI4-Stream Device Receiver Signal Description

Port Name	Direction	Mode/Configuration	Description
AXI4-Stream Device Receiver			
axis_tvalid_i	In	—	Source indicates that data to be transmitted is valid.
axis_tdata_i[ADW[1] – 1:0]	In	—	Payload data receiving channel (byte data or packet data with virtual channel and data type and word count).
axis_tready_o	Out	—	Indicates that AXI4-Stream is ready to accept data. Default is 1'd0.

Note:

1. ADW – AXI4-Stream Data Width
   - If (Bypass Packet Formatter is unchecked) AND (LMMI is unchecked) then ADW = GEAR × NUM_TX_LANE + 24
   - Otherwise ADW = GEAR × NUM_TX_LANE

4.4. Debug Interface

Table 4.4. Debug Interface Signal Description

Port Name	Direction	Mode/Configuration	Description
Debug Interface			
tinit_done_o	Out	Miscellaneous – enabled	tINIT done signal generated from IP. When tINIT counter is checked, this signal asserts after (tINIT value–1) cycles. Otherwise, this signal asserts when both ready_i/ready_o and pll_lock_o are asserted. Default is 1'd0.
pll_lock_o	Out	Miscellaneous – enabled	D-PHY PLL lock signal. Default is 1'd0.
pix2byte_rstn_o	Out	Miscellaneous – enabled *Bypass Packet Formatter* – unchecked Tx Interface Type – CSI-2 *CIL Bypass* – checked	Active low reset signal for pixel2byte FIFOs. This toggles after every valid short and long packets data state of Packet Formatter. Default is 1'd1.
pkt_format_ready_o	Out	Miscellaneous – enabled *Bypass Packet Formatter* – unchecked Tx Interface Type – CSI-2 AXI4 Stream – disabled	Indicates the state of Packet Formatter. This asserts during long packet valid data state of Packet Formatter if *CIL Bypass* – checked. This is tied to 1 if *CIL Bypass* – unchecked. Default is 1'd0.

5. Register Description

For both hard and soft configurations of the D-PHY Tx IP, the Configuration Registers are available when LMMI is enabled. All D-PHY Tx IP Configuration Registers are controlled through the LMMI bus. If the LMMI feature is not enabled, the Hard D-PHY configuration registers (MIPI programmable bits) are set to the default values and the general registers become not actual and, instead, turn to top level input signals. Both byte_clk_o and lmmi_clk_i need to be active when accessing the registers.

5.1. Hard Configured D-PHY Tx IP Configuration Registers (MIPI Programmable Bits)

(Available when *DPHY TX IP = Hard D-PHY*)

Table 5.1. Hard Configured D-PHY Tx Configuration Registers (MIPI Programmable Bits)

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x00	HSEL RX High Speed Select. [0] – Less than ≤1.5 Gbps [1] – Higher than 1.5 Gbps Default depends on the *Target TX Line Rate* attribute.	AUTO_PD_EN Powers down inactive lanes. [0] – Lanes are kept powered up and at LP11. [1] – Lanes powered down. Default is 1'b0.	PRIMARY_SECONDARY Selects the PHY IP forward direction configuration. [0] – Secondary [1] – Primary Default is 1'b1.	DSI_CSI Selects the PHY IP application. [0] – CSI2 [1] – DSI Default depends on the *Tx Interface Type* attribute.
0x01	RXCDRP[1:0] LP-CD threshold voltage. Default is 2'b01. Min – 200 mV, Max – 450 mV		RSEL Loop filter resistance selection. Must be set to 2'b01 for DPHY Tx, otherwise, set to 2'b00.	
0x02	EN_CIL Enables or disables CIL. [0] – CIL bypassed. [1] – CIL enabled. Default depends on the *CIL Bypass* attribute.	RXLPRP[2:0] Adjust the threshold voltage and hysteresis of LP-RX, default setting is 2'b001.		
0x03	TST[0] = 1'b1	PLLCLKBYPASS Bypasses the internal PLL. [0] – PLL Enabled. [1] – PLL Bypassed. Depends on the *D-PHY PLL Mode* attribute.	LOCK_BYP When clock lane exits from ULPS, this input determines if the PLL LOCK signal is used to gate the TxWordClkHS. [0] PLL LOCK gates TxWordClkHS. [1] PLL LOCK signal does not gate TxWordClkHS clock. Default is 1'b0.	Default is 1'b0.
0x04	CN[0]	TST[3:1] = 3'b100		
0x05	CN[4:1] The N parameter of the internal PLL in the equation: Output = M/(N×O). See Table 5.2 for values. Default depends on the *Target TX Line Rate* attribute selected.			
0x06	CM[3:0] LSB of the M parameter of the internal PLL in the equation: Output = M/(N×O). See Table 5.2 for values.			
0x07	CM[7:4] MSB of the M parameter of the internal PLL in the equation: Output = M/(N×O). See Table 5.2 for values. Default depends on the *Target TX Line Rate* attribute selected.			

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x08	TxDataWidthHS[0] LSB High-Speed Transmit Byte Clock.	CO[2:0] The O parameter of the internal PLL in the equation: Output = M/(N×O). See Table 5.2 for values. Default depends on the *Target TX Line Rate* attribute selected.		
0x09	Lane0_sel[0] LSB of Lane0_Sel	RxDataWidthHS[1:0] High-Speed Receive Data Width Select. 2'b00 – 1/8 the HS bit rate 2'b01 – 1/16 the HS bit rate 2'b10 – 1/32 the HS bit rate Default is 2'b01.		TxDataWidthHS[1] MSB High-Speed Transmit Byte Clock. 2'b00 – 1/8 the HS bit rate 2'b01 – 1/16 the HS bit rate 2'b10 – 1/32 the HS bit rate Default depends on the *TX Gear* attribute.
0x0A	Default is 1'b1.	cfg_num_lanes[1:0] Sets the number of active lanes. Value from 0 to 3. Default depends on the *Number of TX Lanes* attribute.		Lane0_sel[1] MSB of Lane0_Sel. This determines which lane acts as data lane0 in HS Operation mode. Value from 0 to 3. Default is 2'b00.
0x0C	uc_PRG_HS_ZERO[1:0]		uc_PRG_HS_PREPARE T_CLK_PREPARE time in the beginning of high-speed transmission mode. For clock pin. 0 – Tperiod of sync_clk[2] 1 – 1.5[1]Tperiod of sync_clk[2] Default depends on the *CIL Bypass* attribute. If *CIL Bypass* is checked, default is 1'b0. Else, default depends on the *t_CLK-PREPARE* attribute. If *t_CLK-PREPARE > 1,* register bit is 1'b1, else 1'b0.	0 Default is 0.
0x0D	uc_PRG_HS_ZERO[5:2] Bits used to program T_CLK_ZERO time in the beginning of high-speed transmission mode. For clock pin. T_CLK_ZERO = (uc_PRG_HS_ZERO+ 4) × (ByteClk Period)			
0x0E	uc_PRG_HS_TRAIL[2:0] Bits used to program T_HS_TRAIL time in the end of high-speed transmission mode. For clock pin. T_HS_TRAIL = (uc_PRG_HS_TRAIL) × (ByteClk Period)			uc_PRG_HS_ZERO[6] Default depends on the *CIL Bypass* attribute. If *CIL Bypass* is checked, default is 0x01. Else default depends on the *t_CLK-ZERO* attribute.
0x0F	2'b01		uc_PRG_HS_TRAIL[4:3] Default depends on the *CIL Bypass* attribute. If *CIL Bypass* is checked, default is 0x01. Else, default depends on the *t_CLK-TRAIL* attribute.	

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x11	u_PRG_HS_ZERO[1:0] *(See MSB below at 0x12)*		u_PRG_HS_PREPARE[1:0] T_HS_PREPARE time in the beginning of high-speed transmission mode. For data pins. 0 – Tperiod of sync_clk[2] 1 – 1.5[1]Tperiod of sync_clk[2] 2 – 2[1] Tperiod of sync_clk[2] 3 – 2.5[1] Tperiod of sync_clk[2] Default depends on the *CIL Bypass* attribute. If *CIL Bypass* is checked, default is 0x1. Else, default depends on the *t_HS-PREPARE* attribute. If *t_HS-PREPARE* < 4, register value is *t_HS-PREPARE-1,* else 2'b11.	
0x12	u_PRG_HS_ZERO[5:2] Bits used to program T_HS_ZERO time in the beginning of high-speed transmission mode. For data pins. T_HS_ZERO = (u_PRG_HS_ZERO + 5) × (ByteClk Period) Default depends on the *CIL Bypass* attribute. If *CIL Bypass* is checked, default is 0x01. Else, default depends on the *t_HS_ZERO* attribute.			
0x13	u_PRG_HS_TRAIL[3:0] Bits used to program T_HS_TRAIL time in the end of high-speed transmission mode. For data pins. T_HS_TRAIL = (uc_PRG_HS_TRAIL) × (ByteClk Period) Default depends on the *CIL Bypass* attribute. If *CIL Bypass* is checked, default is 0x01. Else, default depends on the *t_HS_TRAIL* attribute.			
0x14	2'b00		u_PRG_HS_TRAIL[5:4] *(See LSB above at 0x13)*	
0x1E	0[1]	0[1]	0[1]	cont_clk_mode Continuous clock mode maintains high-speed clock throughout the operation. Clearing this bit enables the IP to go into low power in between high-speed transfers to reduce power. [0] – non-continuous HS clock [1] – continuous HS clock Default depends on the *D-PHY Clock Mode* attribute.

Notes:

1. This bit must be tied to 0 when programming this register. Otherwise, the IP may malfunction.
2. The period for sync_clk is equivalent to *Reference Clock Frequency*/ math.floor((*Reference Clock Frequency* – 1)/20 + 1).

Table 5.2. CN and CO Table of Values

CO		CN			
Control O Value	Actual O Value	Control N Value	Actual N Value	Control N Value	Actual N Value
000	1	11111	1	11010	17
001	2	00000	2	11101	18
010	4	10000	3	11110	19
011	8	11000	4	01111	20
111	16	11100	5	10111	21
—	—	01110	6	11011	22
—	—	00111	7	01101	23

CO		CN			
Control O Value	Actual O Value	Control N Value	Actual N Value	Control N Value	Actual N Value
—	—	10011	8	10110	24
—	—	01001	9	01011	25
—	—	00100	10	00101	26
—	—	00010	11	10010	27
—	—	10001	12	11001	28
—	—	01000	13	01100	29
—	—	10100	14	00110	30
—	—	01010	15	00011	31
—	—	10101	16	00001	32

Table 5.3. CM Table of Values

CM							
Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value
111X0000	16	10001100	76	00001000	136	01000100	196
111X0001	17	10001101	77	00001001	137	01000101	197
111X0010	18	10001110	78	00001010	138	01000110	198
111X0011	19	10001111	79	00001011	139	01000111	199
111X0100	20	10010000	80	00001100	140	01001000	200
111X0101	21	10010001	81	00001101	141	01001001	201
111X0110	22	10010010	82	00001110	142	01001010	202
111X0111	23	10010011	83	00001111	143	01001011	203
111X1000	24	10010100	84	00010000	144	01001100	204
111X1001	25	10010101	85	00010001	145	01001101	205
111X1010	26	10010110	86	00010010	146	01001110	206
111X1011	27	10010111	87	00010011	147	01001111	207
111X1100	28	10011000	88	00010100	148	01010000	208
111X1101	29	10011001	89	00010101	149	01010001	209
111X1110	30	10011010	90	00010110	150	01010010	210
111X1111	31	10011011	91	00010111	151	01010011	211
11000000	32	10011100	92	00011000	152	01010100	212
11000001	33	10011101	93	00011001	153	01010101	213
11000010	34	10011110	94	00011010	154	01010110	214
11000011	35	10011111	95	00011011	155	01010111	215
11000100	36	10100000	96	00011100	156	01011000	216
11000101	37	10100001	97	00011101	157	01011001	217
11000110	38	10100010	98	00011110	158	01011010	218
11000111	39	10100011	99	00011111	159	01011011	219
11001000	40	10100100	100	00100000	160	01011100	220
11001001	41	10100101	101	00100001	161	01011101	221
11001010	42	10100110	102	00100010	162	01011110	222
11001011	43	10100111	103	00100011	163	01011111	223
11001100	44	10101000	104	00100100	164	01100000	224
11001101	45	10101001	105	00100101	165	01100001	225
11001110	46	10101010	106	00100110	166	01100010	226
11001111	47	10101011	107	00100111	167	01100011	227

CM							
Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value
11010000	48	10101100	108	00101000	168	01100100	228
11010001	49	10101101	109	00101001	169	01100101	229
11010010	50	10101110	110	00101010	170	01100110	230
11010011	51	10101111	111	00101011	171	01100111	231
11010100	52	10110000	112	00101100	172	01101000	232
11010101	53	10110001	113	00101101	173	01101001	233
11010110	54	10110010	114	00101110	174	01101010	234
11010111	55	10110011	115	00101111	175	01101011	235
11011000	56	10110100	116	00110000	176	01101100	236
11011001	57	10110101	117	00110001	177	01101101	237
11011010	58	10110110	118	00110010	178	01101110	238
11011011	59	10110111	119	00110011	179	01101111	239
11011100	60	10111000	120	00110100	180	01110000	240
11011101	61	10111001	121	00110101	181	01110001	241
11011110	62	10111010	122	00110110	182	01110010	242
11011111	63	10111011	123	00110111	183	01110011	243
10000000	64	10111100	124	00111000	184	01110100	244
10000001	65	10111101	125	00111001	185	01110101	245
10000010	66	10111110	126	00111010	186	01110110	246
10000011	67	10111111	127	00111011	187	01110111	247
10000100	68	00000000	128	00111100	188	01111000	248
10000101	69	00000001	129	00111101	189	01111001	249
10000110	70	00000010	130	00111110	190	01111010	250
10000111	71	00000011	131	00111111	191	01111011	251
10001000	72	00000100	132	01000000	192	01111100	252
10001001	73	00000101	133	01000001	193	01111101	253
10001010	74	00000110	134	01000010	194	01111110	254
10001011	75	00000111	135	01000011	195	01111111	255

5.2. D-PHY Tx IP Configuration Registers for Timing Parameters

The registers in the following table are used to configure the protocol timing parameters when the design bypasses the hardened CIL or uses the soft logic implementation of the PHY.

Table 5.4. D-PHY Tx Configuration Registers for Timing Parameters

Offset (6 Bits)	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x1F	tLPX[7:0] Duration of any Low-Power state. Default depends on the *t_LPX* attribute.							
0x20	tCLK-PREP[7:0] Duration of the LP-00 clock state immediately before the HS-0 clock state in the LP-to-HS sequence. Default depends on the *t_CLK-PREPARE* attribute.							
0x21	tCLK_HSZERO[7:0] Duration of the clock HS-0 state prior to starting the actual toggling of the high-speed clock. The calculated value must be offset up by N clock cycles because of some internal processing. If *D-PHY TX IP == 'Hard D-PHY'* N = (*TX Gear*/8) - 1 Else: N = 1 Default depends on the (*t_CLK-ZERO* + N) attribute.							
0x22	tCLKPRE[7:0] Duration of the LP-00 clock state immediately before the HS-0 clock state in the LP-to-HS sequence. The calculated value must be offset down by N clock cycles because of some internal processing. If *D-PHY TX IP == 'Hard D-PHY'* N = (*TX Gear*/8) Else: N = 2 Default depends on the (*t_CLK-PRE* – N) attribute.							
0x23	tCLKPOST[7:0] Duration of the HS clock after the last associated Data Lane has transitioned to LP Mode. The interval is defined as the period from the end of tHS-TRAIL to the beginning of tCLK-TRAIL. Default depends on the (*t_CLK_POST*) attribute.							
0x24	tCLKTRAIL[7:0] Duration of the HS-0 state after the last clock bit of an HS transmission burst. The calculated value must be offset down by N clock cycles because of some internal processing. If *D-PHY TX IP == 'Soft D-PHY'* N = 1 Else: N = 0 Default depends on the (*t_CLK-TRAIL* – N) attribute.							
0x25	tCLKEXIT[7:0] Duration of the clock LP-11 state following an HS transmission burst. The calculated value must be offset up by 1 clock cycle because of some internal processing. Default depends on the (*t_CLK-EXIT* + 1) attribute.							
0x26	tDATPREP[7:0] Duration of the LP-00 Line state before the HS-0 Line state. Default depends on *t_HS-PREPARE* attribute.							

Offset (6 Bits)	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x27	tDAT_HSZERO[7:0][1] Delay from the LP-00 State to the assertion of the d_hs_rdy_o signal. The calculated value must be offset up by 1 clock cycle because of some internal processing. The actual HS-ZERO on the D-PHY data lanes depends on these three factors: • The delay between the d_hs_rdy_o assertion and the time the requestor sends the payload of a long packet (tHSZERO_PKTEN). • The number of cycles the packet header (if enabled) can create the sync pattern and the 32-bit header. This varies with the number of lanes and gearing. • The serializer delay. The timing from parallel data input to the serialized output data differs between soft and hard D-PHY implementations. Default depends on the (*t_HS_ZERO* + 1) attribute. Refer to Figure 2.24 for reference.							
0x28	tDATTRAIL[7:0] Duration of the flipped bit after the last payload data bit of an HS transmission burst. The calculated value must be offset by N clock cycles because of some internal processing. If *D-PHY TX IP == 'Hard D-PHY':* N = + (16 / *TX Gear)* (offset up) Else: N = -1 (offset down) Default depends on the (*t_HS_TRAIL* + N) attribute.							
0x29	tDATEXIT[7:0] Duration of the data LP-11 state following an HS transmission burst. The calculated value must be offset up by 1 clock cycle because of some internal processing. Default depends on the (*t_HS_EXIT*+1) attribute.							
0x2D	tSKEWCAL_INIT[7:0] Duration of Initial Skew Calibration.							
0x2E	tSKEWCAL_INIT [15:8] Duration of Initial Skew Calibration. Default depends on the *t_SKEWCAL-INIT* attribute.							
0x2F	tSKEWCAL_PERIOD[7:0] Duration of Periodic Skew Calibration.							
0x30	tSKEWCAL_PERIOD[15:8] Duration of Periodic Skew Calibration. Default depends on the *t_SKEWCAL-PERIOD* attribute.							
0x31	tSKEWCAL_HSZERO Duration when the data lanes are in HS-0 state before transmitting the sync sequence for HS skew calibration. The calculated value must be offset down by 2 clock cycles because of some internal processing. Default depends on the (*t_HS_ZERO during skew calibration – 2)* attribute.							

5.3. D-PHY Tx IP Packet Formatter Registers

These read only registers store the header information of the last packet transmission request received by the IP. These registers are only available when the Packet Formatter is enabled.

Table 5.5. D-PHY Tx Status Registers for Timing Parameters

Offset (6 Bits)	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x2A	vc_id[1:0] Default is 0x0.		data_type[5:0] Default is 0x00.					
0x2B	word_count[15:8] Default is 0x00.							
0x2C	word_count[7:0] Default is 0x00.							

vc_id[1:0] – 2-bit virtual channel ID of the received packet (vc_i).

data_type[5:0] – 6-bit CSI-2 or DSI data type field (dt_i).

word_count[15:0] – 16-bit word count field. This denotes the number of bytes in the payload of a long packet. In a short packet, this contains a 2-byte data (wc_i).

6. Designing with the IP

This section provides information on how to generate the IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

6.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. To generate the D-PHY Tx IP in the Lattice Radiant software, follow these steps:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **CSI-2/DSI D-PHY Transmitter** under **IP, Audio_Video_and_Image_Processing** category. The **Module/IP Block Wizard** opens as shown in Figure 6.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

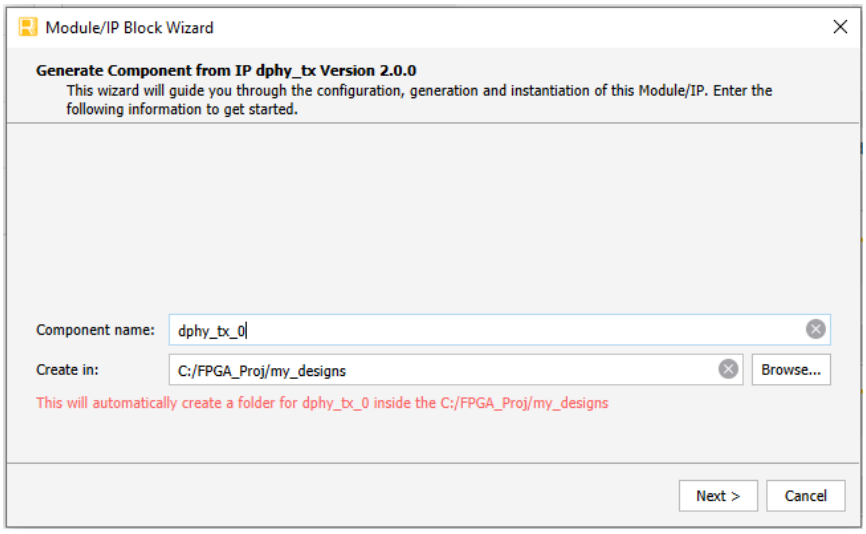

Figure 6.1. Module/IP Block Wizard

3. In the next **Module/IP Block Wizard** window, customize the selected **CSI-2/DSI D-PHY Transmitter IP** using drop-down lists and check boxes. Figure 6.2 shows an example configuration of the CSI-2/DSI D-PHY Transmitter IP. For details on the configuration options, refer to the IP Parameter Description section.

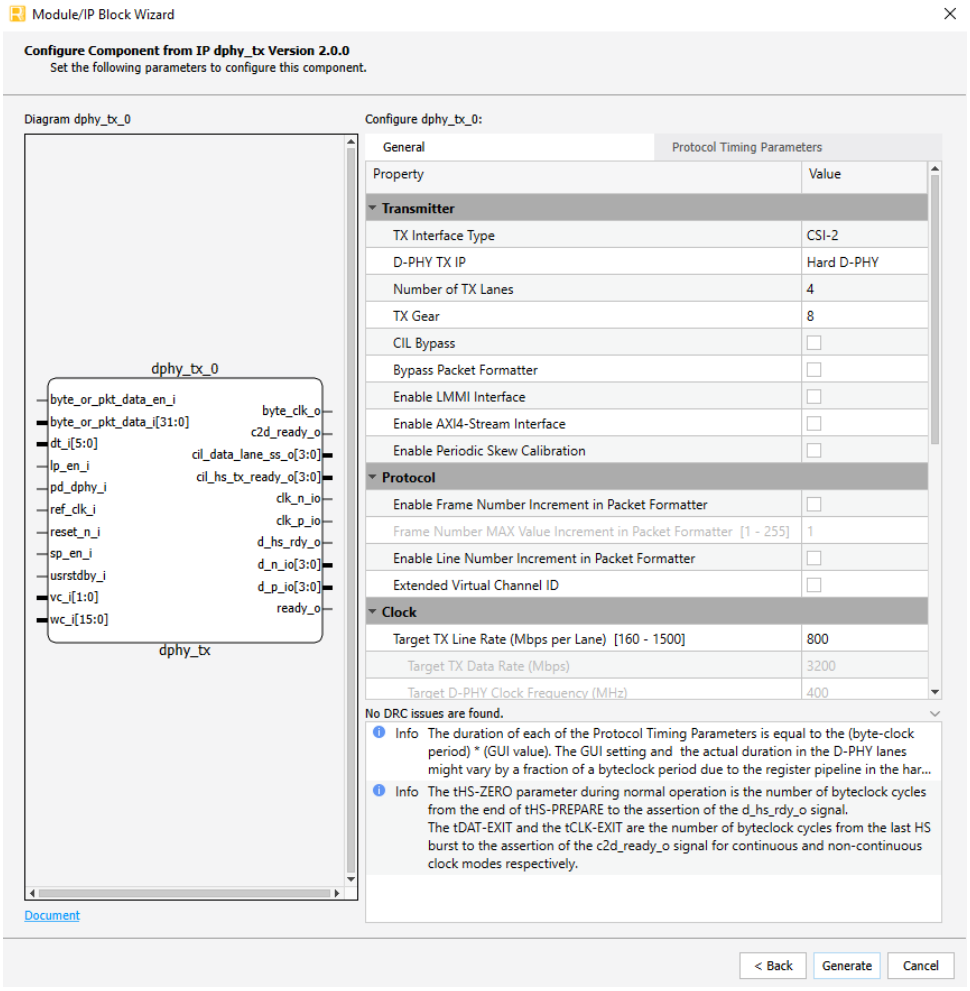

Figure 6.2. IP Configuration

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 6.3.

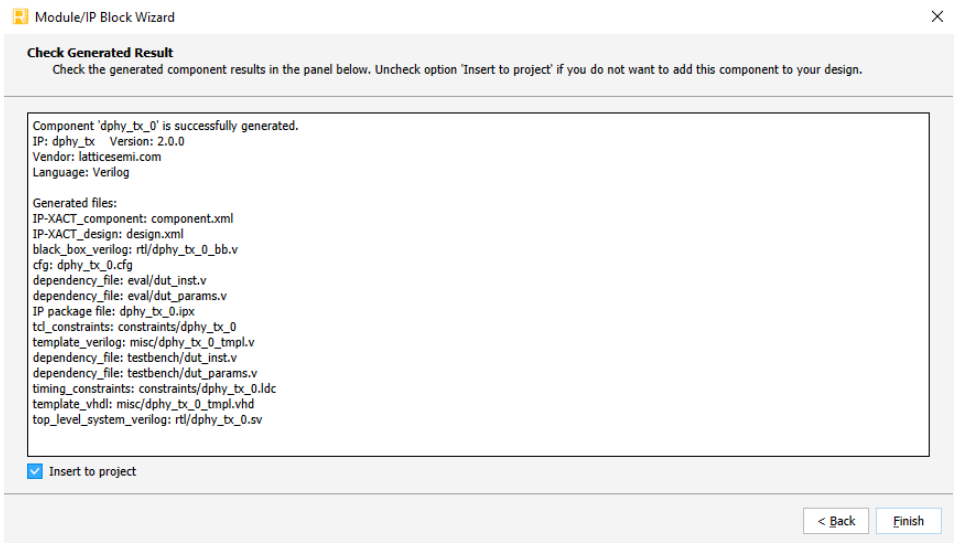

Figure 6.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 6.1.

6.1.1. Generated Files and File Structure

The generated CSI-2/DSI D-PHY Transmitter module package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 6.1.

Table 6.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

An evaluation wrapper file (eval/eval_top.sv) that instantiates the reference source file is also generated. This file provides an example wrapper file that can be used for evaluation purposes.

6.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a PDC File.

Post-Synthesis constraint files (.pdc) contain both timing and non-timing constraint .pdc source files for storing logical timing/physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

6.3. Timing Constraints

CSI-2/DSI D-PHY Transmitter IP generates the following constraint files:

- A legacy pre-synthesis constraint file in LDC format (*<ip_instance_path>/constraints/<instance_name>.ldc*) that is automatically used and propagated by the SW tool.
- A constraint file in SDC format (*<ip_instance_path>/constraints/constraint.sdc*) that contains both pre-synthesis and post-synthesis IP constraints. These constraints are automatically used and propagated by the software tool starting from the Lattice Radiant software version 2024.1. These constraints can be modified if you have a thorough understanding of the effect of each constraint.
- An evaluation post-synthesis constraint file in PDC format (*<ip_instance_path>/eval/constraint_eval.pdc*). In this constraint file, sections 1 and 2 are for evaluation purposes and can be used as a starting point for constraints of the system-level design. You must define the correct clock targets based on your design.

```
#-------------------------------------------------------------------------------
# GENERAL NOTES
#
# This file contains 2 sections:
#
# Section 1: Settings
#   This section is provided to complement Section 2. This is for evaluation
#   purposes only. You must define the correct clock targets based on system-
#   level design.
#
# Section 2: Evaluation Part
#   This section is provided for evaluation purposes only of the IP and should
#   be used to give you starting point for constraints of the system-level
#   design. You need to provide proper timing and physical design constraints
#   to ensure that your design meets the desired performance goals on the FPGA.
#
#-------------------------------------------------------------------------------
```

Figure 6.4. Header of the Generated PDC Files

To run the software implementation flow using the provided evaluation file after the IP is generated, follow these steps:

1. In the **Input Files** section of the Lattice Radiant software project, add the evaluation wrapper file *<ip_instance_path>/eval/eval_top.sv*.
2. In the **Post-Synthesis Constraint Files** section, add *<ip_instance_path>/eval/constraint_eval.pdc*.
3. Run the implementation flow.

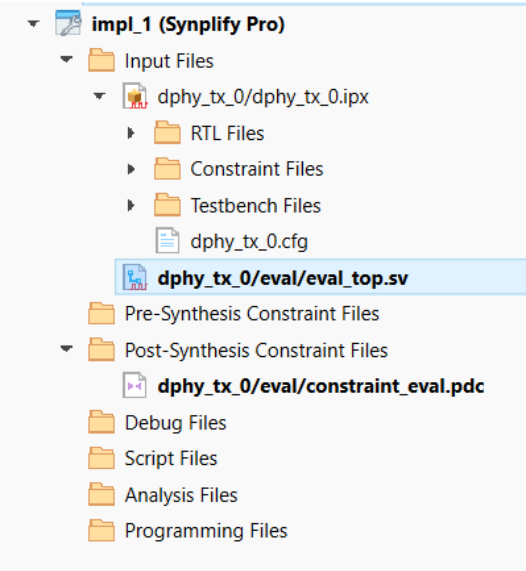

Figure 6.5. Example Evaluation Project Settings

Notes:

- You need to provide proper timing and physical design constraints to ensure that your design meets the desired performance goals on the FPGA.
- The constraint files have been verified during IP evaluation with the evaluation wrapper instantiated directly in the top-level module. The remaining unconstrained paths in the evaluation report are for the input and output delay constraints of the top-level ports of the IP. These ports are expected to be driven and utilized in FPGA fabric and not mapped to FPGA I/O in your system-level design.
- During synthesis, you can ignore clock related warnings as the evaluation IP does not include clock-related constraints in pre-synthesis level.
- During post-synthesis, there may be warnings related to dropped constraints. As the IP supports many configurations and parameter combinations, some default constraints may not be applicable to the selected configuration.

- If *Enable Edge Clock Synchronizer and Divider* is checked and the provided evaluation wrapper *<ip_instance_path>/eval/eval_top.sv* is not used when evaluating only the soft IP, you may encounter the Place and Route error as the Edge Clock Synchronizer clock (eclk_syncclk_o) is illegally mapped to the FPGA I/O. This clock is intended to be connected to a DDR primitive or just left unconnected if unused.

Refer to Lattice Radiant Timing Constraints Methodology for details on how to constrain your design.

6.4. Specifying the Strategy

The Lattice Radiant software provides two predefined strategies: Area and Timing. It also enables you to create customized strategies. For details on how to create a new strategy, refer to the Strategies section of the Lattice Radiant Software user guide.

6.5. Running Functional Simulation

An example simulation environment is provided after you generate the IP. You can find the files in *<ip_instance_path>/testbench/*. This example environment supports limited testing features as the primary intent is to provide a starting point on checking the functionality of the IP. Official IP verification is done through Universal Verification Methodology (UVM).

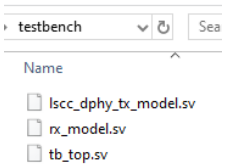

Figure 6.6. Example Simulation Environment File Directory

Default simulation environment instantiates the generated IP *<ip_instance_path>/rtl/<Component name>.sv* as DUT. To instantiate the DUT with the evaluation wrapper file *<ip_instance_path>/eval/eval_top.sv* as top, uncomment the USE_EVAL_TOP_DUT compiler directive on top of the tb_top.sv file.

```
// Testbench Local Settings
// Selects which DUT to instantiate in the testbench.
// When USE_TOP_EVAL_DUT is defined, testbench instantiates top_eval
// as DUT. Otherwise, testbench instantiates the generated IP (IPX).
`define USE_TOP_EVAL_DUT
```

Figure 6.7. Adding USE_TOP_EVAL_DUT in the tb_top.sv File

To run functional simulation, follow these steps:

1. Add testbench file tb_top.sv in the **Input Files** section. Set the file to include in Simulation only, as shown in the following diagram.

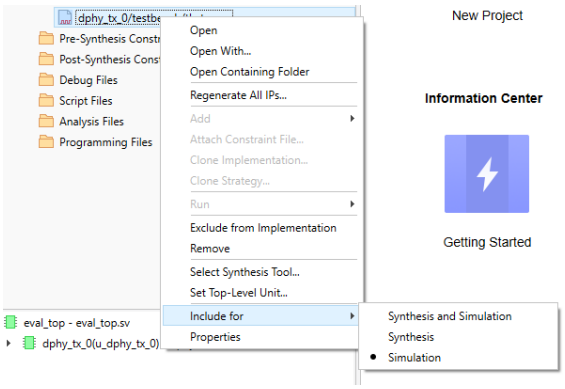

Figure 6.8. Example Steps on How to Include File for Simulation Only

2. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in the following diagram.

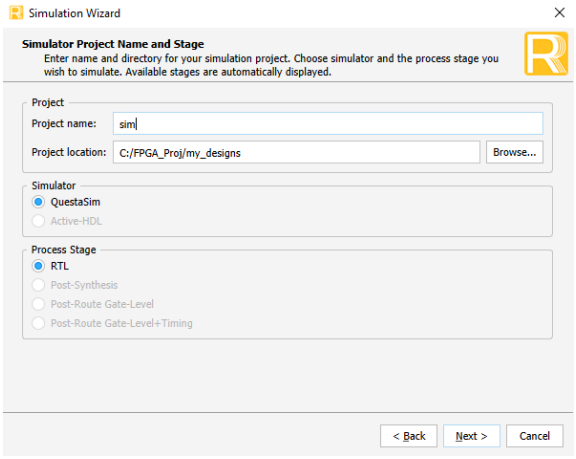

Figure 6.9. Simulation Wizard

3. Click **Next** to open the **Add and Reorder Source** window as shown in the following diagram.

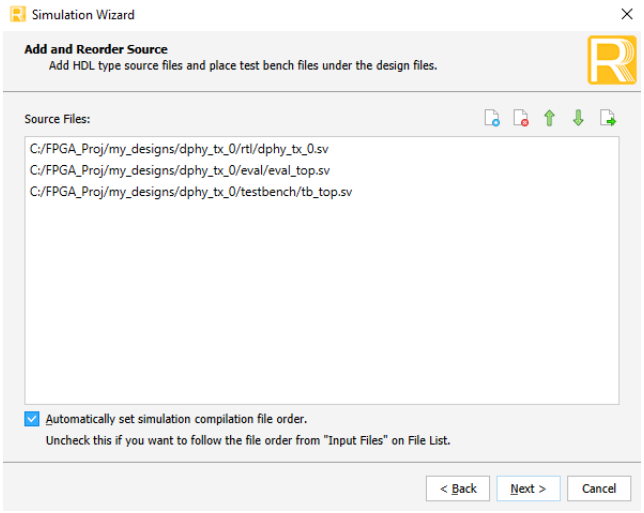

Figure 6.10. Add and Reorder Source

4. Click **Next**. The **Summary** window opens.
5. Set **Run Simulation** to 0 to ensure the simulation runs completely. Click **Finish** to run the simulation.

The waveform in the following diagram shows an example simulation waveform.

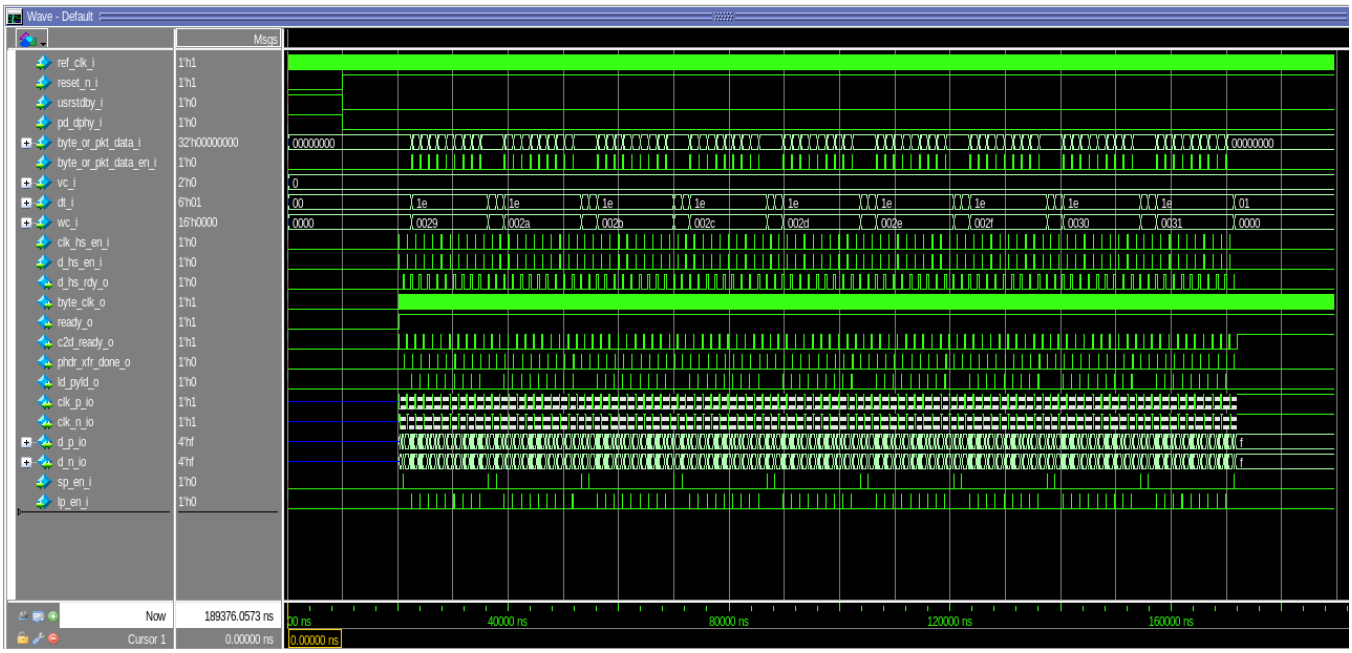

Figure 6.11. Simulation Waveform

6.5.1. Simulation Results

When the simulation is complete, the output in the Transcript window is shown in the following diagram.

```
# 172085057 TEST END
#
#    ***EOT PACKET CHECK PASS***
#    ***PAYLOAD DATA PASS***
#    ***CRC PASS***
# ***SIMULATION PASSED***
```

Figure 6.12. Simulation Log

If your simulation failed, ensure that the reset signals and clock signals are set up as described in the Functional Description section. You can also enable Miscellaneous status signals to debug the functional simulation.

7. Debugging

This section lists possible issues and suggested troubleshooting steps that you can follow.

7.1. Debug Methods

CSI-2/DSI D-PHY Tx IP provides optional pins for observability during the debug process. For more information on the debug signals, refer to Table 4.4.

7.2. Debug Tools

You can use the tool described in the subsection to debug CSI-2/DSI D-PHY Tx IP design issues.

7.2.1. Reveal Analyzer

The Reveal™ Analyzer continuously monitors signals within the FPGA for specific conditions that range from simple to complex conditions. When the trigger condition occurs, the Reveal Analyzer saves signal values preceding, during, and following the event for analysis, including a waveform presentation. The data can be saved in the following format:

- Value change dump file (.vcd) that can be used with tools such as QuestaSim™.
- ASCII tabular format that can be used with tools such as Microsoft® Excel.

Before running the Reveal Analyzer, use the Reveal Inserter to add Reveal modules to your design. In these modules, specify the signals to monitor, define the trigger conditions, and set other preferred options. The Reveal Analyzer supports multiple logic analyzer cores using hard/soft JTAG interface. You can have up to 15 modules, typically one for each clock region of interest. When the modules are set up, regenerate the bitstream data file to program the FPGA.

During debug cycles, this tool uses a divide and conquer method to narrow down to problem areas into many small functional blocks to control and monitor the status of each block.

Refer to the Reveal User Guide for Radiant Software for details on how to use the Reveal Analyzer.

8. Design Considerations

8.1. Design Considerations When D-PHY PLL Mode is Set to External

- Ensure the TX D-PHY settings (for example: number of lanes, TX line bitrate) in the IP GUI are set as intended.
- Ensure the reference clock frequency in the IP GUI matches with the PLL clocks driving the pll_clkop_i and pll_clkos_i pins.
- Ensure the clock that drives the pll_clkos_i pin is set to 90-degree out of phase from the clock that drives the pll_clkop_i pin.

8.2. Limitations

- Escape Mode, Ultra Low Power State (ULPS), and Bus Turnaround sequences are not yet supported.
- Some configurations may fail Static Timing Analysis when compiling your design using LSE. If this happens, consider compiling your design using the Synopsis Synplify Pro.
- When *CIL Bypass* is unchecked, because of the limitation of the hard D-PHY IP when CIL is enabled, HS Sync-Sequence for HS Skew Calibration is only 8 UI instead of 16 UI of all one.
- Some configurations may fail Static Timing Analysis when compiling your design using LSE. If this happens, consider compiling your design using the Synopsis Synplify Pro.
- Some IP configurations may have slower Fmax when used in devices with slow speed grade. The following Fmax values are approximates and may vary depending on the system-level design:
  - Nexus devices: 110 MHz for Gear 8, 150 MHz for Gear 16
  - Avant devices: 162 MHz

Appendix A. Resource Utilization

The following tables show the maximum frequency and resource utilization for a certain IP configuration.

Table A.1. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2024.1 production build
Device Used	LIFCL-40-9BG400C
Performance Grade	9_High-Performance_1.0V
Synthesis Tool	Synplify Pro® V-2023.09LR-1, Build 251R, May 14 2024

Table A.2. Resource Utilization[1]

Lane (Gear)	TX Interface Type	IP Type	Bit Rate Lane	Bypass Packet Formatter[2]	LMMI[2] Bus	AXI[2] Bus	Registers	Fmax (MHz)	LUT[3]	EBR	High-Speed I/O Interfaces
4 (8)	CSI-2	Hard DPHY[4]	1000 Mbps	DIS	DIS	EN	312	195.00	635	0	1 x Hard D-PHY
4 (8)	CSI-2	Soft DPHY	1000 Mbps	DIS	DIS	EN	345	200.00	660	0	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (8)	CSI-2	Hard DPHY[5]	1000 Mbps	DIS	DIS	EN	154	186.50	553	2	1 x Hard D-PHY
4 (16)	CSI-2	Hard DPHY[5]	2500 Mbps	DIS	DIS	DIS	347	194.14	1332	4	1 x Hard D-PHY
4 (16)	CSI-2	Hard DPHY[4]	2500 Mbps	DIS	DIS	DIS	420	181.36	1497	0	1 x Hard D-PHY
4 (8)	DSI	Soft DPHY	1500 Mbps	DIS	DIS	DIS	391	198.65	754	2	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (8)	DSI	Hard DPHY[4]	1500 Mbps	DIS	DIS	DIS	358	193.61	715	2	1 x Hard D-PHY
4 (16)	DSI	Hard DPHY[5]	2500 Mbps	DIS	DIS	DIS	347	184.94	1326	4	1 x Hard D-PHY

Notes:

1. All other settings are default.
2. DIS indicates Disable, which means the **Bypass Packet Formatter**, **Enable LMMI Interface**, or **Enable AXI4-Stream Interface** in the IP GUI is left unchecked. EN indicates enable which means the option in IP GUI is checked.
3. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.
4. Hard D-PHY – CIL Bypassed.
5. Hard D-PHY – CIL Enabled.

Table A.3. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2024.1 production build
Device Used	LIFCL-40-7BG400I
Performance Grade	7_High-Performance_1.0V
Synthesis Tool	Synplify Pro® V-2023.09LR-1, Build 251R, May 14 2024

Table A.4. Resource Utilization[1,6]

Lane (Gear)	TX Interface Type	IP Type	Bit Rate Lane	Bypass Packet Formatter[2]	LMMI[2] Bus	AXI[2] Bus	Registers	Fmax (MHz)	LUT[3]	EBR	High-Speed I/O Interfaces
4 (8)	CSI-2	Hard DPHY[4]	1500 Mbps	DIS	DIS	DIS	312	200	704	0	1 x Hard D-PHY
4 (8)	CSI-2	Soft DPHY	1034 Mbps	DIS	DIS	DIS	345	161.99	734	0	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (8)	CSI-2	Hard DPHY[5]	1500 Mbps	DIS	DIS	DIS	154	157.82	639	2	1 x Hard D-PHY
4 (16)	CSI-2	Hard DPHY[5]	2500 Mbps	DIS	DIS	DIS	348	171.82	1322	4	1 x Hard D-PHY
4 (16)	DSI	Hard DPHY[4]	2500 Mbps	DIS	DIS	DIS	354	152.23	1357	4	1 x Hard D-PHY
4 (8)	DSI	Soft DPHY	1034 Mbps	DIS	DIS	DIS	391	159.01	779	2	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC

Notes:

1. All other settings are default.
1. DIS indicates Disable, which means the **Bypass Packet Formatter**, **Enable LMMI Interface**, or **Enable AXI4-Stream Interface** in the IP GUI is left unchecked. EN indicates enable which means the option in IP GUI is checked.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.
3. Hard D-PHY – CIL Bypassed.
4. Hard D-PHY – CIL Enabled.
5. Fmax is generated using multiple iterations of Place and Route.

Table A.5. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2024.1 production build
Device Used	LAV-AT-E70ES1-3LFG1156C
Performance Grade	3
Synthesis Tool	Synplify Pro® V-2023.09LR-1, Build 251R, May 14 2024

Table A.6. Resource Utilization[1]

Lane (Gear)	TX Interface Type	IP Type	Bit Rate Lane	Bypass Packet Formatter[2]	LMMI[2] Bus	AXI[2] Bus	Registers	Fmax (MHz)	LUT[3]	EBR	High-Speed I/O Interfaces
4 (8)	CSI-2	Soft DPHY	1800 Mbps	DIS	DIS	DIS	350	250	817	0	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (8)	DSI	Soft DPHY	1800 Mbps	DIS	DIS	DIS	396	250	797	1	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC

Notes:

1. All other settings are default.
2. DIS indicates Disable, which means the **Bypass Packet Formatter**, **Enable LMMI Interface**, or **Enable AXI4-Stream Interface** in the IP GUI is left unchecked. EN indicates enable which means the option in IP GUI is checked.
3. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.

Table A.7. Device and Tool Tested

—	Value
Software Version	Lattice Radiant software 2024.1 production build
Device Used	LAV-AT-E70ES1-1LFG1156C
Performance Grade	1
Synthesis Tool	Synplify Pro® V-2023.09LR-1, Build 251R, May 14 2024

Table A.8. Resource Utilization[1,4]

Lane (Gear)	TX Interface Type	IP Type	Bit Rate Lane	Bypass Packet Formatter[2]	LMMI[2] Bus	AXI[2] Bus	Registers	Fmax (MHz)	LUT[3]	EBR	High-Speed I/O Interfaces
4 (8)	CSI-2	Soft DPHY	1800 Mbps	DIS	DIS	DIS	350	250	817	0	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (8)	DSI	Soft DPHY	1800 Mbps	DIS	DIS	DIS	396	250	797	1	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC

Notes:

1. All other settings are default.
2. DIS indicates Disable, which means the **Bypass Packet Formatter**, **Enable LMMI Interface**, or **Enable AXI4-Stream Interface** in the IP GUI is left unchecked. EN indicates enable which means the option in IP GUI is checked.
3. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.
4. Fmax is generated using multiple iterations of Place and Route.

For more information regarding a specific configuration, generate the IP, run synthesis and MAP, and check the MAP reports for resource utilization. Number may vary when using a different software version or targeting a different device density, synthesis tool, or speed grade. For better Static Timing Analysis performance, you are recommended to run multiple iterations of Place and Route and/or set Optimization Goal to Timing in the Strategy section of the software tool.

References

- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- Certus-NX High-Speed I/O Interface (FPGA-TN-02216)
- CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.2, July 2024

Section	Change Summary
All	Performed minor formatting and typo edits.

Introduction	• Updated Table 1.1. CSI-2/DSI DPHY Tx IP Core Quick Facts.
	• Added Lattice Avant device support in the Soft MIPI D-PHY Tx IP Core Features section.
	• Updated Table 1.2. Ordering Part Number.
	  • Added OPNs for Lattice Avant-G, Lattice Avant-X, and Mach XO5-NX devices.
	  • Updated OPNs for CrossLink-NX, Certus-NX, and CertusPro-NX devices.
	• Added IP version 2.0.0 in Table 1.3. IP Validation Level.
	• Added signal name for bidirectional signals in the Signal Names section.

Functional Description	• Removed hsync_start_i and vsync_start_i from the following diagrams:
	  • Figure 2.1. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Enabled
	  • Figure 2.2. D-PHY Tx IP Block Diagram with AXI4-Stream Enabled and LMMI Disabled
	  • Figure 2.3. D-PHY Tx IP Block Diagram with AXI4-Stream Disabled and LMMI Enabled
	  • Figure 2.4. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Disabled
	• Updated the signals when the AXI4-Stream device is not enabled in the AXI4-Stream Device Receiver section.
	• Updated the Soft D-PHY Module section.
	• Updated the Internal PLL section.
	  • Mentioned that the internal PLL mode is only supported in the hard D-PHY of CSI-2/DSI D-PHY Transmitter IP
	  • Updated the data rate equation.
	• Updated the condition for the data lanes in HS-00 state for external requesting module in the Global Operation Module section.
	• Updated the section titles and updated the content in the following sections:
	  • Renamed section from *Short Packet Transmission in CSI-2/DSI Interfaces* to Packet Transmission in CSI-2/DSI Interfaces with Packet Formatter for Soft D-PHY and Hard D-PHY with Soft CIL (CIL Bypass is Checked).
	  • Renamed section from *Long Packet Transmission in CSI-2/DSI Interfaces* to Packet Transmission in CSI-2/DSI Interface with Packet Formatter for Hard D-PHY with Hardened CIL (CIL Bypass is Unchecked).
	  • Renamed section from *Long Packet Transmission in CSI-2/DSI Interfaces without Packet Formatter* to Packet Transmission in CSI-2/DSI Interface without Packet Formatter.
	• Added the following sections:
	  • Non-Continuous D-PHY Clock Mode
	  • CIL-Enabled Debug Ports
	  • Timing Configuration Registers
	• Updated Figure 2.22. D-PHY Tx Input Bus to Enable Periodic Skew Calibration.
	• Updated the Byte Data Arrangement section.

IP Parameter Description	• Updated Table 3.1. General Attributes1.
	  • Updated the *Enable Frame Number Increment in Packet Formatter*, *Enable Line Number Increment in Packet Formatter*, and *Enable Periodic Skew Calibration* attributes.
	  • Added the *Enable Edge Clock Synchronizer and Divider* attribute.
	• Updated Table 3.2. Protocol Timing Parameters Attributes1.
	  • Corrected the attribute name for t_CLK_POST.
	  • Updated the *t_HS-PREPARE*, *t_HS_ZERO during skew calibration*, *t_HS_ZERO*, *t_HS_TRAIL*, *t_CLK-PREPARE*, *t_CLK-ZERO*, and *t_CLK-TRAIL* attributes.
	  • Updated table note on the general timing parameter duration.
	• Added table note on timing parameter duration when *CIL Bypass* is unchecked.

Section	Change Summary
Signal Description	Updated the following tables: • Table 4.1. D-PHY Tx Signal Description • Table 4.2. LMMI Device Target Signal Description • Table 4.3. AXI4-Stream Device Receiver Signal Description • Table 4.4. Debug Interface Signal Description

Register Description	• Added condition when accessing the registers in the Register Description section.
	• Updated the following tables:
	  • Table 5.1. Hard Configured D-PHY Tx Configuration Registers (MIPI Programmable Bits)
	  • Table 5.4. D-PHY Tx Configuration Registers for Timing Parameters
	  • Table 5.5. D-PHY Tx Status Registers for Timing Parameters

Designing with the IP	Updated the following sections: • Generating and Instantiating the IP • Timing Constraints • Running Functional Simulation
Debugging	Updated ModelSim to QuestaSim in the Reveal Analyzer section.
Design Considerations	Added the Limitations section.
Resource Utilization	Updated this section.
References	Updated references.

Revision 2.1, January 2024

Section	Change Summary
Disclaimers	Updated disclaimers.
Inclusive Language	Added inclusive language boilerplate.
Introduction	• Reworked section contents. • Changed LAV-AT-500E to LAV-AT-E70 in Table 1.1. • Reworked *subsection 5.1 Licensing the IP* and *section 6 Ordering Part Number* and renamed to *subsection* 1.4 Licensing and Ordering Information. • Reworked *subsection 4.4 Core Validation* and *subsection 5.2 Hardware Evaluation* and renamed to *subsection* 1.5 IP Validation Summary. • Added Minimum Device Requirements subsection. • Reworked *subsection 1.3 Conventions* and renamed to *subsection* 1.7 Naming Conventions.
Functional Description	• Reworked *section 2 Functional Description* and renamed to *subsection* 2.1 IP Architecture Overview. • Added *subsection* 2.2 User Interfaces. • Reworked *subsection 2.1.4 LMMI Device Target* and moved to *subsection* 2.2.1 LMMI Device Target. • Reworked *subsection 3.6 AXI4-Stream Device Receiver* and moved to *subsection* 2.2.2 AXI4-Stream Device Receiver. • Updated the pll_clkos_i phase shift in *subsection* 2.3.3 External PLL. • Reworked *section 3 Timing Diagrams* and moved to *subsection* 2.6 Timing Diagrams.
IP Parameter Description	Reworked *subsection 2.3 Attribute Summary* and renamed to *section* 3 IP Parameter Description.
Signal Description	• Reworked *subsection 2.2 Signal Description* and moved to *section* 4 Signal Description. • Updated description for pll_clkos_i in Table 4.1.
Register Description	Reworked subsection 2.4 Internal Registers and renamed to *section* 5 Register Description.
Designing with the IP	• Reworked *section 4 Core Generation, Simulation, and Validation* and renamed to *section* 6 Designing with the IP. • Reworked *subsection 4.1 Generating the IP* and renamed to *subsection* 6.1 Generating and Instantiating the IP. • Added *subsection* 6.2 Design Implementation. • Reworked *subsection 4.3 Constraining the IP* and renamed to *subsection* 6.3 Timing Constraints. • Added *subsection* 6.4 Specifying the Strategy.

Section	Change Summary
	• Reworked *subsection 4.2 Running Functional Simulation* and moved to *subsection* 6.5 Running Functional Simulation.
Debugging	Added this section.
Design Considerations	Added this section.
Resource Utilization	Updated for the latest software version.
References	Reworked section contents.

Revision 2.0, June 2023

Section	Change Summary
All	Changed Slave to Receiver/Target/Secondary, and Master to Primary globally.
Introduction	• Added MachXO5-NX device family support to the general introduction. • Added to LFCL-33, LFCPNX-50, LFCMXO5-25, LFCMXO5-55T, and IP Core v1.9.x – Lattice Radiant software 2023.1 to Table 1.1. CSI-2/DSI DPHY Tx IP Core Quick Facts.
Functional Description	• Updated Figure 2.9. MIPI D-PHY Tx LP to HS Transition Flow Diagram on Data Lanes showing the virtual link between LP-11 and LP-Rqst. • Updated Table 2.2. D-PHY Tx IP Core Signal Description removing the support of Avant devices from pll_clkos_i.

Revision 1.9, February 2023

Section	Change Summary
Functional Description	• Updated Table 2.3. Attributes Table1 and Table 2.2. D-PHY Tx IP Core Signal Description. • Updated the Hard D-PHY Module section and added the Soft D-PHY section. • Deleted *The D-PHY Module provides the MIPI D-PHY physical serial data communication layer on which the protocols CSI-2 or DSI runs. This may be a hardened block or a soft logic implementation of the D-PHY using special IOs*. • Deleted The LP11 state brings back the data lane from high-speed mode to low power mode in Global Operation Module section.
All	Deleted Appendix B. Limitations section.
Core Generation, Simulation, and Validation	Added *This IP has not been hardware validated in Lattice Avant* in the Core Validation section.
References	Added reference links for below: • CrossLink-NX FPGA web page at www.latticesemi.com • Certus-NX FPGA web page at www.latticesemi.com • CertusPro-NX FPGA web page at www.latticesemi.com • Avant-E Web Page at www.latticesemi.com

Revision 1.8, November 2022

Section	Change Summary
Functional Description	Added footnote 2 to Table 2.3. Attributes.
Core Generation, Simulation, and Validation	• Updated the Generating the IP section heading. • Updated the Running Functional Simulation section heading and revised step 1 of the Verilog procedure. • Added the Constraining the IP section.
Ordering Part Number	Updated content to add part number for Avant.
Appendix A. Resource Utilization	Changed row to Software Version in Table A.1.
Appendix B. Limitations	General update to this section.

Revision 1.7.1, August 2022

Section	Change Summary

Introduction	• Added Avant to the supported device families in general description.
	• In Table 1.1. CSI-2/DSI DPHY Tx IP Core Quick Facts:
	  • Added Avant to the Supported FPGA Families;
	  • Added LATG1-500 to the Targeted Devices.
	• In the Features section:
	  • Newly added maximum rate up to 1800 Mbps per lane for Avant devices in the Soft MIPI D-PHY Tx IP Core Features section.

Functional Description	• Newly added the first paragraph regarding Avant device support to the External PLL section. • Specified CSI-2/DSI D-PHY Transmistter IP is for CrossLink-NX devices in the Internal PLL section. • Newly added pll_clkos_i port and its related data for Avant device support only to Table 2.2. D-PHY Tx IP Core Signal Description. • Updated Target TX Line Rate (Mbps per Lane) values reflecting that for Avant devices in Table 2.3. Attributes Table.

Revision 1.7, August 2022

Section	Change Summary
Disclaimers	General update.

Introduction	• In the Features section:
	  • Removed MIPI DSI and MIPI CSI-2 interfacing related feature;
	  • Changed to support *DSI Video Modes*;
	  • Changed *maximum rate up to 2500 Mbps per lane* for support of CrossLink-NX devices only in the Hard MIPI D-PHY Tx IP Core Features section;
	  • Changed *maximum rate up to 1500 Mbps per lane* for support of *CrossLink-NX, Certus-NX, and CertusPro-NX devices* in the Soft MIPI D-PHY Tx IP Core Features section.

Functional Description	• Newly added input signal pll_clkos_i to Figure 2.1. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Enabled, Figure 2.2. D-PHY Tx IP Block Diagram with AXI4-Stream Enabled and LMMI Disabled, Figure 2.3. D-PHY Tx IP Block Diagram with AXI4-Stream Disabled and LMMI Enabled, and Figure 2.4. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Disabled. • Updated the description of the External PLL section. • Specified *CSI-2/DSI D-PHY Transmistter IP* is for *CrossLink-NX devices* in the Internal PLL section. • Updated Target TX Line Rate (Mbps per Lane) values in Table 2.3. Attributes.

Revision 1.6, August 2021

Section	Change Summary

Functional Description	• In Table 2.2. D-PHY Tx IP Core Signal Description, changed the description for:
	  • reset_n_i from synchronous active low system reset to asynchronous active low system reset
	  • ref_clk_i by removing the information on its minimum frequency when PLL mode is external.
	• Updated values of TX Global Operation Timing Parameters from 1-63 to 1-255 in Table 2.3. Attributes Table.
	• Updated register sizes in Table 2.7. D-PHY Tx Configuration Registers for Timing Parameters.
	  • Offset 0x1F-0x29: Updated t*[5:0] to t*[7:0].
	  • Offset 0x2D-0x2E: Updated tSKEWCAL_INIT[9:0] to tSKEWCAL_INIT[15:0].
	  • Offset 0x2F-0x30: Updated tSKEWCAL_PERIOD[9:0] to tSKEWCAL_PERIOD[15:0].

Revision 1.5, June 2021

Section	Change Summary
Introduction	Updated content including Table 1.1 to add CertusPro-NX support.
Functional Description	Updated Table 2.3.
Licensing and Evaluation	Updated content to add CertusPro-NX.
Ordering Part Number	Updated content to add part number for CertusPro-NX.

Revision 1.4, February 2021

Section	Change Summary
Functional Description	• Removed ADC IP Core Native Interface from Table 1.1. • Added ready_o output signal in Figure 2.1, Figure 2.2, Figure 2.3, and Figure 2.4. • Added ready_o and updated c2d_ready_o port names in Table 2.2. D-PHY Tx IP Core Signal Description. • Updated t_SKEWCAL-INIT and t_SKEWCAL-PERIOD attribute Values and Default in Table 2.3. Attributes Table.
Timing Diagrams	Added Initial Skew Calibration for Data Rates Above 1.5 Gbps section.

Revision 1.3, November 2020

Section	Change Summary
Introduction	• Updated Table 1.1. CSI-2/DSI DPHY Tx IP Core Quick Facts. • Updated Lattice Implementation. • Updated reference to the Lattice Radiant Software User Guide. • Added support for periodic deskew calibration to the Features section.
Functional Description	• Added skewcal_period_en_i input port to Figure 2.1, Figure 2.2, Figure 2.3, and Figure 2.4. • Updated Figure 2.6 and added contents to the Global Operation Module section. • Added the skewcal_period_en_i signal under D-PHY Tx and updated axis_stready_o description in Table 2.2. D-PHY Tx IP Core Signal Description. • Updated Table 2.3. Attributes Table. • Added Transmitter attributes. • Added TX Global Operation Timing Parameters attributes. • Updated Clock attributes. • Removed 0x03 Bit[0] data from Table 2.4. Hard Configured D-PHY Tx Configuration Registers (MIPI Programmable Bits). • Updated Table 2.7. D-PHY Tx Configuration Registers for Timing Parameters.
Timing Diagrams	• Added the Enable Periodic Skew Calibration section. • Removed Figure 3.6 and Figure 3.7. • Added bullets to internal signals in AXI4-Stream Device Slave section.
Core Generation, Simulation, and Validation	• Updated reference to the Lattice Radiant Software User Guide. • Updated Figure 4.1. Configure Block of D-PHY Tx. • Updated Figure 4.2. Check Generating Result.
References	Updated reference to the Lattice Radiant Software User Guide.

Revision 1.2, August 2020

Section	Change Summary
Introduction	• Updated Table 1.1. • Updated the Hard MIPI D-PHY Tx IP Core Features and Soft MIPI D-PHY Tx IP Core Features sections.
Functional Description	General update to this section.
Signal Description	Updated Table 2.2. D-PHY Tx IP Core Signal Description.

Section	Change Summary
Attribute Summary	Updated Table 2.3. Attributes Table.
Internal Registers	Removed this section.
Core Generation, Simulation, and Validation	Updated figures in procedures.
Ordering Part Number	Added part numbers.
Appendix A. Resource Utilization	Added this section.
Appendix B. Limitations	Added this section.

Revision 1.1, February 2020

Section	Change Summary
Introduction	• Updated Table 1.1 to add LIFCL-17 as targeted device. • Updated Hard MIPI D-PHY Tx IP Core Features and Soft MIPI D-PHY Tx IP Core Features sections.
Attributes Table	Updated Table 2.1. Attributes Table.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release.

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