MIC5323

High PSRR Low Noise 300 mA µCap Ultra-Low Dropout LDO Regulator

Features

- Ultra Low Dropout Voltage of 120 mV @ 300 mA
- Input Voltage Range: 2.65 to 5.5V
- Stable with Ceramic Output Capacitor
- 300 mA Guaranteed Output Current
- Low Output Noise — 20 µVrms
- High PSRR, up to 80 dB @ 1 kHz
- Less than 30 µs Turn-on Time with CBYP = 0.1 µF
- High Output Accuracy: ±2.0% Over Temperature
- Thermal Shutdown Protection
- Current Limit Protection
- 6-Lead 2 mm × 2 mm UDFN Package
- 5-Lead Thin SOT-23 Package

Applications

- Cellular Phones
- Notebook and Tablet Computers
- Fiber Optic Modules
- Portable Electronics
- Instrumentation Systems
- Audio Codec power supplies

General Description

The MIC5323 is a high-performance, 300 mA LDO regulator, offering extremely high PSRR and very low noise while consuming low ground current.

Ideal for battery operated applications, the MIC5323 features 2% accuracy, extremely low dropout voltage (120 mV @ 300 mA), and low ground current at light load (typically 90 µA). When disabled, the MIC5323 typically consumes less than 1 µA.

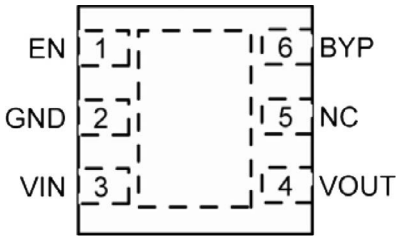
The MIC5323 is a µCap design operating with small ceramic output capacitors for stability, thereby reducing required board space and component cost.

The MIC5323 is available in fixed output voltages and adjustable output voltages in the super compact 6-lead 2 mm × 2 mm UDFN and 5-lead thin SOT-23 package.

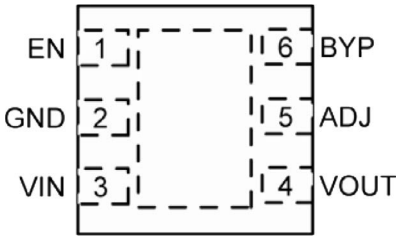
Additional voltage options are available. Contact Microchip marketing.

Package Types

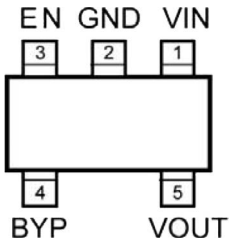
MIC5323-x.xYMT (Fixed)
6-Lead 2 mm x 2 mm UDFN (MT), *Top View*



MIC5323YMT (Adjustable)
6-Lead 2 mm x 2 mm UDFN (MT), *Top View*



MIC5323-x.xYD5 (Fixed)
5-Lead Thin SOT-23 (D5), *Top View*

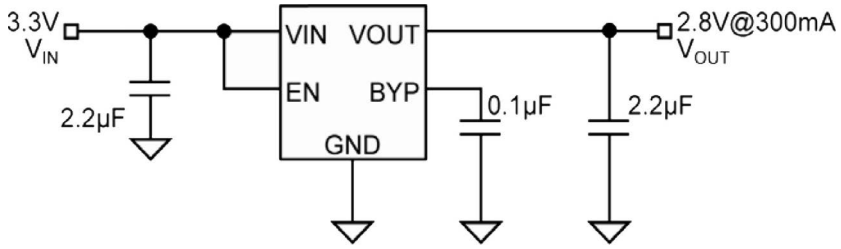


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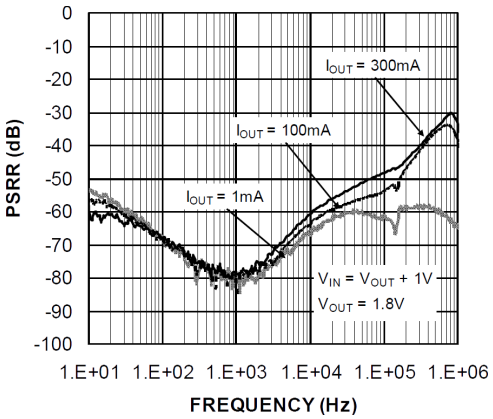
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Typical Application Circuits

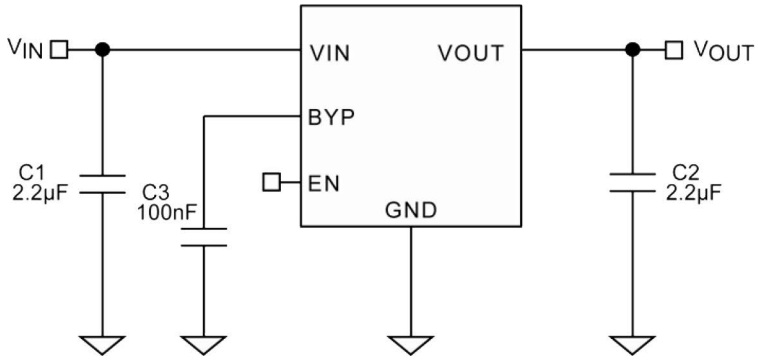
MIC5323 Typical Application Circuit



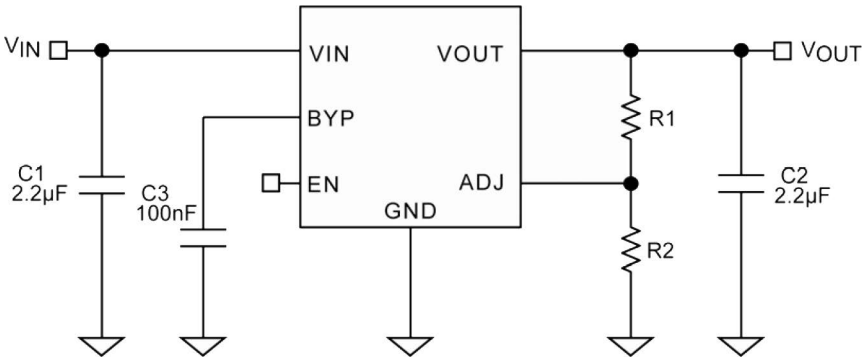
Power Supply Rejection Ratio (CBYP = 0.1 µF)



Typical Application Circuit (Fixed Output)



Typical Application Circuit (Adjustable Output)

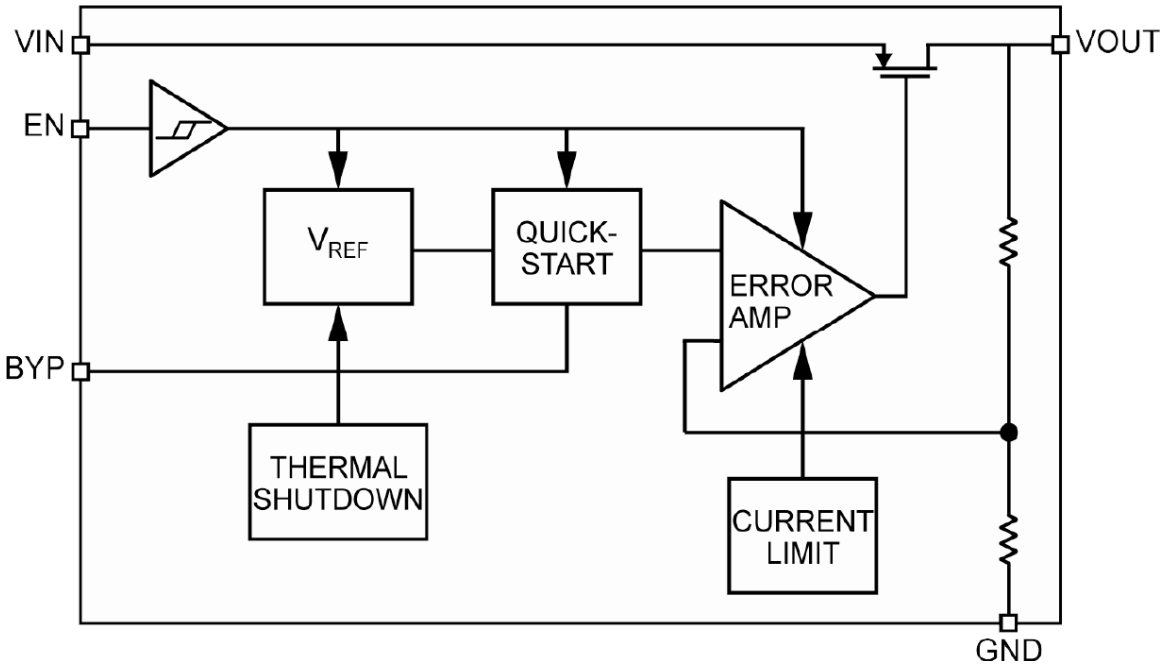


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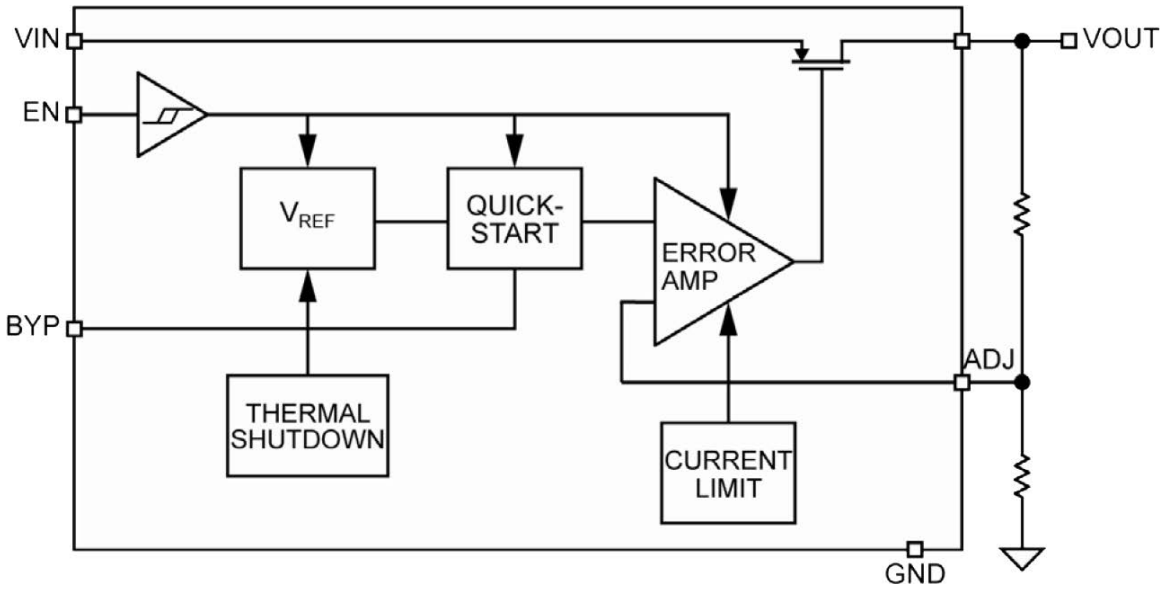
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Functional Block Diagrams

MIC5323 Block Diagram - Fixed



MIC5323 Block Diagram - Adjustable



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Input Voltage (V_{IN})..... 0V to +6V
Enable Input Voltage (V_{EN}) ..... 0V to +6V
Power Dissipation (P_D) Note 1 ..... Internally Limited
ESD Rating (Note 2)..... 2 kV

Operating Ratings ‡

Supply Input Voltage (V_{IN})..... +2.65V to +5.5V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

$V_{IN} = V_{OUT} + 1.0V$; $C_{OUT} = 2.2\ \mu F$; $I_{OUT} = 100\ \mu A$; $T_J = 25°C$, **bold** values indicate –40°C to +125°C, unless noted. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy	V_{OUT}	**–2.0**	—	**2.0**	%	Variation from nominal V_{OUT}, I_{OUT} = 100 µA to 300 mA
Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	—	0.02	**0.3**	%/V	$V_{IN} = V_{OUT}$ + 1V to 5.5V
Load Regulation (Note 2)	$\Delta V_{OUT}/V_{OUT}$	—	0.1	**0.5**	%	I_{OUT} = 100 µA to 300 mA
Dropout Voltage	V_{DO}	—	20	**35**	mV	I_{OUT} = 50 mA, V_{OUT} > 2.8V
		—	60	**85**		I_{OUT} = 150 mA, V_{OUT} > 2.8V
		—	120	**170**		I_{OUT} = 300 mA, V_{OUT} > 2.8V
		—	25	**45**		I_{OUT} = 50 mA, $V_{OUT} \le$ 2.8V
		—	75	**110**		I_{OUT} = 150 mA, $V_{OUT} \le$ 2.8V
		—	150	**220**		I_{OUT} = 300 mA, $V_{OUT} \le$ 2.8V
Ground Pin Current (Note 3)	I_{GND}	—	90	**150**	µA	I_{OUT} = 0 mA to 300 mA
Ground Current in Shutdown	I_{SHDN}	—	0.5	**2**	µA	V_{EN} = 0V
Ripple Rejection	PSRR	—	80	—	dB	f = 1 kHz; C_{OUT} = 2.2 µF; C_{BYP} = 0.1 µF
		—	65	—		f = 20 kHz; C_{OUT} = 2.2 µF; C_{BYP} = 0.1 µF
Current Limit	I_{LIM}	**350**	600	**900**	mA	V_{OUT} = 0V
Output Voltage Noise	e_N	—	20	—	μV_{RMS}	C_{OUT} = 2.2 µF; C_{BYP} = 0.1 µF; 10 Hz to 100 kHz
Turn-On Time	t_{ON}	—	30	**150**	µs	C_{OUT} = 2.2 µF; C_{BYP}= 0.1 µF; I_{OUT} = 300 mA

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ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_{IN} = V_{OUT} + 1.0V$; $C_{OUT} = 2.2\ \mu F$; $I_{OUT} = 100\ \mu A$; $T_J = 25°C$, **bold** values indicate –40°C to +125°C, unless noted. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Input Voltage	V_{IL}	—	—	**0.2**	V	Logic Low
	V_{IH}	**1.2**	—	—	V	Logic High
Enable Input Current	I_{IL}	—	0.01	**1**	µA	$V_{IL} \le 0.2V$
	I_{IH}	—	0.01	**1**		$V_{IH} \ge 1.2V$

Note 1: Specification for packaged product only.

2: Regulation is measured at constant junction temperature using low duty cycle pulse testing, changes in output voltage due to heating effects are covered by the thermal regulation specification.

3: Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–40	—	+125	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 3 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
6-Lead 2 mm × 2 mm UDFN	θ_{JA}	—	93	—	°C/W	—
5-Lead Thin SOT-23	θ_{JA}	—	235	—	°C/W	—

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

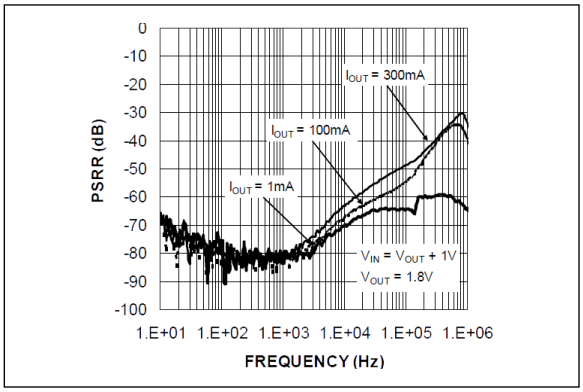


FIGURE 2-1: *Power Supply Rejection Ratio (C_{BYP} = 1 µF).*

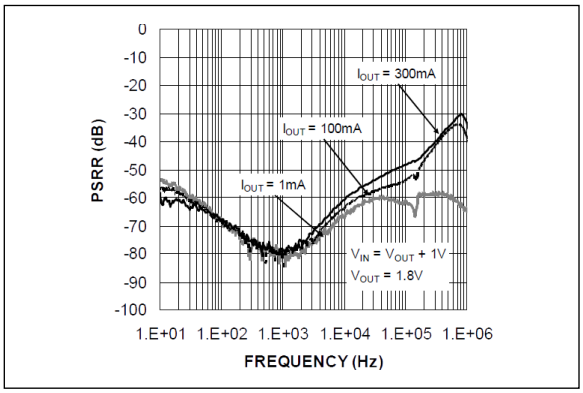


FIGURE 2-2: *Power Supply Rejection Ratio (C_{BYP} = 0.1 µF).*

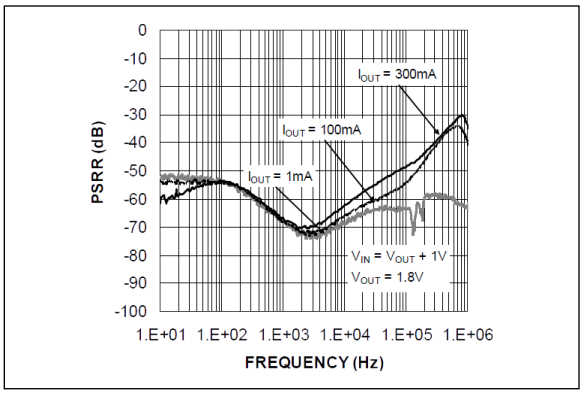


FIGURE 2-3: *Power Supply Rejection Ratio (C_{BYP} = 0.01 µF).*

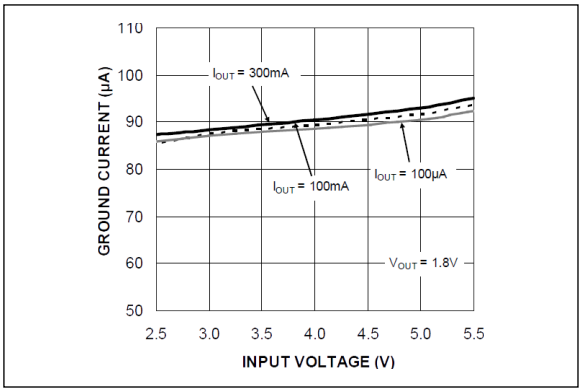


FIGURE 2-4: *Ground Current vs. Input Voltage.*

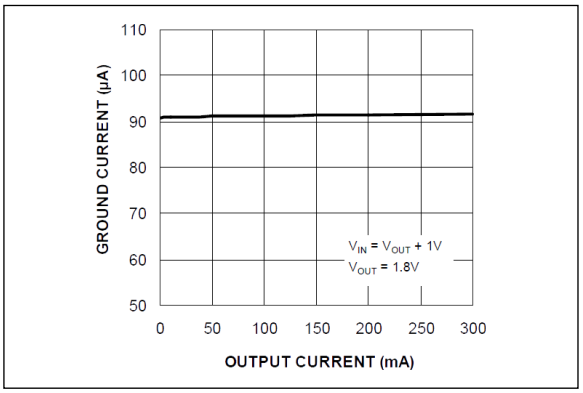


FIGURE 2-5: *Ground Current vs. Output Current.*

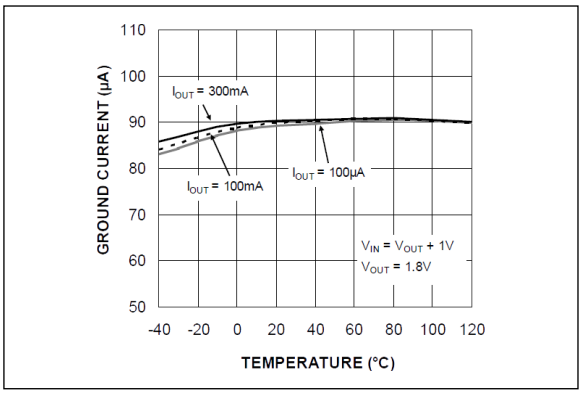


FIGURE 2-6: *Ground Current vs. Temperature.*

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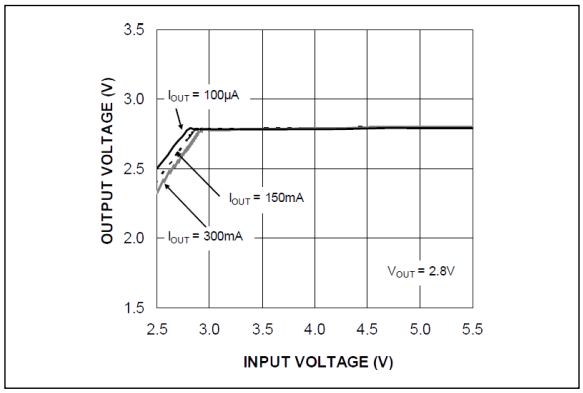


FIGURE 2-7: *Output Voltage vs. Input Voltage.*

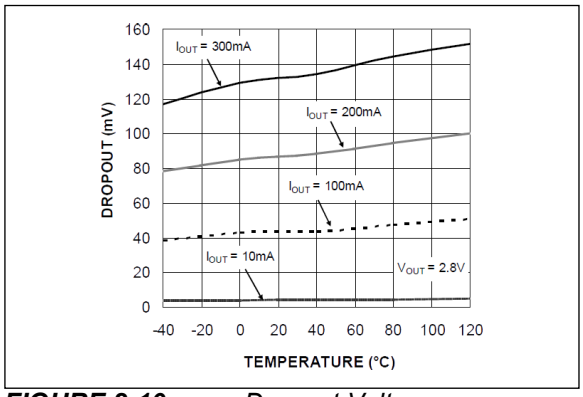


FIGURE 2-10: *Dropout Voltage vs. Temperature.*

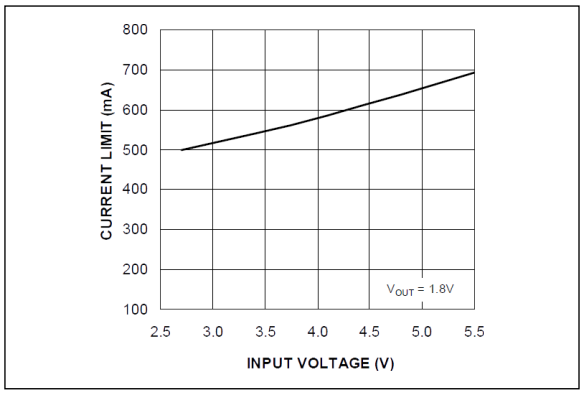


FIGURE 2-8: *Current Limit vs. Input Voltage.*

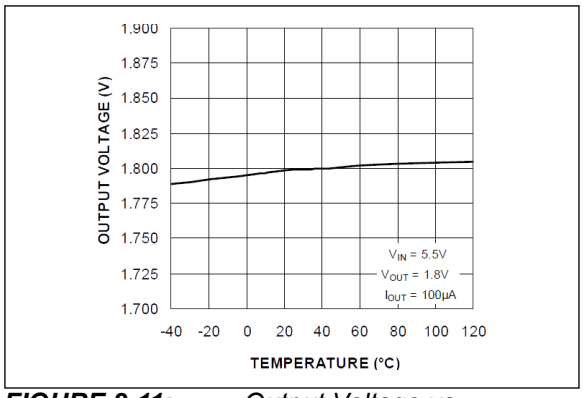


FIGURE 2-11: *Output Voltage vs. Temperature.*

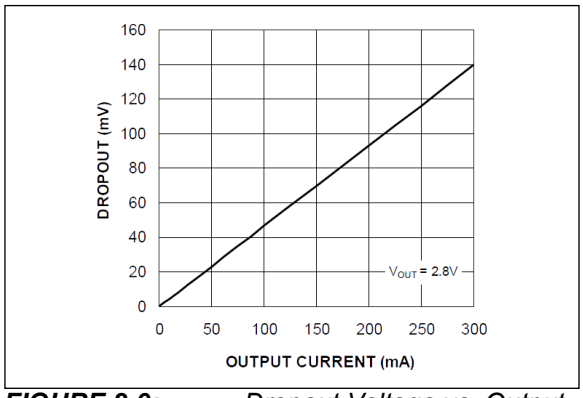


FIGURE 2-9: *Dropout Voltage vs. Output Current.*

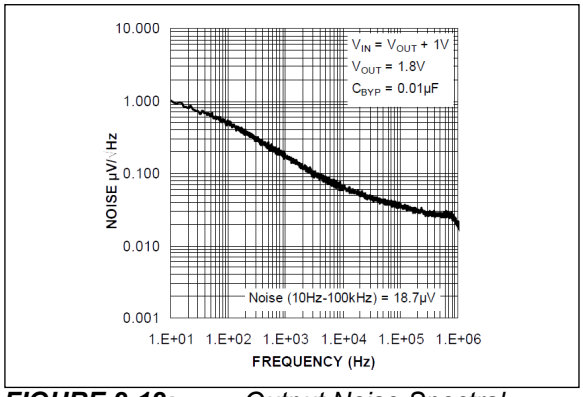


FIGURE 2-12: *Output Noise Spectral Density.*

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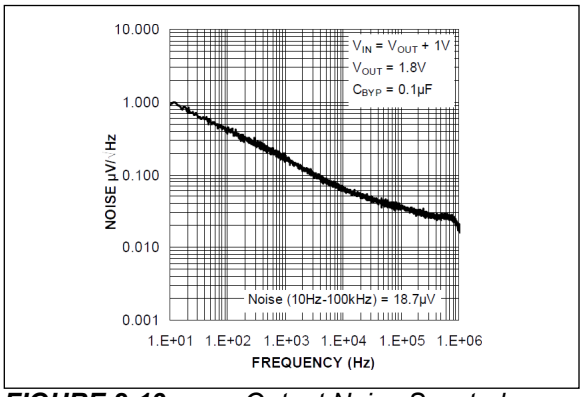


FIGURE 2-13: *Output Noise Spectral Density.*

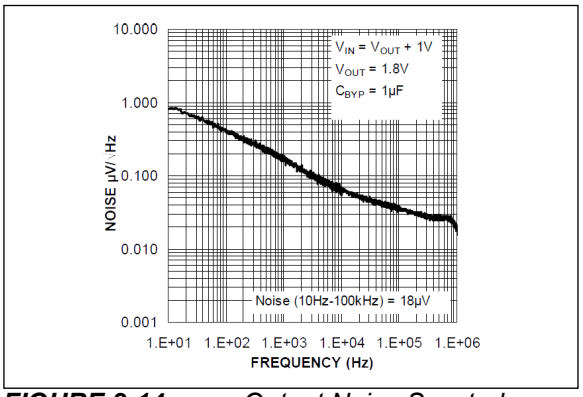


FIGURE 2-14: *Output Noise Spectral Density.*

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3.0 FUNCTIONAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

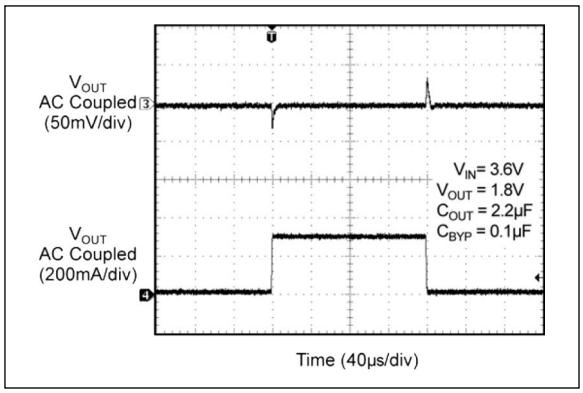


FIGURE 3-1: *Load Transient (10 mA to 300 mA).*

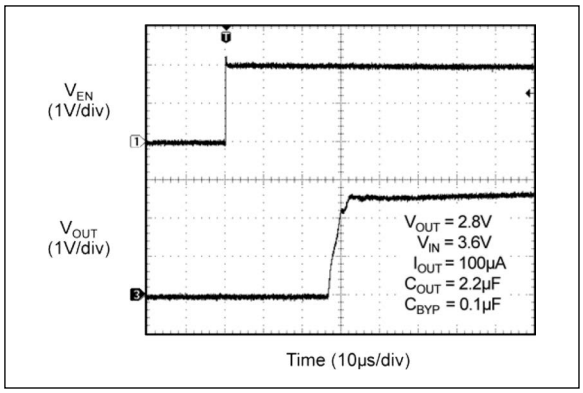


FIGURE 3-3: *Startup.*

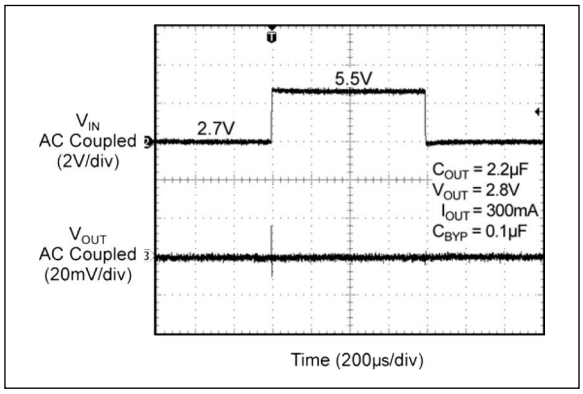


FIGURE 3-2: *Line Transient (2.7V to 5.5V).*

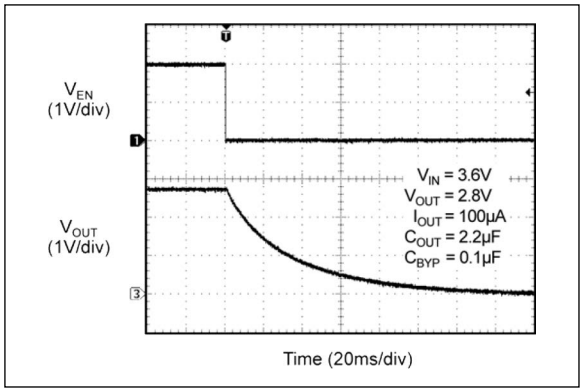


FIGURE 3-4: *Shutdown.*

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4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Pin Number UDFN (Adj.)	Pin Number UDFN (Fixed)	Pin Number TSOT 23-5 (Fixed)	Pin Name	Description
1	1	3	EN	Enable Input: Active High. High = on, low = off. Do not leave floating.
2	2	2	GND	Ground.
3	3	1	VIN	Supply Input.
4	4	5	VOUT	Output Voltage.
5	—	—	ADJ	Adjust Input: Connect to external resistor voltage divider network.
—	5	—	NC	No connection for fixed voltage parts.
6	6	4	BYP	Reference Bypass: Connect external 0.1 µF capacitor to GND for reduced output noise. May be left open.
EPAD	EPAD	—	EPAD	Exposed Heatsink Pad: Connect to ground plane for performance enhancement.

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5.0 APPLICATION INFORMATION

5.1 Enable/Shutdown

The MIC5323 comes with an active high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a “zero” off mode current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. The active high enable pin uses CMOS technology, and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

5.2 Input Capacitor

The MIC5323 is a high performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 2.2µF capacitor is required from the input-to-ground to provide stability. Low ESR ceramic capacitors provide optimal performance using a minimum amount of space. Additional high frequency capacitors, such as small valued NPO dielectric type capacitors, help filter out high-frequency noise, and are a good practice in any RF based circuit.

5.3 Output Capacitor

The MIC5323 requires an output capacitor of 2.2 µF or greater to maintain stability. The design is optimized for use with low ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 2.2 µF ceramic output capacitor, and it does not improve significantly with larger capacitance.

X7R/X5R dielectric type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors change capacitance by 15% over their operating temperature range, making them the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

5.4 Bypass Capacitor

A capacitor can be placed from the noise bypass pin to ground to reduce output voltage noise. The capacitor bypasses the internal reference. A 0.1 µF capacitor is recommended for applications that require low noise outputs. The bypass capacitor can be increased, further reducing noise and improving PSRR. Turn-on time increases slightly with respect to bypass capacitance.

A unique, quick-start circuit allows the MIC5323 to drive a large capacitor on the bypass pin without significantly slowing turn on time. Refer to the Typical Characteristics section for performance with different bypass capacitors.

5.5 No Load Stability

Unlike many other voltage regulators, the MIC5323 will remain stable and in regulation with no load. This is especially important in CMOS RAM keep alive applications.

5.6 Adjustable Regulator Application

Adjustable regulators use the ratio of two resistors to multiply the reference voltage to produce the desired output voltage. The MIC5323 can be adjusted from 1.25V to 5.5V by using two external resistors (Figure 5-1). The resistors set the output voltage based on the following equation:

EQUATION 5-1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

$$V_{REF} = 1.25V$$

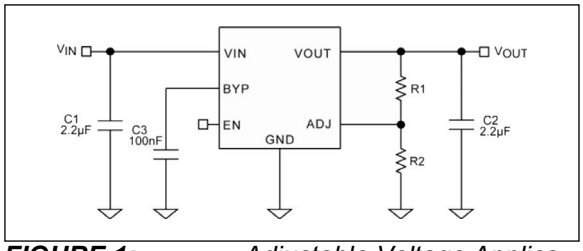


FIGURE 1: *Adjustable Voltage Application.*

5.7 Thermal Considerations

The MIC5323 is designed to provide 300 mA of continuous current in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. Given that the input voltage is 3.3V, the output voltage is 2.8V and the output current = 300 mA.

The actual power dissipation of the regulator circuit can be determined using the equation:

EQUATION 5-2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + (V_{IN} \times I_{GND})$$

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Because this device is CMOS and the ground current is typically <100 µA over the load range, the power dissipation contributed by the ground current is < 1% and can be ignored for this calculation.

EQUATION 5-3:

$$P_D = (3.3V - 2.8V) \times 300mA$$
$$P_D = 0.15W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 5-4:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where $T_{J(MAX)}$ is the maximum junction temperature, 125°C, and θ_{JA} represents the junction-to-ambient thermal resistance, 93°C/W.

Substituting PD for $P_{D(MAX)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit consuming P_D watts.

The maximum power dissipation must not be exceeded for proper operation. For example, when operating the MIC5323-2.8YMT at an input voltage of 3.3V and 300 mA load with a minimum footprint layout, the maximum ambient can be solved for as follows:

EQUATION 5-5:

$$0.15\dot{W} = \frac{125°C - T_A}{93°C/W}$$
$$T_A = 111°C$$

Therefore, a 2.8V application at 300 mA of output current can accept an ambient operating temperature of 111°C in a 6-lead 2 mm × 2 mm UDFN package.

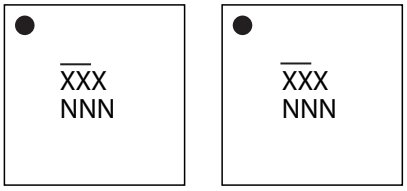
For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the “Regulator Thermals” section of Microchip’s Designing with Low-Dropout Voltage Regulators handbook.

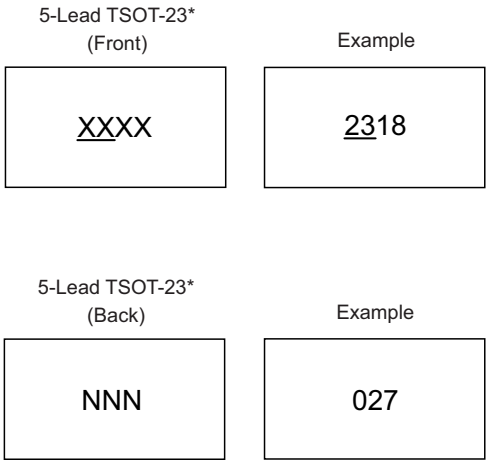
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6.0 PACKAGING INFORMATION

6.1 Package Marking Information





PACKAGE MARKING DRAWING SYMBOLS LEGEND

Symbol	Definition
XX . . . X	Product code or customer-specific information. (Note 1, Note 2)
YYWW	Date code, where YY is the last 2 digits of calendar year and WW is the work week (i.e., week of January 1 is week 01). (Note 3)
M	Month of assembly (if applicable). January is represented by “A” and each month thereafter follows the order of the alphabet through “L” for December.
NNN	Alphanumeric traceability code. (Note 3, Note 4)
(e3)	Pb-free JEDEC designator for Matte Tin (Sn).
*	Indicates this package is Pb-free. The Pb-free JEDEC designator (the symbol in the row above this one) can be found on the outer packaging for this package.
●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note 1: If the full Microchip part number cannot fit on one line, it will be carried over to the next line, limiting the number of available characters for customer-specific information. The package may or may not include the corporate logo.

2: Any underbar (_) and/or overbar (¯) symbols shown in a package marking drawing may not be to scale.

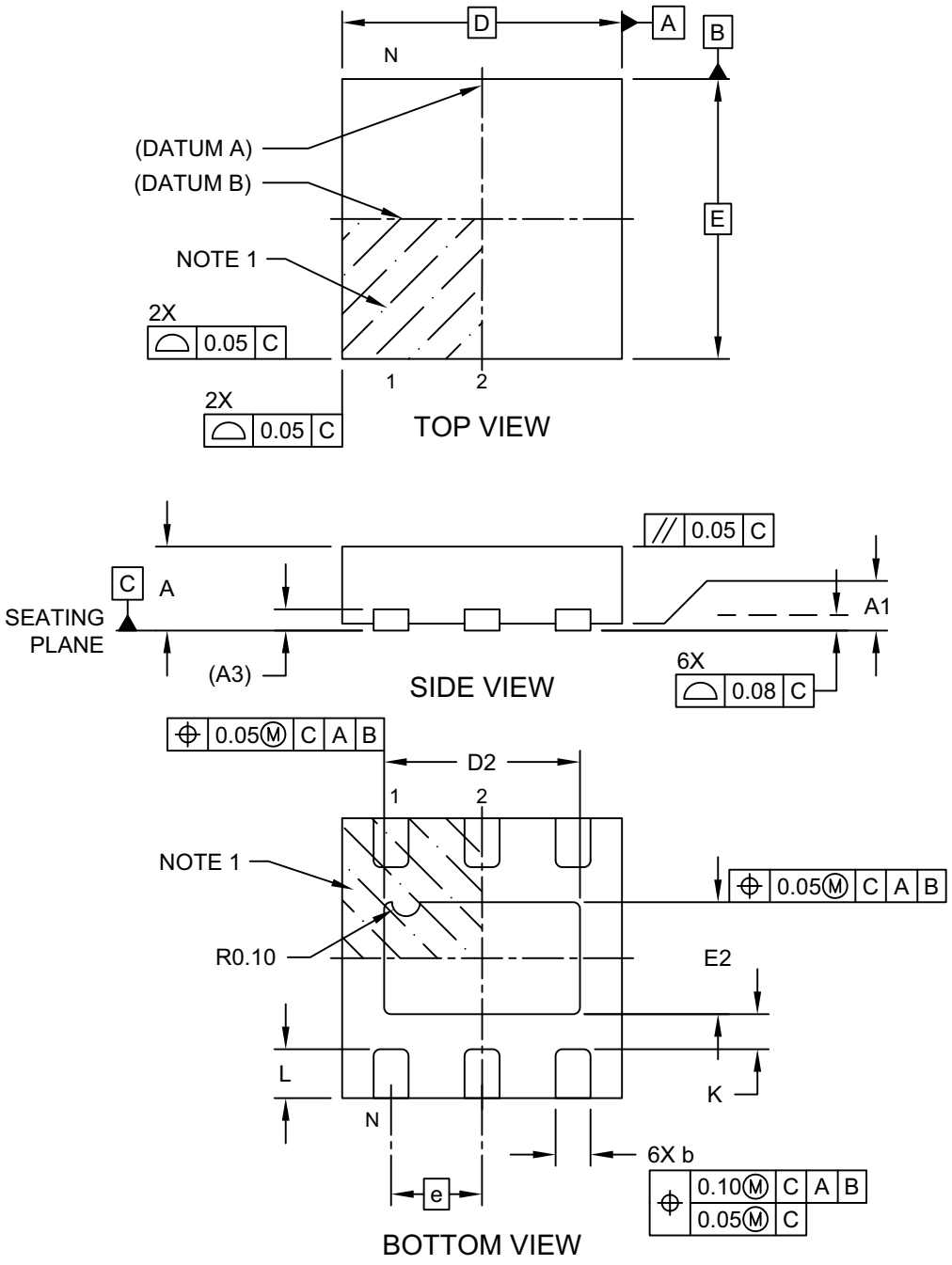
3: If the full date code (YYWW) and the alphanumeric traceability code (NNN)—usually marked together on the last or only line of a package marking as the seven-character YYWWNNN—cannot fit on the package together, the codes will be truncated based on the number of available character spaces, as follows: 6 characters = YWWNNN; 5 characters = WWNNN; 4 characters = WNNN; 3 characters = NNN; 2 characters = NN; 1 character = N.

4: Some products might have a “Y” symbol at the end of the last or only line in a package marking, usually at the end of the alphanumeric traceability code (NNN or truncated versions), to indicate the product is Pb-free.

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6-Lead 2 mm x 2 mm UDFN [HSA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



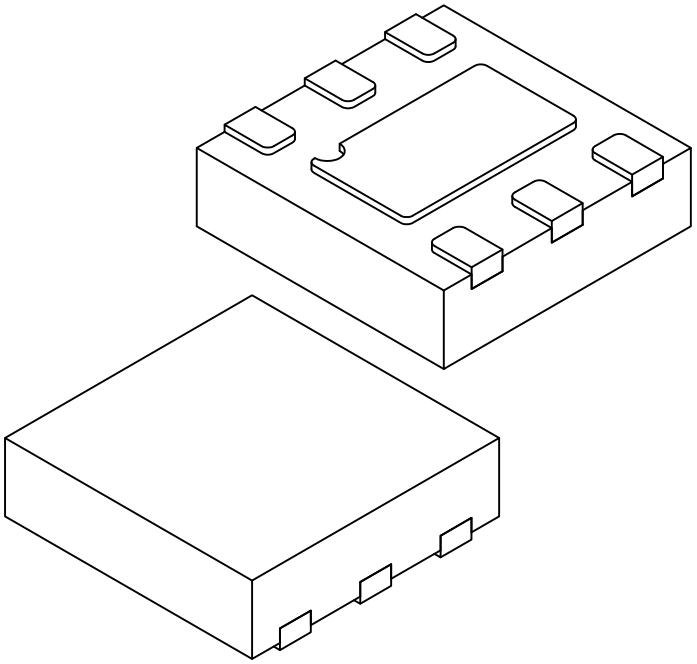
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6-Lead 2 mm x 2 mm UDFN [HSA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.75	0.80	0.85
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

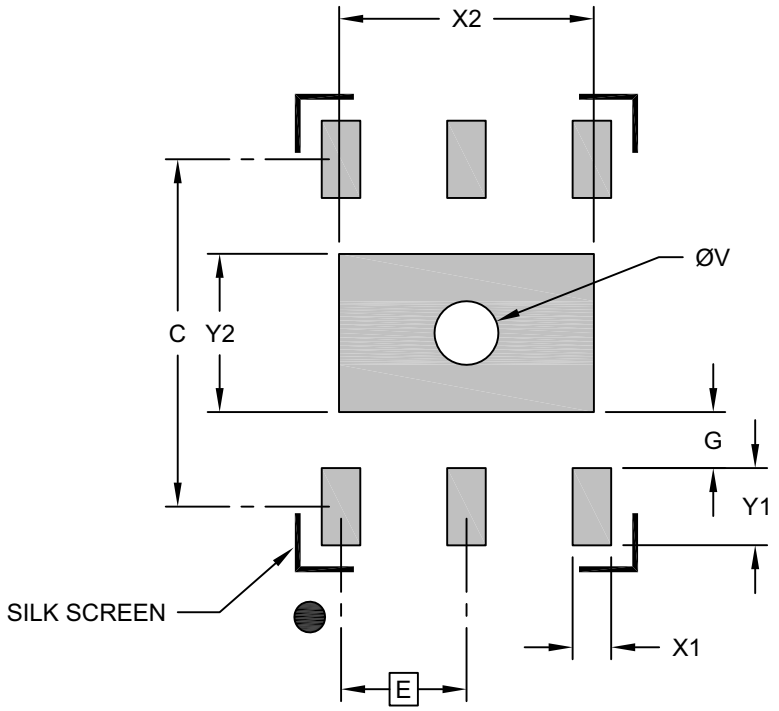
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6-Lead 2 mm x 2 mm UDFN [HSA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Center Pad Width	X2			1.32
Center Pad Length	Y2			0.82
Contact Pad Spacing	C		1.80	
Contact Pad Width (X6)	X1			0.20
Contact Pad Length (X6)	Y1			0.40
Contact Pad to Center Pad (X6)	G	0.29		
Thermal Via Diameter	V		0.33	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

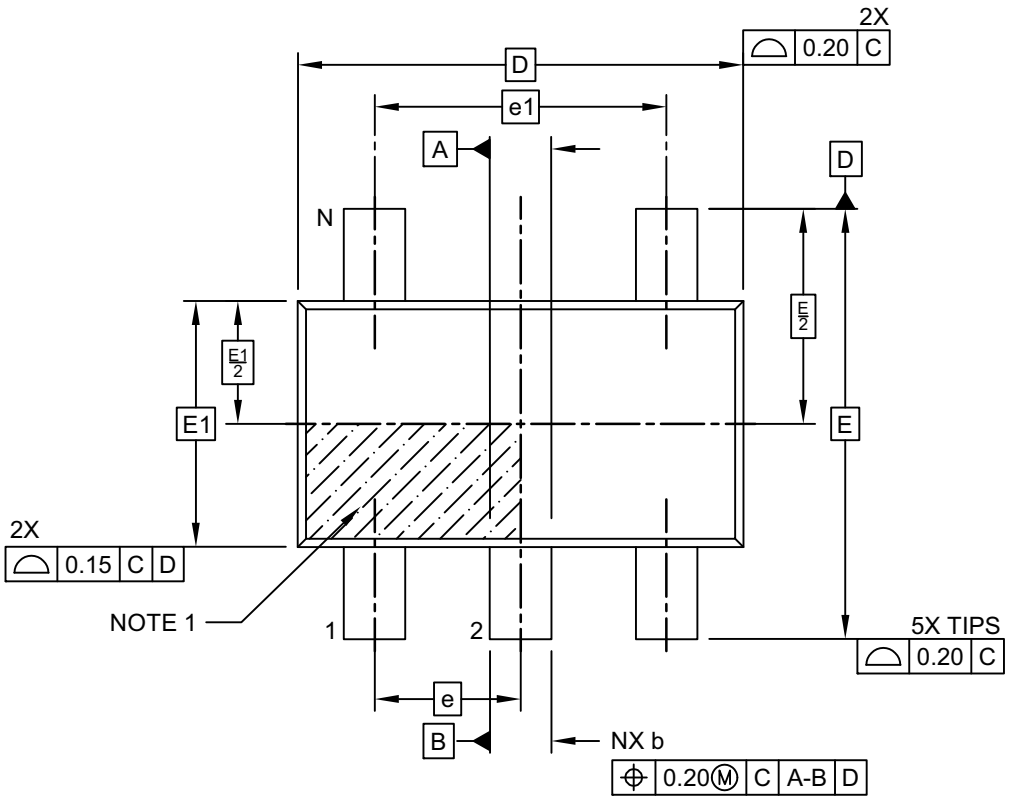
Microchip Technology Drawing C04-3156-HSA Rev A

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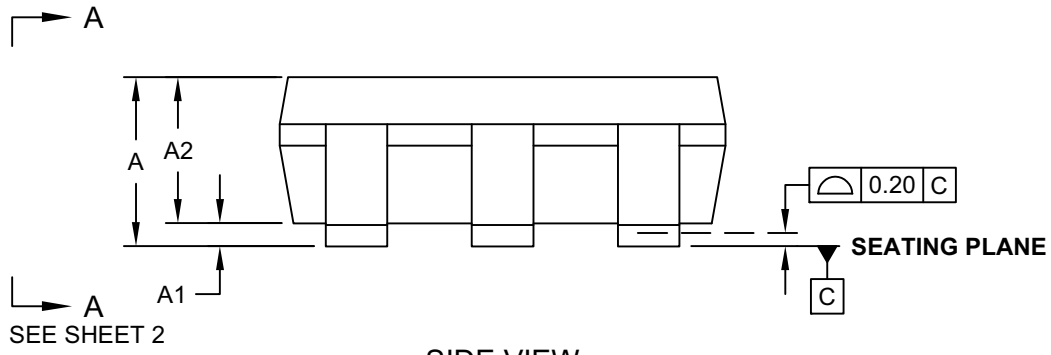
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5-Lead Thin SOT-23 [D5A] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



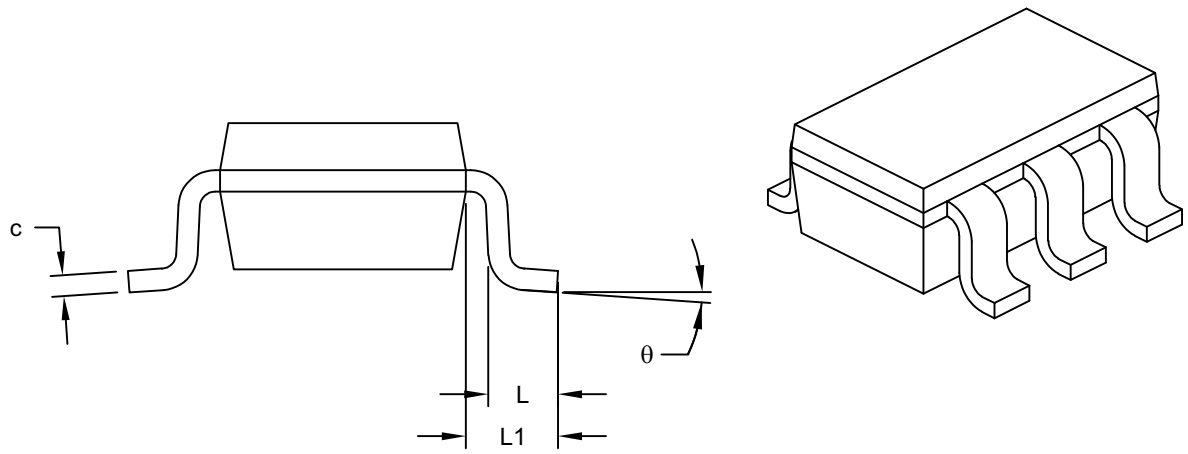
SIDE VIEW

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5-Lead Thin SOT-23 [D5A] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	-	-	1.00
Molded Package Thickness	A2	0.84	0.87	0.90
Standoff	A1	0.00	-	0.10
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.40	0.50
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	4°
Lead Thickness	c		0.127 REF	
Lead Width	b	0.30	-	0.50

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

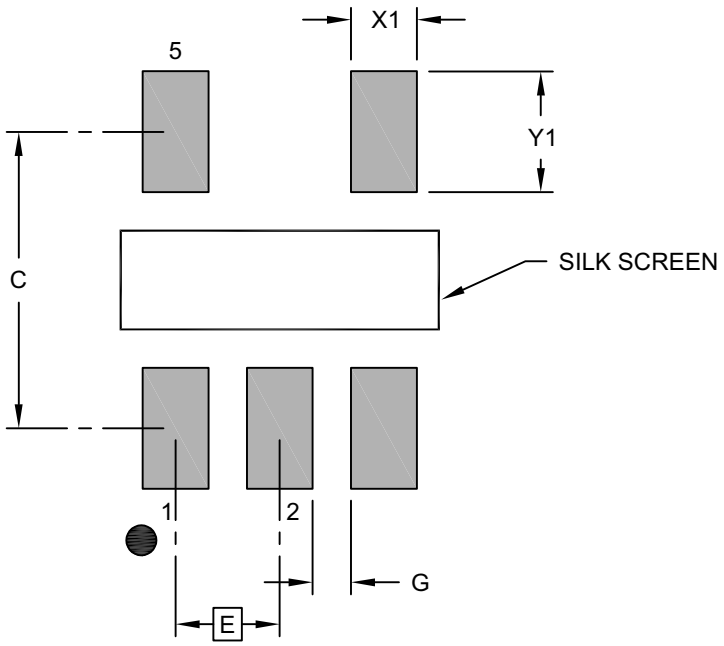
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5-Lead Thin SOT-23 [D5A] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.60	
Contact Pad Width (X5)	X1			0.60
Contact Pad Length (X5)	Y1			1.10
Contact Pad to Center Pad (X2)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3179 Rev A

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APPENDIX A: REVISION HISTORY

Revision A (July 2026)

- Converted Micrel document MIC5323 to Microchip data sheet format as DS20007021A.
- Minor text changes throughout.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	-XX	X	XX	-XX
Device	Output Voltages	Temp. Range	Package	Media Type

Device:	MIC5323	=	High PSRR Low Noise 300 mA µCap Ultra-Low Dropout LDO Regulator
Output Voltages:	<blank>	=	Adjustable
	-1.8	=	1.8V
	-2.8	=	2.8V
	-3.3	=	3.3V
Temperature Range:	Y	=	–40°C to +125°C
Package:	D5	=	5-Lead Thin SOT-23
	MT	=	6-Lead 2 mm x 2 mm UDFN
Media Type:	-TR	=	3,000/Reel (D5 option only)
	-TR	=	5,000/Reel (MT option only)

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) MIC5323-1.8YD5-TR

MIC5323, 1.8V Output Voltage, –40°C to +125°C Temp. Range, 5-Lead Thin SOT-23 Package, 3,000/Reel

b) MIC5323-2.8YD5-TR

MIC5323, 2.8V Output Voltage, –40°C to +125°C Temp. Range, 5-Lead Thin SOT-23 Package, 3,000/Reel

c) MIC5323-3.3YD5-TR

MIC5323, 3.3V Output Voltage, –40°C to +125°C Temp. Range, 5-Lead Thin SOT-23 Package, 3,000/Reel

d) MIC5323-1.8YMT-TR

MIC5323, 1.8V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead 2 mm x 2 mm UDFN Package, 5,000/Reel

e) MIC5323-2.8YMT-TR

MIC5323, 2.8V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead 2 mm x 2 mm UDFN Package, 5,000/Reel

f) MIC5323-3.3YMT-TR

MIC5323, 3.3V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead 2 mm x 2 mm UDFN Package, 5,000/Reel

g) MIC5323YMT-TR

MIC5323, Adjustable Output Voltage, –40°C to +125°C Temp. Range, 6-Lead 2 mm x 2 mm UDFN Package, 5,000/Reel

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