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Verdin iMX8M Plus

Datasheet



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Revision History

Date	Doc. Rev.	Module Version	Changes
19-Oct-2020	Rev. 0.90	V1.0	Initial Release
23-Oct-2020	Rev. 0.91	V1.0	Correction of CTRL_SLEEP_MOCI# signal type from open drain to CMOS Section 1.6.4: Update document links for Wi-Fi module Minor changes
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1. Introduction

1.1 Verdin SoM Family

The Verdin System on Module (SoM) family eliminates much of the complexity associated with modern-day electronic design. Complicated circuitry such as high-speed impedance-controlled layouts with high component density utilizing blind and buried via technology is encapsulated on the SoM. This allows the customer to create a carrier board that focuses solely on application-specific electronics, making the project substantially less complex. The Verdin module takes this one step further and implements an interface pinout that allows direct connection of real-world I/O ports without the need to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high-speed serial technologies that require impedance-controlled differential pairs. Direct Breakout™ allows them to easily route such interfaces to common connectors in a simple, robust fashion.

The Verdin SoM features a wide input voltage range that allows it to be powered from a broad range of power sources (e.g., directly from a USB power supply or a single lithium cell). Due to increasing transistor density and the need for more power-efficient devices, the I/O voltage level is trending to decrease from 3.3V to 1.8V. For this reason, the Verdin family of SoMs supports a 1.8V I/O voltage level only. Both the wide input voltage range and the 1.8V I/O voltage make the power supply designs for a Verdin carrier board simple, easy, and cost-efficient. These features altogether make the Verdin family of SoMs perfectly suited for battery-powered applications as well.

1.2 NXP i.MX 8M Plus SoC

The Verdin iMX8M Plus SoM is based on the NXP® i.MX 8M Plus family of embedded System on Chips (SoCs). The i.MX 8M Plus family consists of the i.MX 8M Plus Quad, i.MX 8M Plus Quad Lite, and i.MX 8M Plus Dual. The top-tier i.MX 8M Plus Quad features four Cortex-A53 cores as the main processor cluster. The cores provide complete 64-bit Armv8-A support while maintaining seamless backward compatibility with 32-bit Armv7-A software. The main cores run at up to 1.8 GHz for commercial graded products and 1.6 GHz for industrial temperature range products.

In addition to the main CPU complex, the i.MX 8M Plus features a Cortex-M7 processor, which peaks up to 800 MHz. This processor is independent of the main complex. However, it has shared access to the peripheral interface. This heterogeneous multicore system allows for running additional real-time operating systems on the M7 cores for time- and security-critical tasks.

Depending on the version, the SoC features a Neural Processing Unit (NPU) with up to 2.3 TOPS that can significantly accelerate machine learning tasks. Some SoC versions also feature a Video Processing Unit (VPU) for accelerating video decoding and encoding. The optional Image Signal Processing (ISP) core accelerates the camera interface by providing a complete video and still picture input block. It features image processing and color space conversion.

The i.MX 8M Plus SoC features inline ECC (error-correcting code) for the LPDDR4 DRAM for high system reliability and safety.

The i.MX 8M Plus Quad features the GC7000 UltraLite 3D Graphics Processing Unit (GPU) from Vivante®. The GPU provides eight Vega shader core which peaks up to 16 GFLOPS and supports OpenGL® ES 3.0, OpenCL® 1.2, and Vulkan®. In addition to the GPU, the SoC features the GC520L Composition Processing Core (CPC).

The i.MX 8M Plus SoC incorporates DVFS (Dynamic Voltage and Frequency Switching) and thermal throttling, enabling the system to continuously adjust both the operating frequency and the voltage in response to changes in workload and temperature, thus achieving the best performance with the lowest power consumption.

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1.3 Verdin iMX8M Plus SoM

The Verdin iMX8M Plus targets a wide range of applications, including Industrial Automation, Medical, Transportation, Smart Cities, Test and Measurement, and many more.

The SoM is available with an optional Dual-Band (2.4/5 GHz) Wi-Fi ac/a/b/g/n and Bluetooth 5/BLE interface. The Wi-Fi module features MHF4 compatible connectors for external antennas. The module is pre-certified for FCC (US), CE (Europa), IC (Canada), TELEC (Japan), and WPC (India).

The selected i.MX 8M Plus SoC for the Verdin iMX8M Plus SoM features a Neural Processing Unit (NPU) for speech recognition with keyword detection and noise reduction as well as image recognition. The SoCs also features a Video Processing Unit (VPU) to offload the main processor from video encoding and decoding tasks. The integrated Image Signal Processor (ISP) can handle up to two camera input streams with an aggregated throughput of up to 375 megapixels per second.

The inline ECC for the external LPDDDR4 DRAM adds additional safety for high industrial system reliability.

The module offers a wide range of interfaces ranging from simple GPIOs, industry-standard I2C, SPI, CAN-FD, and UART buses to PCI Express interfaces. The Verdin iMX8M Plus module features a Gigabit Ethernet PHY with Time-Sensitive Networking (TSN) and IEEE1588 support on the module. The SoC features a second Ethernet MAC with an RGMII interface for adding a Gigabit Ethernet PHY on the carrier board for dual Ethernet applications.

1.4 Main Features

1.4.1 CPU

	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
i.MX 8MP Family SoC	MIMX8ML4CVNKZAx	MIMX8ML8DVNLZAx	MIMX8ML8CVNKZAx
Arm Cortex-A53 CPU Cores	4	4	4
Arm Cortex-M7 CPU Cores	1	1	1
L1 Instruction Cache (each core)	32 KB (A53) 32 KB (M7)	32 KB (A53) 32 KB (M7)	32 KB (A53) 32 KB (M7)
L1 Data Cache (each core)	32 KB (A53) 32 KB (M7)	32 KB (A53) 32 KB (M7)	32 KB (A53) 32 KB (M7)
L2 Cache (shared by all A35 cores)	512 KB (A53)	512 KB (A53)	512 KB (A53)
Tightly Coupled Memory	256 KB (M7)	256 KB (M7)	256 KB (M7)
Maximum CPU frequency	1.6 GHz (A53) 800 MHz (M7)	1.8 GHz (A53) 800 MHz (M7)	1.6 GHz (A53) 800 MHz (M7)
NEON MPE	Yes	Yes	Yes
NPU	-	Yes	Yes
NPU Performance	-	2.3 TOP/s	2.3 TOP/s
ISP	-	Yes	Yes
ISP Performance	-	375 Mpixel/s HDR	375 Mpixel/s HDR
VPU	-	Yes	Yes
Resource Domain Controller	Yes	Yes	Yes
Arm TrustZone	Yes	Yes	Yes
High Assurance Boot	Yes	Yes	Yes

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	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
Cryptographic Acceleration and Assurance Module	Yes	Yes	Yes
Secure Real-Time Clock	Yes	Yes	Yes
Secure JTAG Controller	Yes	Yes	Yes
Secure Non-Volatile Storage*	Yes	Yes	Yes

* Secure Non-Volatile Storage (SNVS) runs from the main VCC, not the VCC_BACKUP. Therefore, it can only be used if VCC is permanently applied to the module.

1.4.2 Memory

	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
LPDDR4 RAM Size	1 GB	2 GB	4 GB
LPDDR4 RAM Speed	4000 MT/s (2 GHz)	4000 MT/s (2 GHz)	4000 MT/s (2 GHz)
LPDDR4 RAM Memory Width	1x32 bit	1x32 bit	1x32 bit
LPDDR4 Inline ECC	Yes	Yes	Yes
eMMC NAND Flash (8-bit) V5.0 *	8 GB	16 GB	16 GB
I^2C EEPROM	2 Kb	2 Kb	2 Kb

*eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear leveling in the eMMC controller helps to ensure that cells are getting worn out evenly. More information can be found here https://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.4.3 Interfaces

	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
Wi-Fi IEEE 802.11 ac/a/b/g/n Dual-Band (2.4/5 GHz)	-	-	1
Bluetooth 5/BLE	-	-	1
MIPI DSI	1 (4 Data Lanes)	1 (4 Data Lanes)	1 (4 Data Lanes)
HDMI 2.0a (2160p30)	1	1	1
LVDS (1x dual-channel or 2x single channel)	1	1	1
USB 2.0 OTG	1	1	1
USB 3.1 Gen 1 OTG	1*	1*	1*
USB 2.0 host	1	1	1
USB 3.1 Gen 1 host	1	1	1
Gigabit Ethernet (MDI)	1	1	1
RGMII	1	1	1
PCIe (Gen 3)	1	1	1
MIPI CSI-2	1+1* (4 Data Lanes)	1+1* (4 Data Lanes)	1+1* (4 Data Lanes)
SPI	1+2*	1+2*	1+2*
QSPI	1	1	1
UART	4	4	4

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	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
I^2C	4+1*	4+1*	4+1*
I^2S	2+4*	2+4*	2+4*
PWM	3+1*	3+1*	3+1*
SD/SDIO/MMC	1	1	1
GPIO	10+85*	10+85*	10+85*
CAN-FD	2	-	2
CAN	-	2	-
ADC	4	4	4
JTAG	1	1	1
S/PDIF (RX and TX)	1*	1*	1*
TPM 2.0 Module	-	-	-

*These interfaces are available on pins that are not defined as *"Always Compatible"* or *"Reserved"* interfaces in the Verdin architecture. The pins are either located in the *"Module-specific"* area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. See section 1.5 for more information.

1.4.4 Graphics Processing Unit

	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
Vivante GC7000UL GPU Units	1	1	1
Vega Shader cores	8	8	8
OpenGL® ES 3.0, 2.0, 1.1	Yes	Yes	Yes
OpenGL® 3.0, 2.1	Yes	Yes	Yes
OpenVG® 1.1	Yes	Yes	Yes
OpenCL® 1.2	Yes	Yes	Yes
Vulkan	Yes	Yes	Yes
GC520L CPC Units	1	1	1

1.4.5 HD Video Decode (VPU)

	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
H.265 HEVC Main, Main 10 (up to level 5.1) 1080p60	-	Yes	Yes
VP9 Profile 0, 2 1080p60	-	Yes	Yes
VP8 1080p60	-	Yes	Yes
H.264 AVC Baseline, Main and High profile 1080p60	-	Yes	Yes
VP8 1080p60	-	Yes	Yes

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1.4.6 HD Video Encode (VPU)

	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
H.265 HEVC 1080p60	-	Yes	Yes
H.264 AVC 1080p60	-	Yes	Yes

1.4.7 Image Signal Processor

	Verdin iMX8M Plus QuadLite 1GB IT	Verdin iMX8M Plus Quad 2GB	Verdin iMX8M Plus Quad 4GB WB IT
YCbCr420 and YCbCr422 input	-	Yes	Yes
RAW8, RAW10, RAW12, and RAW14 input	-	Yes	Yes
High Dynamic Range (HDR)	-	Yes	Yes
Dewrap engine	-	Yes	Yes

1.4.8 Supported Operating Systems

- ✓ Toradex Reference Images (Yocto Project BSP layers)
- ✓ TorizonCore
- ✓ Android
- ✓ For other operating systems, please contact Toradex

1.5 Interface Overview

Features of the Verdin module are split into three distinct categories: *"Always Compatible"*, *"Reserved"*, and *"Module-specific"*. The *"Always Compatible"* and *"Reserved"* pins are also referred to as the "Verdin Standard" pins.

Additionally to this definition, the i.MX 8M Plus SoC allows for alternate functions. As an example, many pins can, apart from their primary function, also work as GPIOs.

"Always Compatible" interfaces are features that shall be present on each SoM in the Verdin Family. Customers can count on upgradeability and maximum scalability regarding these interfaces.

"Reserved" interfaces are features that are defined and reserved but possibly missing on some SoM models due to lack of availability. It could be that a particular SoC does not provide a specific interface or that there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means any Verdin SoM can be reliably inserted into any Verdin carrier board without causing damage due to incompatible *"Reserved"* pins.

A *"Module-specific"* feature is a feature that is not guaranteed to be functionally or electrically compatible between modules. Suppose a carrier board design uses such features. In that case, it is possible that other modules in the Verdin module family do not provide these features and instead provide other features on the associated pins. In this case, Verdin modules that are suitable for use in the carrier board design may be restricted. An incompatible SoM/carrier board combination may disable all functionality or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

The alternate functions group means that an interface is provided as an additional function on an *"Always Compatible"*, *"Reserved"*, or *"Module-specific"* pin. These functions can only be used if the primary function of the pin is not used.

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The table in Figure 1 shows the interfaces that are supported on the Verdin iMX8M Plus module along with the group in which that feature is provided: *"Always Compatible"*, *"Reserved"*, *"Module-specific"*, or *alternate function*. The PWM interface is an example of an interface feature that makes use of standard and alternate function pins; one PWM interface is available as *"Always Compatible"*, two as *"Reserved"*, and a fourth one is available as an alternate function of the USB_2_OC#, I2S_1_D_OUT, CSI_1_MCLK, and I2C_4_CSI_SCL signals. Check section 4.4 for a list of all alternate functions of the SODIMM pins. The Toradex Pinout Designer is a powerful tool for configuring the Verdin iMX8M Plus Module pin multiplexing. The tool allows us to compare the interfaces of different Verdin modules. More information on this tool can be found here: https://developer.toradex.com/knowledge-base/pinout-designer

Feature	Total	*"Always Compatible"*	*"Reserved"*	*"Module-specific"*	Alternate Function
MIPI DSI	1		1		
HDMI 2.0a	1		1		
LVDS (1x dual-channel or 2x single channel)	1			1	
USB 2.0 OTG	1	1			
USB 3.1 Gen 1 OTG (Requires USB 2.0 OTG)	1			1	
USB 2.0 host	1	1			
USB 3.1 Gen 1 host (Requires USB 2.0 Host)	1		1		
Gigabit Ethernet (MDI)	1	1			
RGMII	1		1		
PCIe (Gen 3)	1		1		
MIPI CSI-2	2		1	1	
SPI	3	1		1	1
QSPI	1		1		
UART	4	3	1		
I^2C	5	1	3		1
I^2S	6		2		4
PWM	4	1	2		1
SD/SDIO/MMC	1	1			
GPIO	95	10		4	81
CAN/CAN-FD	2		2		
ADC	4		4		
JTAG	1		1		
S/PDIF (RX and TX)	1				1

Figure 1: Verdin iMX8M Plus Module Interfaces

1.6 Reference Documents

1.6.1 NXP i.MX 8M Plus

You will find additional details about the i.MX 8M Plus SoC in the Datasheet and Reference Manual provided by NXP.
https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS

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1.6.2 Ethernet Transceiver

Verdin iMX8M Plus utilizes a Microchip KSZ9131RNX Gigabit Ethernet Transceiver (PHY).
https://www.microchip.com/wwwproducts/en/KSZ9131

1.6.3 ADC

Verdin iMX8M Plus utilizes a Texas Instrument TLA2024 four-channel ADC with 12-bit and I²C.
https://www.ti.com/lit/gpn/tla2024

1.6.4 Wi-Fi and Bluetooth Module

Some Verdin iMX8M Plus models utilize an AzureWave AW-CM276NF wireless module. The AW-CM276NF datasheet is available from AzureWave:
https://www.azurewave.com/wireless-modules-nxp.html
Information on pre-certified antennas and cables can be found here:
https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products
Certification documents are available on the Toradex website:
https://developer.toradex.com/knowledge-base/certification-documents-for-azurewave-aw-cm276nf-wi-fi-bluetooth-module

1.6.5 TPM 2.0 Module

The Verdin iMX8M Plus can be assembled with a Trusted Platform Module (TPM 2.0), the ATTPM20P from Microchip. The complete documentation is only available under a Microchip NDA.
https://www.microchip.com/wwwproducts/en/ATTPM20P

1.6.6 EEPROM

The Verdin iMX8M Plus has an on-module I²C EEPROM, the M24C02 from ST.
https://www.st.com/en/memories/m24c02-r.html

1.6.7 RTC

The Verdin iMX8M Plus has a low-power RX8130CE real-time clock from Epson.
https://www5.epsondevice.com/en/products/rtc/rx8130ce.html

1.6.8 Verdin Carrier Board Design Guide

This document provides additional information about the Verdin form factor. A custom carrier board should follow the Verdin Carrier Board Design Guide to make the board compatible with the Verdin module family. Please study this document in detail before starting your carrier board design.
https://docs.toradex.com/108140-verdin-carrier-board-design-guide.pdf

1.6.9 Verdin Family Specification

This document outlines the specification which defines the Verdin Computer-on-Module family. It describes the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also explains the mechanical form factor, including key dimensions and possible thermal solutions. The document will be available soon on the Toradex website.

1.6.10 Layout Design Guide

This document contains information about high-speed layout design and additional factors that help get the carrier board layout right the first time.
https://docs.toradex.com/102492-layout-design-guide.pdf

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1.6.11 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information regularly. You can find an abundance of additional information there.

Please note that the Developer Center is common to all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Verdin iMX8M Plus.
https://developer.toradex.com/

1.6.12 Verdin Carrier Board Schematics

We provide complete schematics plus an Altium project file that includes library symbols and IPC-7351 compliant footprints for the Verdin Software Development Board and other carrier boards, free of charge. This resource is of great help when designing your own carrier board.
https://developer.toradex.com/carrier-board-design/reference-designs

1.6.13 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin, Apalis, and Colibri Modules. The tool allows comparing the interfaces across different modules.
https://developer.toradex.com/carrier-board-design/pinout-designer-tool

1.7 Naming Conventions

The naming of i.MX 8M Plus based products can be confusing. In this document, a consistent naming convention is used. It is essential to notice the punctuation and spaces in the names. Do not confuse the i.MX 8M Plus with the i.MX 8 or the i.MX 8M. These are three different SoC families with different features.

1.7.1 Naming of NXP System on Chip

i.MX 8 Series	A series of different SoC families which consist of the i.MX 8, i.MX 8M, i.MX 8M Plus, i.MX 8M Mini, i.MX 8M Nano, as well as the i.MX 8X families. This document only contains information on the Verdin module, which uses an i.MX 8M Plus family SoC. For information on other i.MX 8 Series based modules, please visit the Toradex website.
i.MX 8M Plus	The NXP i.MX 8M Plus SoC family, which consists of the i.MX 8M Plus Quad, i.MX 8M Plus Quad Lite, and i.MX 8M Plus Dual. Whenever this document uses the term i.MX 8M Plus, all versions of the i.MX 8M Plus SoC family are meant.
i.MX 8MP	Short name for the i.MX 8M Plus SoC family.
i.MX 8M Plus Quad	The top-tier SoC of the i.MX 8M Plus family. It features a quad-core Cortex-A53 main CPU with VPU, ISP, and an optional NPU
i.MX 8MPQ	Short name for the i.MX 8M Plus Quad.
i.MX 8M Plus Quad Lite	Quad-Core SoC of the i.MX 8M Plus family, which does not include the VPU, NPU, and ISP.
i.MX 8MPQL	Short name for the i.MX 8M Plus Quad Lite.
i.MX 8M Plus Dual	Dual Core Cortex-A53 version of the i.MX 8M Plus family. It contains VPU, NPU, and ISP.
i.MX 8MPD	Short name for the i.MX 8M Plus Dual.

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1.7.2 Naming of Toradex Verdin Modules

Verdin iMX8M Plus	Verdin module based on the i.MX 8M Plus family SoC. Whenever this document uses the term Verdin iMX8M Plus, all versions of the Verdin iMX8MP are meant.
Verdin iMX8MP	Short name for the Verdin iMX8M Plus. Whenever this document uses the term Verdin iMX8MP, all versions of the Verdin iMX8M Plus are meant.
Verdin iMX8M Plus Quad 4GB WB IT	Verdin module based on the i.MX 8M Plus Quad processor with 4GB memory, Wi-Fi and Bluetooth function, and IT temperature range.
Verdin iMX8MP Q 4GB WB IT	Short name for the Verdin iMX8M Plus Quad 2GB WB IT.
Verdin iMX8M Plus Quad 2GB	Verdin module based on the i.MX 8M Plus Quad processor with 2GB memory, no Wi-Fi and Bluetooth function, and commercial temperature range.
Verdin iMX8MP Q 2GB	Short name for the Verdin iMX8M Plus Quad 2GB IT.

1.8 Build to Order Options

The Verdin iMX8M Plus module is available in different variants (see section 1.4). In addition to these stock-keeping units (SKU), it is possible to order customized versions of the module. These versions are built to order (BTO). This means the lead time is longer since they are not kept in stock. Additional setup costs may apply for such versions. Please get in touch with your local Toradex sales team to discuss a BTO version of the Verdin iMX8M Plus module. More information can be found here: https://developer.toradex.com/knowledge-base/customized-colibri.

The following customization options are technically possible for the Verdin iMX8M Plus:

- SoC variants:
  - i.MX 8M Plus Quad with VPU, NPU, and ISP
  - i.MX 8M Plus Quad with VPU and ISP, no NPU
  - i.MX 8M Plus Quad Lite without VPU, NPU, and ISP
  - i.MX 8M Plus Dual with VPU, NPU, and ISP
- RAM capacity
- eMMC capacity
- I²C EEPROM capacity
- Industrial or commercial temperature range. Please note that only the industrial temperature version of the SoC features CAN-FD. The consumer one features regular CAN.
- With or without Wi-Fi and Bluetooth module
- With or without on-module Ethernet PHY
- With or without Trusted Platform Module (TPM 2.0)
- With or without ADC
- Full input voltage range (3.135V to 5.5V) or limited input voltage range (3.3V +/-5%)

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2. Architecture Overview

2.1 Block Diagram

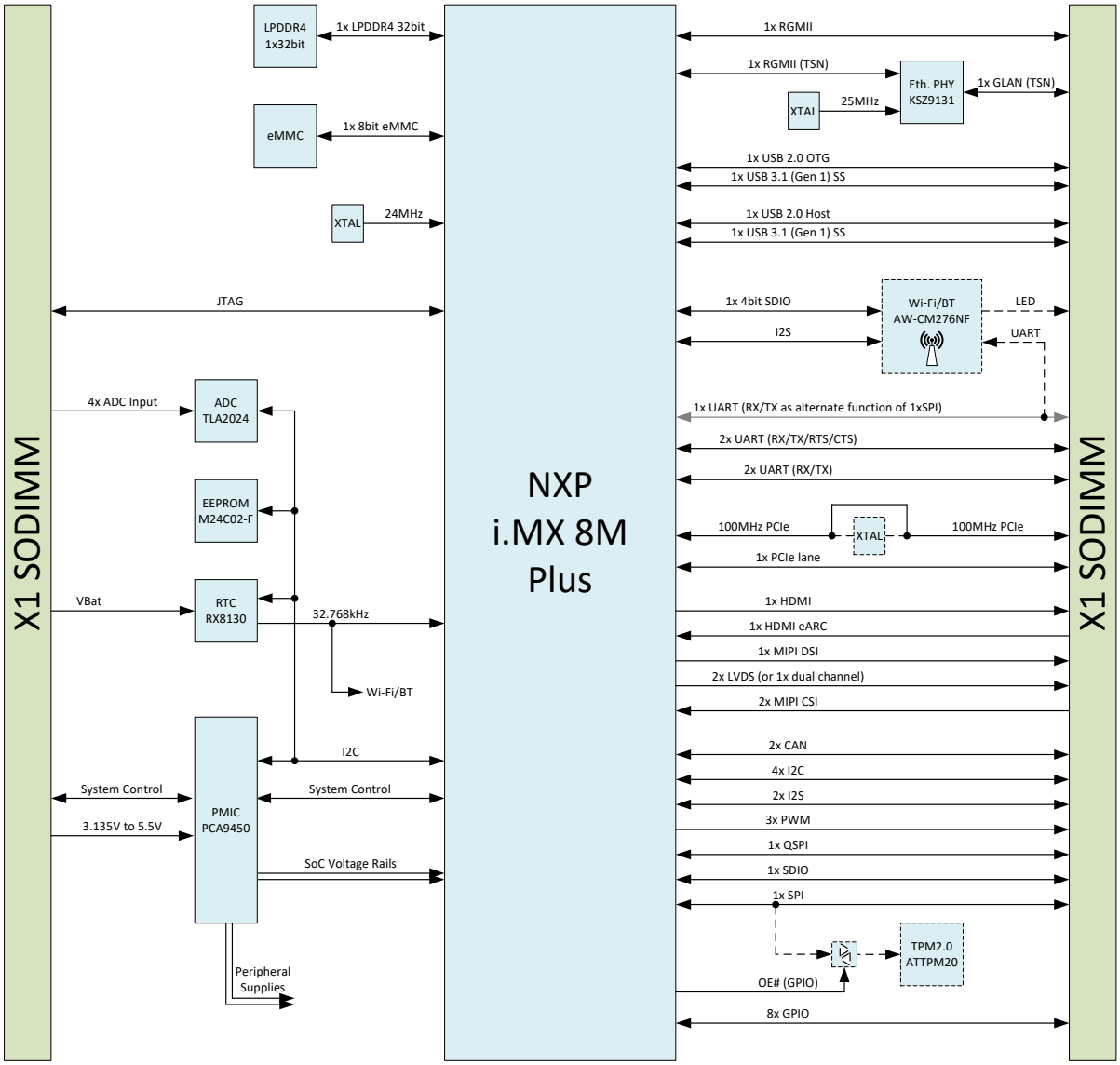


Figure 2 Verdin iMX8M Plus Block Diagram

Dashed lines indicate assembly options. See also section 1.8 for more information on build-to-order options.

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3. Verdin iMX8M Plus Connector

3.1 Pin Numbering

The Verdin module follows the same pin numbering scheme as the SODIMM DDR4 standard. Pins on the top side of the module have an odd number, while the pins on the bottom side have an even number.

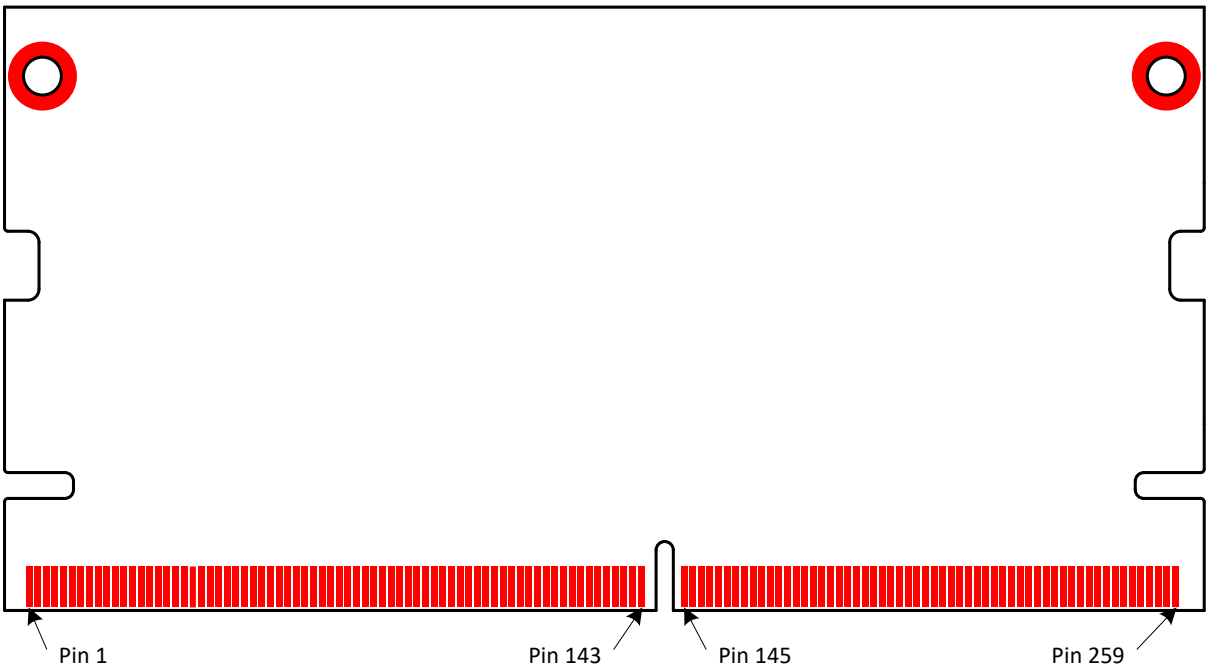


Figure 3: Pin numbering schema on the top side of the module

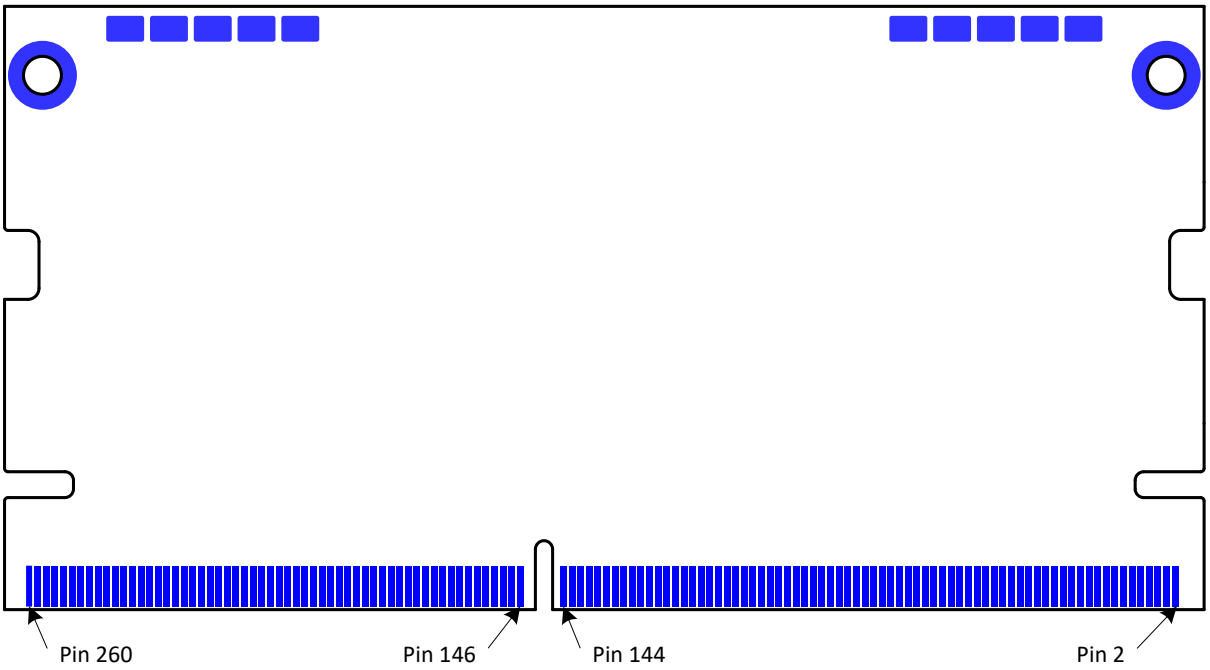


Figure 4: Pin numbering schema on the bottom side of the module (bottom view)

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3.1 Assignment

The following table describes the SODIMM connector pinout. Some pins are shaded dark grey as *"Module-specific"* interfaces. These pins might not be compatible with other modules in the Verdin family. Please be aware that you might lose compatibility when using other Verdin modules on your carrier board if you use these interfaces. It should be noted that *"Module-specific"* interfaces will be kept common across modules that share such interfaces wherever possible. For example, if both modules A and module B have an LVDS interface available in the same configurations as a *"Module-specific"* interface, they shall be assigned to the same pins in the *"Module-specific"* interface area of the connector. Hence, both module A and module B shall share compatibility between these parts of the *"Module-specific"* interface.

- X1: Pin number on the SODIMM edge connector (X1).
- Verdin Signal Name: The name of the signal according to the Verdin form factor definition. This name corresponds to the default usage of the pin. Some of the pins also have an alternate function. However, to be compatible with other Verdin modules, only the default function should be used, and the carrier board should be implemented according to the Verdin Carrier Board Design Guide.
- i.MX 8MP Ball Name: The name of the pin of the i.MX 8M Plus SoC.
- Non i.MX 8MP Ball: Connections to non-SoC balls such as peripherals and power supply.

Table 3-1 X1 Connector

X1 Pin	Verdin Signal Name	i.MX 8MP Ball Name	Non i.MX 8MP Ball	Note
1	JTAG_1_TDI	JTAG_TDI		
3	JTAG_1_TRST#	POR_B		Reset circuit driving CPU reset
5	JTAG_1_TDO	JTAG_TDO		
7	JTAG_1_VREF		1.8V	Reference output (max 10mA)
9	JTAG_1_TCK	JTAG_TCK		
11	GND		GND	
13	JTAG_1_TMS	JTAG_TMS		
15	PWM_1	SPDIF_EXT_CLK		
17	GPIO_9_DSI	SAI2_TXC		
19	PWM_3_DSI	SAI5_RXC		
21	GPIO_10_DSI	SAI3_RXFS		
23	DSI_1_D3_N	MIPI_DSI1_D3_N		
25	DSI_1_D3_P	MIPI_DSI1_D3_P		
27	GND		GND	
29	DSI_1_D2_N	MIPI_DSI1_D2_N		
31	DSI_1_D2_P	MIPI_DSI1_D2_P		
33	GND		GND	
35	DSI_1_CLK_N	MIPI_DSI1_CLK_N		
37	DSI_1_CLK_P	MIPI_DSI1_CLK_P		
39	GND		GND	
41	DSI_1_D1_N	MIPI_DSI1_D1_N		
43	DSI_1_D1_P	MIPI_DSI1_D1_P		
45	GND		GND	
47	DSI_1_D0_N	MIPI_DSI1_D0_N		
49	DSI_1_D0_P	MIPI_DSI1_D0_P		

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X1 Pin	Verdin Signal Name	i.MX 8MP Ball Name	Non i.MX 8MP Ball	Note
51	GND		GND	
53	I2C_2_DSI_SDA	I2C2_SDA		
55	I2C_2_DSI_SCL	I2C2_SCL		
57	I2C_3_HDMI_SDA	HDMI_DDC_SDA		
59	I2C_3_HDMI_SCL	HDMI_DDC_SCL		
61	HDMI_1_HPD	HDMI_HPD		
63	HDMI_1_CEC	HDMI_CEC		
65	GND		GND	
67	HDMI_1_TXC_N	HDMI_TXC_N		
69	HDMI_1_TXC_P	HDMI_TXC_P		
71	GND		GND	
73	HDMI_1_TXD0_N	HDMI_TXD0_N		
75	HDMI_1_TXD0_P	HDMI_TXD0_P		
77	GND		GND	
79	HDMI_1_TXD1_N	HDMI_TXD1_N		
81	HDMI_1_TXD1_P	HDMI_TXD1_P		
83	GND		GND	
85	HDMI_1_TXD2_N	HDMI_TXD2_N		
87	HDMI_1_TXD2_P	HDMI_TXD2_P		
89	GND		GND	
91	CSI_1_MCLK	SAI3_MCLK		
93	I2C_4_CSI_SDA	I2C3_SDA		
95	I2C_4_CSI_SCL	I2C3_SCL		
97	GND		GND	
99	CSI_1_D3_P	MIPI_CSI1_D3_P		
101	CSI_1_D3_N	MIPI_CSI1_D3_N		
103	GND		GND	
105	CSI_1_D2_P	MIPI_CSI1_D2_P		
107	CSI_1_D2_N	MIPI_CSI1_D2_N		
109	GND		GND	
111	CSI_1_CLK_P	MIPI_CSI1_CLK_P		
113	CSI_1_CLK_N	MIPI_CSI1_CLK_N		
115	GND		GND	
117	CSI_1_D1_P	MIPI_CSI1_D1_P		
119	CSI_1_D1_N	MIPI_CSI1_D1_N		
121	GND		GND	
123	CSI_1_D0_P	MIPI_CSI1_D0_P		
125	CSI_1_D0_N	MIPI_CSI1_D0_N		
127	GND		GND	
129	UART_1_RXD	UART1_RXD		
131	UART_1_TXD	UART1_TXD		
133	UART_1_RTS	SAI2_TXFS		
135	UART_1_CTS	SAI2_RXD0		
137	UART_2_RXD	UART2_RXD		
139	UART_2_TXD	UART2_TXD		
141	UART_2_RTS	SD1_DATA5		

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X1 Pin	Verdin Signal Name	i.MX 8MP Ball Name	Non i.MX 8MP Ball	Note
143	UART_2_CTS	SD1_DATA4		
145	GND		GND	
147	UART_3_RXD	UART3_RXD		
149	UART_3_TXD	UART3_TXD		
151	UART_4_RXD	UART4_RXD		
153	UART_4_TXD	UART4_TXD		
155	USB_1_EN	GPIO1_IO12		
157	USB_1_OC#	GPIO1_IO13		
159	USB_1_VBUS	USB1_VBUS		
161	USB_1_ID	USB1_ID		
163	USB_1_D_N	USB1_D_N		
165	USB_1_D_P	USB1_D_P		
167	GND		GND	
169	USB_2_SSTX_N	USB2_TX_N		
171	USB_2_SSTX_P	USB2_TX_P		
173	GND		GND	
175	USB_2_SSRX_N	USB2_RX_N		
177	USB_2_SSRX_P	USB2_RX_P		
179	GND		GND	
181	USB_2_D_N	USB2_D_N		
183	USB_2_D_P	USB2_D_P		
185	USB_2_EN	GPIO1_IO14		
187	USB_2_OC#	GPIO1_IO15		
189	ETH_2_RGMII_INT#	SAI1_TXD6		
191	ETH_2_RGMII_MDIO	SAI1_RXD3		
193	ETH_2_RGMII_MDC	SAI1_RXD2		
195	GND		GND	
197	ETH_2_RGMII_RXC	SAI1_TXC		
199	ETH_2_RGMII_RX_CTL	SAI1_TXFS		
201	ETH_2_RGMII_RXD_0	SAI1_RXD4		
203	ETH_2_RGMII_RXD_1	SAI1_RXD5		
205	ETH_2_RGMII_RXD_2	SAI1_RXD6		
207	ETH_2_RGMII_RXD_3	SAI1_RXD7		
209	GND		GND	
211	ETH_2_RGMII_TX_CTL	SAI1_TXD4		
213	ETH_2_RGMII_TXC	SAI1_TXD5		
215	ETH_2_RGMII_TXD_3	SAI1_TXD3		
217	ETH_2_RGMII_TXD_2	SAI1_TXD2		
219	ETH_2_RGMII_TXD_1	SAI1_TXD1		
221	ETH_2_RGMII_TXD_0	SAI1_TXD0		
223	GND		GND	
225	ETH_1_MDI0_P	_ETH_PHY	TXRXP_A	KSZ9131 Pin 2
227	ETH_1_MDI0_N	_ETH_PHY	TXRXM_A	KSZ9131 Pin 3
229	GND		GND	

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X1 Pin	Verdin Signal Name	i.MX 8MP Ball Name	Non i.MX 8MP Ball	Note
231	ETH_1_MDI1_N	_ETH_PHY	TXRXM_B	KSZ9131 Pin6
233	ETH_1_MDI1_P	_ETH_PHY	TXRXP_B	KSZ9131 Pin5
235	ETH_1_LED_1	_ETH_PHY	LED1	KSZ9131Pin17 (buffered)
237	ETH_1_LED_2	_ETH_PHY	LED2	KSZ9131Pin15 (buffered)
239	ETH_1_MDI2_P	_ETH_PHY	TXRXP_C	KSZ9131 Pin 7
241	ETH_1_MDI2_N	_ETH_PHY	TXRXM_C	KSZ9131 Pin 8
243	GND		GND	
245	ETH_1_MDI3_N	_ETH_PHY	TXRXM_D	KSZ9131 Pin 11
247	ETH_1_MDI3_P	_ETH_PHY	TXRXP_D	KSZ9131 Pin 10
249	VCC_BACKUP	_RTC_BAT	VBAT	RX8130 Pin 10
251	VCC		VCC	3.135 to 5.5V input
253	VCC		VCC	3.135 to 5.5V input
255	VCC		VCC	3.135 to 5.5V input
257	VCC		VCC	3.135 to 5.5V input
259	VCC		VCC	3.135 to 5.5V input
2	ADC_1		AIN3	TLA2024 Pin 7
4	ADC_2		AIN2	TLA2024 Pin 6
6	ADC_3		AIN1	TLA2024 Pin 5
8	ADC_4		AIN0	TLA2024 Pin 4
10	GND		GND	
12	I2C_1_SDA	I2C4_SDA		
14	I2C_1_SCL	I2C4_SCL		
16	PWM_2	GPIO1_IO11		
18	GND		GND	
20	CAN_1_TX	SPDIF_TX		
22	CAN_1_RX	SPDIF_RX		
24	CAN_2_TX	SAI2_TXD0		
26	CAN_2_RX	SAI2_MCLK		
28	GND		GND	
30	I2S_1_BCLK	SAI5_MCLK		
32	I2S_1_SYNC	SAI5_RXD1		
34	I2S_1_D_OUT	SAI5_RXFS		
36	I2S_1_D_IN	SAI1_RXD0		
38	I2S_1_MCLK	SAI1_MCLK		
40	GND		GND	
42	I2S_2_BCLK	SAI3_TXC		
44	I2S_2_SYNC	SAI3_TXFS		
46	I2S_2_D_OUT	SAI3_TXD		
48	I2S_2_D_IN	SAI3_RXD		

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X1 Pin	Verdin Signal Name	i.MX 8MP Ball Name	Non i.MX 8MP Ball	Note
50	GND		GND	
52	QSPI_1_CLK	NAND_ALE		
54	QSPI_1_CS#	NAND_CE0_B		
56	QSPI_1_IO0	NAND_DATA00		
58	QSPI_1_IO1	NAND_DATA01		
60	QSPI_1_IO2	NAND_DATA02		
62	QSPI_1_IO3	NAND_DATA03		
64	QSPI_1_CS2#	NAND_READY_B		Only regular GPIO
66	QSPI_1_DQS	NAND_DQS		
68	GND		GND	
70	SD_1_D2	SD2_DATA2 [1)]		Switchable output voltage
72	SD_1_D3	SD2_DATA3 [1)]		Switchable output voltage
74	SD_1_CMD	SD2_CMD [1)]		Switchable output voltage
76	SD_1_PWR_EN	SAI2_RXC		
78	SD_1_CLK	SD2_CLK [1)]		Switchable output voltage
80	SD_1_D0	SD2_DATA0 [1)]		Switchable output voltage
82	SD_1_D1	SD2_DATA1 [1)]		Switchable output voltage
84	SD_1_CD#	SD2_CD_B [1)]		Switchable output voltage
86	GND		GND	
88	MSP_1	LVDS0_CLK_N		
90	MSP_2	LVDS0_CLK_P		
92	MSP_3		GPIO[22]/ PCIE_W_DISABLEn	AW-CM276NF Pin 63, **Only on module with Wi-Fi**
94	MSP_4	LVDS0_D0_N		
96	MSP_5	LVDS0_D0_P		
98	GND		GND	
100	MSP_6	LVDS0_D1_N		
102	MSP_7	LVDS0_D1_P		
104	MSP_8		CONFIG_HOST[0]	AW-CM276NF Pin 8, **Only on module with Wi-Fi, Maximum voltage 1.8V**, leave unconnected
106	MSP_9	LVDS0_D2_N		
108	MSP_10	LVDS0_D2_P		
110	GND		GND	
112	MSP_11	LVDS0_D3_N		
114	MSP_12	LVDS0_D3_P		
116	MSP_13	ECSPI2_MISO	GPIO[14]/TCK/ WLAN Wake Host	AW-CM276NF Pin 46, **Only on module with Wi-Fi, Also connected to SoC Pin**
118	MSP_14	LVDS1_CLK_N		
120	MSP_15	LVDS1_CLK_P		
122	GND		GND	
124	MSP_16	LVDS1_D0_N		
126	MSP_17	LVDS1_D0_P		
128	MSP_18	ECSPI2_SS0	GPIO[13]/ BT Wake Host	AW-CM276NF Pin 28, **Only on module with Wi-Fi, Also connected to SoC Pin**
130	MSP_19	LVDS1_D1_N		
132	MSP_20	LVDS1_D1_P		

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X1 Pin	Verdin Signal Name	i.MX 8MP Ball Name	Non i.MX 8MP Ball	Note
134	GND		GND	
136	MSP_21	LVDS1_D2_N		
138	MSP_22	LVDS1_D2_P		
140	MSP_23		IRQ#	RX8130 Pin 6
142	MSP_24	LVDS1_D3_N		
144	MSP_25	LVDS1_D3_P		
146	GND		GND	
148	MSP_26	MIPI_CSI2_D0_N		
150	MSP_27	MIPI_CSI2_D0_P		
152	MSP_28	ECSPI2_MOSI	GPIO[9]/ UART_SIN	AW-CM276NF Pin 56, **Only on module with Wi-Fi,** **Also connected to SoC Pin**
154	MSP_29	MIPI_CSI2_D1_N		
156	MSP_30	MIPI_CSI2_D1_P		
158	GND		GND	
160	MSP_31	MIPI_CSI2_CLK_N		
162	MSP_32	MIPI_CSI2_CLK_P		
164	MSP_33	ECSPI2_SCLK	GPIO[8]/ UART_SOUT	AW-CM276NF Pin 55, **Only on module with Wi-Fi,** **Also connected to SoC Pin**
166	MSP_34	MIPI_CSI2_D2_N		
168	MSP_35	MIPI_CSI2_D2_P		
170	GND		GND	
172	MSP_36	MIPI_CSI2_D3_N	GPIO[13]/ BT Wake Host	
174	MSP_37	MIPI_CSI2_D3_P	GPIO[14]/TCK/ WLAN Wake Host	
176	MSP_38		GPIO[3]/ BT_LED	AW-CM276NF Pin 65, **Only on module with Wi-Fi**
178	MSP_39	USB1_TX_N		
180	MSP_40	USB1_TX_P		
182	GND		GND	
184	MSP_41	USB1_RX_N		
186	MSP_42	USB1_RX_P		
188	MSP_43		GPIO[2]/ WLAN_LED	AW-CM276NF Pin 64, **Only on module with Wi-Fi**
190	MSP_44	EARC_N_HPD		
192	MSP_45	EARC_P_UTIL		
194	GND		GND	
196	SPI_1_CLK	ECSPI1_SCLK		
198	SPI_1_MISO	ECSPI1_MISO		
200	SPI_1_MOSI	ECSPI1_MOSI		
202	SPI_1_CS	ECSPI1_SS0		
204	GND		GND	
206	GPIO_1	GPIO1_IO00		
208	GPIO_2	GPIO1_IO01		
210	GPIO_3	GPIO1_IO05		
212	GPIO_4	GPIO1_IO06		
214	PWR_1V8_MOCI		1.8V Output	Max. 250mA

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X1 Pin	Verdin Signal Name	i.MX 8MP Ball Name	Non i.MX 8MP Ball	Note
216	GPIO_5_CSI	GPIO1_IO07		
218	GPIO_6_CSI	GPIO1_IO08		
220	GPIO_7_CSI	SAI1_RXD1		
222	GPIO_8_CSI	SAI1_RXC		
224	GND		GND	
226	PCIE_1_CLK_N	PCIE_REF_PAD_CLK_N		
228	PCIE_1_CLK_P	PCIE_REF_PAD_CLK_P		
230	GND		GND	
232	PCIE_1_L0_RX_N	PCIE_RXN_N		
234	PCIE_1_L0_RX_P	PCIE_RXN_P		
236	GND		GND	
238	PCIE_1_L0_TX_N	PCIE_TXN_N		
240	PCIE_1_L0_TX_P	PCIE_TXN_P		
242	GND		GND	
244	PCIE_1_RESET#	SAI1_TXD7		
246	CTRL_RECOVERY_MICO#	BOOT_MODE0		Inverted signal, open-drain
248	CTRL_PWR_BTN_MICO#			Open-drain
250	CTRL_FORCE_OFF_MOCI#		Power Management	Open-drain, 5V tolerant
252	CTRL_WAKE1_MICO#	SAI1_RXFS		
254	CTRL_PWR_EN_MOCI		Power Management	
256	CTRL_SLEEP_MOCI#	SAI3_RXC		10kΩ pull-down resistor on module
258	CTRL_RESET_MOCI#		Power Management	Open-drain, 3.3V tolerant
260	CTRL_RESET_MICO#		Power Management	

[1] It is possible to change the IO voltage of the main SD interface from 3.3V (default) to 1.8V. The SD card driver may use this to switch to 1.8V for higher speed modes (SD UHS-I). Please note that the voltage can only be changed for all pins simultaneously and not individually. Therefore, use these pins with care.

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4. I/O Pins

4.1 Function Multiplexing

Low-speed I/O pins of the NXP i.MX 8M Plus SoC can be configured for any of the (and up to) seven alternate functions. Most of the pins can also be used as GPIOs (General-Purpose I/O, sometimes also referred to as Digital I/O). For example, the i.MX 8M Plus signal pin on the SODIMM finger pin 131 has the primary function UART1_TX (Verdin standard function UART_1_TXD). Besides this UART function, the pin can also be configured as ECSPI3_MOSI (SPI master out, slave in) and GPIO5_IO23 (GPIO).

The default setting for this pin is the primary function UART1_TX. It is strongly recommended, whenever possible, to use a pin for a function that is compatible with all Verdin modules. This guarantees the best compatibility with the standard software and with other modules in the Verdin family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the table listed in chapter 4.4, there is a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

4.2 Pin Control

The alternate function of each pin can be changed independently. Every pin has a Pad Mux Register in which the following settings can be configured (some settings might not be available for certain pins). The register is called IOMUXC_SW_MUX_CTL_PAD_x, where x is the name of the i.MX 8M Plus pin. More information about the available register settings can be found in the i.MX 8M Plus Reference Manual.

Table 4-1 Pad Mux Register

Bit	Field	Description	Remarks
31-5	Reserved		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enabled	Force the selected mux mode input path
3	Reserved		
2-0	MUX_MODE	000 Select mux mode: ALT0 mux port 001 Select mux mode: ALT1 mux port 010 Select mux mode: ALT2 mux port 011 Select mux mode: ALT3 mux port 100 Select mux mode: ALT4 mux port 101 Select mux mode: ALT5 mux port (GPIO) 110 Select mux mode: ALT6 mux port	Check section 4.4 for the available alternate function of the pin

For most pins, the ALT5 multiplexing option is reserved for the GPIO function. However, there are a few pins that feature the GPIO function on ALT0. Carefully check the table in section 4.4 and the reference manual provided by NXP.

The pins have an additional register that allows the configuration of pull-up/down resistors, drive strength, and other settings. The register is called IOMUXC_SW_PAD_CTL_PAD_x, where x is the name of the i.MX 8M Plus pin. Some settings might not be available on certain pins. More information about the available register settings can be found in the i.MX 8M Plus Reference Manual.

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Table 4-2 Pad Control Register

Bit	Field	Description	Remarks
31-9	Reserved		
8	PE	0 Pull resistor disabled 1 Pull resistor enable	
7	HYS	0 CMOS input 1 Schmitt trigger input	
6	PUE	0 Select pull-down resistor 1 Select pull-up resistor	Typical pull-up value 22kΩ Typical pull-down value 23kΩ
5	ODE	0 Output is CMOS 1 Output is open-drain	
4-3	FSE	0x Slow Slew Rate 1x Fast Slew Rate	Use a slow slew rate, if possible, for reducing EMC problems
2-0	DSE	00x Drive strength X1 01x Drive strength X2 10x Drive strength X4 11x Drive strength X6	If possible, decrease the drive strength to reduce EMC problems

Input functions that are available at more than one physical pin require an additional input multiplexer. This multiplexer is configured by a register called IOMUXC_x_SELECT_INPUT, where x is the name of the input function. More information about this register can be found in the i.MX 8M Plus Reference Manual.

4.3 Pin Reset Status

After a reset, the i.MX 8M Plus pins can be in different modes. Most of them are pulled low. A few are high impedance or pulled up. Please check the table in chapter 4.4 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

Please be aware. The pin reset status is only guaranteed during the release of the reset signal. During the power-up sequence, the states of the pins might be undefined until the related IO bank voltage is enabled on the module.

Reset Status Description

PD: Pull-down (input)
PU: Pull-up (input)
Z: High impedance (input)

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4.4 SoC Functions List

Below is a list of all the i.MX 8M Plus pins that are available on the SODIMM connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT5 function. The alternate functions used to provide the primary interfaces, done to ensure the best compatibility with other Verdin modules, are highlighted.

Function Short Forms

ADC:	Analog to Digital Converter input
CAAM:	Cryptographic Acceleration and Assurance Module
CAN:	Controller Area Network
CCM:	Clock Control Module
CSI:	Camera Serial Interface
CSU:	Central Security Unit
EARC:	Enhanced Audio Return Channel (for HDMI)
ECC:	Error-Correcting Code
ECSPI:	Enhanced Configurable SPI
ENET:	Ethernet MAC interface
GPIO:	General-Purpose Input Output
GPC:	General Power Controller
GPT:	General Purpose Timer
HDMI:	High-Definition Multimedia Interface
I2C:	Inter-Integrated Circuit
ISP:	Image Signal Processor
JTAG:	Test Interface
LVDS:	FPD-Link/FlatLink Display interface
MIPI_CSI:	MIPI CSI Subsystem
MIPI_DSI:	MIPI DSI Subsystem
NAND:	Interface for NAND Flash
NPU:	Neural Processing Unit
PCIE:	PCI Express
PDM:	Pulse-Density Modulation Microphone Input
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
SAI:	Serial Interface for Audio (I2S and AC97)
SDMA:	Smart Direct Memory Access Controller
SNVS:	Secure Non-Volatile Storage
SPDIF:	Sony/Philips Digital Interface
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)
VPU:	Video Processing Unit (acceleration for video encoding and decoding)

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X1 Pin	i.MX 8M Plus Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	Default Mode	Reset State	Power Block
1	JTAG_TDI	G16	JTAG_TDI							ALT0	PU	NVCC_JTAG
5	JTAG_TDO	F14	JTAG_TDO							ALT0	PU	NVCC_JTAG
9	JTAG_TCK	G18	JTAG_TCK							ALT0	PU	NVCC_JTAG
13	JTAG_TMS	G14	JTAG_TMS							ALT0	PU	NVCC_JTAG
15	SPDIF_EXT_CLK	AC18	SPDIF1_EXT_CLK	PWM1_OUT		GPT1_COMPARE3		GPIO5_IO5		ALT5	PD	NVCC_SAI2_SAI3
17	SAI2_TXC	AH15	SAI2_TX_BCLK	SAI5_TX_DATA2		CAN1_RX		GPIO4_IO25	PDM_BIT_STREAM1	ALT5	PD	NVCC_SAI2_SAI3
19	SAI5_RXC	AD14	SAI5_RX_BCLK	SAI1_TX_DATA1	PWM3_OUT	I2C6_SDA	PDM_CLK	GPIO3_IO20		ALT5	PD	NVCC_SAI1_SAI5
21	SAI3_RXFS	AJ19	SAI3_RX_SYNC	SAI2_RX_DATA1	SAI5_RX_SYNC	SAI3_RX_DATA1	SPDIF1_IN	GPIO4_IO28	PDM_BIT_STREAM0	ALT5	PD	NVCC_SAI2_SAI3
53	I2C2_SDA	AE8	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT	USDHC3_WP	ECSPI1_SS0		GPIO5_IO17		ALT5	PD	NVCC_I2C_UART
55	I2C2_SCL	AH6	I2C2_SCL	ENET_QOS_1588_EVENT1_IN	USDHC3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_AUX_IN	GPIO5_IO16		ALT5	PD	NVCC_I2C_UART
57	HDMI_DDC_SDA	AF22	HDMI_SDA			I2C5_SDA	CAN1_RX	GPIO3_IO27		ALT5	PD	NVCC_ECSPI_HDMI
59	HDMI_DDC_SCL	AC22	HDMI_SCL			I2C5_SCL	CAN1_TX	GPIO3_IO26		ALT5	PD	NVCC_ECSPI_HDMI
61	HDMI_HPD	AE22	HDMI_HPD	HDMI_HPD_O		I2C6_SDA	CAN2_RX	GPIO3_IO29		ALT5	PD	NVCC_ECSPI_HDMI
63	HDMI_CEC	AD22	HDMI_CEC			I2C6_SCL	CAN2_TX	GPIO3_IO28		ALT5	PD	NVCC_ECSPI_HDMI
91	SAI3_MCLK	AJ20	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		SPDIF1_OUT	GPIO5_IO2	SPDIF1_IN	ALT5	PD	NVCC_SAI2_SAI3
93	I2C3_SDA	AJ6	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO19		ALT5	PD	NVCC_I2C_UART
95	I2C3_SCL	AJ7	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO18		ALT5	PD	NVCC_I2C_UART
129	UART1_RXD	AD6	UART1_RX	ECSPI3_SCLK				GPIO5_IO22		ALT5	PD	NVCC_I2C_UART
131	UART1_TXD	AJ3	UART1_TX	ECSPI3_MOSI				GPIO5_IO23		ALT5	PD	NVCC_I2C_UART
133	SAI2_TXFS	AJ17	SAI2_TX_SYNC	SAI5_TX_DATA1	ENET_QOS_1588_EVENT3_OUT	SAI2_TX_DATA1	UART1_CTS_B	GPIO4_IO24	PDM_BIT_STREAM2	ALT5	PD	NVCC_SAI2_SAI3
135	SAI2_RXD0	AJ14	SAI2_RX_DATA0	SAI5_TX_DATA0	ENET_QOS_1588_EVENT2_OUT	SAI2_TX_DATA1	UART1_RTS_B	GPIO4_IO23	PDM_BIT_STREAM3	ALT5	PD	NVCC_SAI2_SAI3
137	UART2_RXD	AF6	UART2_RX	ECSPI3_MISO		GPT1_COMPARE3		GPIO5_IO24		ALT5	PD	NVCC_I2C_UART
139	UART2_TXD	AH4	UART2_TX	ECSPI3_SS0		GPT1_COMPARE2		GPIO5_IO25		ALT5	PD	NVCC_I2C_UART
141	SD1_DATA5	AA29	USDHC1_DATA5	ENET1_TX_ER		I2C1_SDA	UART2_CTS_B	GPIO2_IO7		ALT5	PD	NVCC_SD1
143	SD1_DATA4	U26	USDHC1_DATA4	ENET1_RGMII_TX_CTL		I2C1_SCL	UART2_RTS_B	GPIO2_IO6		ALT5	PD	NVCC_SD1
147	UART3_RXD	AE6	UART3_RX	UART1_CTS_B	USDHC3_RESET_B	GPT1_CAPTURE2	CAN2_TX	GPIO5_IO26		ALT5	PD	NVCC_I2C_UART
149	UART3_TXD	AJ4	UART3_TX	UART1_RTS_B	USDHC3_VSELECT	GPT1_CLK	CAN2_RX	GPIO5_IO27		ALT5	PD	NVCC_I2C_UART
151	UART4_RXD	AJ5	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B	GPT1_COMPARE1	I2C6_SCL	GPIO5_IO28		ALT5	PD	NVCC_I2C_UART
153	UART4_TXD	AH5	UART4_TX	UART2_RTS_B		GPT1_CAPTURE1	I2C6_SDA	GPIO5_IO29		ALT5	PD	NVCC_I2C_UART
155	GPIO1_IO12	A5	GPIO1_IO12	USB1_OTG_PWR				SDMA2_EXT_EVENT1		ALT0	PD	NVCC_GPIO1
157	GPIO1_IO13	A6	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT		ALT0	PD	NVCC_GPIO1
185	GPIO1_IO14	A4	GPIO1_IO14	USB2_OTG_PWR			USDHC3_CD_B	PWM3_OUT	CCM_CLKO1	ALT0	PD	NVCC_GPIO1
187	GPIO1_IO15	B5	GPIO1_IO15	USB2_OTG_OC			USDHC3_WP	PWM4_OUT	CCM_CLKO2	ALT0	PD	NVCC_GPIO1
189	SAI1_TXD6	AC12	SAI1_TX_DATA6	SAI6_RX_SYNC	SAI6_TX_SYNC		ENET1_RX_ER	GPIO4_IO18		ALT5	PD	NVCC_SAI1_SAI5
191	SAI1_RXD3	AJ8	SAI1_RX_DATA3	SAI5_RX_DATA3		PDM_BIT_STREAM3	ENET1_MDIO	GPIO4_IO5		ALT5	PD	NVCC_SAI1_SAI5
193	SAI1_RXD2	AH9	SAI1_RX_DATA2	SAI5_RX_DATA2		PDM_BIT_STREAM2	ENET1_MDC	GPIO4_IO4		ALT5	PD	NVCC_SAI1_SAI5
197	SAI1_TXC	AJ12	SAI1_TX_BCLK	SAI5_TX_BCLK			ENET1_RGMII_RXC	GPIO4_IO11		ALT5	PD	NVCC_SAI1_SAI5
199	SAI1_TXFS	AF12	SAI1_TX_SYNC	SAI5_TX_SYNC			ENET1_RGMII_RX_CTL	GPIO4_IO10		ALT5	PD	NVCC_SAI1_SAI5
201	SAI1_RXD4	AD10	SAI1_RX_DATA4	SAI6_TX_BCLK	SAI6_RX_BCLK		ENET1_RGMII_RD0	GPIO4_IO6		ALT5	PD	NVCC_SAI1_SAI5
203	SAI1_RXD5	AE10	SAI1_RX_DATA5	SAI6_TX_DATA0	SAI6_RX_DATA0	SAI1_RX_SYNC	ENET1_RGMII_RD1	GPIO4_IO7		ALT5	PD	NVCC_SAI1_SAI5
205	SAI1_RXD6	AH10	SAI1_RX_DATA6	SAI6_TX_SYNC	SAI6_RX_SYNC		ENET1_RGMII_RD2	GPIO4_IO8		ALT5	PD	NVCC_SAI1_SAI5
207	SAI1_RXD7	AH12	SAI1_RX_DATA7	SAI6_MCLK	SAI1_TX_SYNC	SAI1_TX_DATA4	ENET1_RGMII_RD3	GPIO4_IO9		ALT5	PD	NVCC_SAI1_SAI5
211	SAI1_TXD4	AH13	SAI1_TX_DATA4	SAI6_RX_BCLK	SAI6_TX_BCLK		ENET1_RGMII_TX_CTL	GPIO4_IO16		ALT5	PD	NVCC_SAI1_SAI5
213	SAI1_TXD5	AH14	SAI1_TX_DATA5	SAI6_RX_DATA0	SAI6_TX_DATA0		ENET1_RGMII_TXC	GPIO4_IO17		ALT5	PD	NVCC_SAI1_SAI5
215	SAI1_TXD3	AD12	SAI1_TX_DATA3	SAI5_TX_DATA3			ENET1_RGMII_TD3	GPIO4_IO15		ALT5	PD	NVCC_SAI1_SAI5
217	SAI1_TXD2	AH11	SAI1_TX_DATA2	SAI5_TX_DATA2			ENET1_RGMII_TD2	GPIO4_IO14		ALT5	PD	NVCC_SAI1_SAI5
219	SAI1_TXD1	AJ10	SAI1_TX_DATA1	SAI5_TX_DATA1			ENET1_RGMII_TD1	GPIO4_IO13		ALT5	PD	NVCC_SAI1_SAI5
221	SAI1_TXD0	AJ11	SAI1_TX_DATA0	SAI5_TX_DATA0			ENET1_RGMII_TD0	GPIO4_IO12		ALT5	PD	NVCC_SAI1_SAI5
12	I2C4_SDA	AD8	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO21		ALT5	PD	NVCC_I2C_UART
14	I2C4_SCL	AF8	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B	ECSPI2_MISO		GPIO5_IO20		ALT5	PD	NVCC_I2C_UART

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X1 Pin	i.MX 8M Plus Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	Default Mode	Reset State	Power Block
16	GPIO1_IO11	D8	GPIO1_IO11	USB2_OTG_ID	PWM2_OUT		USDHC3_VSELECT	CCM_PMIC_READY		ALT0	PD	NVCC_GPIO1
20	SPDIF_TX	AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	CAN1_TX	GPIO5_IO3		ALT5	PD	NVCC_SAI2_SAI3
22	SPDIF_RX	AD18	SPDIF1_IN	PWM2_OUT	I2C5_SDA	GPT1_COMPARE2	CAN1_RX	GPIO5_IO4		ALT5	PD	NVCC_SAI2_SAI3
24	SAI2_TXD0	AH16	SAI2_TX_DATA0	SAI5_TX_DATA3	ENET_QOS_1588_EVENT2_IN	CAN2_TX	ENET_QOS_1588_EVENT2_AUX_IN	GPIO4_IO26	SRC_BOOT_MODE4	ALT5	PD	NVCC_SAI2_SAI3
26	SAI2_MCLK	AJ15	SAI2_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_IN	CAN2_RX	ENET_QOS_1588_EVENT3_AUX_IN	GPIO4_IO27	SAI3_MCLK	ALT5	PD	NVCC_SAI2_SAI3
30	SAI5_MCLK	AF14	SAI5_MCLK	SAI1_TX_BCLK	PWM1_OUT	I2C5_SDA		GPIO3_IO25	CAN2_RX	ALT5	PD	NVCC_SAI1_SAI5
32	SAI5_RXD1	AD16	SAI5_RX_DATA1	SAI1_TX_DATA3	SAI1_TX_SYNC	SAI5_TX_SYNC	PDM_BIT_STREAM1	GPIO3_IO22	CAN1_TX	ALT5	PD	NVCC_SAI1_SAI5
34	SAI5_RXFS	AC14	SAI5_RX_SYNC	SAI1_TX_DATA0	PWM4_OUT	I2C6_SCL		GPIO3_IO19		ALT5	PD	NVCC_SAI1_SAI5
36	SAI1_RXD0	AC10	SAI1_RX_DATA0	SAI5_RX_DATA0	SAI1_TX_DATA1	PDM_BIT_STREAM0	ENET1_1588_EVENT1_IN	GPIO4_IO2		ALT5	PD	NVCC_SAI1_SAI5
38	SAI1_MCLK	AE12	SAI1_MCLK	SAI5_MCLK	SAI1_TX_BCLK		ENET1_TX_CLK	GPIO4_IO20		ALT5	PD	NVCC_SAI1_SAI5
42	SAI3_TXC	AH19	SAI3_TX_BCLK	SAI2_TX_DATA2	SAI5_RX_DATA2	GPT1_CAPTURE1	UART2_TX	GPIO5_IO0	PDM_BIT_STREAM2	ALT5	PD	NVCC_SAI2_SAI3
44	SAI3_TXFS	AC16	SAI3_TX_SYNC	SAI2_TX_DATA1	SAI5_RX_DATA1	SAI3_TX_DATA1	UART2_RX	GPIO4_IO31	PDM_BIT_STREAM3	ALT5	PD	NVCC_SAI2_SAI3
46	SAI3_TXD	AH18	SAI3_TX_DATA0	SAI2_TX_DATA3	SAI5_RX_DATA3	GPT1_CAPTURE2	SPDIF1_EXT_CLK	GPIO5_IO1	SRC_BOOT_MODE5	ALT5	PD	NVCC_SAI2_SAI3
48	SAI3_RXD	AF18	SAI3_RX_DATA0	SAI2_RX_DATA3	SAI5_RX_DATA0		UART2_RTS_B	GPIO4_IO30	PDM_BIT_STREAM1	ALT5	PD	NVCC_SAI2_SAI3
52	NAND_ALE	N25	NAND_ALE	QSPI_A_SCLK	SAI3_TX_BCLK	ISP_FL_TRIG_0	UART3_RX	GPIO3_IO0		ALT5	PD	NVCC_NAND
54	NAND_CE0_B	L26	NAND_CE0_B	QSPI_A_SS0_B	SAI3_TX_DATA0	ISP_SHUTTER_TRIG_0	UART3_TX	GPIO3_IO1		ALT5	PD	NVCC_NAND
56	NAND_DATA00	R25	NAND_DATA00	QSPI_A_DATA0	SAI3_RX_DATA0	ISP_FLASH_TRIG_0	UART4_RX	GPIO3_IO6		ALT5	PD	NVCC_NAND
58	NAND_DATA01	L25	NAND_DATA01	QSPI_A_DATA1	SAI3_TX_SYNC	ISP_PRELIGHT_TRIG_0	UART4_TX	GPIO3_IO7		ALT5	PD	NVCC_NAND
60	NAND_DATA02	L24	NAND_DATA02	QSPI_A_DATA2	USDHC3_CD_B	UART4_CTS_B	I2C4_SDA	GPIO3_IO8		ALT5	PD	NVCC_NAND
62	NAND_DATA03	N24	NAND_DATA03	QSPI_A_DATA3	USDHC3_WP	UART4_RTS_B	ISP_FL_TRIG_1	GPIO3_IO9		ALT5	PD	NVCC_NAND
64	NAND_READY_B	T28	NAND_READY_B		USDHC3_RESET_B		I2C3_SCL	GPIO3_IO16		ALT5	PD	NVCC_NAND
66	NAND_DQS	R26	NAND_DQS	QSPI_A_DQS	SAI3_MCLK	ISP_SHUTTER_OPEN_0	I2C3_SCL	GPIO3_IO14		ALT5	PD	NVCC_NAND
70	SD2_DATA2	AA26	USDHC2_DATA2		ECSPI2_SS0	SPDIF1_OUT	PDM_BIT_STREAM2	GPIO2_IO17		ALT5	PD	NVCC_SD2
72	SD2_DATA3	AA25	USDHC2_DATA3		ECSPI2_MISO	SPDIF1_IN	PDM_BIT_STREAM3	GPIO2_IO18	SRC_EARLY_RESET	ALT5	PD	NVCC_SD2
74	SD2_CMD	AB28	USDHC2_CMD		ECSPI2_MOSI	UART4_TX	PDM_CLK	GPIO2_IO14		ALT5	PD	NVCC_SD2
76	SAI2_RXC	AJ16	SAI2_RX_BCLK	SAI5_TX_BCLK		CAN1_TX	UART1_RX	GPIO4_IO22	PDM_BIT_STREAM1	ALT5	PD	NVCC_SAI2_SAI3
78	SD2_CLK	AB29	USDHC2_CLK		ECSPI2_SCLK	UART4_RX		GPIO2_IO13		ALT5	PD	NVCC_SD2
80	SD2_DATA0	AC28	USDHC2_DATA0		I2C4_SDA	UART2_RX	PDM_BIT_STREAM0	GPIO2_IO15		ALT5	PD	NVCC_SD2
82	SD2_DATA1	AC29	USDHC2_DATA1		I2C4_SCL	UART2_TX	PDM_BIT_STREAM1	GPIO2_IO16		ALT5	PD	NVCC_SD2
84	SD2_CD_B	AD29	USDHC2_CD_B					GPIO2_IO12		ALT5	PD	NVCC_SD2
116	ECSPI2_MISO [1]	AH20	ECSPI2_MISO	UART4_CTS_B	I2C4_SCL	SAI7_MCLK	CCM_CLKO1	GPIO5_IO12		ALT5	PD	NVCC_ECSPI_HDMI
128	ECSPI2_SS0 [1]	AJ22	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA		CCM_CLKO2	GPIO5_IO13		ALT5	PD	NVCC_ECSPI_HDMI
152	ECSPI2_MOSI [1]	AJ21	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI7_TX_DATA0		GPIO5_IO11		ALT5	PD	NVCC_ECSPI_HDMI
164	ECSPI2_SCLK [1]	AH21	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TX_BCLK		GPIO5_IO10		ALT5	PD	NVCC_ECSPI_HDMI
196	ECSPI1_SCLK	AF20	ECSPI1_SCLK	UART3_RX	I2C1_SCL	SAI7_RX_SYNC		GPIO5_IO6		ALT5	PD	NVCC_ECSPI_HDMI
198	ECSPI1_MISO	AD20	ECSPI1_MISO	UART3_CTS_B	I2C2_SCL	SAI7_RX_DATA0		GPIO5_IO8		ALT5	PD	NVCC_ECSPI_HDMI
200	ECSPI1_MOSI	AC20	ECSPI1_MOSI	UART3_TX	I2C1_SDA	SAI7_RX_BCLK		GPIO5_IO7		ALT5	PD	NVCC_ECSPI_HDMI
202	ECSPI1_SS0	AE20	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI7_TX_SYNC		GPIO5_IO9		ALT5	PD	NVCC_ECSPI_HDMI
206	GPIO1_IO00	A7	GPIO1_IO0	CCM_ENET_PHY_REF_CLK_ROOT		ISP_FL_TRIG_0		CCM_REF_CLK_32K	CCM_EXT_CLK1	ALT0	PD	NVCC_GPIO1
208	GPIO1_IO01	E8	GPIO1_IO1	PWM1_OUT		ISP_SHUTTER_TRIG_0		CCM_REF_CLK_24M	CCM_EXT_CLK2	ALT0	PD	NVCC_GPIO1
210	GPIO1_IO05	B4	GPIO1_IO5	M7_NMI		ISP_FL_TRIG_1		CCM_PMIC_READY		ALT0	PU	NVCC_GPIO1
212	GPIO1_IO06	A3	GPIO1_IO6	ENET_QOS_MDC		ISP_SHUTTER_TRIG_1		USDHC1_CD_B	CCM_EXT_CLK3	ALT0	PD	NVCC_GPIO1
216	GPIO1_IO07	F6	GPIO1_IO7	ENET_QOS_MDIO		ISP_FLASH_TRIG_1		USDHC1_WP	CCM_EXT_CLK4	ALT0	PD	NVCC_GPIO1
218	GPIO1_IO08	A8	GPIO1_IO8	ENET_QOS_1588_EVENT0_IN	PWM1_OUT	ISP_PRELIGHT_TRIG_1	ENET_QOS_1588_EVENT0_AUX_IN	USDHC2_RESET_B		ALT0	PD	NVCC_GPIO1
220	SAI1_RXD1	AF10	SAI1_RX_DATA1	SAI5_RX_DATA1		PDM_BIT_STREAM1	ENET1_1588_EVENT1_OUT	GPIO4_IO3		ALT5	PD	NVCC_SAI1_SAI5
222	SAI1_RXC	AH8	SAI1_RX_BCLK	SAI5_RX_BCLK		PDM_CLK	ENET1_1588_EVENT0_OUT	GPIO4_IO1		ALT5	PD	NVCC_SAI1_SAI5
244	SAI1_TXD7	AJ13	SAI1_TX_DATA7	SAI6_MCLK		PDM_CLK	ENET1_TX_ER	GPIO4_IO19		ALT5	PD	NVCC_SAI1_SAI5

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X1 Pin	i.MX 8M Plus Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	Default Mode	Reset State	Power Block
252	SAI1_RXFS	AJ9	SAI1_RX_SYNC	SAI5_RX_SYNC			ENET1_1588_EVENT0_IN	GPIO4_IO0		ALT5	PD	NVCC_SAI1_SAI5
256	SAI3_RXC	AJ18	SAI3_RX_BCLK	SAI2_RX_DATA2	SAI5_RX_BCLK	GPT1_CLK	UART2_CTS_B	GPIO4_IO29	PDM_CLK	ALT5	PD	NVCC_SAI2_SAI3

[1] Only available on modules with Wi-Fi/Bluetooth, this pin is shared with a Wi-Fi module signal

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5. Interface Description

5.1 Power Signals

Table 5-1 Power Supply Pins

X1 Pin #	Verdin Signal Name	I/O	Description	Remarks
251, 253, 255, 257, 259	VCC	I	3.135V to 5.5V main power supply	Use decoupling capacitors on the carrier board
10, 11, 18, 27, 28, 33, 39, 40, 45, 50, 51, 65, 68, 71, 77, 83, 86, 89, 97, 98, 103, 109, 110, 115, 121, 122, 127, 134, 145, 146, 158, 167, 170, 173, 179, 182, 194, 195, 204, 209, 223, 224, 229, 230, 236, 242, 243	GND	I	Digital Ground	
249	VCC_BACKUP	I	RTC Power supply can be connected to a backup battery.	Can be left unconnected if the internal RTC is not used. VCC, not VCC_BACKUP, powers the SNVS supplies of the SoC.

Table 5-2 Power Management Pins

X1 Pin #	Verdin Signal Name	I/O	Type	Remarks
258	CTRL_RESET_MOCI#	O	OD 3.3V	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# does not get asserted. The output is an open-drain type without a pull-up resistor on the module. The signal is 3.3V tolerant. The carrier board can pull the signal up to 1.8V or 3.3V. It can be left floating on the carrier board.
254	CTRL_PWR_EN_MOCI	O	1.8V	Enable signal for the power rails of the carrier board peripherals. This output remains high during sleep modes.
256	CTRL_SLEEP_MOCI#	O	1.8V	Enable signal for the power rails on the carrier board peripherals, which need to be turned off during sleep mode. It is only high during the running mode. The signal is standard GPIO with an on-module 10k pull-down resistors. The signal is defined during the power-up sequence. The signal can be left floating on the carrier board.
260	CTRL_RESET_MICO#	I	OD 1.8V	Open-drain input, which resets the module if shorted to ground on carrier board. There is a 100k on-module pull-up to the 1.8V SNVS rail present. This means it can be left floating on the carrier board.
248	CTRL_PWR_BTN_MICO#	I	OD 1.8V	Long pulling down is shutting down the module. Short pulling down is turning on module from off state. Open-drain input with 100k pull-up resistor to the 1.8V SNVS rail is on the module. It can be left floating on the carrier board.
246	CTRL_RECOVERY_MICO#	I	OD 1.8V	Shorting to the ground during power-up is setting the module into recovery mode. There is a 10k pull-up on the module. It can be left floating on the carrier board.
252	CTRL_WAKE1_MICO#	I	1.8V	Wake-capable pin, which allows you to resume from sleep mode. There are no pull resistors on the carrier board. It can be left floating on the carrier board if the wake feature is disabled in the software. It is a regular SoC GPIO.
250	CTRL_FORCE_OFF_MOCI#	O	OD 5V	Output for forcing the turning-off of the main power rail. This signal needs to be ignored for the first 400ms during the power-up sequence. The signal is 5V tolerant. The carrier board can pull the signal up to 1.8V, 3.3V, or 5V. It can be left floating on the carrier board.

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The Verdin iMX8M Plus features the NXP PCA9450C power management IC (PMIC). In addition to managing the power-up and down sequence, this IC also controls the voltage level of specific power rails. When applying the main power to the Verdin module, the PMIC will ramp up all rails, then release the POR_B signal at the end. This reset is used for the SoC and some of the on-module peripherals. It is available as a buffered output on pin 258 of the SODIMM module edge connector. This CTRL_RESET_MOCI# signal is an open-drain signal without pull-up resistors on the module. Since the pin is 3.3V tolerant, the carrier board can pull it up to 1.8V or 3.3V.

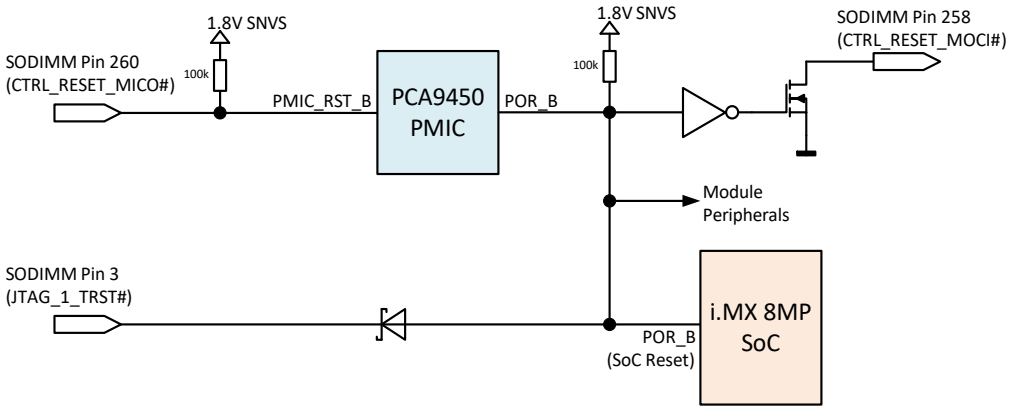


Figure 5 RESET_MOCI# circuit

The Verdin standard features a reset input (CTRL_RESET_MICO#, pin 260). This input is connected to the PMIC_RST_B input of the PCA9450A PMIC. The PMIC is programmed to do a power-down sequence when the PMIC_RST_B signal is set low. The power-down sequence is followed by a power-up sequence if the CTRL_RESET_MICO# is released. The CTRL_RESET_MICO# pin can be left floating if not needed.

Since the i.MX 8M Plus does not feature a dedicated JTAG reset input, the JTAG_1_TRST# (pin 3) is connected over a Schottky diode to the general reset of the module. This means the JTAG_1_TRST# signal is resetting the complete module but does not do a power cycle.

The Verdin iMX8M Plus features a power button input signal (CTRL_PWR_BTN_MICO#, pin 248). This input signal is connected directly to the ONOFF input of the i.MX 8M Plus SoC. A short press (<5s) starts the power-up sequence if the module is shut down. If the module is running, a short press (<5s) will create an interrupt. It depends on the operating system's settings whether this interrupt will initiate a power-down sequence or some other reaction. A long press (>5s) of the CTRL_PWR_BTN_MICO# will initiate the power-down sequence of the PMIC, independent of the operating system (force off). Since the Verdin standard defines that a module always starts booting when the main power rail is applied, a pulse generator circuit on the module generates a short power button press signal after the main input rail is attached to the module.

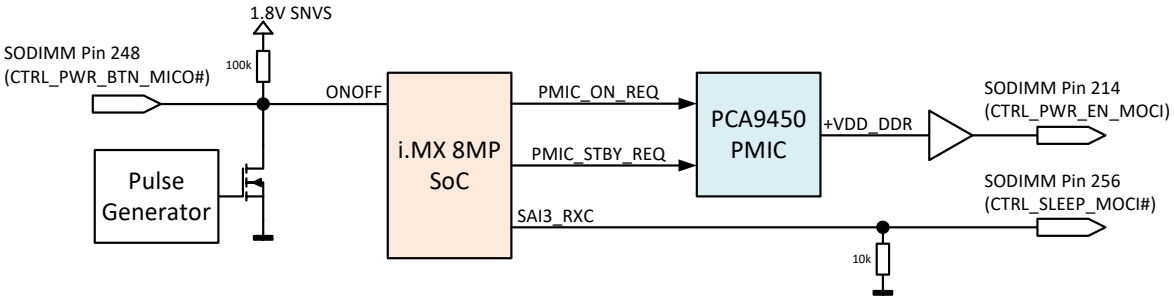


Figure 6 Power enable circuit

It is possible to turn off the power rails for the on-module Ethernet PHY completely to save power. GPIO2_IO20 controls the rails. The control is active-on. This means setting the GPIO high will

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enable the rails, while setting it low will disable them. The power rails for the Wi-Fi module are not individually switchable. However, the Wi-Fi module has a power-down pin that turns off the internal power rails and reduces the current to around 0.6mA. The Wi-Fi module features a power-on reset. No external reset is required. However, the firmware needs to be downloaded to the Wi-Fi module every time the power rail is turned on. The GPIO2_IO11 controls the power-down. Setting this GPIO low sets the Wi-Fi module in the power-down mode.

Table 5-3 On-Module Peripheral Power Control

GPIO	i.MX 8MP Ball Name	Peripheral Power Rail
GPIO2_IO11	SD1_STROBE	Wi-Fi and Bluetooth Module
GPIO2_IO20	SD2_WP	Ethernet PHY

The Verdin iMX8M Plus features a CTRL_FORCE_OFF_MOCI# signal which is intended to be used for killing the main power rail. This signal is generated from the PMIC. For preventing the signals is triggered during a reset cycle, the CTRL_FORCE_OFF_MOCI# is delayed. This means the CTRL_FORCE_OFF_MOCI# is asserted around 1.5s after the PMIC has been powered off. The 1.5 seconds is a typical value. The actual delay can vary between modules and temperatures.

5.1.1 Power Supply Use Case Examples

The power control pins of the Verdin module are very flexible and allow different use cases for the power supply on the carrier board. The following block diagrams are just examples. There are other options possible.

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Verdin Development Board Use Case

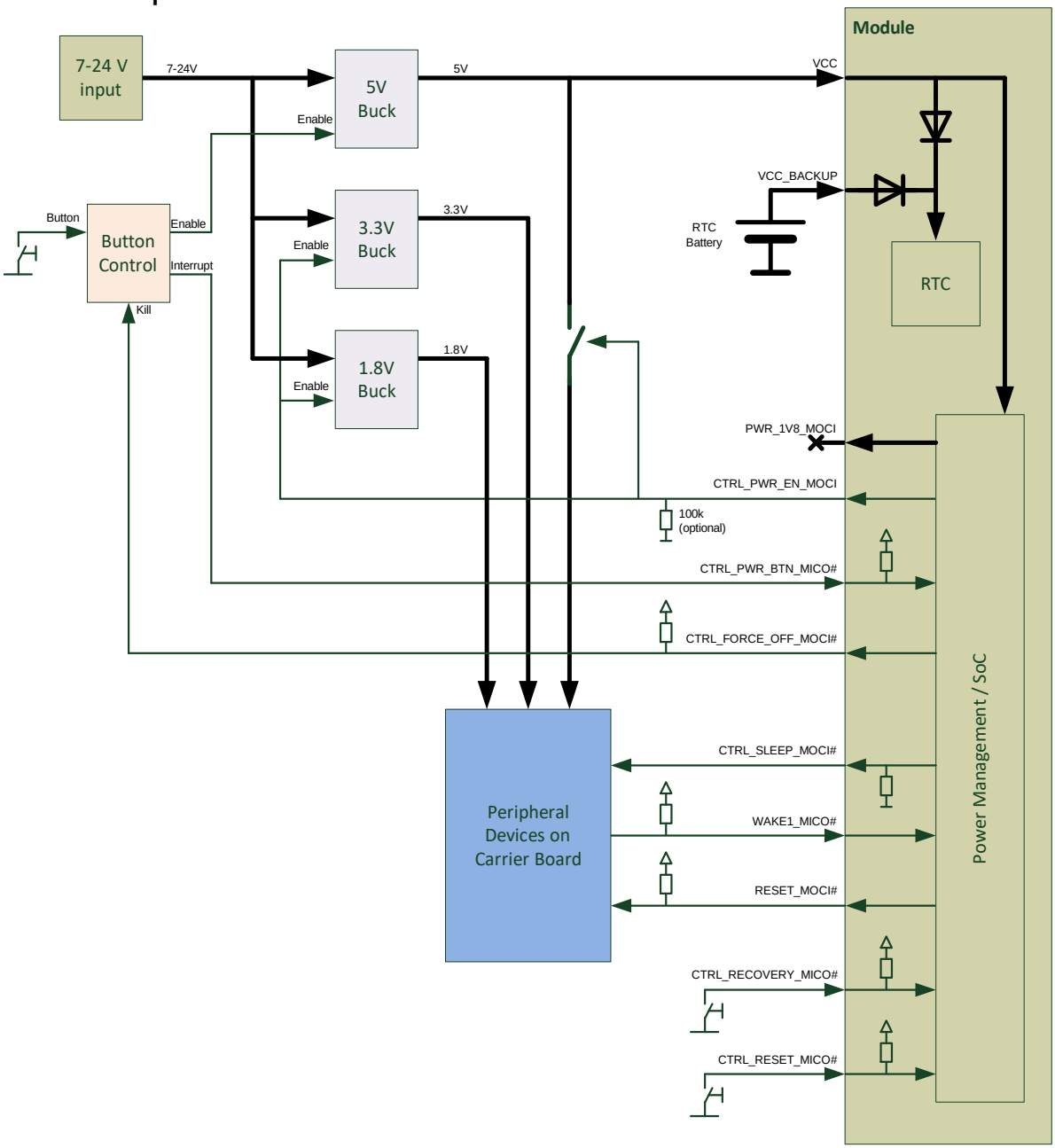


Figure 7 Verdin Development Power Supply Block Diagram

On the Verdin Development Board, the module gets powered from a 5V buck regulator. This regulator is enabled by a button control IC. Short pressing the power button will enable the 5V buck regulator, which powers up the Verdin module. The Verdin module then enables the carrier board's peripheral power rails by asserting the CTRL_PWR_EN_MOCI signal.

If the module is running, a short pressing of the power button will generate an interrupt output at the power button control IC. This interrupt is connected to the CTRL_PWR_BTN_MICO# input of the module. A falling edge on this input will cause a software interrupt. Depending on the configuration, the OS will then start shutting down the software and ramping down power rails on the module. The module asserts the CTRL_FORCE_OFF_MOCI# signal, which kills the enable output of the power button control IC. This disables the main 5V rail.

If the module is running, a long pressing of the power button (>5s) generates an emergency power shutdown of the system. The power button control IC is forwarding the long press event to the CTRL_PWR_BTN_MICO# input of the module PMIC. The PMIC is shutting down all power rails

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without software interaction. In the end, the CTRL_FORCE_OFF# is asserted, which turns off the main 5V regulator.

Minimalistic Carrier Board Power Supply Use Case

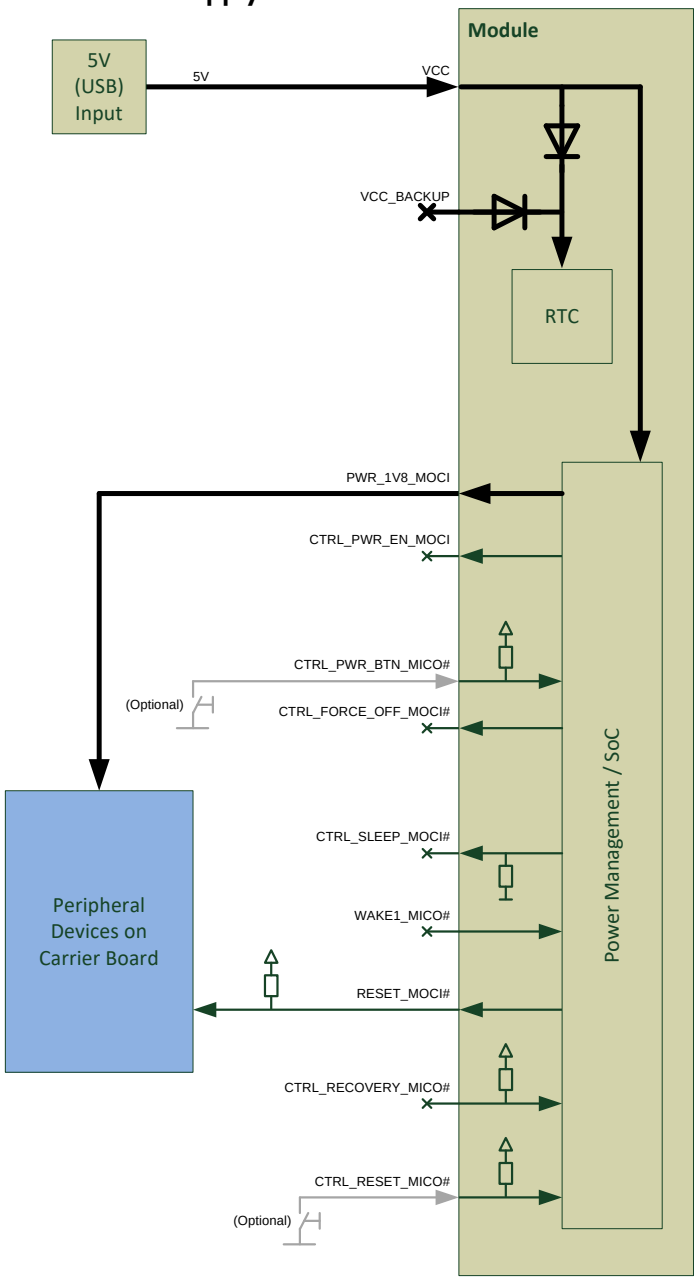


Figure 8 Minimalistic Power Supply Block Diagram

The Verdin module can run directly from any power source between 3.135V and 5.5V. This means the module can run directly from a 5V USB power port. As soon as the main power is plugged in, the module starts to ramp up all the voltages and boots. The PWR_1V8_MOCI can deliver up to 250mA for peripherals on the carrier board.

Optional, a simple push-button can be added to the CTRL_PWR_BTN_MICO# and the CTRL_RESET_MICO# input. Short pressing the power button when the system is booted, a software interrupt is generated. Depending on the configuration, the OS will start shutting down the software and ramping down power rails on the module (including the PWR_1V8_MOCI). In this off-state, the system can be turned on by pressing the power button again.

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A long pressing on the power button (>5s) initiates an emergency power shutdown. All power rails will be turned off. The module can be turned back on by using the power button.

Single Cell Battery Powered Use Case

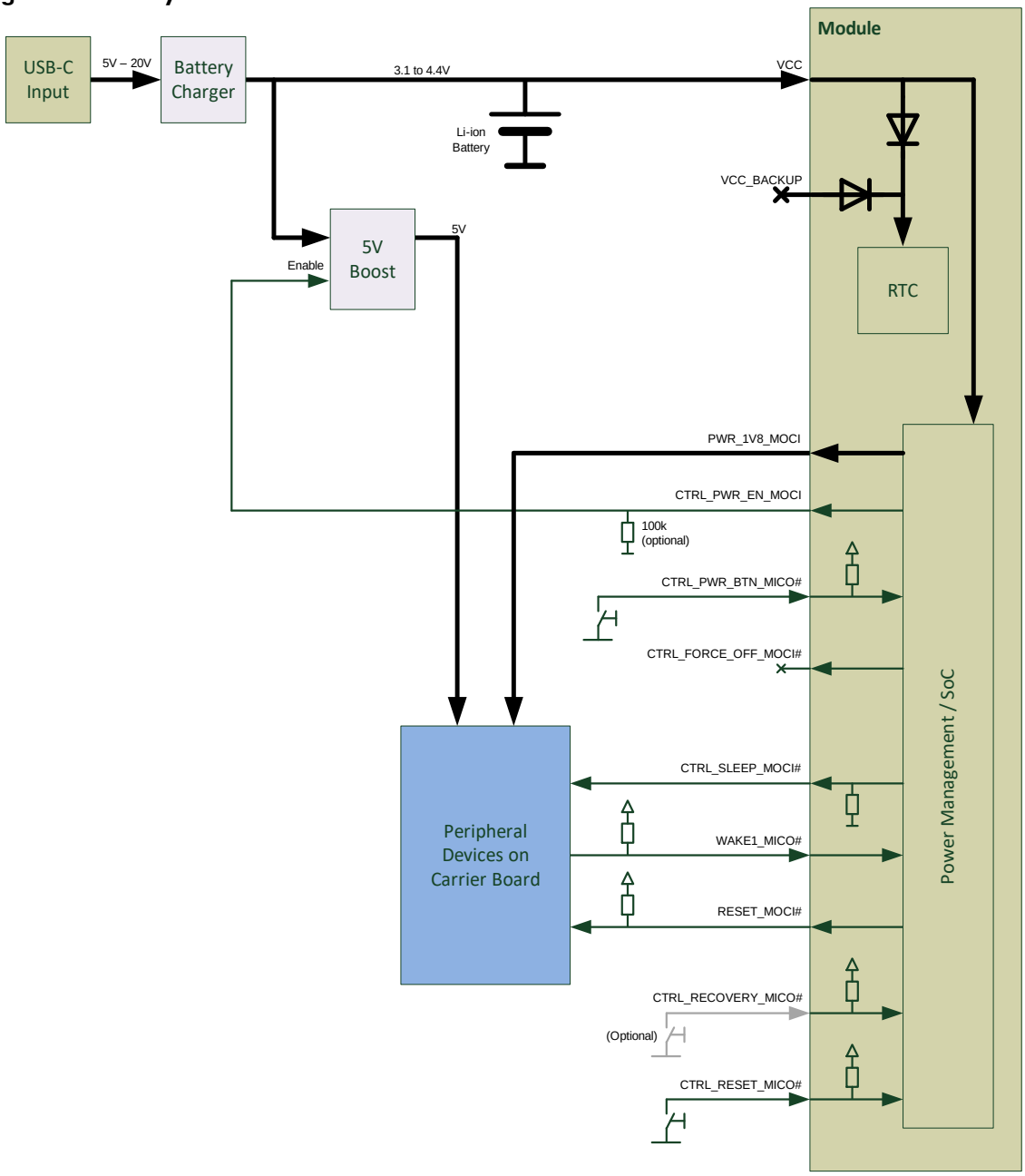


Figure 9 Single Cell Battery Power Supply Block Diagram

The wide input voltage range of the Verdin module allows it to run directly from a single cell Li-ion battery. If any buck or boost regulators are required for the peripherals on the carrier board, make sure they can also run from the voltage range of the battery system. The external regulators can be enabled by using the CTRL_PWR_EN_MOC signal.

The simple push-button on the CTRL_PWRBTN_MICO# input can be used to turn on the module, create software interrupts (short pressing), or initiate an emergency power off (long pressing).

The CTRL_SLEEP_MOCI# signal can be used to turn off peripheral rails that are not used while the system is in low power mode to save battery. The WAKE1_MICO# input can be used for waking up the system from sleep modes. Alternatively, the power button can also be used for generating a wake event.

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5.2 GPIOs

The Verdin form factor features ten dedicated general-purpose input-output (GPIO) pins. Four are reserved for the MIPI CSI camera interface and two for the MIPI DSI display interface. Besides these 10 GPIOs, several pins can be used as GPIO if their primary function is not used. For compatibility reasons, it is recommended to use the ten dedicated GPIOs first.

Table 5-4 Dedicated GPIO signals

X1 Pin#	Verdin Standard Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
206	GPIO_1	GPIO1_IO00	GPIO1_IO0	I/O	
208	GPIO_2	GPIO1_IO01	GPIO1_IO1	I/O	
210	GPIO_3	GPIO1_IO05	GPIO1_IO5	I/O	
212	GPIO_4	GPIO1_IO06	GPIO1_IO6	I/O	
216	GPIO_5_CSI	GPIO1_IO07	GPIO1_IO7	I/O	Reserved general-purpose IO for MIPI CSI camera interface
218	GPIO_6_CSI	GPIO1_IO08	GPIO1_IO8	I/O	
220	GPIO_7_CSI	SAI1_RXD1	GPIO4_IO3	I/O	
222	GPIO_8_CSI	SAI1_RXC	GPIO4_IO1	I/O	
17	GPIO_9_DSI	SAI2_TXC	GPIO4_IO25	I/O	Reserved general-purpose IO for MIPI DSI display interface
21	GPIO_10_DSI	SAI3_RXFS	GPIO4_IO28	I/O	

5.2.1 Wakeup Source

In principle, all GPIOs can be used to wake up the Verdin iMX8M Plus module from a suspended state. In the Verdin module standard, pin 252 is the default wakeup source. Only this pin is guaranteed to be wakeup compatible with other Verdin modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Verdin modules.

Table 5-5 Verdin Wakeup Source

X1 Pin#	Verdin Standard Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
252	CTRL_WAKE1_MICO#	SAI1_RXFS	GPIO4_IO0	I/O	Standard external wake signal

5.3 Ethernet

In the Verdin module standard, there are two Ethernet ports. One port is a 10/100/1000 Mbit media-dependent interface. This interface has the Ethernet PHY on the module. The second port is a gigabit media independent interface (RGMII). The two Ethernet MAC that the i.MX 8M Plus SoC provides are slightly different. Both Ethernet controllers support Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588. Only one Ethernet controller features additional Time-Sensitive Networking (TSN). This controller is used for the on-module Gigabit Ethernet PHY, the Microchip KSZ9131. The second Ethernet controller (without TSN) is available as an RGMII interface on the module edge connector pins.

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Table 5-6 Media Dependent Ethernet Pins

X1 Pin #	Verdin Signal Name	KSZ9131 Signal Name	I/O	Description	Remarks
225	ETH_1_MDI0_P	TXRXP_A	I/O	Media Dependent Interface	
227	ETH_1_MDI0_N	TXRXM_A	I/O	Media Dependent Interface	
233	ETH_1_MDI1_P	TXRXP_B	I/O	Media Dependent Interface	
231	ETH_1_MDI1_N	TXRXM_B	I/O	Media Dependent Interface	
239	ETH_1_MDI2_P	TXRXP_C	I/O	Media Dependent Interface	
241	ETH_1_MDI2_N	TXRXM_C	I/O	Media Dependent Interface	
247	ETH_1_MDI3_P	TXRXP_D	I/O	Media Dependent Interface	
245	ETH_1_MDI3_N	TXRXM_D	I/O	Media Dependent Interface	
237	ETH_1_LED_2	LED2	O	LED indication output	Is low if a link (any speed) is established
235	ETH_1_LED_1	LED1	O	LED indication output	Toggles during RX/TX activity

If only fast Ethernet is required, 10/100Mbit magnetics providing only two lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

The Gigabit Ethernet MAC in the SoC integrates an accurate IEEE 1588 compliant timer for clock synchronization for distributed control nodes used in industrial automation applications. The interface features external IEEE 1588 synchronization pins on alternate functions. The Ethernet interface supports Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN).

The KSZ9131 INT# signal (pin 38) is connected to the GPIO1_IO10 ball of the i.MX 8M Plus SoC.

Table 5-7 IEEE 1588 Signals (alternate functions, not compatible with other Verdin modules)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
218	GPIO_6_CSI	GPIO1_IO08	ENET_QOS_1588_EVENT0_IN	I	IEEE 1588 input capture signal for first Ethernet MAC with on-module PHY
55	I2C_2_DSI_SCL	I2C2_SCL	ENET_QOS_1588_EVENT1_IN	I	
24	CAN_2_TX	SAI2_TXD0	ENET_QOS_1588_EVENT2_IN	I	
26	CAN_2_RX	SAI2_MCLK	ENET_QOS_1588_EVENT3_IN	I	
218	GPIO_6_CSI	GPIO1_IO08	ENET_QOS_1588_EVENT0_AUX_IN	I	IEEE 1588 auxiliary input signal for first Ethernet MAC with on-module PHY
55	I2C_2_DSI_SCL	I2C2_SCL	ENET_QOS_1588_EVENT1_AUX_IN	I	
24	CAN_2_TX	SAI2_TXD0	ENET_QOS_1588_EVENT2_AUX_IN	I	
26	CAN_2_RX	SAI2_MCLK	ENET_QOS_1588_EVENT3_AUX_IN	I	
53	I2C_2_DSI_SDA	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT	O	IEEE 1588 output compare for first Ethernet MAC with on-module PHY
135	UART_1_CTS	SAI2_RXD0	ENET_QOS_1588_EVENT2_OUT	O	
133	UART_1_RTS	SAI2_TXFS	ENET_QOS_1588_EVENT3_OUT	O	

The signals of the second Ethernet MAC are available on the module edge connector as RGMII signals. This allows having a second (specialized) Ethernet PHY on the carrier board for dual Ethernet applications. The RGMII signals are available on the "*Reserved*" Verdin pins.

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Table 5-8 RGMII signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
199	ETH_2_RGMII_RX_CTL	SAI1_TXFS	ENET1_RGMII_RX_CTL	I	RGMII_RX_CTL
197	ETH_2_RGMII_RXC	SAI1_TXC	ENET1_RGMII_RXC	I	RGMII_RXC
201	ETH_2_RGMII_RXD_0	SAI1_RXD4	ENET1_RGMII_RD0	I	RGMII_RXD0
203	ETH_2_RGMII_RXD_1	SAI1_RXD5	ENET1_RGMII_RD1	I	RGMII_RXD1
205	ETH_2_RGMII_RXD_2	SAI1_RXD6	ENET1_RGMII_RD2	I	RGMII_RXD2
207	ETH_2_RGMII_RXD_3	SAI1_RXD7	ENET1_RGMII_RD3	I	RGMII_RXD3
211	ETH_2_RGMII_TX_CTL	SAI1_TXD4	ENET1_RGMII_TX_CTL	O	RGMII_TX_CTL
213	ETH_2_RGMII_TXC	SAI1_TXD5	ENET1_RGMII_TXC	O	RGMII_TXC
221	ETH_2_RGMII_TXD_0	SAI1_TXD0	ENET1_RGMII_TD0	O	RGMII_TXD0
219	ETH_2_RGMII_TXD_1	SAI1_TXD1	ENET1_RGMII_TD1	O	RGMII_TXD1
217	ETH_2_RGMII_TXD_2	SAI1_TXD2	ENET1_RGMII_TD2	O	RGMII_TXD2
215	ETH_2_RGMII_TXD_3	SAI1_TXD3	ENET1_RGMII_TD3	O	RGMII_TXD3
193	ETH_2_RGMII_MDC	SAI1_RXD2	ENET1_MDC	O	RGMII_MDC
191	ETH_2_RGMII_MDIO	SAI1_RXD3	ENET1_MDIO	I/O	RGMII_MDIO
189	ETH_2_RGMII_INT#	SAI1_TXD6	GPIO4_IO18	I	Control interrupt input

The second Ethernet interface could also be used as an RMII interface for a 10/100 Mbit/s PHY. However, this format is not in the Verdin standard. This means that the mapping of the signals is not guaranteed to be compatible with other modules. If compatibility with other Verdin modules is required, the RGMII mapping is the preferred interface mode.

Table 5-9 RMII signals (alternate functions, not compatible with other Verdin modules)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
201	ETH_2_RGMII_RXD_0	SAI1_RXD4	ENET1_RGMII_RD0	I	RMII_RXD0
203	ETH_2_RGMII_RXD_1	SAI1_RXD5	ENET1_RGMII_RD1	I	RMII_RXD1
189	ETH_2_RGMII_INT#	SAI1_TXD6	ENET1_RX_ER	I	RMII_RXER
221	ETH_2_RGMII_TXD_0	SAI1_TXD0	ENET1_RGMII_TD0	O	RMII_TXD0
219	ETH_2_RGMII_TXD_1	SAI1_TXD1	ENET1_RGMII_TD1	O	RMII_TXD1
143	UART_2_CTS	SD1_DATA4	ENET1_RGMII_TX_CTL	O	RMII_TXEN
211	ETH_2_RGMII_TX_CTL	SAI1_TXD4			
199	ETH_2_RGMII_RX_CTL	SAI1_TXFS	ENET1_RGMII_RX_CTL	I	RMII_CRS_DV
193	ETH_2_RGMII_MDC	SAI1_RXD2	ENET1_MDC	O	RMII_MDC
191	ETH_2_RGMII_MDIO	SAI1_RXD3	ENET1_MDIO	I/O	RMII_MDIO
38	I2S_1_MCLK	SAI1_MCLK	ENET1_TX_CLK	O	50MHz Reference clock that is provided from the MAC to the PHY
38	I2S_1_MCLK	SAI1_MCLK	ENET1_TX_CLK	I	50MHz Reference clock that is provided from the PHY to the MAC
189	ETH_2_RGMII_INT#	SAI1_TXD6	GPIO4_IO18	I	RMII_INT#
141	UART_2_RTS	SD1_DATA5	ENET1_TX_ER	O	RMII_TXER (optional)
244	PCIE_1_RESET#	SAI1_TXD7			

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The second Ethernet MAC also supports IEEE 1588 for clock synchronization. There are up to four external IEEE 1588 synchronization pins on alternate functions. These pins are not compatible with other Verdin modules.

Table 5-10 IEEE 1588 Signals (alternate functions, not compatible with other Verdin modules)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
252	CTRL_WAKE1_MICO#	SAI1_RXFS	ENET1_1588_EVENT0_IN	I	IEEE 1588 input capture signal for second Ethernet MAC (RGMII/RMII)
36	I2S_1_D_IN	SAI1_RXD0	ENET1_1588_EVENT1_IN	I	
222	GPIO_8_CSI	SAI1_RXC	ENET1_1588_EVENT0_OUT	O	IEEE 1588 output compare for second Ethernet MAC (RGMII/RMII)
220	GPIO_7_CSI	SAI1_RXD1	ENET1_1588_EVENT1_OUT	O	

5.4 Wi-Fi and Bluetooth

The Verdin iMX8M Plus is available with optional on-module Wi-Fi and Bluetooth interfaces. The addition of "WB" in the product name indicates that a version features Wi-Fi and Bluetooth. These Verdin module versions make use of the AW-CM276NF Dual-Band Wi-Fi and Bluetooth module from AzureWave.

Features:

- Wi-Fi 802.11a/b/g/n/ac
- Dual-Band 5 GHz and 2.4GHz
- Up to 866.7 Mbps
- 20/40/80 MHz channel bandwidth
- Station/Client Mode, Access Point Mode, Wi-Fi- Direct Mode, and Simultaneous Station and Access point mode
- Bluetooth 5.0 (BR/EDR), BLE
- Murata HSC (MXHP32) connector for the dual external antenna in 2x2 configuration, compatible to IPX/IPEX connector MHF4 series
- Pre-certified for CE (Europe), FCC (United States), IC (Canada), TELEC (Japan), and WPC (India). See https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products

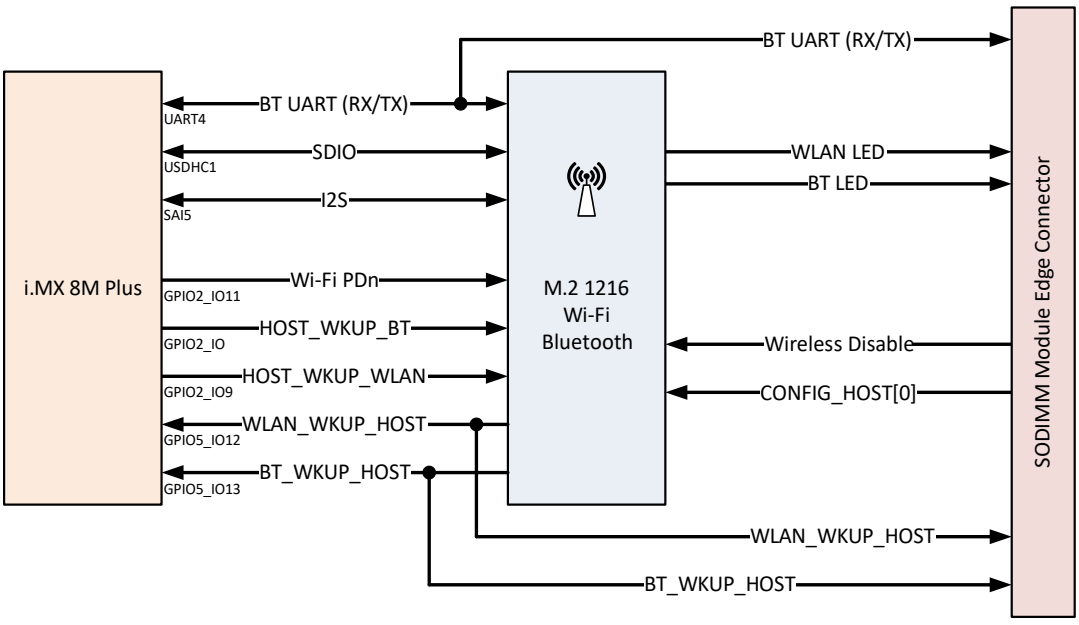


Figure 10: Wi-Fi and Bluetooth block diagram

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The Wi-Fi module is connected over a 4-bit SDIO interface with the i.MX 8M Plus SoC. It uses the USDHC1 instance of the SoC. For Bluetooth Audio, an additional I2S interface is available between the SoC and the Wi-Fi module, which uses the SAI5 instance of the SoC. The RX and TX signals of the Bluetooth UART interface are connected to an alternate location of the UART4 of the SoC. This interface can only be used if the Verdin standard UART_4 is not in use. Bluetooth UART pins are also available on the module edge connector. Using Bluetooth Audio and Bluetooth UART requires a different firmware for the AzureWave module, which is not provided in the default BSP.

Table 5-11 Signal Pins between AW-CM276NF and i.MX 8M Plus

AW-CM276NF Pin Name	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
SD_CMD	SD1_CLK	USDHC1_CLK	I/O	4-bit SDIO interface for Wi-Fi and Bluetooth
SD_DAT[0]	SD1_DATA0	USDHC1_DATA0	I/O	
SD_DAT[1]	SD1_DATA1	USDHC1_DATA1	I/O	
SD_DAT[2]	SD1_DATA2	USDHC1_DATA2	I/O	
SD_DAT[3]	SD1_DATA3	USDHC1_DATA3	I/O	
SD_CLK	SD1_CMD	USDHC1_CMD	I	
GPIO[6]/PCM_CLK	SAI5_RXD2	SAI5_TX_BCLK	I	I^2S interface for Bluetooth audio
GPIO[7]/PCM_SYNC	SAI2_RXFS	SAI5_TX_SYNC	I	
GPIO[4]/PCM_DIN	SAI5_RXD3	SAI5_TX_DATA0	I	
GPIO[5]/PCM_DOUT	SAI5_RXD0	SAI5_RX_DATA0	O	
GPIO[15]/ TMS/ Host Wake WLAN	SD1_DATA7	GPIO2_IO9	I	HOST_WKUP_WLAN : SoC to AW-CM276NF Wi-Fi Wakeup
GPIO[12]/ UART Host Wake BT	SD1_DATA6	GPIO2_IO8	I	HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup
GPIO[14]/TCK/ WLAN Wake Host	ECSPI2_MISO	GPIO5_IO12	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output, the signal is also available on the SODIMM connector
GPIO[13]/BT IRQ(O)	ECSPI2_SS0	GPIO5_IO13	O	BT_WKUP_HOST: AW-CM276NF Bluetooth wake output, the signal is also available on the SODIMM connector
GPIO[9]/UART_SIN	ECSPI2_MOSI	UART4_TX	I	BT UART mode: RX data, the signal is also available on the SODIMM connector
GPIO[8]/UART_SOUT	ECSPI2_SCLK	UART4_RX	O	BT UART mode: TX data, the signal is also available on the SODIMM connector
PDn	SD1_STROBE	GPIO2_IO11	I	Power Down of complete Wi-Fi/BT module (active low). Firmware needs to be re-downloaded after powering on again.

The AW-CM276NF features four wake signals of which are connected to the SoC. Two are input signals (one for the Wi-Fi and one for Bluetooth), allowing for waking up the radio. The other two signals are wake output signals (one for the Wi-Fi and one for Bluetooth) for waking up the host. These signals are connected to SoC pins and are available on the SODIMM connector. The actually available sleep functions ad wake signals depend on the firmware loaded into the AzureWave module.

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Table 5-12 *"Module-specific"* Signal Pins of the AW-CM276NF on SODIMM Connector

X1 Pin#	Verdin Std Function	AW-CM276NF Pin Name	I/O	Description
116	MSP_13	GPIO[14]/TCK/ WLAN Wake Host	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output, the signal is also connected to the SoC
128	MSP_18	GPIO[13]/BT IRQ(O)	O	BT_WKUP_HOST: AW-CM276NF Bluetooth wake output, the signal is also connected to the SoC
188	MSP_43	GPIO[2]/WLAN_LED	O	Wi-Fi activity LED
176	MSP_38	GPIO[3]/BT_LED	O	Bluetooth activity LED
152	MSP_28	GPIO[9]/UART_SIN	I	BT UART mode: RX data, the signal is also connected to the SoC
164	MSP_33	GPIO[8]/UART_SOUT	O	BT UART mode: TX data, the signal is also connected to the SoC
92	MSP_3	GPIO[22]/PCIE_W_DISABLEn	I	PCIe Wireless Disable Input (active low), the pull-up resistor is on the module, can be left floating
104	MSP_8	CONFIG_HOST[0]	I	Strapping input, can be left floating. Connect to the ground for the UART Bluetooth feature (contact Toradex)

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. More information can be found on this site: https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products.

5.5 USB

Table 5-13 USB Overview

Verdin USB Port	Speed capabilities (SoC)	Role capabilities (SoC)	Speed according to Verdin standard	Role according to Verdin standard	Additional module-specific and alternate functions (non-Verdin standard)	Recovery Mode
USB_1	USB 3.1 Gen. 1	Host and client	USB 2.0	OTG (host and client)	USB SuperSpeed signals to complement the USB 2.0 signals and create a USB 3.1 Gen. 1 dual role port	Supported
USB_2	USB 3.1 Gen. 1	Host and client	USB 3.1 Gen. 1	Host-only	OTG_ID signal to complement the host-only interface and create a OTG (host, client) port	Not Supported

The i.MX 8M Plus SoC features two identical USB 2.0 ports which are both OTG capable. However, in the Verdin standard, only the USB_1 port is an OTG port, while USB_2 is only a host port. Therefore, it is recommended to use only the USB_1 as an OTG port. The USB_1 port is also used for the serial mode (recovery mode). Both USB ports of the i.MX 8M Plus SoC feature USB 3.1 Gen 1 SuperSpeed (previously called USB 3.0, backward compatible with USB 2.0). Only USB_2 supports the SuperSpeed signals required for a USB 3.1 Gen 1 capable interface in the Verdin standard. However, the SuperSpeed signals of the USB_1 interface are available on module-specific pins. The location of these SuperSpeed signals is not guaranteed to be compatible with other Verdin modules. Therefore, it is recommended for compatibility purposes to use the USB_1 only with the USB 2.0 signals.

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Table 5-14 USB_1 Interface Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
165	USB_1_D_P	USB1_D_P	USB1_D_P	I/O	Positive Differential USB Signal, OTG capable
163	USB_1_D_N	USB1_D_N	USB1_D_N	I/O	Negative Differential USB Signal, OTG capable
159	USB_1_VBUS	USB1_VBUS	USB1_VBUS	I	Use this pin to detect if VBUS is present. This pin is a 5V input.
161	USB_1_ID	USB1_ID	USB1_ID	I	Use this pin to detect the ID pin if you use the port in OTG mode.
155	USB_1_EN	GPIO1_IO12	USB1_OTG_PWR	O	This pin enables the external USB voltage supply for the USB_1 interface.
157	USB_1_OC#	GPIO1_IO13	USB1_OTG_OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USB_1 interface.
186	MSP_42	USB1_RX_P	USB1_RX_P	I	Differential receiving signal for USB SuperSpeed, **not compatible** with other Verdin modules.
184	MSP_41	USB1_RX_N	USB1_RX_N	I	
180	MSP_40	USB1_TX_P	USB1_TX_P	O	Differential transmission signal for USB SuperSpeed, **not compatible** with other Verdin modules.
178	MSP_39	USB1_TX_N	USB1_TX_N	O	

Table 5-15 USB_2 Interface Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
183	USB_2_D_P	USB2_D_P	USB2_D_P	I/O	Positive Differential USB Signal
181	USB_2_D_N	USB2_D_N	USB2_D_N	I/O	Negative Differential USB Signal
177	USB_2_SSRX_P	USB2_RX_P	USB2_RX_P	I	Differential receiving signal for USB SuperSpeed
175	USB_2_SSRX_N	USB2_RX_N	USB2_RX_N	I	
171	USB_2_SSTX_P	USB2_TX_P	USB2_TX_P	O	Differential transmission signal for USB SuperSpeed
169	USB_2_SSTX_N	USB2_TX_N	USB2_TX_N	O	
185	USB_2_EN	GPIO1_IO14	USB2_OTG_PWR	O	This pin enables the external USB voltage supply for the USB_2 interface.
187	USB_2_OC#	GPIO1_IO15	USB2_OTG_OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USB_2 interface.
16	PWM_2	GPIO1_IO11	USB2_OTG_ID	I	OTG ID pin for USB_2 port. This is not a standard pin, **not compatible** with other Verdin modules.

5.6 Display

The i.MX 8M Plus SoC features a total of three display controllers called LCDIF. One LCDIF drives the MIPI DSI interface, one the HDMI, and one the LVDS interface. As long as no more than two instances are in use simultaneously, up to 1080p60 is supported. With all three instances in use, it is possible to run one instance with 1080p60 and two instances with 720p60.

The MIPI DSI and the HDMI port are “Reserved” Verdin interfaces and therefore compatible with other Verdin modules. The LVDS is not part of the standard interfaces. These signals are located on the module-specific pins. This means using the LVDS interface can prevent compatibility with other Verdin modules. Therefore, the MIPI DSI and HDMI ports are the preferred display interfaces. If an LVDS display is used and compatibility with other Verdin modules is required, a MIPI DSI to LVDS bridge on the carrier board should be considered.

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5.6.1 Display Serial Interface (DSI)

The interface uses the MIPI D-PHY for the physical layer, compatible with the version 1.2 specifications. The maximum data transfer per lane is 1.5Gbps. Bi-directional data transmission is available on lane 0. Resolutions up 1920x1080p60 with 24-bit RGB are supported. It also supports a 10Mbps data rate for low power operation.

Table 5-16 DSI interface signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
37	DSI_1_CLK_P	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P	O	DSI Interface clock
35	DSI_1_CLK_N	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N		
49	DSI_1_D0_P	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P	I/O	DSI Interface data lane 0
47	DSI_1_D0_N	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N		
43	DSI_1_D1_P	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P	O	DSI Interface data lane 1
41	DSI_1_D1_N	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N		
31	DSI_1_D2_P	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P	O	DSI Interface data lane 2
29	DSI_1_D2_N	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N		
25	DSI_1_D3_P	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P	O	DSI Interface data lane 3
23	DSI_1_D3_N	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N		
55	I2C_2_DSI_SCL	I2C2_SCL	I2C2_SCL	O	I^2C interface, intended to be used as DDC or for controlling DSI bridges on carrier board
53	I2C_2_DSI_SDA	I2C2_SDA	I2C2_SDA	I/O	
19	PWM_3_DSI	SAI5_RXC	PWM3_OUT	O	Display backlight brightness control
21	GPIO_10_DSI	SAI3_RXFS	GPIO4_IO28	O	DSI_1_BKL_EN; Display backlight enable
17	GPIO_9_DSI	SAI2_TXC	GPIO4_IO25	I	DSI_1_INT#; Interrupt input, intended to be used as hotplug detect or for interrupt messages from DSI bridges on carrier board

5.6.2 HDMI

HDMI provides a unified method of transferring video and audio data over a TMDS compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI standard.

HDMI Features

- HDMI 2.0a up to 4K30 (3840x2160@30Hz)
- Pixel Clock from 25MHz up to 297MHz
- Supports digital sound
- CEC interface
- Enhanced Audio Return Channel (eARC), optional and not compatible with other Verdin modules.

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Table 5-17 HDMI interface signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
69	HDMI_1_TXC_P	HDMI_TXC_P	HDMI_TXC_P	O	HDMI Differential Clock
67	HDMI_1_TXC_N	HDMI_TXC_N	HDMI_TXC_N		
75	HDMI_1_TXD0_P	HDMI_TXD0_P	HDMI_TXD0_P	O	HDMI Differential Data 0
73	HDMI_1_TXD0_N	HDMI_TXD0_N	HDMI_TXD0_N		
81	HDMI_1_TXD1_P	HDMI_TXD1_P	HDMI_TXD1_P	O	HDMI Differential Data 1
79	HDMI_1_TXD1_N	HDMI_TXD1_N	HDMI_TXD1_N		
87	HDMI_1_TXD2_P	HDMI_TXD2_P	HDMI_TXD2_P	O	HDMI Differential Data 2
85	HDMI_1_TXD2_N	HDMI_TXD2_N	HDMI_TXD2_N		
59	I2C_3_HDMI_SCL	HDMI_DDC_SCL	HDMI_SCL	O	Dedicated I^2C interface, intended to be used as DDC
57	I2C_3_HDMI_SDA	HDMI_DDC_SDA	HDMI_SDA	I/O	
63	HDMI_1_CEC	HDMI_CEC	HDMI_CEC	I/O	HDMI Consumer Electronic Control.
61	HDMI_1_HPD	HDMI_HPD	HDMI_HPD	I	Hot Plug Detect
192	MSP_45	EARC_P_UTIL	EARC_P_UTIL	I	Enhanced Audio Return Channel, not a standard Verdin interface. Therefore, not compatible with other Verdin modules.
190	MSP_44	EARC_N_HPD	EARC_N_HPD		

5.6.3 LVDS

The official name for the LVDS interface is actually FPD-Link or FlatLink, which uses the low voltage differential signaling (LVDS) technology. However, very often, this interface is simply called LVDS.

The LVDS interface serializes the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to Seven parallel signals. For an 18-bit RGB interface, including the control signals (Display Enable, Vertical, and Horizontal Sync), each FPD_Link/FlatLink channel requires three LVDS data pairs. The additional color bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two color-mapping standards for the 24-bit interface. The less common “24-bit / 18-bit compatible” (JEIDA format, Intel 24.0 LVDS data format) standard packs the two low significant bits of each color into the fourth LVDS pair. This standard is backward compatible with the 18-bit mode. It is possible to connect an 18-bit display to a 24-bit interface or vice versa. The more common 24-bit color mapping standard (VESA format, Intel 24.1 LVDS data format) serializes the two most significant bits of each color into the fourth LVDS pair. This mode is not backward-compatible. Therefore, only 24-bit displays can be connected to a 24-bit host with this color mapping. The LVDS interfaces of Verdin iMX8M Plus are configurable to support different color mappings and depths. This ensures compatibility with 18-bit and 24-bit displays with both kinds of color mappings.

Figure 11 shows the LVDS output signals for the “24-bit /18-bit Compatible Color Mapping” (JEIDA format, Intel 24.0 LVDS data format)

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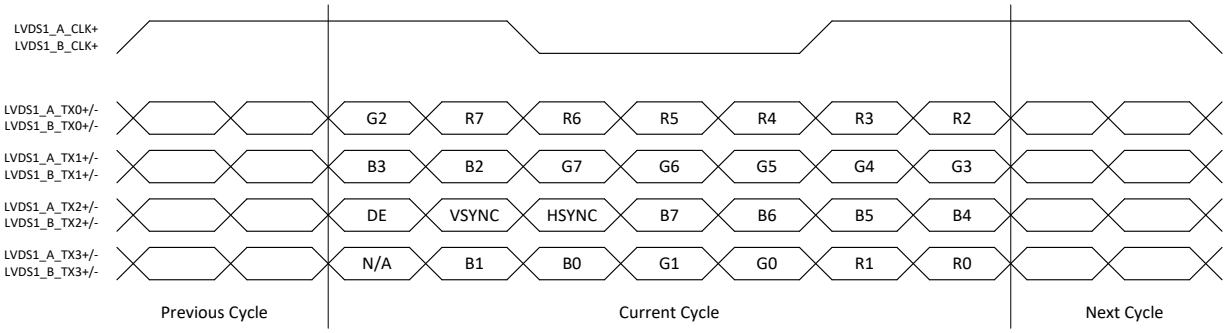


Figure 11: 24-bit / 18-bit Compatible Color Mapping (Intel 24.0 LVDS Data Format)

Figure 12 shows the LVDS output signals for the common 24-bit color mapping (VESA format, Intel 24.1 LVDS data format).

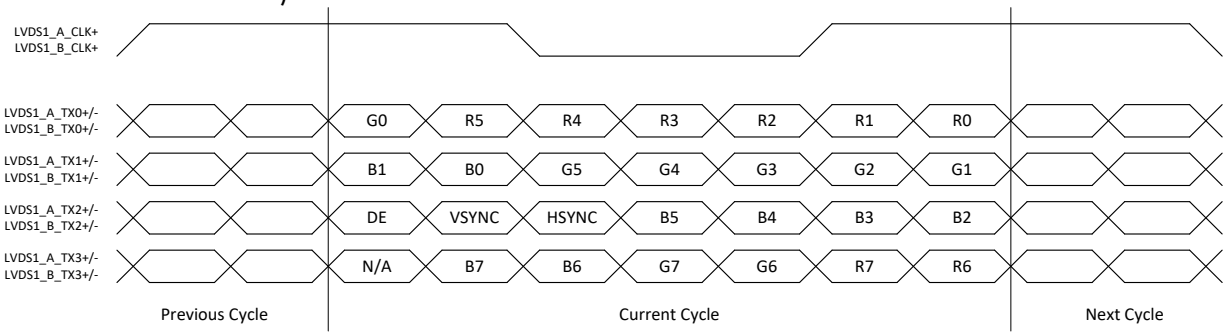


Figure 12: Common 24-bit VESA Color Mapping (Intel 24.1 LVDS Data Format)

Figure 13 shows the LVDS output signals for the 18-bit interface.

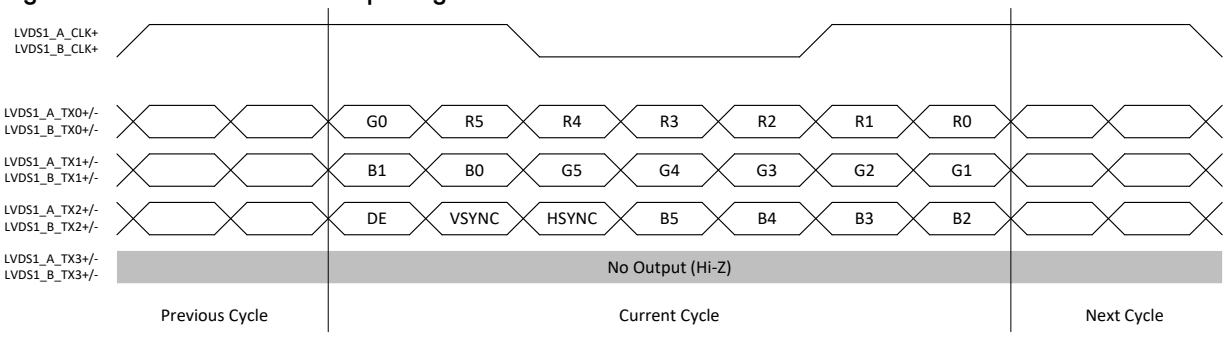


Figure 13: 18-bit Mode

A single channel LVDS interface can support resolutions up to 1366x768 pixels @60 frames per second (80MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual-channel configuration, the odd bits are transmitted in the first channel, and the even bits are sent in the second channel. The dual-channel LVDS interface can support resolutions up to 1920x1080 @60fps (160MHz pixel clock maximum).

The i.MX 8M Plus SoC features one LVDS interface that can be configured for a single or dual-channel with 18 and 24-bit. The LVDS signals are on module-specific pins. Therefore, they are not guaranteed to be compatible with other Verdin modules. If compatibility between different Verdin modules is required, a MIPI DSI to LVDS bridge IC on the carrier board should be considered.

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Table 5-18 LVDS interface signals (not compatible with other Verdin modules)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
90	MSP_2	LVDS0_CLK_P	LVDS0_CLK_P	O	LVDS Clock out for channel 0 (odd pixels/single channel)
88	MSP_1	LVDS0_CLK_N	LVDS0_CLK_N		
96	MSP_5	LVDS0_D0_P	LVDS0_D0_P	O	LVDS data lane 0 for channel 0 (odd pixels/single channel)
94	MSP_4	LVDS0_D0_N	LVDS0_D0_N		
102	MSP_7	LVDS0_D1_P	LVDS0_D1_P	O	LVDS data lane 1 for channel 0 (odd pixels/single channel)
100	MSP_6	LVDS0_D1_N	LVDS0_D1_N		
108	MSP_10	LVDS0_D2_P	LVDS0_D2_P	O	LVDS data lane 2 for channel 0 (odd pixels/single channel)
106	MSP_9	LVDS0_D2_N	LVDS0_D2_N		
114	MSP_12	LVDS0_D3_P	LVDS0_D3_P	O	LVDS data lane 3 for channel 0 (odd pixels/single channel; unused for 18-bit)
112	MSP_11	LVDS0_D3_N	LVDS0_D3_N		
120	MSP_15	LVDS1_CLK_P	LVDS1_CLK_P	O	LVDS Clock out for channel 1 (even pixels/unused for single channel)
118	MSP_14	LVDS1_CLK_N	LVDS1_CLK_N		
126	MSP_17	LVDS1_D0_P	LVDS1_D0_P	O	LVDS data lane 0 for channel 1 (odd pixels/unused for single channel)
124	MSP_16	LVDS1_D0_N	LVDS1_D0_N		
132	MSP_20	LVDS1_D1_P	LVDS1_D1_P	O	LVDS data lane 1 for channel 1 (odd pixels/unused for single channel)
130	MSP_19	LVDS1_D1_N	LVDS1_D1_N		
138	MSP_22	LVDS1_D2_P	LVDS1_D2_P	O	LVDS data lane 2 for channel 1 (odd pixels/unused for single channel)
136	MSP_21	LVDS1_D2_N	LVDS1_D2_N		
144	MSP_25	LVDS1_D3_P	LVDS1_D3_P	O	LVDS data lane 3 for channel 1 (odd pixels/unused for single channel; unused for 18-bit)
142	MSP_24	LVDS1_D3_N	LVDS1_D3_N		

5.7 Camera Interface

The NXP i.MX 8M Plus supports two quad lane MIPI CSI-2 interfaces for connecting compatible cameras. The interface is compatible with single, dual, and quad lane CSI cameras. The interface uses MIPI D-PHY as the physical layer. The interface supports RGB, YUV, and RAW color space definitions. One MIPI CSI-2 interface is in the *"Reserved"* class of the Verdin specifications. This instance is compatible with other Verdin modules and, therefore, the preferred one. The second CSI-2 interface is located on module-specific pins. Compatibility with other Verdin modules is not guaranteed for these pins.

Features

- Scalable data lane support, 1 to 4 Data Lanes
- MIPI CSI-2 specification V1.3 (except for the C-PHY feature)
- MIPI D-PHY specification V1.2
- Unidirectional master operation supported
- Supported primary and secondary image format: YUV420, YUV420 (legacy), YUV420 (CSPS), YUV 422 (8-bit and 10-bit), RGB565, RGB666, RGB888, RAW6, RAW7, RAW8, RAW10, RAW12, and RAW14
- User-defined byte-based data packet supported

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Table 5-19 MIPI CSI-2 interface signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	CSI Signal Name	I/O	Description
111	CSI_1_CLK_P	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P	I	CSI interface clock
113	CSI_1_CLK_N	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N		
123	CSI_1_D0_P	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P	I/O	CSI interface data lane 0
125	CSI_1_D0_N	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N		
117	CSI_1_D1_P	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P	I	CSI interface data lane 1
119	CSI_1_D1_N	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N		
105	CSI_1_D2_P	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P	I	CSI interface data lane 2
107	CSI_1_D2_N	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N		
99	CSI_1_D3_P	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P	I	CSI interface data lane 3
101	CSI_1_D3_N	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N		

In addition to the MIPI CSI-2 interface pins, the Verdin offers a dedicated I²C interface and a master clock output for the camera. Unfortunately, the iMX8M Plus MIPI CSI IP does not provide a dedicated clock. Thus, a master clock signal from the digital audio interface is provided on the module edge connector at pin 91. The clock source can be selected from either the SAI3 or SAI5 interface. Please carefully check whether the required signal is available from the SAI master clock and is not in conflict with any other digital audio interface. To reduce EMC and simplify software design, it is recommended to generate the master clock on the carrier board or camera.

Table 5-20 Additional Camera Interface Signals

X1 Pin#	Verdin Signal Name	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
95	I2C_4_CSI_SCL	I2C3_SCL	I2C3_SCL	I/O	Camera control I²C
93	I2C_4_CSI_SDA	I2C3_SDA	I2C3_SDA	O	
91	CSI_1_MCLK	SAI3_MCLK	SAI3_MCLK	O	Camera master clock. Source: audio master clock of SAI5 or SAI3
			SAI5_MCLK		
216	GPIO_5_CSI	GPIO1_IO07	GPIO1_IO7	I/O	Dedicated camera GPIO signals.
218	GPIO_6_CSI	GPIO1_IO08	GPIO1_IO8	I/O	
220	GPIO_7_CSI	SAI1_RXD1	GPIO4_IO3	I/O	
222	GPIO_8_CSI	SAI1_RXC	GPIO4_IO1	I/O	

The second MIPI CSI-2 interface is available on module-specific pins that are not guaranteed to be compatible with other Verdin modules.

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Table 5-21 Second MIPI CSI-2 interface signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	CSI Signal Name	I/O	Description
162	MSP_32	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P	I	CSI interface clock
160	MSP_31	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N		
150	MSP_27	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P	I/O	CSI interface data lane 0
148	MSP_26	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N		
156	MSP_30	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P	I	CSI interface data lane 1
154	MSP_29	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N		
168	MSP_35	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P	I	CSI interface data lane 2
166	MSP_34	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N		
174	MSP_37	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P	I	CSI interface data lane 3
172	MSP_36	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N		

5.8 PCI Express

The NXP i.MX 8M Plus features a single-lane PCI Express (PCIe) interface. The PCIe interface is compliant with the PCIe 3.0 base specifications and supports up to 8Gb/s data rate (Gen3). It is backward-compatible with previous standards that support 5Gb/s (Gen2) and 2.5Gb/s (Gen1).

The 100MHz PCIe reference clock is generated by the SoC and is made available for the peripherals over the module edge connector pins. All the required source termination for the reference clock is on the Verdin module.

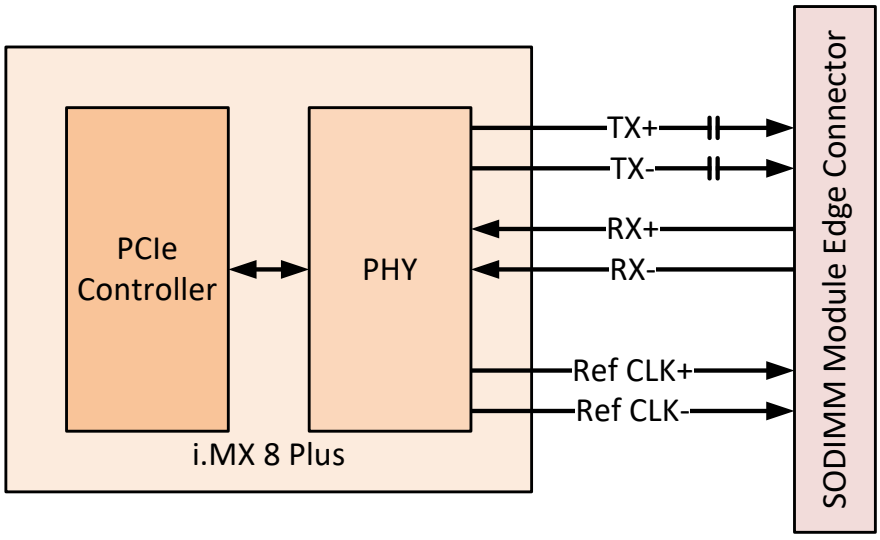


Figure 14: PCIe block diagram

PCIe is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Verdin Carrier Board Design Guide and Layout Design Guide for more information.

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Table 5-22 PCIe Interface Signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
228	PCIE_1_CLK_P	PCIE_REF_PAD_CLK_P	PCIE1_REF_PAD_CLK_P	O	100MHz reference clock differential pair. Sourced by a reference clock oscillator
226	PCIE_1_CLK_N	PCIE_REF_PAD_CLK_N	PCIE1_REF_PAD_CLK_N		
240	PCIE_1_L0_TX_P	PCIE_TXN_P	PCIE1_TXN_P	O	Transmit data lane 0
238	PCIE_1_L0_TX_N	PCIE_TXN_N	PCIE1_TXN_N		
234	PCIE_1_L0_RX_P	PCIE_RXN_P	PCIE1_RXN_P	I	Receive data lane 0
232	PCIE_1_L0_RX_N	PCIE_RXN_N	PCIE1_RXN_N		
244	PCIE_1_RESET#	SAI1_TXD7	GPIO4_IO19	O	Dedicated reset output for PCIe

5.9 I²C

The NXP i.MX 8M Plus SoC features six I²C controllers, five of which can be used externally. They implement the I²C V2.1 specification. The port I2C1 is used for the on-module PMIC, RTC, EEPROM, Secure Element, and ADC and is therefore not available externally.

All five externally available I²C can be used for general-purpose applications. However, the Verdin standard dedicates three of them for use with the MIPI CSI-2 camera input, the MIPI DSI display output, and the HDMI output. These three interfaces are in the *"Reserved"* category. There is a proper general-purpose I²C port in the *"Always Compatible"* category. The fifth I²C port is only available as an alternate function of other pins. Therefore, this interface is not compatible with other Verdin modules.

The Verdin I2C_3_HDMI port is dedicated to the HDMI interface. The SoC pins that are connected to these module edge pins have two compatible multiplexing options. There is a dedicated HDMI_DDC interface available, as well as a general-purpose I²C interface (I2C5 instance). Depending on the HDMI driver, the dedicated HDMI_DDC or the general-purpose I²C is used. If the dedicated HDMI_DDC is in use, the I2C5 port could be used on other module edge pins that offer the I2C5 as an alternate function. However, this configuration is not compatible with other Verdin modules.

There are many low-speed devices that use I²C interfaces such as RTCs and sensors, but it is also commonly used to configure other devices such as cameras or displays. The I²C Bus can also be used to communicate with SMB (System Management Bus) devices.

Table 5-23 Verdin standard I²C Signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I2C Port	Description
14	I2C_1_SCL	I2C4_SCL	I2C4_SCL	I2C4	Generic I²C
12	I2C_1_SDA	I2C4_SDA	I2C4_SDA		
55	I2C_2_DSI_SCL	I2C2_SCL	I2C2_SCL	I2C2	I²C port for the DSI interface. Intended to be used as DDC or for controlling DSI bridges on the carrier board.
53	I2C_2_DSI_SDA	I2C2_SDA	I2C2_SDA		
59	I2C_3_HDMI_SCL	HDMI_DDC_SCL	I2C5_SCL	I2C5	Dedicated DDC port for HDMI. I2C5 or HDMI_DDC is available on these pins
57	I2C_3_HDMI_SDA	HDMI_DDC_SDA	I2C5_SDA		
95	I2C_4_CSI_SCL	I2C3_SCL	I2C3_SCL	I2C4	I²C port for the camera interface
93	I2C_4_CSI_SDA	I2C3_SDA	I2C3_SDA		

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Table 5-24 Additional I²C Signal Pins (not compatible with other Verdin modules)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I2C Port	Description
82	SD_1_D1	SD2_DATA1	I2C4_SCL	I2C4	Alternate pins for the I2C4 port
116	MSP_13	ECSPI2_MISO			
60	QSPI_1_IO2	NAND_DATA02	I2C4_SDA		
80	SD_1_D0	SD2_DATA0			
128	MSP_18	ECSPI2_SS0			
198	SPI_1_MISO	ECSPI1_MISO	I2C2_SCL	I2C2	Alternate pins for the I2C2 port
202	SPI_1_CS	ECSPI1_SS0	I2C2_SDA		
20	CAN_1_TX	SPDIF_TX	I2C5_SCL	I2C5	Alternate pins for the I2C5 port
22	CAN_1_RX	SPDIF_RX	I2C5_SDA		
30	I2S_1_BCLK	SAI5_MCLK			
64	QSPI_1_CS2#	NAND_READY_B	I2C3_SCL	I2C3	Alternate pins for the I2C3 port
66	QSPI_1_DQS	NAND_DQS			
164	MSP_33	ECSPI2_SCLK			
152	MSP_28	ECSPI2_MOSI	I2C3_SDA		
34	I2S_1_D_OUT	SAI5_RXFS	I2C6_SCL	I2C6	Additional I2C6 port
63	HDMI_1_CEC	HDMI_CEC			
151	UART_4_RXD	UART4_RXD			
19	PWM_3_DSI	SAI5_RXC	I2C6_SDA		
61	HDMI_1_HPD	HDMI_HPD			
153	UART_4_TXD	UART4_TXD			

5.9.1 Real-Time Clock (RTC)

The Verdin iMX8M Plus module features an RTC IC on the module. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for timekeeping. If the main power supply is provided to the module, the RTC is sourced from this rail. However, If the RTC needs to be retained even without the module's main voltage, a coin cell must be applied to the VCC_BACKUP (pin 249) supply pin.

5.10 UART

The i.MX 8MP SoC features a total of four UARTs. In the Verdin module specifications, there are four standard UARTs available. UART_1 and UART_2 are general-purpose interfaces. Only the RX and TX signals of these interfaces are in the *"Always Compatible"* section. In contrast, the additional RTS/CTS signals for hardware flow control are located in the *"Reserved"* section.

UART_3 is in the *"Always Compatible"* section and is intended to be used for the main OS terminal (A53 cores) as a debug port. It could be used for general-purpose, but we recommend making this interface available for debugging purposes. UART_4 is in the *"Reserved"* class. This interface is intended to be used for the real-time operating system (M7 core). The interface may be used as a general-purpose UART.

The UARTs of the i.MX 8MP SoC can be configured either in the DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) mode. Changing the mode will change the direction of all UART pins (data and all control signals). To ensure compatibility with the entire Verdin family, the SoCs need to be configured in **DCE** mode, even though the data direction is defined in DTE mode in the Verdin standard.

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Particular attention should be paid to the names of the i.MX 8MP data signals. In the correct DTE mode, TX and RTS signals are outputs while the RX and CTS signals are inputs. In DCE mode, all signals change their direction. Unfortunately, the data directions of the i.MX 8MP SoC are mixed up. In DCE mode, TX and CTS signals are outputs while RX and RTS are inputs. In DTE mode, RX and RTS are outputs, and TX and CTS are inputs. Therefore, the SoC must be set to DCE mode with the RTS and CTS signals swapped on the module. This means the SoC signal UARTx_CTS_B is connected to the UART_x_RTS edge connector pin and vice versa.

UART Features

- 9-bit or multidrop mode (RS-485) support
- 7 or 8 data bits for RS-232 characters
- 9-bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- RS-485 driver direction control via CTS_B signal
- IrDA support up to 115.2 Kbit/s
- Auto baud rate detection (up to 115.2 Kbit/s)
- DCE/DTE capability
- Two independent 32-entry FIFO to transmit and receive

Table 5-25 *"Always Compatible"* UART Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
129	UART_1_RXD	UART1_RXD	UART1_RX	I	Received Data of general-purpose UART_1
131	UART_1_TXD	UART1_TXD	UART1_TX	O	Transmitted Data of general-purpose UART_1
137	UART_2_RXD	UART2_RXD	UART2_RX	I	Received Data of general-purpose UART_2
139	UART_2_TXD	UART2_TXD	UART2_TX	O	Transmitted Data of general-purpose UART_2
147	UART_3_RXD	UART3_RXD	UART3_RX	I	Received Data of A53 debug UART_3
149	UART_3_TXD	UART3_TXD	UART3_TX	O	Transmitted Data of A53 debug UART_3

Table 5-26 *"Reserved"* UART Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
133	UART_1_RTS	SAI2_TXFS	UART1_CTS_B	O	Request to Send of general-purpose UART_1
135	UART_1_CTS	SAI2_RXD0	UART1_RTS_B	I	Clear to Send of general-purpose UART_1
141	UART_2_RTS	SD1_DATA5	UART2_CTS_B	O	Request to Send of general-purpose UART_2
143	UART_2_CTS	SD1_DATA4	UART2_RTS_B	I	Clear to Send of general-purpose UART_2
151	UART_4_RXD	UART4_RXD	UART4_RX	I	Received Data of M7 debug UART_4
153	UART_4_TXD	UART4_TXD	UART4_TX	O	Transmitted Data of M7 debug UART_4

In addition to the UART signals in the *"Always Compatible"* and *"Reserved"* class, there are UART signals available as alternate functions of other pins. These pins are not compatible with other Verdin modules. Therefore, they should be used very carefully.

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Table 5-27 Alternate Function UART Signal Pins (not compatible)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
76	SD_1_PWR_EN	SAI2_RXC	UART1_RX	I	Received Data of general-purpose UART_1
147	UART_3_RXD	UART3_RXD	UART1_CTS_B	O	Request to Send of general-purpose UART_1
149	UART_3_TXD	UART3_TXD	UART1_RTS_B	I	Clear to Send of general-purpose UART_1
44	I2S_2_SYNC	SAI3_TXFS	UART2_RX	I	Received Data of general-purpose UART_2
80	SD_1_D0	SD2_DATA0			
42	I2S_2_BCLK	SAI3_TXC	UART2_TX	O	Transmitted Data of general-purpose UART_2
82	SD_1_D1	SD2_DATA1			
151	UART_4_RXD	UART4_RXD	UART2_CTS_B	O	Request to Send of general-purpose UART_2
256	CTRL_SLEEP_MOCI#	SAI3_RXC			
48	I2S_2_D_IN	SAI3_RXD	UART2_RTS_B	I	Clear to Send of general-purpose UART_2
153	UART_4_TXD	UART4_TXD			
52	QSPI_1_CLK	NAND_ALE	UART3_RX	I	Received Data of A53 debug UART_3
196	SPI_1_CLK	ECSPI1_SCLK			
54	QSPI_1_CS#	NAND_CE0_B	UART3_TX	O	Transmitted Data of A53 debug UART_3
200	SPI_1_MOSI	ECSPI1_MOSI			
198	SPI_1_MISO	ECSPI1_MISO	UART3_CTS_B	O	Request to Send of A53 debug UART_3
202	SPI_1_CS	ECSPI1_SS0	UART3_RTS_B	I	Clear to Send of A53 debug UART_3
56	QSPI_1_IO0	NAND_DATA00	UART4_RX	I	Received Data of M7 debug UART_4
78	SD_1_CLK	SD2_CLK			
164	MSP_33	ECSPI2_SCLK			
58	QSPI_1_IO1	NAND_DATA01	UART4_TX	O	Transmitted Data of M7 debug UART_4
74	SD_1_CMD	SD2_CMD			
152	MSP_28	ECSPI2_MOSI			
60	QSPI_1_IO2	NAND_DATA02	UART4_CTS_B	O	Request to Send of M7 debug UART_4
116	MSP_13	ECSPI2_MISO			
62	QSPI_1_IO3	NAND_DATA03	UART4_RTS_B	I	Clear to Send of M7 debug UART_4
128	MSP_18	ECSPI2_SS0			

5.11 SPI

The i.MX 8MP SoC features a total of three SPI interfaces. These interfaces are called Enhanced Configurable Serial Peripheral Interface (ECSPI) in the NXP documentation. One of the SPI interfaces is available on the Verdin module as an *"Always Compatible"* interface. The other two SPI interfaces are available as an alternate function of other interface pins.

The SPI ports operate at up to 60 Mbps in master write mode and up to 30 Mbps in master read mode for the *"Always Compatible"* instance. Some other instance has a reduced maximum operation frequency. Carefully check the NXP datasheet for more information. The ports provide full-duplex, synchronous, serial communication between the Verdin module and internal or external peripheral devices.

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In the Verdin module standard, only the SPI master mode is specified. Therefore, the slave mode might not be compatible with other modules. The signal direction in the following tables corresponds to the SPI master mode.

Table 5-28 *"Always Compatible"* SPI Port Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
200	SPI_1_MOSI	ECSPI1_MOSI	ECSPI1_MOSI	O	Master Output, Slave Input
198	SPI_1_MISO	ECSPI1_MISO	ECSPI1_MISO	I	Master Input, Slave Output
202	SPI_1_CS	ECSPI1_SS0	ECSPI1_SS0	I/O	Slave Select
196	SPI_1_CLK	ECSPI1_SCLK	ECSPI1_SCLK	I/O	Serial Clock

Table 5-29 Alternate Function SPI Port Signal Pins (not compatible)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
55	I2C_2_DSI_SCL	I2C2_SCL	ECSPI1_MISO	I	Alternate pin for Master Input, Slave Output
53	I2C_2_DSI_SDA	I2C2_SDA	ECSPI1_SS0	I/O	Alternate pin for Slave Select
74	SD_1_CMD	SD2_CMD	ECSPI2_MOSI	O	Master Output, Slave Input
93	I2C_4_CSI_SDA	I2C3_SDA			
152	MSP_28	ECSPI2_MOSI			
14	I2C_1_SCL	I2C4_SCL	ECSPI2_MISO	I	Master Input, Slave Output
72	SD_1_D3	SD2_DATA3			
116	MSP_13	ECSPI2_MISO			
12	I2C_1_SDA	I2C4_SDA	ECSPI2_SS0	I/O	Slave Select
70	SD_1_D2	SD2_DATA2			
128	MSP_18	ECSPI2_SS0			
78	SD_1_CLK	SD2_CLK	ECSPI2_SCLK	I/O	Serial Clock
95	I2C_4_CSI_SCL	I2C3_SCL			
164	MSP_33	ECSPI2_SCLK			
131	UART_1_TXD	UART1_TXD	ECSPI3_MOSI	O	Master Output, Slave Input
137	UART_2_RXD	UART2_RXD	ECSPI3_MISO	I	Master Input, Slave Output
139	UART_2_TXD	UART2_TXD	ECSPI3_SS0	I/O	Slave Select
129	UART_1_RXD	UART1_RXD	ECSPI3_SCLK	I/O	Serial Clock

5.12 Quad Serial Peripheral Interface (QuadSPI, QSPI)

In addition to the regular SPI controller (which is called ECSPI in the NXP documentation), the i.MX 8M Plus features a Flexible SPI Controller (FlexSPI) with up to two SPI channels. However, only one channel is available on the module edge connector pins. The controller supports single, dual, quad, and octal mode data transfer. Since the second SPI channel is not available, the octal mode cannot be used. The interface can be used for accessing NAND and NOR flashes over the QuadSPI standard. Additionally, it can also be used for interfacing HyperBus and FPGA devices.

The Verdin standard offers one QuadSPI channel with two chip selects for up to two memory devices in the *"Reserved"* pin class. However, only the first chip select pin is available from the FlexSPI controller. The second chip select pin on the module edge connector is a regular GPIO. Therefore, the support for dual device memory is limited.

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Table 5-30 QSPI Modes

i.MX 8MP Function	Single Mode	Dual Mode	Quad Mode
A_SCLK	SCLK (Flash A1)	SCLK (Flash A1)	SCLK (Flash A1)
A_SS0_B	SS_B (Flash A1)	SS_B (Flash A1)	SS_B (Flash A1)
A_DATA[0]	MOSI (Flash A1)	DATA0 (Flash A1)	DATA0 (Flash A1)
A_DATA[1]	MISO (Flash A1)	DATA1 (Flash A1)	DATA1 (Flash A1)
A_DATA[2]			DATA2 (Flash A1)
A_DATA[3]			DATA3 (Flash A1)

Table 5-31 QSPI Signal Pins (in *"Reserved"* class)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
54	QSPI_1_CS#	NAND_CE0_B	QSPI_A_SS0_B	O	Chip Select 0
64	QSPI_1_CS2#	NAND_READY_B	GPIO3_IO16	O	Regular GPIO, no support from the FlexSPI controller.
52	QSPI_1_CLK	NAND_ALE	QSPI_A_SCLK	O	Serial Clock
56	QSPI_1_IO0	NAND_DATA00	QSPI_A_DATA0	I/O	Serial I/O for command, address, and data
58	QSPI_1_IO1	NAND_DATA01	QSPI_A_DATA1	I/O	Serial I/O for command, address, and data
60	QSPI_1_IO2	NAND_DATA02	QSPI_A_DATA2	I/O	Serial I/O for command, address, and data
62	QSPI_1_IO3	NAND_DATA03	QSPI_A_DATA3	I/O	Serial I/O for command, address, and data
66	QSPI_1_DQS	NAND_DQS	QSPI_A_DQS	I	Data Strobe signal, required by some high-speed DDR devices

5.13 PWM (Pulse Width Modulation)

The i.MX 8MP features a four-channel general-purpose Pulse Width Modulator (PWM). It has a 16-bit counter and is optimized to generate simple sound samples as well as create tones. It has a 16-bit resolution, and there is a 4-level deep FIFO available to minimize the interrupt overhead. There is a 12-bit pre-scaler available for dividing the clock.

There are 3 PWM signals on the Verdin standard. PWM_1 is the only one in the *"Always Compatible"* class. Both PWM_1 and PWM_2 are general-purpose pulse with modulation outputs. The third interface is dedicated to the DSI output for the display backlight inverter control. The fourth PWM output of the i.MX 8MP SoC is available as an alternate function. Therefore, it is advised to prioritize the other PWM pins over the fourth one since it is not guaranteed that it is compatible with other modules.

Table 5-32 Standard PWM Interface Signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
15	PWM_1	SPDIF_EXT_CLK	PWM1_OUT	O	General-purpose PWM *"Always Compatible"*
16	PWM_2	GPIO1_IO11	PWM2_OUT	O	General-purpose PWM *"Reserved"*
19	PWM_3_DSI	SAI5_RXC	PWM3_OUT	O	Dedicated PWM for display backlight *"Reserved"*

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Table 5-33 Additional PWM Interface Signals (not compatible with other Verdin modules)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
12	I2C_1_SDA	I2C4_SDA	PWM1_OUT	O	Alternate pins for general-purpose PWM_1
30	I2S_1_BCLK	SAI5_MCLK			
208	GPIO_2	GPIO1_IO01			
218	GPIO_6_CSI	GPIO1_IO08			
14	I2C_1_SCL	I2C4_SCL	PWM2_OUT	O	Alternate pins for general-purpose PWM_1
22	CAN_1_RX	SPDIF_RX			
157	USB_1_OC#	GPIO1_IO13			
20	CAN_1_TX	SPDIF_TX	PWM3_OUT	O	Alternate pins for general display backlight PWM
93	I2C_4_CSI_SDA	I2C3_SDA			
185	USB_2_EN	GPIO1_IO14			
34	I2S_1_D_OUT	SAI5_RXFS	PWM4_OUT	O	Additional general-purpose PWM
91	CSI_1_MCLK	SAI3_MCLK			
95	I2C_4_CSI_SCL	I2C3_SCL			
187	USB_2_OC#	GPIO1_IO15			

5.14 SD/MMC

The i.MX 8MP SoC provides three SDIO interfaces. One is used internally for the eMMC Flash. A second one is available on the module edge connector pins as *"Always Compatible"* Verdin SD Memory Card Interface. The third interface is used for the Wi-Fi and Bluetooth module. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, and eMMC devices.

i.MX 8MP SDIO interface	Max Bus Width	Description
USDHC1	4-bit	Used for the on-module Wi-Fi and Bluetooth interface. Not available at the module edge connector
USDHC2	4-bit	*"Always Compatible"* Verdin SD interface
USDHC3	8-bit	Connected to the internal eMMC boot device. Not available at the module edge connector

Features:

- Supports SD Memory Card Specification 2.0 and 3.0
- Supports SDIO Card Specification Version 2.0 and 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, 4.41, 5.0, and 5.1
- Supports addressing larger capacity SD 3.0 or SDXC cards up to 2 TB
- Supports SPI mode
- Supports SD UHS-I mode (up to 208MHz) with a 1.8V IO voltage level.
- 3.3V and 1.8V IO voltage mode supported

For being compliant with SD Memory Cards, the 3.3V IO voltage level needs to be supported. For higher bus speed in the UHS-I class, in addition to the 3.3V, the 1.8V IO voltage level needs to be supported as well. Additionally, the interface needs to be able to switch between these two voltage levels. The SD interface in the *"Always Compatible"* class supports both IO voltage levels. No external pull-up resistors are required on the carrier board. There are pull-up resistors on the module.

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Table 5-34 *SD Card Speed Modes (applicable only for USDHC2)*

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MB/s	3.3V	
High Speed	50 MHz	25 MB/s	3.3V	
SDR12	25 MHz	12.5 MB/s	1.8V	
SDR25	50 MHz	25 MB/s	1.8V	
DDR50	50 MHz	50 MB/s	1.8V	UHS-I
SDR50	100 MHz	50 MB/s	1.8V	
SDR104	208 MHz	104 MB/s	1.8V	

The IO voltage of the SDIO power block can be changed independently from the other IO blocks, but all SDIO block signals change their voltages together. The IO voltage of the Verdin *"Always Compatible"* interface (i.MX 8M Plus USDHC2) is provided by the LDO5 output of the power management IC (PMIC). The voltage level is controlled by the dedicated VSELECT output of the USDHC2 interface, located on the GPIO1_IO04 ball of the SoC.

Table 5-35 *"Always Compatible"* SD Card Interface Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Voltage	Description
74	SD_1_CMD	SD2_CMD	USDHC2_CMD	I/O	3.3/1.8V	Command, enable SoC pull-up resistor
80	SD_1_D0	SD2_DATA0	USDHC2_DATA0	I/O	3.3/1.8V	Serial Data 0, enable SoC pull-up resistor
82	SD_1_D1	SD2_DATA1	USDHC2_DATA1	I/O	3.3/1.8V	Serial Data 1, enable SoC pull-up resistor
70	SD_1_D2	SD2_DATA2	USDHC2_DATA2	I/O	3.3/1.8V	Serial Data 2, enable SoC pull-up resistor
72	SD_1_D3	SD2_DATA3	USDHC2_DATA3	I/O	3.3/1.8V	Serial Data 3, enable SoC pull-up resistor
78	SD_1_CLK	SD2_CLK	USDHC2_CLK	O	3.3/1.8V	Serial Clock
84	SD_1_CD#	SD2_CD_B	USDHC2_CD_B	I	3.3/1.8V	Card Detect, enable SoC pull-up resistor
76	SD_1_PWR_EN	SAI2_RXC	GPIO4_IO22	O	1.8V	Enable pin for SD card power rail. Regular GPIO pin which does not change IO voltage level with the rest of the SD card signal pins

5.15 Digital Audio Interfaces

The i.MX 8M Plus SoC features six Synchronous Audio Interfaces (SAI). The SAI interfaces can be used as I²S (also known as Inter-IC Sound, Integrated Interchip Sound, or IIS) or as Intel® Audio Codec '97 (also known as AC'97 or AC97). The Verdin standard defines two I²S interfaces in the *"Reserved"* pin class. Since AC'97 is not part of the Verdin standard, it is recommended to use I²S for better compatibility with other Verdin modules. In addition to the two standard I²S interfaces, another I²S is connected to the Wi-Fi module for Bluetooth audio features. The following table provides an overview of the SAI interfaces. Please note the numbering of the SAI ports in the SoC. The ports are numbered from 1 to 3 and from 5 to 7. SAI port 4 does not exist.

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Table 5-36 SAI Instance Configuration

Instance	Tx/Rx Data Lines (stereo)	Max. Sampling Rate	Use Case
SAI1	8/8	768KHz/32-bit	Available as Verdin standard I2S_1 interface
SAI2	4/4	768KHz/32-bit	Available on module edge connector as alternate function.
SAI3	2/2	768KHz/32-bit	Available as Verdin standard I2S_2 interface.
SAI5	4/4	768KHz/32-bit	Connected to the Wi-Fi/Bluetooth module. Also available on module edge connector as alternate function
SAI6	1/1	768KHz/32-bit	Available on module edge connector as alternate function.
SAI7	1/1	384KHz/32-bit	Available on module edge connector as alternate function.
SPDIF-1	1/1		Available on module edge connector as alternate function.
PDM	0/4		PDM Microphone Interface. Available on module edge connector as alternate function.
HDMI Tx			Supported through HDMI PHY (audio output stream of HDMI)
eARC			Supported through eARC PHY (HDMI audio input, not compatible with other Verdin modules)
ASRC		384KHz/32-bit	Internal audio sample rate converter for up to 32 audio channels simultaneous

The SAI interfaces support word sizes of between 8-bit and 32-bit. Some instances support up to 8 RX and 8 TX lines. However, not all combinations are possible due to pin multiplexing limitations, and not all interface pins are available on the module edge connector. The Toradex Pinout Designer tool can help check the pin multiplexing, especially for the alternate functions which are not standard in the Verdin specifications. Each transmit and receive data line features an asynchronous 128x32-bit FIFO that provides an automatic graceful restart after FIFO error without software intervention.

Table 5-37 Standard Digital Audio Port Signals (compatible with other modules)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
36	I2S_1_D_IN	SAI1_RXD0	SAI1_RX_DATA0	I	Data Input to i.MX 8MP
34	I2S_1_D_OUT	SAI5_RXFS	SAI1_TX_DATA0	O	Data Output from i.MX 8MP
32	I2S_1_SYNC	SAI5_RXD1	SAI1_TX_SYNC	I/O	Field Select (Transmit Frame Sync)
30	I2S_1_BCLK	SAI5_MCLK	SAI1_TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
38	I2S_1_MCLK	SAI1_MCLK	SAI1_MCLK	O	Master clock output.
48	I2S_2_D_IN	SAI3_RXD	SAI3_RX_DATA0	I	Data Input to i.MX 8MP
46	I2S_2_D_OUT	SAI3_TXD	SAI3_TX_DATA0	O	Data Output from i.MX 8MP
44	I2S_2_SYNC	SAI3_TXFS	SAI3_TX_SYNC	I/O	Field Select (Transmit Frame Sync)
42	I2S_2_BCLK	SAI3_TXC	SAI3_TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)

For controlling the I^2S codec, an additional I^2C interface may be required, and the generic I^2C interface I2C_1 is recommended for this purpose. There are alternate multiplexing options available for the SAI ports that are used as standard Verdin I^2S interfaces. These signals are available as alternate functions of other interfaces. Therefore, they are not compatible with other Verdin modules and should be used with care.

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Table 5-38 Additional signals and multiplexing options for I2S_1 (SAI1) Standard Digital Audio Port

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
220	GPIO_7_CSI	SAI1_RXD1	SAI1_RX_DATA1	I	Data Input to i.MX 8MP
193	ETH_2_RGMII_MDC	SAI1_RXD2	SAI1_RX_DATA2	I	Data Input to i.MX 8MP
191	ETH_2_RGMII_MDIO	SAI1_RXD3	SAI1_RX_DATA3	I	Data Input to i.MX 8MP
201	ETH_2_RGMII_RXD_0	SAI1_RXD4	SAI1_RX_DATA4	I	Data Input to i.MX 8MP
203	ETH_2_RGMII_RXD_1	SAI1_RXD5	SAI1_RX_DATA5	I	Data Input to i.MX 8MP
205	ETH_2_RGMII_RXD_2	SAI1_RXD6	SAI1_RX_DATA6	I	Data Input to i.MX 8MP
207	ETH_2_RGMII_RXD_3	SAI1_RXD7	SAI1_RX_DATA7	I	Data Input to i.MX 8MP
203	ETH_2_RGMII_RXD_1	SAI1_RXD5	SAI1_RX_SYNC	I/O	Field Select (Receive Frame Sync)
252	CTRL_WAKE1_MICO#	SAI1_RXFS			
222	GPIO_8_CSI	SAI1_RXC	SAI1_RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
221	ETH_2_RGMII_TXD_0	SAI1_TXD0	SAI1_TX_DATA0	O	Alternate Data Output from i.MX 8MP
19	PWM_3_DSI	SAI5_RXC	SAI1_TX_DATA1	O	Data Output from i.MX 8MP
36	I2S_1_D_IN	SAI1_RXD0			
219	ETH_2_RGMII_TXD_1	SAI1_TXD1			
217	ETH_2_RGMII_TXD_2	SAI1_TXD2	SAI1_TX_DATA2	O	Data Output from i.MX 8MP
32	I2S_1_SYNC	SAI5_RXD1	SAI1_TX_DATA3	O	Data Output from i.MX 8MP
215	ETH_2_RGMII_TXD_3	SAI1_TXD3			
207	ETH_2_RGMII_RXD_3	SAI1_RXD7	SAI1_TX_DATA4	O	Data Output from i.MX 8MP
211	ETH_2_RGMII_TX_CTL	SAI1_TXD4			
213	ETH_2_RGMII_TXC	SAI1_TXD5	SAI1_TX_DATA5	O	Data Output from i.MX 8MP
189	ETH_2_RGMII_INT#	SAI1_TXD6	SAI1_TX_DATA6	O	Data Output from i.MX 8MP
244	PCIE_1_RESET#	SAI1_TXD7	SAI1_TX_DATA7	O	Data Output from i.MX 8MP
199	ETH_2_RGMII_RX_CTL	SAI1_TXFS	SAI1_TX_SYNC	I/O	Alternate Field Select (Transmit Frame Sync)
207	ETH_2_RGMII_RXD_3	SAI1_RXD7			
38	I2S_1_MCLK	SAI1_MCLK	SAI1_TX_BCLK	I/O	Alternate Serial Clock (Transmit Bit Clock)
197	ETH_2_RGMII_RXC	SAI1_TXC			

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Table 5-39 Additional signals and multiplexing options for I2S_2 (SAI3) Standard Digital Audio Port

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
56	QSPI_1_IO0	NAND_DATA00	SAI3_RX_DATA0	I	Alternate Data Input to i.MX 8MP
21	GPIO_10_DSI	SAI3_RXFS	SAI3_RX_DATA1	I	Data Input to i.MX 8MP
21	GPIO_10_DSI	SAI3_RXFS	SAI3_RX_SYNC	I/O	Field Select (Receive Frame Sync)
256	CTRL_SLEEP_MOCI#	SAI3_RXC	SAI3_RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
44	I2S_2_SYNC	SAI3_TXFS	SAI3_TX_DATA1	O	Data Output from i.MX 8MP
58	QSPI_1_IO1	NAND_DATA01	SAI3_TX_SYNC	I/O	Alternate Field Select (Transmit Frame Sync)
52	QSPI_1_CLK	NAND_ALE	SAI3_TX_BCLK	I/O	Alternate Serial Clock (Transmit Bit Clock)
26	CAN_2_RX	SAI2_MCLK	SAI3_MCLK	O	Master clock output.
66	QSPI_1_DQS	NAND_DQS			
91	CSI_1_MCLK	SAI3_MCLK			

In Addition to the two SAI interfaces available as standard I²S interfaces, other SAI instances are available as alternate functions of different interfaces. These signals are not compatible with other Verdin modules. Carefully check the pin multiplexing since not all combinations are possible.

Table 5-40 SAI2 Signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
135	UART_1_CTS	SAI2_RXD0	SAI2_RX_DATA0	I	Data Input to i.MX 8MP
21	GPIO_10_DSI	SAI3_RXFS	SAI2_RX_DATA1	I	Data Input to i.MX 8MP
256	CTRL_SLEEP_MOCI#	SAI3_RXC	SAI2_RX_DATA2	I	Data Input to i.MX 8MP
48	I2S_2_D_IN	SAI3_RXD	SAI2_RX_DATA3	I	Data Input to i.MX 8MP
76	SD_1_PWR_EN	SAI2_RXC	SAI2_RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
24	CAN_2_TX	SAI2_TXD0	SAI2_TX_DATA0	O	Data Output from i.MX 8MP
44	I2S_2_SYNC	SAI3_TXFS	SAI2_TX_DATA1	O	Data Output from i.MX 8MP
133	UART_1_RTS	SAI2_TXFS			
135	UART_1_CTS	SAI2_RXD0			
42	I2S_2_BCLK	SAI3_TXC	SAI2_TX_DATA2	O	Data Output from i.MX 8MP
46	I2S_2_D_OUT	SAI3_TXD	SAI2_TX_DATA3	O	Data Output from i.MX 8MP
133	UART_1_RTS	SAI2_TXFS	SAI2_TX_SYNC	I/O	Field Select (Transmit Frame Sync)
17	GPIO_9_DSI	SAI2_TXC	SAI2_TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
26	CAN_2_RX	SAI2_MCLK	SAI2_MCLK	O	Master clock output.

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Table 5-41 SAI5 Signals (SAI port is shared with the Wi-Fi audio)

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
36	I2S_1_D_IN	SAI1_RXD0	SAI5_RX_DATA0	I	Data Input to i.MX 8MP
48	I2S_2_D_IN	SAI3_RXD			
32	I2S_1_SYNC	SAI5_RXD1	SAI5_RX_DATA1	I	Data Input to i.MX 8MP
44	I2S_2_SYNC	SAI3_TXFS			
220	GPIO_7_CSI	SAI1_RXD1			
42	I2S_2_BCLK	SAI3_TXC	SAI5_RX_DATA2	I	Data Input to i.MX 8MP
193	ETH_2_RGMII_MDC	SAI1_RXD2			
46	I2S_2_D_OUT	SAI3_TXD	SAI5_RX_DATA3	I	Data Input to i.MX 8MP
191	ETH_2_RGMII_MDIO	SAI1_RXD3			
21	GPIO_10_DSI	SAI3_RXFS	SAI5_RX_SYNC	I/O	Field Select (Receive Frame Sync)
34	I2S_1_D_OUT	SAI5_RXFS			
252	CTRL_WAKE1_MICO#	SAI1_RXFS			
19	PWM_3_DSI	SAI5_RXC	SAI5_RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
222	GPIO_8_CSI	SAI1_RXC			
256	CTRL_SLEEP_MOCI#	SAI3_RXC			
135	UART_1_CTS	SAI2_RXD0	SAI5_TX_DATA0	O	Data Output from i.MX 8MP
221	ETH_2_RGMII_TXD_0	SAI1_TXD0			
133	UART_1_RTS	SAI2_TXFS	SAI5_TX_DATA1	O	Data Output from i.MX 8MP
219	ETH_2_RGMII_TXD_1	SAI1_TXD1			
17	GPIO_9_DSI	SAI2_TXC	SAI5_TX_DATA2	O	Data Output from i.MX 8MP
217	ETH_2_RGMII_TXD_2	SAI1_TXD2			
24	CAN_2_TX	SAI2_TXD0	SAI5_TX_DATA3	O	Data Output from i.MX 8MP
215	ETH_2_RGMII_TXD_3	SAI1_TXD3			
32	I2S_1_SYNC	SAI5_RXD1	SAI5_TX_SYNC	I/O	Field Select (Transmit Frame Sync)
199	ETH_2_RGMII_RX_CTL	SAI1_TXFS			
76	SD_1_PWR_EN	SAI2_RXC	SAI5_TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
197	ETH_2_RGMII_RXC	SAI1_TXC			
26	CAN_2_RX	SAI2_MCLK	SAI5_MCLK	O	Master clock output.
30	I2S_1_BCLK	SAI5_MCLK			
38	I2S_1_MCLK	SAI1_MCLK			
91	CSI_1_MCLK	SAI3_MCLK			

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Table 5-42 SAI6 Signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
203	ETH_2_RGMII_RXD_1	SAI1_RXD5	SAI6_RX_DATA0	I	Data Input to i.MX 8MP
213	ETH_2_RGMII_TXC	SAI1_TXD5			
189	ETH_2_RGMII_INT#	SAI1_TXD6	SAI6_RX_SYNC	I/O	Field Select (Receive Frame Sync)
205	ETH_2_RGMII_RXD_2	SAI1_RXD6			
201	ETH_2_RGMII_RXD_0	SAI1_RXD4	SAI6_RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
211	ETH_2_RGMII_TX_CTL	SAI1_TXD4			
203	ETH_2_RGMII_RXD_1	SAI1_RXD5	SAI6_TX_DATA0	O	Data Output from i.MX 8MP
213	ETH_2_RGMII_TXC	SAI1_TXD5			
189	ETH_2_RGMII_INT#	SAI1_TXD6	SAI6_TX_SYNC	O	Data Output from i.MX 8MP
205	ETH_2_RGMII_RXD_2	SAI1_RXD6			
201	ETH_2_RGMII_RXD_0	SAI1_RXD4	SAI6_TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
211	ETH_2_RGMII_TX_CTL	SAI1_TXD4			
207	ETH_2_RGMII_RXD_3	SAI1_RXD7	SAI6_MCLK	O	Master clock output.
244	PCIE_1_RESET#	SAI1_TXD7			

Table 5-43 SAI2 Signals

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
198	SPI_1_MISO	ECSPI1_MISO	SAI7_RX_DATA0	I	Data Input to i.MX 8MP
196	SPI_1_CLK	ECSPI1_SCLK	SAI7_RX_SYNC	I/O	Field Select (Receive Frame Sync)
200	SPI_1_MOSI	ECSPI1_MOSI	SAI7_RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
152	MSP_28	ECSPI2_MOSI	SAI7_TX_DATA0	O	Data Output from i.MX 8MP
202	SPI_1_CS	ECSPI1_SS0	SAI7_TX_SYNC	O	Data Output from i.MX 8MP
164	MSP_33	ECSPI2_SCLK	SAI7_TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
116	MSP_13	ECSPI2_MISO	SAI7_MCLK	O	Master clock output.

5.15.1 Synchronous Audio Interface used as I²S

The SAI can be used as I²S interfaces, the default use case for the Verdin standard. The interface supports either master or slave mode. In the Verdin standard, the master configuration is most compatible with other modules. Therefore, it is the preferred configuration. The following signals are used for a simple I²S interface:

Table 5-44 Synchronous Audio Interface used as Maser I2S

i.MX 8MP Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 8MP
SAIx.RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 8MP
SAIx.TX_SYNC	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx.TX_BCLK	SCK	I/O	Serial Continuous Clock

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Table 5-45 Synchronous Audio Interface used as Slave I²S

i.MX 8MP Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 8MP
SAIx.TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 8MP
SAIx.RX_SYNC	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx.RX_BCLK	SCK	I/O	Serial Continuous Clock

5.15.2 Synchronous Audio Interface used as AC'97

The SAI interface can be configured as an AC'97 compatible interface. The AC'97 Audio interface does not need an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97 Audio codec does require a master reference clock. This can be either one of the SAI master clock outputs or a separate crystal/oscillator can be used. Please take care of the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host and not to the signal direction.

Table 5-46 Synchronous Audio Interface used as AC'97

i.MX 8MP Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.RX_DATA[0]	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 8MP
SAIx.TX_DATA[0]	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 8MP
SAIx.TX_SYNC	SYNC	O	AC'97 Audio Sync
SAIx.TX_BCLK	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

5.15.3 PDM Microphone Interface

The i.MX 8M Plus SoC features up to four PDM microphone input signals. PDM stands for Pulse-Density Modulation and is a popular digital interface for delivering audio from microphones to the SoC. The PDM bitstream is time-multiplexed and contains audio information in two channels (left and right). This means a total of eight microphones can be attached to the PDM interface of the i.MX 8M Plus.

Since the PDM is not a standard interface of Verdin, these signals are available only as alternate functions. Therefore, the PDM microphone interface is not guaranteed to be compatible with other Verdin Modules.

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Table 5-47 PDM Microphone Interface Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
21	GPIO_10_DSI	SAI3_RXFS	PDM_BIT_STREAM0	I	Stereo PDM microphone stream
36	I2S_1_D_IN	SAI1_RXD0			
80	SD_1_D0	SD2_DATA0			
17	GPIO_9_DSI	SAI2_TXC	PDM_BIT_STREAM1	I	Stereo PDM microphone stream
32	I2S_1_SYNC	SAI5_RXD1			
48	I2S_2_D_IN	SAI3_RXD			
76	SD_1_PWR_EN	SAI2_RXC			
82	SD_1_D1	SD2_DATA1			
220	GPIO_7_CSI	SAI1_RXD1			
42	I2S_2_BCLK	SAI3_TXC	PDM_BIT_STREAM2	I	Stereo PDM microphone stream
70	SD_1_D2	SD2_DATA2			
133	UART_1_RTS	SAI2_TXFS			
193	ETH_2_RGMII_MDC	SAI1_RXD2			
44	I2S_2_SYNC	SAI3_TXFS	PDM_BIT_STREAM3	I	Stereo PDM microphone stream
72	SD_1_D3	SD2_DATA3			
135	UART_1_CTS	SAI2_RXD0			
191	ETH_2_RGMII_MDIO	SAI1_RXD3			
19	PWM_3_DSI	SAI5_RXC	PDM_CLK	O	Clock output for microphones
74	SD_1_CMD	SD2_CMD			
222	GPIO_8_CSI	SAI1_RXC			
244	PCIE_1_RESET#	SAI1_TXD7			
256	CTRL_SLEEP_MOCI#	SAI3_RXC			

5.15.4 S/PDIF (Sony-Philips Digital Interface)

The S/PDIF interface supports both input and output. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard.

The S/PDIF interface is not part of the Verdin standard. Therefore, the signals are available as alternate functions of other interface pins. This means the S/PDIF is not compatible with other Verdin modules.

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Table 5-48 S/PDIF Data Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
20	CAN_1_TX	SPDIF_TX	SPDIF1_OUT	O	Serial data output
70	SD_1_D2	SD2_DATA2			
91	CSI_1_MCLK	SAI3_MCLK			
21	GPIO_10_DSI	SAI3_RXFS	SPDIF1_IN	I	Serial data input
22	CAN_1_RX	SPDIF_RX			
72	SD_1_D3	SD2_DATA3			
91	CSI_1_MCLK	SAI3_MCLK			
15	PWM_1	SPDIF_EXT_CLK	SPDIF1_EXT_CLK	I	External clock input
46	I2S_2_D_OUT	SAI3_TXD			

5.16 Analog Inputs

The i.MX 8M Plus SoC itself does not feature an ADC input. Since analog inputs are in the *"Reserved"* category of Verdin interfaces, there is a dedicated I²C ADC on the Verdin iMX8M Plus module. The 12-bit ADC TLA2024 from Texas Instruments offers up to four single-ended analog inputs. The delta-sigma ADC features an internal reference voltage.

The TLA2024 can be configured into differential mode as well. In this mode, the ADC_1 and ADC_2 are combined to a differential input while the ADC_3 and ADC_4 are combined. This differential mode is not part of the Verdin standard and potentially not compatible with other modules.

The ADC features a programmable input gain which can be selected for input ranges of ±256mV, 512mV, ±1.024V, ±2.048V, and ±4.096V. Since the ADC is powered with 3.3V, the actual input range is limited by the absolute maximum input voltage range of -0.3V to 3.6V. However, to be compatible with other Verdin modules, it is recommended to limit the input voltage from 0V to 1.8V.

The TLA2024 is connected to the I2C1 I²C port of the SoC. The device has the address 0x49. The same I²C port is also shared with the on-module PMIC, RTC, and EEPROM.

Features

- 12-bit ADC
- Delta-Sigma algorithm
- Programmable gain amplifier for input ranges from ±256mV to ±4.096V
- 4-channel single-ended or 2-channel fully differential
- Internal FIFO with channel-scan mode
- Programmable data rate from 128SPS to 3.3kSPS

Table 5-49 Analog Inputs Pins

X1 Pin#	Verdin Std Function	TLA2024 Pin#	TLA2024 Pin Name	I/O	Remarks
2	ADC_1	7	AIN3	I	Analog Input 1
4	ADC_2	6	AIN2	I	Analog Input 2
6	ADC_3	5	AIN1	I	Analog Input 3
8	ADC_4	4	AIN0	I	Analog Input 4

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5.17 Controller Area Network (CAN)

The i.MX 8M Plus SoC features two Flexible Controller Area Network (FlexCAN) interfaces. Both of them are available as Verdin *"Reserved"* interfaces and therefore compatible with other Verdin modules. Depending on the SoC version, the CAN interfaces support flexible data rates (CAN FD). Check section 1.4.3 for more information on which CAN version is supported by the selected Verdin iMX8M Plus module.

Features:

- CAN FD support on selected Verdin iMX8M Plus modules
- CAN 2.0B compliant
- Compliant with ISO11898-1
- Flexible mailboxes for up to 64-byte data length (configurable as RX or TX)
- Flexible message buffers for a total of 64 messages of 8bytes data length (configurable for RX and TX)
- Listen-only mode
- Loop-back mode
- Timestamp based on 16-bit free-running timer
- Maskable interrupts

Table 5-50 CAN Signal Pins (compatible with other Verdin modules)

X1 Pin#	Verdin Signal Name	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
20	CAN_1_TX	SPDIF_TX	CAN1_TX	O	CAN port 1 transmit pin
22	CAN_1_RX	SPDIF_RX	CAN1_RX	I	CAN port 1 receive pin
24	CAN_2_TX	SAI2_TXD0	CAN2_TX	O	CAN port 2 transmit pin
26	CAN_2_RX	SAI2_MCLK	CAN2_RX	I	CAN port 2 receive pin

The CAN signals are also available on other module edge connector pins as alternate functions. However, the location of these signals is not compatible with other Verdin modules. Therefore, it is highly recommended to use the compatible pins in the previous table.

Table 5-51 Alternate location of CAN Signal Pins (not compatible with other Verdin modules)

X1 Pin#	Verdin Signal Name	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
32	I2S_1_SYNC	SAI5_RXD1	CAN1_TX	O	Alternate CAN port 1 transmit pin
59	I2C_3_HDMI_SCL	HDMI_DDC_SCL			
76	SD_1_PWR_EN	SAI2_RXC			
17	GPIO_9_DSI	SAI2_TXC	CAN1_RX	I	Alternate CAN port 1 receive pin
57	I2C_3_HDMI_SDA	HDMI_DDC_SDA			
63	HDMI_1_CEC	HDMI_CEC	CAN2_TX	O	Alternate CAN port 2 transmit pin
147	UART_3_RXD	UART3_RXD			
30	I2S_1_BCLK	SAI5_MCLK	CAN2_RX	O	Alternate CAN port 2 transmit pin
61	HDMI_1_HPD	HDMI_HPD			
149	UART_3_TXD	UART3_TXD			

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5.18 JTAG

The JTAG interface usually is not required for programming the Verdin. However, it can be helpful for debugging the Cortex-M7 Core or very advanced debugging of the Cortex-A Cores. The i.MX 8M Plus SoC does not feature a JTAG_TRST# reset input. Instead, the TRST# pin of the module edge connector is connected to the regular RESET_MOCI# input over a diode circuit. This means using the TRST# signal is resetting the whole module, not just the JTAG interface.

Instead of using the JTAG port, it is possible to reprogram the module using the Recovery Mode over USB. To flash the module in recovery mode (and for debugging), it is strongly recommended that the USB_1 interface is accessible even if not needed in the production system. Additionally, UART_3 for the console of the main CPUs (A53) and UART_4 for debugging the M7 core should be accessible as well.

Table 5-52 JTAG Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MP Ball Name	i.MX 8MP Function	I/O	Description
1	JTAG_1_TDI	JTAG_TDI	JTAG_TDI	I	Test Data In
5	JTAG_1_TDO	JTAG_TDO	JTAG_TDO	O	Test Data Out
9	JTAG_1_TCK	JTAG_TCK	JTAG_TCK	I	Test Clock
13	JTAG_1_TMS	JTAG_TMS	JTAG_TMS	I	Test Mode Select
3	JTAG_1_TRST#			I	Test reset, connected to regular RESET_MOCI#, which resets the whole module
7	JTAG_1_VREF			O	1.8V reference output for JTAG adapter

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6. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Verdin iMX8M Plus even when the bootloader is no longer capable of booting the module. In the standard development process, this mode is not needed. When the module is in recovery mode, the USB_1 interface connects it to a host computer. You will find additional information at our Developer Center (https://developer.toradex.com).

The dedicated recovery pin (SODIMM pin 246) needs to be pulled down with ≤1kΩ during the initial power on (cold boot) of the module to enter recovery mode. The CTRL_RECOVERY_MICO# function on the SODIMM pin 246 is standardized in the Verdin module specifications. It is highly recommended to add at least a test point on the carrier board to the pin 246 to be able to enter recovery mode. There is no need for a pull-up resistor on the carrier board.

Important: make sure that there is no bootable SD card plugged into the slot. Otherwise, the module tries to boot from the external SD card instead of going into the USB serial loader.

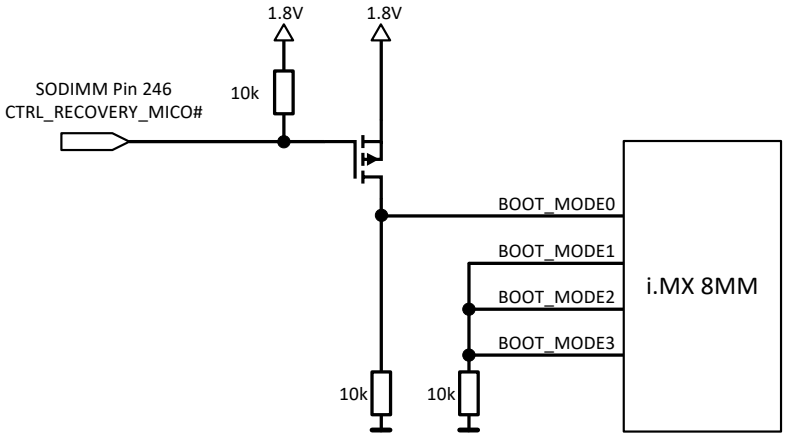


Figure 15: Recovery Mode Circuit

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7. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document, which can be downloaded from our website at:

https://developer.toradex.com/products/verdin-som-family/modules/verdin-imx8m-plus#tab-erratakown-issues

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8. Technical Specifications

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VCC	Main power supply	-0.3	6	V
VCC_BACKUP	RTC power supply	-0.3	6.5	V
IO_1.8V	SoC IO pins with 1.8V logic level	-0.3	2.1	V
IO_3.3V	SoC IO pins with 3.3V logic level (SDIO)	-0.3	3.6	V
ADC	ADC analog input	-0.3	3.6	V
USB_1_VBUS	Input voltage at USB_1_VBUS	-0.3	5.5	V

8.2 Recommended Operation Conditions

Table 8-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
VCC	Main power supply	3.135	3.3 or 5	5.5	V
VCC_BACKUP	RTC power supply	1.1	3.0	5.5	V

8.3 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Verdin product family. Following those recommendations ensures that the carrier board being designed will be compatible with all existing and future Verdin modules. For details, please refer to the Verdin Family Specification or the Verdin Carrier Board Design Guide.

For designing carrier boards for a particular Verdin module only, please consult our Developer Website for module-specific power consumption information. However, please note that scaling the carrier board power supplies for a particular module only may cause compatibility issues with other existing and future modules within the Verdin family.

8.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Verdin module standard. This specification can be found in the Verdin Carrier Board Design Guide.

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8.5 Mechanical Characteristics

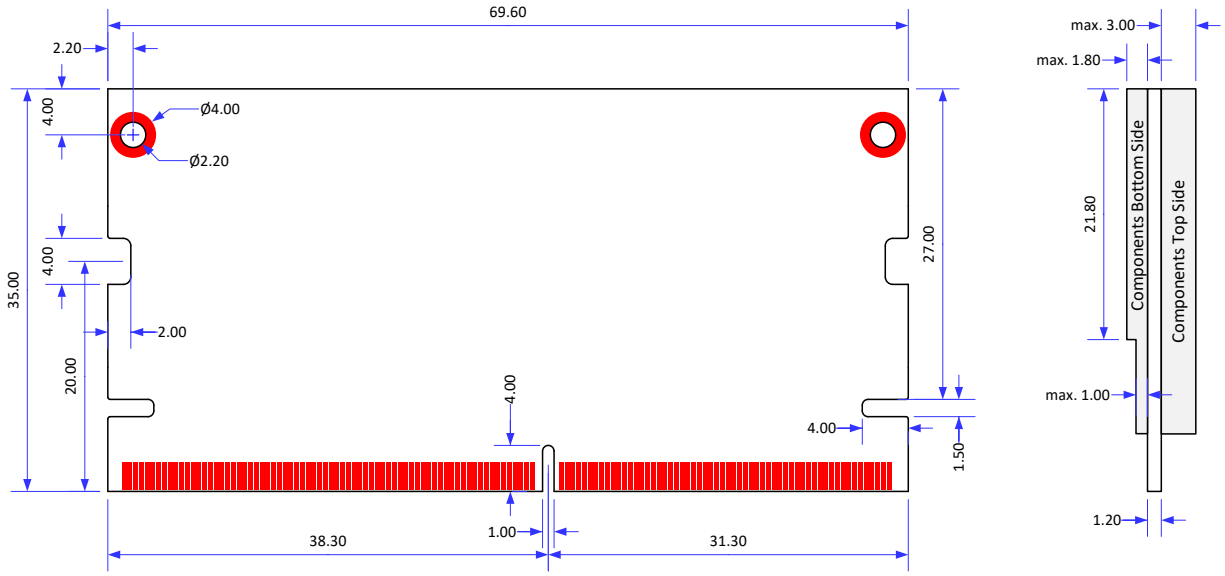


Figure 16 Mechanical dimensions of the Verdin module (top view)
Tolerance for all measures: +/- 0.1mm, unless otherwise specified

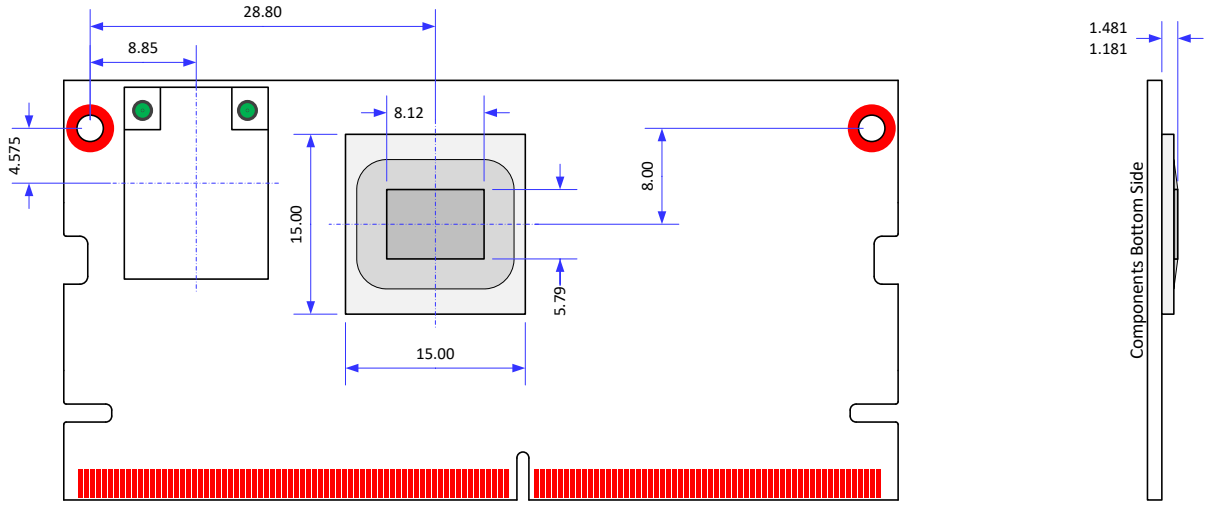


Figure 17 Mechanical position of i.MX 8M Plus SoC (top view)
Tolerance for all measures: +/- 0.1mm, unless otherwise specified

8.5.1 Sockets for the Verdin Modules

The Verdin module uses the SODIMM DDR4 memory module edge connector. This connector has 260 pins and is available from different manufacturers in various board-to-board stacking heights from 4mm to 9.2mm. Toradex recommends using the TE Connectivity 2309409-2 with a stacking height of 5.2mm, which provides a board-to-board distance of 2.62mm.

A list of other SODIMM DDR4 connector manufacturers is given below:

Amphenol: https://www.amphenol-icc.com/product-series/ddr4-so-dimm.html
TE Connectivity: https://www.te.com/usa-en/products/connectors/card-socket-connectors/memory-sockets.html

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8.6 Thermal Specification

The Verdin iMX8M Plus incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling, enabling the system to continuously adjust the operating frequency and voltage in response to the changes in workload and temperature. The i.MX 8M Plus SoC features DVFS on the CPU cluster and the GPU. This allows the Verdin iMX8M Plus to deliver higher performance at lower average power consumption than other solutions.

The Verdin iMX8M Plus modules come with embedded temperature sensors. The sensors measure the die (junction) temperature and determine whether the cores need to be throttled to prevent overheating. If the temperature of the i.MX 8M Plus reaches the maximum permitted temperature limit, the system will automatically shut down.

Here are some general considerations for you to follow:

- Suppose you only use the peak performance for a short time. In that case, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to the smaller leakage currents while idle. A die temperature increase from 25°C to 125°C will increase the leakage by a factor of 10.

In general, the more effective the thermal solution is, the more performance you can get out of the Verdin iMX8M Plus Module.

Table 8-3 1.1 Thermal Specification Verdin iMX8M Plus Quad 4GB WB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8MP only. ($R_{\theta JA}$)[2]		20.44		°C/W
Thermal Resistance Junction-to-Top of i.MX 8MP chip case. ($R_{\theta JCtop}$)[2]		TBD		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-2A, board mounted horizontal, natural convection.
[3] The Wi-Fi module is currently only validated from -30°C to 85°C. Validation down to -40°C is pending. The rest of the components are rated for the complete -40°C to 85°C temperature range.

Table 8-4 1.1 Thermal Specification Verdin iMX8M Plus Quad 2GB

Description	Min	Typ	Max	Unit
Operating temperature range	0		70[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	0		95	°C
Thermal Resistance Junction-to-Ambient, i.MX 8MP only. ($R_{\theta JA}$)[2]		20.44		°C/W
Thermal Resistance Junction-to-Top of i.MX 8MP chip case. ($R_{\theta JCtop}$)[2]		TBD		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-2A, board mounted horizontal, natural convection.

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Table 8-5 1.1 Thermal Specification Verdin iMX8M Plus QuadLite 1GB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8MP only. ($R_{\theta JA}$)[2]		20.44		°C/W
Thermal Resistance Junction-to-Top of i.MX 8MP chip case. ($R_{\theta JCtop}$)[2]		TBD		°C/W

[1] Depending on the cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-2A, board mounted horizontal, natural convection.

8.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at https://www.toradex.com/support/product-compliance

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