

International **IR** Rectifier

POWER MOSFET THRU-HOLE (TO-257AA)

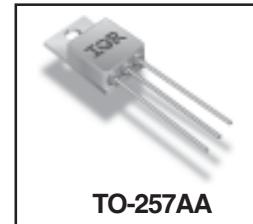
PD-91292D

IRFY440C, IRFY440CM 500V, N-CHANNEL **HEXFET®** MOSFET TECHNOLOGY

Product Summary

Part Number	R _{DS(on)}	I _D	Eyelets
IRFY440C	0.85 Ω	7.0A	Ceramic
IRFY440CM	0.85 Ω	7.0A	Ceramic

HEXFET® MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.



Features:

- Simple Drive Requirements
- Ease of Parallelizing
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets
- Ideally Suited For Space Level Applications

Absolute Maximum Ratings

	Parameter		Units
I _D @ V _{GS} = 10V, T _C = 25°C	Continuous Drain Current	7.0	A
I _D @ V _{GS} = 10V, T _C = 100°C	Continuous Drain Current	4.4	
I _{DM}	Pulsed Drain Current ①	28	W
P _D @ T _C = 25°C	Max. Power Dissipation	100	
	Linear Derating Factor	0.8	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	510	mJ
I _{AR}	Avalanche Current ①	7.0	A
E _{AR}	Repetitive Avalanche Energy ①	10	mJ
dV/dt	Peak Diode Recovery dV/dt ③	3.5	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{TSG}	Storage Temperature Range		
	Lead Temperature	300(0.063in./1.6mm from case for 10 sec)	g
	Weight	4.3 (Typical)	

For footnotes refer to the last page

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IRFY440C, IRFY440CM

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Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	$\text{V}_{\text{GS}} = 0\text{V}, \text{I}_D = 1.0\text{mA}$
$\Delta \text{BV}_{\text{DSS}}/\Delta T_j$	Temperature Coefficient of Breakdown Voltage	—	0.78	—	$\text{V}/^\circ\text{C}$	Reference to 25°C , $\text{I}_D = 1.0\text{mA}$
$\text{R}_{\text{DS(on)}}$	Static Drain-to-Source On-State Resistance	—	—	0.85	Ω	$\text{V}_{\text{GS}} = 10\text{V}, \text{I}_D = 4.4\text{A}$ ④
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	2.0	—	4.0	V	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}, \text{I}_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	4.7	—	—	$\text{S} (\text{A})$	$\text{V}_{\text{DS}} > 15\text{V}, \text{I}_{\text{DS}} = 4.4\text{A}$ ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	$\text{V}_{\text{DS}} = 400\text{V}, \text{V}_{\text{GS}} = 0\text{V}$
		—	—	250		$\text{V}_{\text{DS}} = 400\text{V}, \text{V}_{\text{GS}} = 0\text{V}, \text{T}_j = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$\text{V}_{\text{GS}} = 20\text{V}$
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		$\text{V}_{\text{GS}} = -20\text{V}$
Q_g	Total Gate Charge	—	—	68.5	nC	$\text{V}_{\text{GS}} = 10\text{V}, \text{I}_D = 7.0\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	12.5		$\text{V}_{\text{DS}} = 250\text{V}$
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	42.4		
$t_{\text{d(on)}}$	Turn-On Delay Time	—	—	21	ns	$\text{V}_{\text{DD}} = 250\text{V}, \text{I}_D = 7.0\text{A}, \text{V}_{\text{GS}} = 10\text{V}, \text{R}_G = 9.1\Omega$
t_r	Rise Time	—	—	73		
$t_{\text{d(off)}}$	Turn-Off Delay Time	—	—	72		
t_f	Fall Time	—	—	51		
$\text{L}_{\text{S}} + \text{L}_{\text{D}}$	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	1300	—	pF	$\text{V}_{\text{GS}} = 0\text{V}, \text{V}_{\text{DS}} = 25\text{V}$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	310	—		
C_{rss}	Reverse Transfer Capacitance	—	120	—		

Source-Drain Diode Ratings and Characteristics

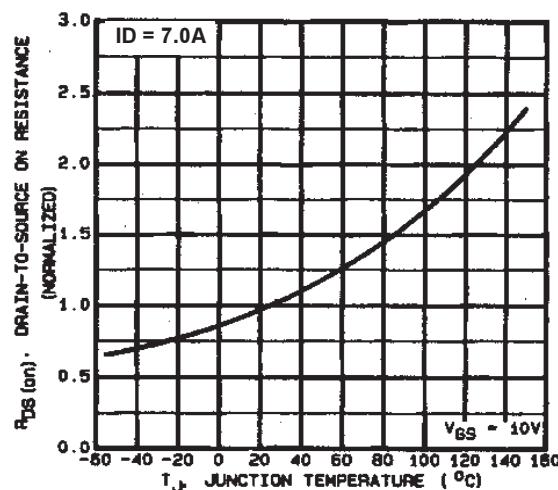
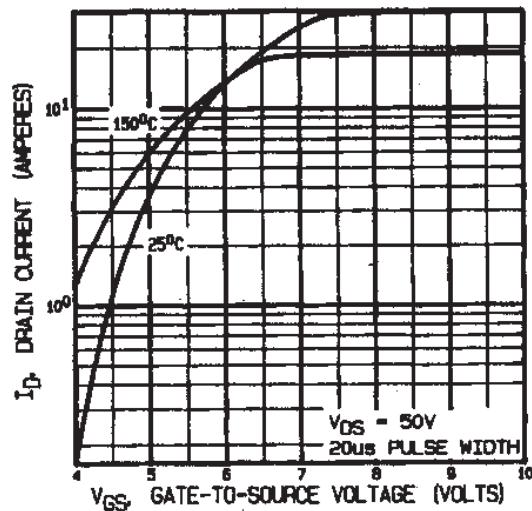
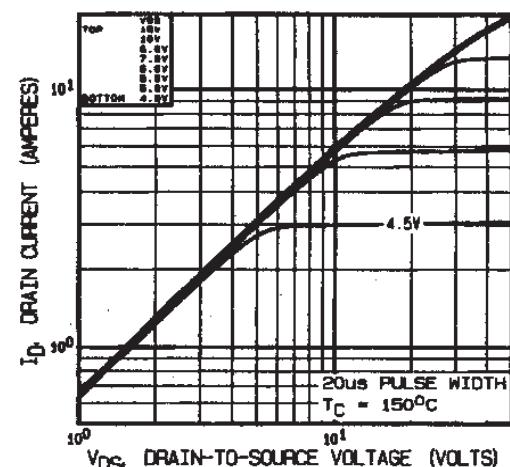
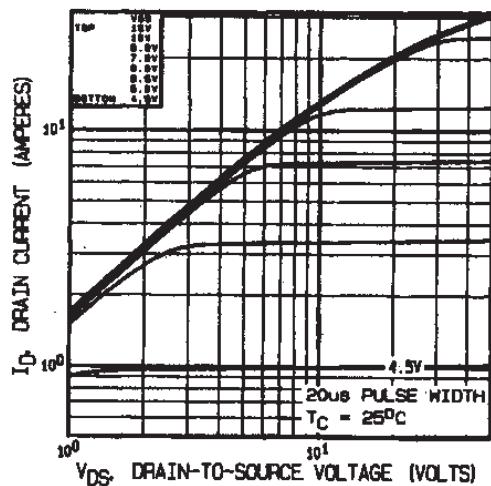
	Parameter	Min	Typ	Max	Units	Test Conditions
I_{S}	Continuous Source Current (Body Diode)	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	28		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$\text{T}_j = 25^\circ\text{C}, \text{I}_{\text{S}} = 7.0\text{A}, \text{V}_{\text{GS}} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	—	700	nS	$\text{T}_j = 25^\circ\text{C}, \text{I}_{\text{F}} = 7.0\text{A}, \text{dI}/\text{dt} \leq 100\text{A}/\mu\text{s}$ $\text{V}_{\text{DD}} \leq 50\text{V}$ ④
Q_{RR}	Reverse Recovery Charge	—	—	8.9	μC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $\text{L}_{\text{S}} + \text{L}_{\text{D}}$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	1.25	$^\circ\text{C}/\text{W}$	
R_{thCS}	Case-to-sink	—	0.21	—		
R_{thJA}	Junction-to-Ambient	—	—	80		Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page



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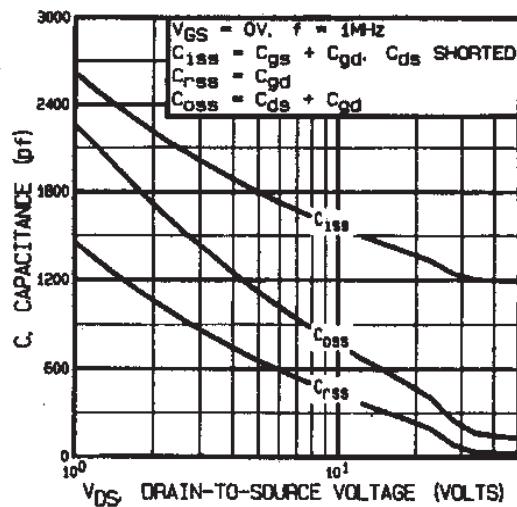


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

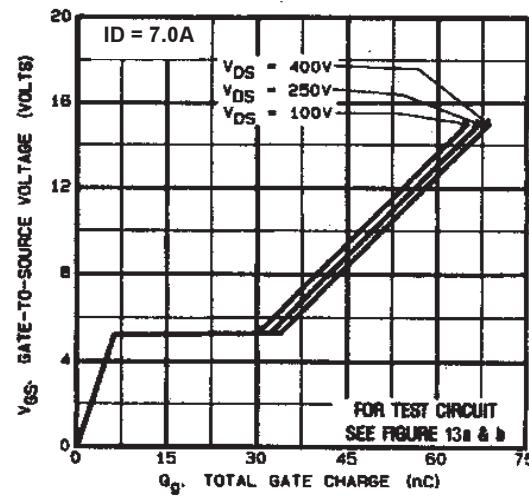


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

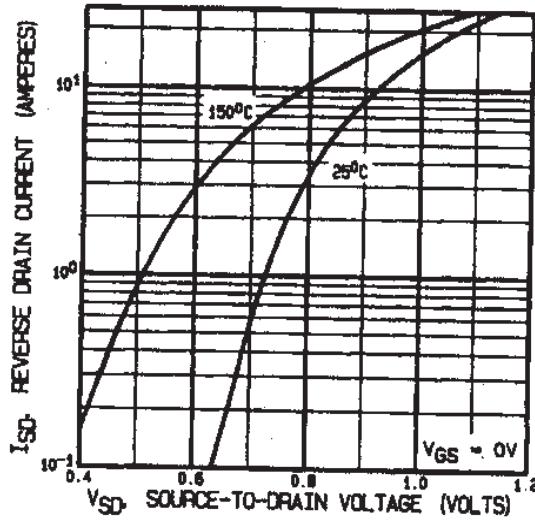


Fig 7. Typical Source-Drain Diode
Forward Voltage

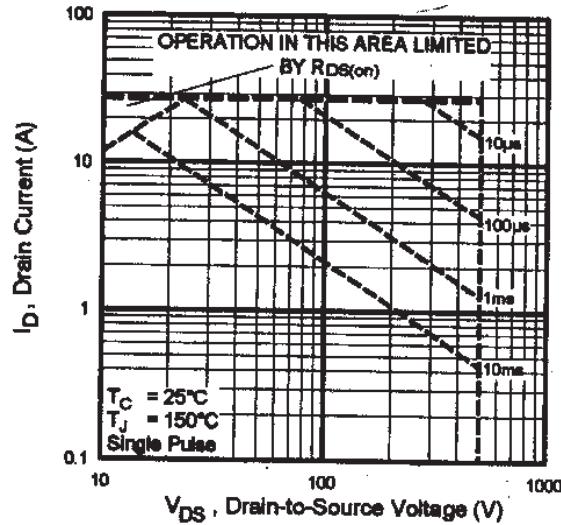


Fig 8. Maximum Safe Operating Area

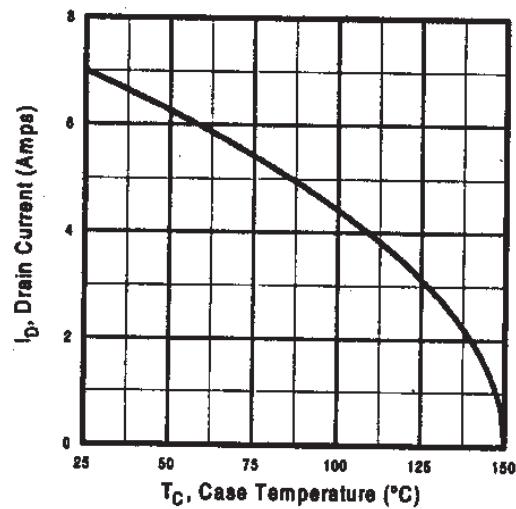


Fig 9. Maximum Drain Current Vs.
Case Temperature

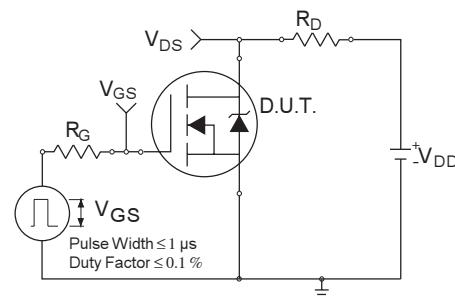


Fig 10a. Switching Time Test Circuit

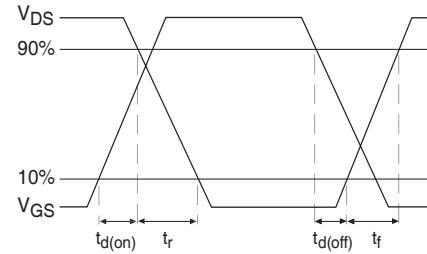


Fig 10b. Switching Time Waveforms

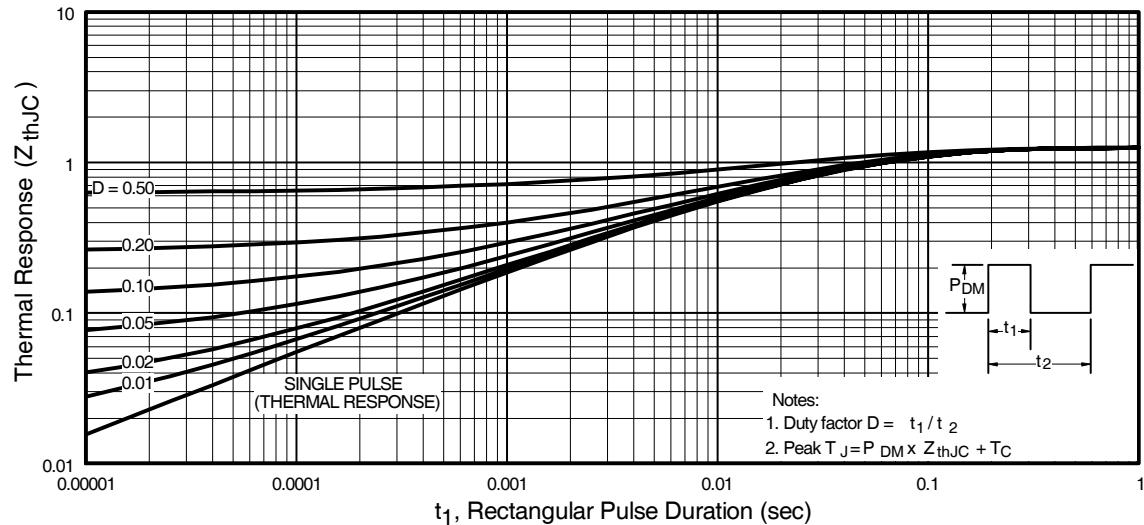


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

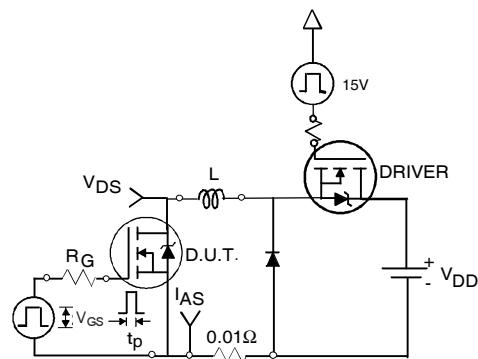


Fig 12a. Unclamped Inductive Test Circuit

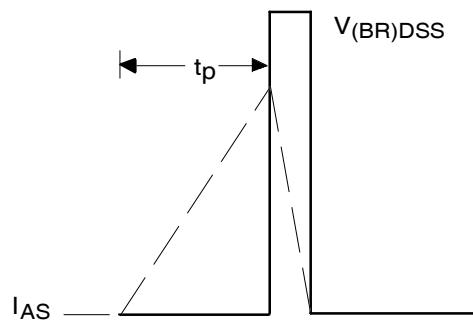
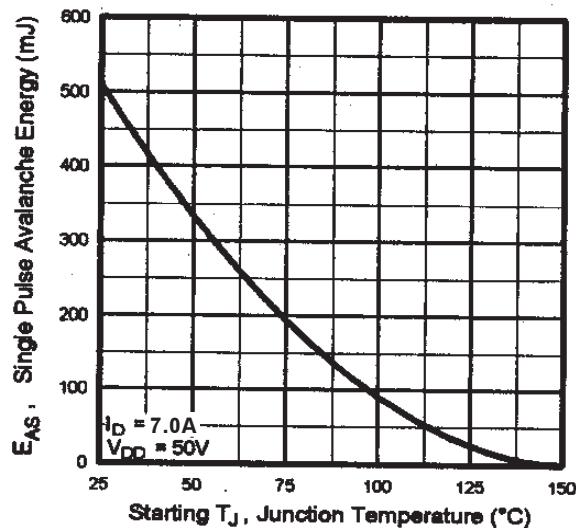


Fig 12b. Unclamped Inductive Waveforms

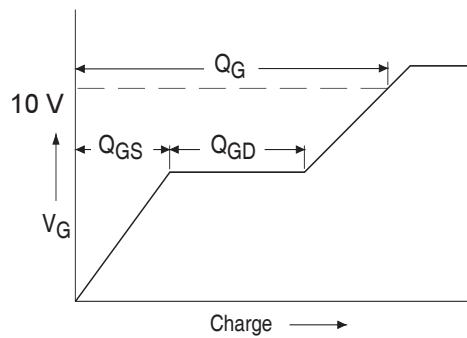


Fig 13a. Basic Gate Charge Waveform

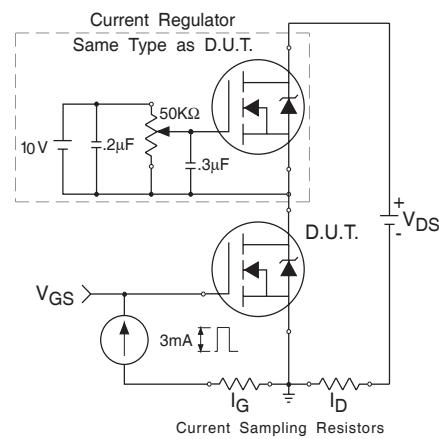


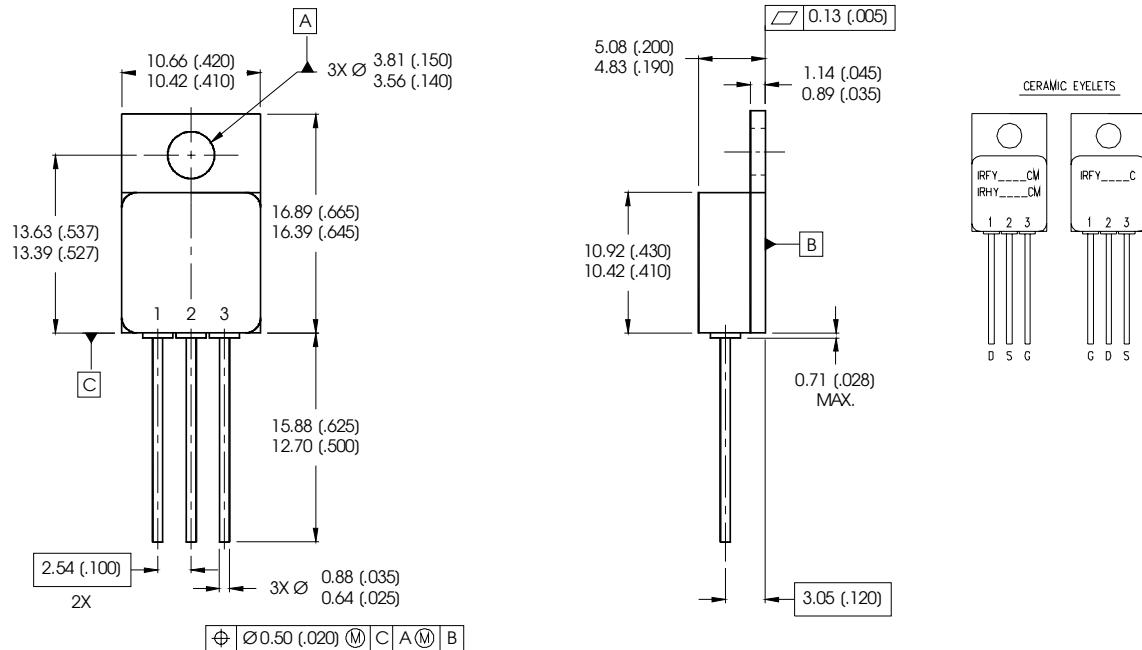
Fig 13b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 20mH$
Peak $I_L = 7.0A$, $V_{GS} = 10V$

- ③ $I_{SD} \leq 7.0A$, $di/dt \leq 100A/\mu s$,
 $V_{DD} \leq 500V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — TO-257AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA

LEGEND

D - DRAIN
S - SOURCE
G - GATE

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

IR LEOMINSTER : 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776

TAC Fax: (310) 252-7903

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Data and specifications subject to change without notice. 05/2005