Platform Manager 2

In-System Programmable Hardware Management Controller

Data Sheet

FPGA-DS-02036-2.3

August 2021

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1. Features

1.1. Ten Rail Voltage Monitoring and Measurement

- UV/OV Fault Detection Accuracy – 0.2% Typ.
- Fault Detection Speed <100 µs
- High Voltage, Single Ended and Differential Sensing

1.2. Two Channel Wide-Range Current Monitoring and Measurement

- High-side current Measurement up to 12 V
- Programmable OC/UC Fault Detect
- Detects Current faults in < 1 µs

1.3. Three Temperature Monitoring and Measurement Channels

- Programmable OT/UT Faults Threshold
- Two channels of Temperature Monitoring using external diodes
- One On-Chip Temperature Monitor

1.4. Four High-Side MOSFET Drivers

- Programmable Charge Pump

1.5. Four Precision Trim and Margin Channels

- Closed Loop Operation
- Voltage Scaling and VID Support

1.6. Ten General Purpose Input / Output

- 5 V tolerant I/O

1.7. Non-Volatile Fault Logging

1.8. Programmed through JTAG or I^2C

- Background Update with Dual-Boot Backup

1.9. FPGA Resources

- 1280 LUT, 98 I/O Version (LPTM21)
- 1280 LUT, 33 I/O Version (LPTM21L)

1.10. RAM and Flash Memories

1.11. Scalable Hardware Management Architecture

- Glueless interface to Hardware Management Expander (L-ASC10)
- Migrate between LPTM21 and larger density MachXO2™, MachXO3™, and ECP5™ devices to extend logic and I/O resources

1.12. System Level Support

- Operating voltage from 2.8 V to 3.46 V
- Industrial and commercial temperature ranges
- 237-ball ftBGA (LPTM21)
- 100-ball caBGA (LPTM21L)
- RoHS compliant and halogen-free

1.13. Applications

- Telecommunication and Networking
- Industrial, Test and Measurement
- Medical Systems
- Servers and Storage Systems
- High Reliability Systems

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2. Application Diagram

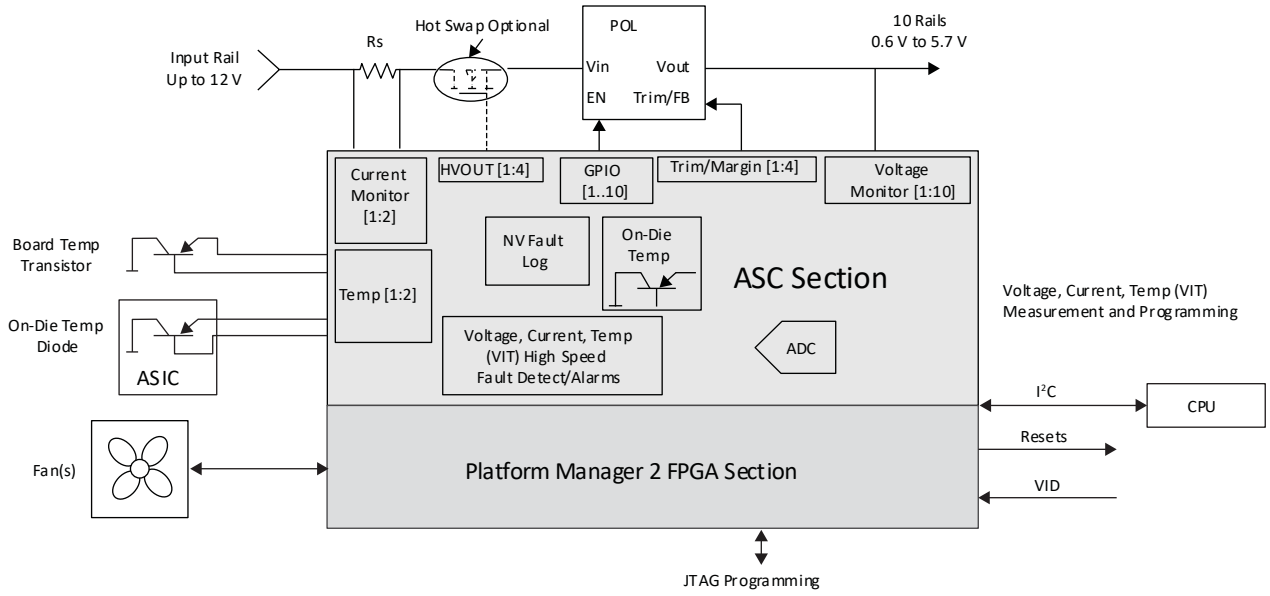

Figure 2.1. Hardware Management Application Block Diagram

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3. Description

The Lattice Platform Manager 2 device is a fast-reacting, programmable logic based hardware management controller. Platform Manager 2 is an integrated solution combining analog sense and control elements with scalable programmable logic resources. This unique approach allows Platform Manager 2 to integrate Power Management (Power Sequencing, Voltage Monitoring, Trimming and Margining), Thermal Management (Temperature Monitoring, Fan Control, Power Control), and Control Plane functions (System Configuration, I/O Expansion, etc.) as a single device.

Architecturally, the Platform Manager 2 device can be divided into two sections – Analog Sense and Control and FPGA. The Analog Sense and Control (ASC) section provides three types of analog sense channels: voltage (nine standard channels and one high voltage channel), current (one standard voltage and one high voltage) and temperature (two external and one internal).

Each of the analog sense channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. In addition, each of the current sense channels provides a fast fault detect (one µs response time) for detecting short circuit events. The temperature sense channels can be configured to work with different external transistor or diode configurations.

The Analog Sense and Control section also provides ten general purpose 5 V tolerant open-drain digital input/output pins that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for general purpose logic interface functions. In addition, four high-voltage charge pumped outputs (HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers to control high-side MOSFET switches. These HVOUT outputs can also be programmed as static output signals or as switched outputs (to support external charge pump implementation) operating at a dedicated duty cycle and frequency.

The ASC section incorporates four TRIM outputs for controlling the output voltages of DC-DC converters. Each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode of the trimming block.

The internal 10-bit A/D converter can be used to measure the voltage and current through the I^2C bus. The ADC is also used in the digital closed loop control mode of the trimming block.

The ASC section also provides the capability of logging up to 16 status records into its nonvolatile EEPROM memory. Each record includes voltage, current and temperature monitor signals along with digital input and output levels.

The ASC section includes an output control block (OCB) which allows certain inputs and control signals a direct connection to the digital outputs or HVOUTs, bypassing the ASC-I/F for a faster response. The OCB is used to connect the fast current fault detect signal to an FPGA input directly. It also supports functions such as Hot Swap with a programmable hysteretic controller.

The FPGA section contains non-volatile low cost programmable logic of 1280 Look-Up Tables (LUTs). In addition to the LUT-based logic, the FPGA section features Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), flexible I/Os, and hardened versions of commonly used functions such as SPI controller, I^2C controller and Timer/counter. The FPGA I/Os offer enhanced features such as drive strength control, slew rate control, buskeeper latches, internal pull-up or pull-down resistors, and open-drain outputs. These features are controllable on a “per-pin” basis.

The power management, thermal management and control plane logic functions are implemented in the FPGA section of Platform Manager 2. The FPGA receives the analog comparator values and inputs from the ASC section and sends output commands to the ASC section through the dedicated ASC-interface (ASC-I/F) high-speed, reliable serial channel. The FPGA hardware management functions are implemented using the Platform Designer tool inside Lattice Diamond software. The Platform Designer tool includes an easy to use sequence and monitor logic builder tool and a set of pre-engineered components for functions like time-stamped fault logging, voltage by identification (VID), and fan control.

The Platform Manager 2 is designed to enable seamless scaling of the number of voltage, current and temperature sense channels in the system by adding external Hardware Management Expanders. Hardware Management Expanders can be realized with either the Analog Sense and Control (ASC) L-ASC10 device or the LPTM21L (100-Ball caBGA package) device. The algorithm implemented within the FPGA section can access and control these external ASCs through the dedicated ASC-I/F. Larger systems with up to eight expanders can be created by using a MachXO2, MachXO3, or ECP5 FPGA in place of the Platform Manager 2 device. The expander devices are connected in a scalable, star topology to Platform Manager 2, MachXO2, MachXO3, or ECP5.

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The Platform Manager 2 has an I^2C interface which is used by the FPGA section for ASC interface configuration. The I^2C interface also provides the mechanism for parameter measurement or I/O control or status. For example, voltage trim targets can be set over the I^2C bus and measured voltage, current, or temperature values can be read over the I^2C bus.

The Platform Manager 2 device can be programmed in-system through JTAG or I^2C interfaces. The configuration is stored in on-chip non-volatile memory. Upon power-on, the FPGA section configuration is transferred to the on-chip SRAM and the device operates from SRAM. It is possible to update the non-volatile memory content in the background without interrupting the system operation.

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4. Block Diagram

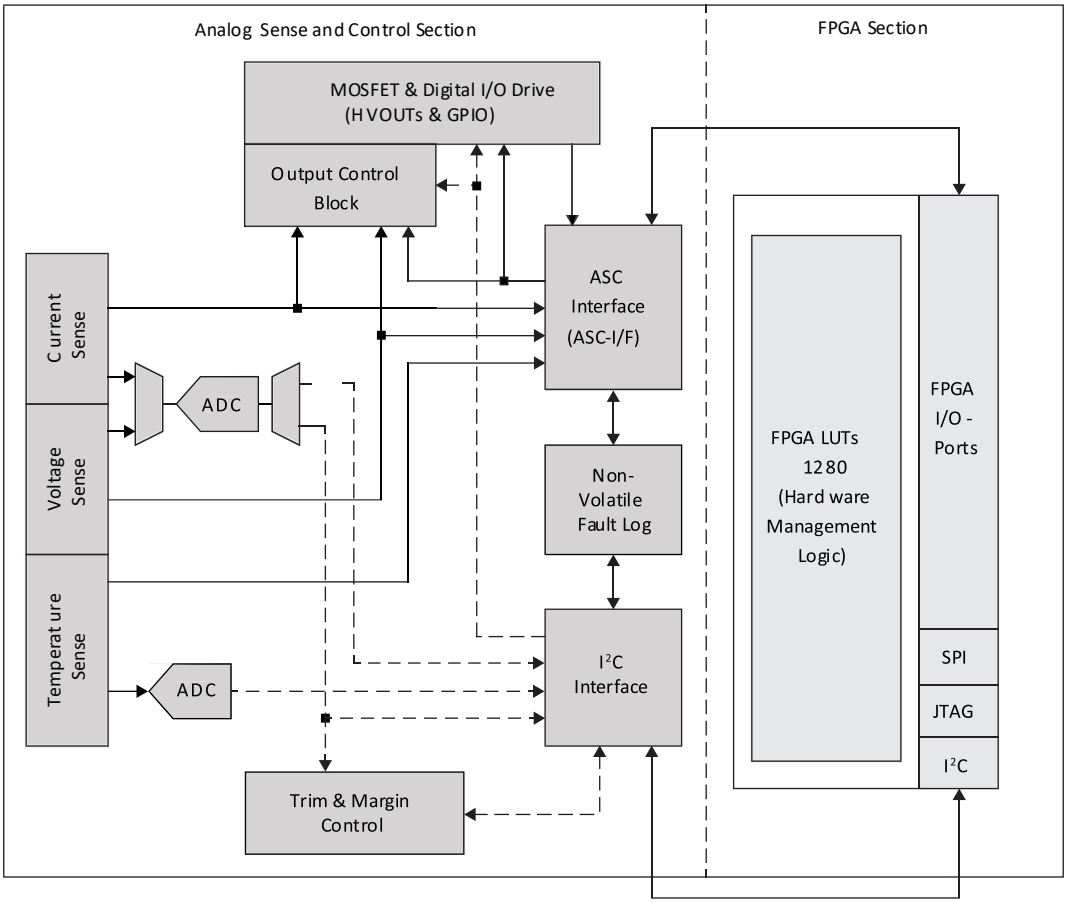

Figure 4.1. Platform Manager 2 Block Diagram

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Table 4.1. Platform Manager 2 Device Features

	LPTM21	LPTM21L
Analog Sense and Control Section		
Voltage Monitor Inputs	10	10
Current Monitor Inputs	2	2
Temperature Monitor Inputs	2	2
Trim Outputs	4	4
High Voltage Outputs	4	4
GPIO pins (5 V tolerant)	10	10
FPGA Section		
LUTs	1280	1280
Digital I/O Count (PIO)1	95	32
Primary Clock Inputs (PCLK)	6	4
Distributed RAM (Kbits)	10	10
EBR SRAM (Kbits)	64	64
Number of EBR SRAM Blocks (9 Kbits/block)	7	7
UFM (Kbits)	64	64
Hardened Functions		
I^2C	2	2
SPI	1	1
Timer/Counter	1	1
Packaging (Both Sections)		
Balls	237	100
Size	ftBGA (17 mm x 17 mm)	caBGA (10 mm x 10 mm)

Note: Digital I/O count does not include SDA_M, SCL_M or JTAGENB pins.

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5. DC and Switching Characteristics

5.1. Absolute Maximum Ratings

Table 5.1. Absolute Maximum Ratings[1, 2, 3]

Symbol	Parameter	Conditions	Min	Max.	Units
Supply Voltages					
V_{CCA}	ASC Supply	—	–0.5	3.75	V
V_{CC}	FPGA Core Supply Voltage4	—	–0.5	3.75	V
V_{CCIO}	FPGA Output Supply Voltage4	—	–0.5	3.75	V
Monitor and I/O Pin Voltages					
V_{IN_VMON}	VMON input voltage	—	–0.5	6	V
V_{IN_VMONGS}	VMON input voltage ground sense	—	–0.5	6	V
V_{IN_HIMONP}	High voltage IMON input voltage	—	–0.5	13.3	V
$V_{IN\_HIMONN\_HVMON}$	High voltage IMON return / VMON input voltage	—	–0.5	13.3	V
V_{DIFF_HIMON}	High voltage IMON differential voltage	—	–2.0	2.0	V
V_{IN_IMONP}	Low voltage IMON1 input voltage	—	–0.5	6.0	V
V_{IN_IMONN}	Low voltage IMON1 return voltage	—	–0.5	6.0	V
V_{DIFF_IMON}	Low voltage IMON1 differential voltage	—	–2.0	2.0	V
V_{IN_TMONP}	TMON input voltage	—	–0.5	VCCA	V
V_{IN_TMONN}	TMON return voltage	—	–0.5	VCCA	V
V_{IN_GPIO}	Digital input voltage (ASC Section)	—	–0.5	6	V
V_{OUT}	Open-drain output voltage (ASC Section)	HVOUT [1:4]	–0.5	13.3	V
		GPIO[1:10]	–0.5	6	V
V_{TRIM}	TRIM output voltage	—	–0.5	VCCA	V
V_{TRI_FPGA}	FPGA PIO Tri-State Voltage Applied[5, 4]	—	–0.5	3.75	V
V_{IN_FPGA}	FPGA PIO Dedicated Input Voltage Applied[4]	—	–0.5	3.75	V
Other					
$I_{SINKMAX}$	Maximum Sink Current on any ASC Section output	—	—	23	mA
T_S	Device Storage Temperature (Ambient)	—	–55	+125	°C
T_J	Junction Temperature	—	–40	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of –2 V to (VIHMAX +2) volts is permitted for a duration of < 20 ns.
5. The dual function I^2C pins SCL_M and SDA_M are limited to –0.25 to 3.75 V or to –0.3 V with a duration of < 20 ns.

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5.2. Recommended Operating Conditions

Table 5.2. Recommended Operating Conditions[1]

Symbol	Parameter	Conditions	Min	Max.	Units
Supply Voltages					
V_{CCA}	ASC Supply	—	2.8	3.465	V
V_{CC}	FPGA Core Supply Voltage	—	2.8	3.465	V
V_{CCIO}[2, 3]	FPGA Output Supply Voltage	—	1.14	3.465	V
Monitor and I/O Pin Voltages					
V_{IN_VMON}	VMON input voltage	—	–0.3	5.9	V
V_{IN_VMONGS}	VMON input voltage ground sense	—	–0.2	0.3	V
V_{IN_HIMONP}	High voltage IMON input voltage[4]	—	4.5	13.2	V
$V_{IN\_HIMONN\_HVMON}$	High voltage IMON return /VMON voltage[4]	—	4.5	13.2	V
V_{DIFF_HIMON}	High voltage IMON differential voltage	—	0	500	mV
V_{IN_IMONP}	Low voltage IMON1 input voltage	Low Side Sense Disabled	0.6	5.9	V
		Low Side Sense Enabled	–0.3	1.0	V
V_{IN_IMONN}	Low voltage IMON1 return voltage	Low Side Sense Disabled	0.6	5.9	V
		Low Side Sense Enabled	–0.3	1.0	V
V_{DIFF_IMON}	Low voltage IMON1 differential voltage	—	0	500	mV
V_{IN_GPIO}	Digital input voltage (ASC Section)	—	–0.3	5.5	V
V_{OUT}	Open-drain output voltage (ASC Section)	HVOUT [1:4]	–0.3	13.2	V
		GPIO[1:10]	–0.3	5.5	V
Other					
T_{JCOM}	Junction Temperature (Commercial)	—	0	+85	°C
T_{JIND}	Junction Temperature (Industrial)	—	–40	+100	°C

Notes:

1. Like power supplies must be tied together. For example, if VCCIO and VCC are both the same voltage, they must also be the same supply. VCCA, VCC, VCCIO0 and VCCIO1 should all be tied together. See the System Connections section for more details.
2. See recommended voltage by I/O standard in subsequent table.
3. VCCIO pins of unused I/O banks should be connected to the VCC power supply on boards.
4. HIMON circuits are operational down to 3 V. Accuracy is guaranteed within Recommended Operating Conditions.

5.3. Power Supply Ramp Rates

Table 5.3. Power Supply Ramp Rates

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all VCC and VCCIO power supplies.	0.01	—	100	V/ms

Note: Assumes monotonic ramp rates.

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5.4. Power-On-Reset and Flash Download Time

Table 5.4. Power-On-Reset and Flash Download Time

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Analog Sense and Control Section						
T_{RST}	Delay from VTH to start-up state	—	—	—	100	us
T_{SAFE}	Delay from RESETb release to ASC Safe State Exit and I/O Release[2, 3]	—	—	1.8	—	ms
T_{SAFE2}	Delay from WRCLK start to ASC Safe State Exit and I/O Release[2, 3, 4]	—	56	—	—	us
T_{GOOD}	Delay from I/O release to AGOOD asserted high in FPGA section[5]	—		16	—	us
T_{BRO}	Minimum duration brown out required to trigger RESETb	—	1	—	5	us
T_{POR}	Delay from Brown out to reset state	—		—	13	us
V_{TL}	Threshold below which RESETb is LOW	—		—	2.3	V
V_{TH}	Threshold above which RESETb is Hi-Z	—	2.7	—	—	V
V_T	Threshold above which RESETb is valid	—	0.8	—	—	V
C_L	Capacitive load on RESETb	—		—	200	pF
FPGA Section						
$V_{CC\_PORUPEXT}$[1]	Power-On-Reset ramp up trip point (external VCC power supply)	—	1.5	—	2.1	V
$V_{PORUPIO}$[1]	Power-On_Reset ramp up trip point (VCCIO0 power supply)	—	0.9	—	1.06	V
$T_{refresh}$[6]	Flash Download Time (Power-On-Reset to Device I/O active)	—	—	1.9	—	ms

Notes:

1. These POR trip points are provided for guidance only. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Both T_{SAFE} and T_{SAFE2} must complete before I/O are released from Safe State.
3. During the calibration period before T_{SAFE} and T_{SAFE2}, the ASC may ignore RESETb being driven low. After T_{SAFE} and T_{SAFE2}, the ASC can be reset by another device by driving RESETb low.
4. Safe State is released at ASC after a fixed number (64) of WRCLK cycles (typ.8 MHz frequency) and three ASC-I/F data packets are properly detected.
5. AGOOD asserted in the FPGA section on the next ASC-I/F packet after I/O exits Safe State as ASC.
6. FPGA section flash download time has a direct influence on WRCLK start time. See Figure 4.1.

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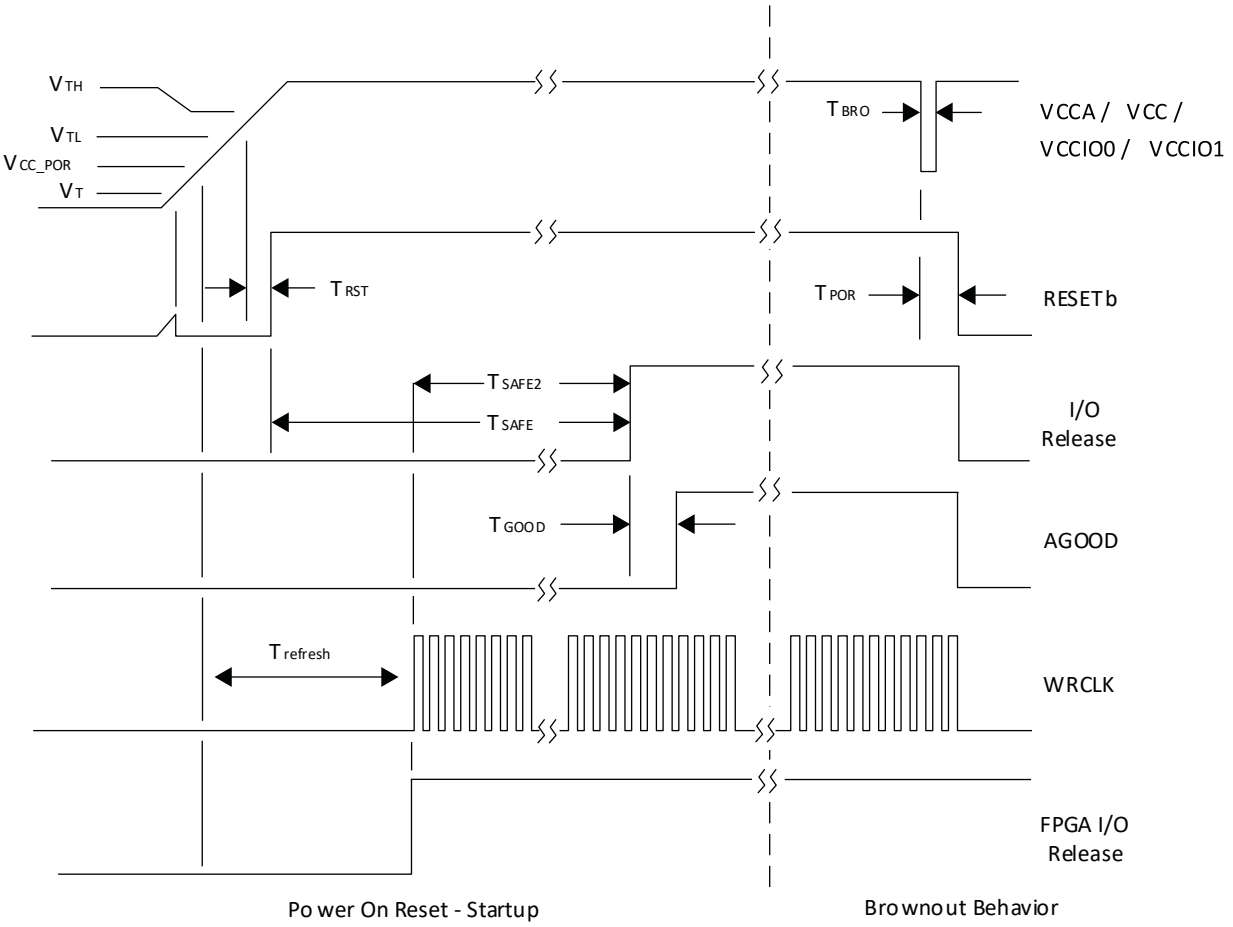

Figure 5.1. Platform Manager 2 Power-On Reset

5.5. DC Electrical Characteristics

Table 5.5. DC Electrical Characteristics

Symbol	Parameter	Min	Typ[5]	Max.	Units
I_{CCA}	Supply Current (Analog Section)	—	25	35	mA
$I_{CC-HVOUT}$	Supply Current Adder per HVOUT, VHVOUT = 12 V, Isrc = 100 uA	—	—	2	mA
I_{CC}[1,2,3,4]	Static Core Supply Current (FPGA Section)	—	3.49	—	mA
I_{CCIO}[1,2,3,4,6]	Static Bank Power Supply, VCCIO = 2.5 V	—	500	—	µA

Notes:

1. For further information on FPGA section supply current, please see details of additional technical documentation at the end of this datasheet.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. To determine the FPGA section peak start-up current data, use the Power Calculator tool.
5. Tj = 25C, power supplies at nominal voltage.
6. Does not include pull-up/pull-down.

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5.6. Programming and Erase Supply Current

Table 5.6. Programming and Erase Supply Current

Symbol	Parameter	Min	Typ5	Max.	Units
I_{CCA}	Supply Current (Analog Section)	—	—	40	mA
I_{CC}[1,2,3,4]	Core Supply Current (FPGA Section)	—	18.8	—	mA
I_{CCIO}[1,2,3,4,6]	Bank Power Supply, VCCIO = 2.5 V	—	500	—	µA

Notes:

1. For further information on FPGA section supply current, please see details of additional technical documentation at the end of this datasheet.
2. Assumes all FPGA section inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. Tj = 25C, power supplies at nominal voltage.
6. Per bank, does not include pull-up/pull-down.

5.7. FPGA Configuration Memory Programming / Erase Specifications

Table 5.7. FPGA Configuration Memory Programming / Erase Specifications

Symbol	Parameter	Min.	Max1	Units
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100°C junction temperature	10	—	Years
	Data retention at 85°C junction temperature	20	—	

Note: Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

5.8. FPGA I/O Hot Socketing Specifications

Table 5.8. FPGA I/O Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/–1000	µA

Notes:

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

5.9. ESD Performance

Please refer to the Platform Manager 2 Product Family Qualification Summary for complete qualification data, including ESD performance.

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5.10. Digital Specifications

Table 5.9. Digital Specifications

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Analog Sense and Control Section						
I_{IL},I_{IH}	Input leakage, no pull-up, pull-down[7]	—	—	—	+/ 10	µA
I_{PD}	Active Pull-Down Current[7]	GPIO[1:10] configured as Inputs, Internal Pull-Down enabled	—	200	—	µA
$I_{PD-ASCIF}$	Input Leakage (WDAT and WRCLK)[8]	Internal Pull-Down	—	175	—	µA
$I_{OH-HVOUT}$	Output Leakage Current	HVOUT[1:4] in open drain mode and pulled up to 12 V	—	35	100	µA
$I_{PU-RESETb}$	Input Pull-Up Current (RESETb)	—	—	–50	—	µA
V_{IL}	Voltage input, logic low	GPIO[1:10]	—	—	0.8	V
		SCL_S/SDA_S	—	—	30% V_{CCA}	
V_{IH}	Voltage input, logic high	GPIO[1:10]	2.0	—	—	V
		SCL_S/SDA_S	70% V_{CCA}	—	—	
V_{OL}	HVOUT[1:4] (open drain mode)	ISINK = 10 mA	—	—	0.8	V
	GPIO[1:10]	ISINK = 20 mA	—	—	0.8	
$I_{SINKTOTAL}$[6]	All digital outputs	—	—	—	130	mA
FPGA Section – Programmable I/O						
I_{IL},I_{IH}[1,4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and VCCIO –0.97 V < V_{IN} < V_{CCIO}	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} –0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < V_{IN} < V_{CCIO}	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0< V_{IN} < 0.7 V_{CCIO}	–30	—	–309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < V_{IN} < V_{CCIO}	30	—	305	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCIO}	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points	—	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V V_{CC} = Typ. V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pF
C2	Dedicated Input Capacitive	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V V_{CC} = Typ. V_{IO} = 0 to V_{IH} (MAX)	3	5.5	7	pF

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Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
V_{HYST}	Hysteresis for Schmitt Trigger Inputs5	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysI/O Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the highto-low transition. For true LVDS output pins in the FPGA section, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to MachXO2 sysI/O Usage Guide (FPGA-TN-02158).
6. Sum of maximum current sink from all digital outputs combined. Reliable operation is not guaranteed if this value is exceeded.
7. During safe-state, all GPIO default to output, see the Safe State section for more details. GPIO[1:6] and GPIO[10] default to active low output. This will result in a leakage current dependent on the input voltage which can exceed the specified input leakage
8. WRCLK and WDAT pins may see transients above 1 mA in hot socket conditions. DC levels will remain below 1 mA.

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5.11. Voltage Monitors

Table 5.10. Voltage Monitors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{VMON_in}	Input Resistance	—	55	65	75	kΩ
C_{VMON_in}	Input Capacitance	—	—	8	—	pF
V_{MON} Range	Programmable trip-point Range	—	0.075		5.734	Volts
V_{MON} Accuracy	Absolute accuracy of any trip-point – Differential VMON pins	VMON voltage > 0.650 V	—	0.2	0.7	%
	Single-ended VMON pins	VMON voltage > 0.650 V	—	0.3	0.9	%
V_{MON} HYST	Hysteresis of any trip-point (relative to setting)	—	—	1	—	%
V_{MON} CMR	Differential VMON Common mode rejection ratio	—	—	60	—	dB
V_Z Sense	Low Voltage Sense Trip Point Error – Differential VMON1-4	Trip Point = 0.075 V	–5		+5	mV
		Trip Point = 0.150 V	–5	—	+5	mV
		Trip Point = 0.300 V	–10	—	+10	mV
		Trip Point = 0.545 V	–15	—	+15	mV
	Low Voltage Sense Trip Point Error – Single-Ended VMON5-9	Trip Point = 0.080 V	–10	—	+10	mV
		Trip Point = 0.155 V	–15	—	+15	mV
		Trip Point = 0.310 V	–25	—	+25	mV
		Trip Point = 0.565 V	–55	—	+55	mV
High Voltage Monitor						
H_{VMON} Range	High Voltage VMON programmable trip-point range	—	0.3	—	13.2	Volts
H_{VMON} Accuracy	HVMON Absolute accuracy of any trip-point	HVMON voltage > 1.8 V	—	0.4	1.0	%
V_Z Sense	Low Voltage Sense Trip Point Error - HVMON pin	Trip Point = 0.220 V	–20	—	+20	mV
		Trip Point = 0.425 V	–35	—	+35	mV
		Trip Point = 0.810 V	–75	—	+75	mV
		Trip Point = 1.280 V	–130	—	+130	mV

Note: VMON accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details.

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5.12. Current Monitors

Table 5.11. Current Monitors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IMONPleak}$	IMON1P input leakage	Low Side Sense Disabled Fast Trip Point V_{sns} = 500 mV	–2	—	250	µA
		Low Side Sense Enabled Fast Trip Point V_{sns} = 500 mV	–2	—	40	µA
$I_{IMONNleak}$	IMON1N input leakage	Low Side Sense Disabled Fast Trip Point V_{sns} = 500 mV	–2	—	2	µA
		Low Side Sense Enabled Fast Trip Point V_{sns} = 500 mV	–200	—	2	µA
$I_{HIMONPleak}$	HIMONP input leakage	Fast Trip Point V_{sns} = 500 mV	—	—	550	µA
$I_{HIMONNleak}$	HIMONN_HVMON input leakage	—	—	—	350	µA
$I_{MONA/B}$ Accuracy[2]	HIMON, IMON1A/B Comparator Trip Point accuracy	Gain = 100x	—	8	—	%
		Gain = 50x	—	5	—	%
		Gain = 25x	—	3	—	%
		Gain = 10x	—	2	—	%
$I_{MONA/B}$ Gain	Programmable Gain Setting	Four settings in software	—	10	—	V/V
			—	25	—	V/V
			—	50	—	V/V
			—	100	—	V/V
I_{MONF} Accuracy[2]	Fast comparator trip-point accuracy	V_{sns}[1] = 50 mV, 100 mV, or 150 mV	—	8	—	%
		V_{sns} = 200 mV, 250 mV, or 300 mV	—	5	—	%
		V_{sns} = 400 mV or 500 mV	—	3	—	%
t_{IMONF}	Fast comparator response time	—	—	—	1	µs

Notes:

1. V_{sns} is the differential voltage between IMON1P and IMON1N (or HIMONP and HIMONN).
2. IMON accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details.

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5.13. ADC Characteristics

Table 5.12. ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution	—	—	10	—	Bits
$t_{CONVERT}$	Conversion Time from I^2C Request	—	—	—	200	µs
Voltage Monitors						
$V_{VMON-IN}$	Input Range Full scale	Programmable Attenuator = 1	0	—	2.048	V
		Programmable Attenuator = 3	0	—	5.91	
LSB	ADC Step Size	Programmable Attenuator = 1	—	2	—	mV
		Programmable Attenuator = 3	—	6	—	
$E_{VMON-attenuator}$	Error due to attenuator	Programmable Attenuator = 3	—	+/– 0.1	—	%
High Voltage Monitor						
$V_{HVMON-IN}$	Input Range Full scale	Programmable Attenuator = 4	0	—	8.192	V
		Programmable Attenuator = 8	0	—	13.21	
LSB	ADC Step Size	Programmable Attenuator = 4	—	8	—	mV
		Programmable Attenuator = 8	—	16	—	
$E_{HVMON-attenuator}$	Error due to attenuator	Programmable Attenuator = 4	—	+/–0.2	—	%
		Programmable Attenuator = 8	—	+/–0.4	—	%
Current Monitors						
$t_{IMON-sample}$	Sample period of HVIMON and IMON1 conversions for averaged value	4 Settings via I^2C command	—	1	—	ms
			—	2	—	
			—	4	—	
			—	8	—	
$V_{IMON-IN}$	Input Range Full scale1	Programmable Gain 10x	0	—	200	mV
		Programmable Gain 25x	0	—	80	
		Programmable Gain 50x	0	—	40	
		Programmable Gain 100x	0	—	20	
LSB	ADC Step Size	Programmable Gain 10x	—	0.2	—	mV
		Programmable Gain 25x	—	0.08	—	
		Programmable Gain 50x	—	0.04	—	
		Programmable Gain 100x	—	0.02	—	

Note: Differential voltage applied across HIMONP/IMON1P and HIMONN/IMO1N before programmable gain amplification.

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5.14. ADC Error Budget Over Entire Operating Temperature Range

Table 5.13. ADC Error Budget Over Entire Operating Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TADC Error	Total ADC Measurement Error at Any Voltage (Differential Analog Inputs)[1, 3]	Measurement Range 600 mV - 2.048 V, VMONxGS > -100 mV, Attenuator =1	–8	+/– 4	8	mV
		Measurement Range 600 mV - 2.048 V, VMONxGS > –200 mV, Attenuator =1	—	+/– 6	—	mV
		Measurement Range 0 - 2.048 V, VMONxGS > –200 mV, Attenuator =1	—	+/– 10	—	mV
	Total Measurement Error at Any Voltage (Single-Ended Analog Inputs including IMON)[1, 2, 3]	Measurement Range 600 mV - 2.048 V, Attenuator =1	–8	+/– 4	8	mV

Notes:

1. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specs of the ADC.
2. Programmable gain error on IMON not included.
3. ADC accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details.

5.15. Temperature Monitors

Table 5.14. Temperature Monitors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{MON_REMOTE} Accuracy[1, 7]	Temp Error – Remote Sensor	Ta = –40 to +85oC Td = –64 to 127oC	—	1	—	°C
T_{MON_INT} Accuracy[7]	Internal Sensor – Relative to ambient[6]	Ta=–40 to +85 oC	—	1	—	°C
Resolution		—	—	0.25	—	°C
T_{MON} Range	Programmable threshold range	—	–64	—	155	°C
T_{MON} Offset	Temperature offset	Programmable in software	–63.75	—	63.75	°C
T_{MON} Hysteresis	Hysteresis of trip points	Programmable in software	0	—	63	°C
t_{TMON_settle}[2]	Temperature measurement settling time[3]	Measurement Averaging Coefficient = 1	—	15	—	ms
		Measurement Averaging Coefficient = 8	—	120	—	ms
		Measurement Averaging Coefficient = 16	—	240	—	ms
Tn	Ideality Factor ***n***	Programmable in software	0.9	—	2	—
T_{limit}	Temperature measurement limit[4]	—	—	—	160	°C
C_{TMON}	Maximum Capacitance between T_{MONP} and T_{MONN} pins	—	—	—	200	pF
$R_{TMONSeries}$	Equivalent external resistance to sensor[5]	—	—	—	200	Ω

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Notes:

1. Accuracy number is valid for the use of a grounded collector PNP configuration, programmed with proper ideality factor, and 16x measurement filter enabled. Any other device or configuration can have additional errors, including beta, series resistance and ideality factor accuracy. See Temperature Monitor Inputs section for more details.
2. Settling time based on one T_{MON} enabled. For multiple T_{MON}s, settling time can be multiplied by the number of enabled T_{MON} channels.
3. Settling time is defined as the time is takes a step change to settle to within 1% of the measured value.
4. All values above Tlimit read as 0x3FF over I^2C. There is no cold temperature limiting reading, although performance is not specified below –64°C.
5. This is the maximum series resistance which the T_{MON} circuit can compensate out. Equivalent series resistance includes all board trace wiring (T_{MONP} and T_{MONN}) as well as parasitic base and emitter resistances. Re=1/gm should not be included as part of series resistance.
6. Internal sensor is subject to self-heating, dependent on PCB design and device configuration. Self-heating not included in published accuracy.
7. T_{MON} accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details.

5.16. High Voltage FET Drivers

Table 5.15. High Voltage FET Drivers

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PP}	Gate driver output voltage	Four settings in software	—	12	—	Volts
			—	10	—	
			—	8	—	
			—	6	—	
I_{OUTSRC}	Gate driver source current (HIGH state)	Four settings in software	—	12.5	—	µA
			—	25	—	
			—	50	—	
			—	100	—	
$I_{OUTSINK}$	Gate driver sink current (LOW state)	Four settings in software	—	100	—	µA
			—	250	—	
			—	500	—	
			—	3000	—	
Frequency	Switched Mode Frequency	Two settings in software	—	15.625	—	kHz
			—	31.25	—	
Duty Cycle	Switched Mode Programmable Duty Cycle Range	Programmable in software	6.25	—	93.75	%
	Duty Cycle step size	—	—	6.25	—	%

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5.17. Margin/Trim DAC Output Characteristics

Table 5.16. Margin/Trim DAC Output Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
	Resolution	—	—	8 (7 + sign)	—	Bits
FSR	Full scale range	—	—	+/– 320	—	mV
LSB	LSB step size	—	—	2.5	—	mV
I_{OUT}	Output source/sink current	—	–200	—	200	µA
I_{TRIM_Hi-Z}	Tri-state mode leakage	—	—	0.1	—	µA
BPZ	Bipolar zero output voltage (code=80h)	Four settings in software	—	0.6	—	V
			—	0.8	—	
			—	1.0	—	
			—	1.25	—	
t_S	TrimCell output voltage settling time[1]	DAC code changed from 80H to FFH or 80H to 00H	—	—	2.5	ms
		Single DAC code change	—	260	—	µs
C_LOAD	Maximum load capacitance	—	—	—	50	pF
TOSE	Total open loop supply voltage error[2]	Full scale DAC corresponds to +/– 5% supply voltage variation	–1%	—	+1%	V/V

Notes:

1. To 1% of set value with 50 pF load connected to trim pins.
2. Total resultant error in the trimmed power supply output voltage referred to any DAC code due to DAC's INL, DNL, gain, output impedance, offset error and bipolar offset error across the temperature, V_{CCA} ranges of the device.

5.18. Fault Log

Table 5.17. Fault Log

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Records	Number of available fault log records in EEPROM	V,I,T Log to User Tag EEPROM	—	16	—	Records
		Full Featured Log to UFM	512[1]	—	—	Records
$t_{faultTrigger}$	Minimum active time of trigger signal to start fault recording	—	64	—	—	µs
$t_{faultRecord}$	Time to copy fault record to EEPROM	—	—	—	5	ms
$t_{faultWrite}$	Time to complete writing fault record in EEPROM	V,I,T Log to User Tag EEPROM	—	—	10	ms
		Full Featured Log to UFM[2]	—	—	5	ms
$t_{TimeStamp}$	Timebase for Full Featured Fault Logging	Internally Generated Time Stamp	—	1	—	s

Notes:

1. Number of records depends on design. For more details see Fault Logging Using Platform Manager 2 (TN1277).
2. For maximum design: 8-ASCs, 4-user bytes, and 32-bit time stamp.

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5.19. Analog Sense and Control Oscillator

Table 5.18. Analog Sense and Control Oscillator

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
CLK_{ASC}	Internal ASC0 Clock	—	7.6	8	8.4	MHz
CLK_{ext}	Externally Applied Clock	—	7.6	8	8.4	MHz

5.20. FPGA Section sysI/O™ Recommended Operating Conditions

Table 5.19. FPGA Section sysI/OTM Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI[3]	3.135	3.3	3.465	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.465	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

Notes:

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. The FPGA section has dedicated LVDS buffers.
3. Input on the bottom bank (Ball Functions with the prefix 'PB' in Table 10.2) of the FPGA section only.

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5.21. FPGA Section sysI/O Single-Ended DC Electrical Characteristics

Table 5.20. FPGA Section sysI/O Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max[4] (mA)	I_{OH} Max[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	4	–2
							8	–6
					0.2	V_{CCIO} - 0.2	0.1	–0.1
PCI	–0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} - 0.18	V_{REF} +0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} - 0.125	V_{REF} +0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} - 0.125	V_{REF} +0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} - 0.1	V_{REF} +0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} - 0.1	V_{REF} +0.1	3.6	NA	NA	NA	NA

Notes:

1. Platform Manager 2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where Platform Manager 2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. Platform Manager 2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to MachXO2 sysI/O Usage Guide (FPGA-TN-02158).
3. The I^2C pins SCL_M and SDA_M are limited to a V_{IL} min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8 mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

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5.22. FPGA Section sysI/O Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side (Ball Functions with the prefix 'PT' in Table 10.2) of the FPGA section.

5.22.1. LVDS

Over Recommended Operating Conditions

Table 5.21. FPGA Section sysI/O Differential Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3	0	—	2.605	V
		V_{CCIO} = 2.5	0	—	2.05	V
V_{THD}	Differential Input Threshold	—	±100	—	—	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100Ω	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100Ω	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

LVDS Emulation

FPGA section outputs can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 5.2 is one possible solution for LVDS standard implementation. Resistor values in Figure 5.2 are industry standard values for 1% resistors.

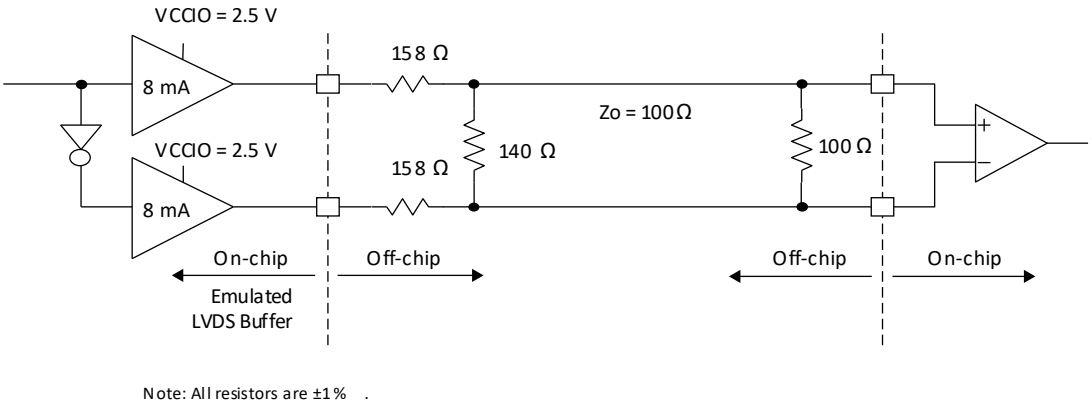

Figure 5.2. LVDS Using External Resistors (LVDS25E)

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Table 5.22. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	158	Ω
R_P	Driver parallel resistor	140	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	6.03	mA

BLVDS

FPGA section outputs support the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 5.3 is one possible solution for bi-directional multi-point differential signals.

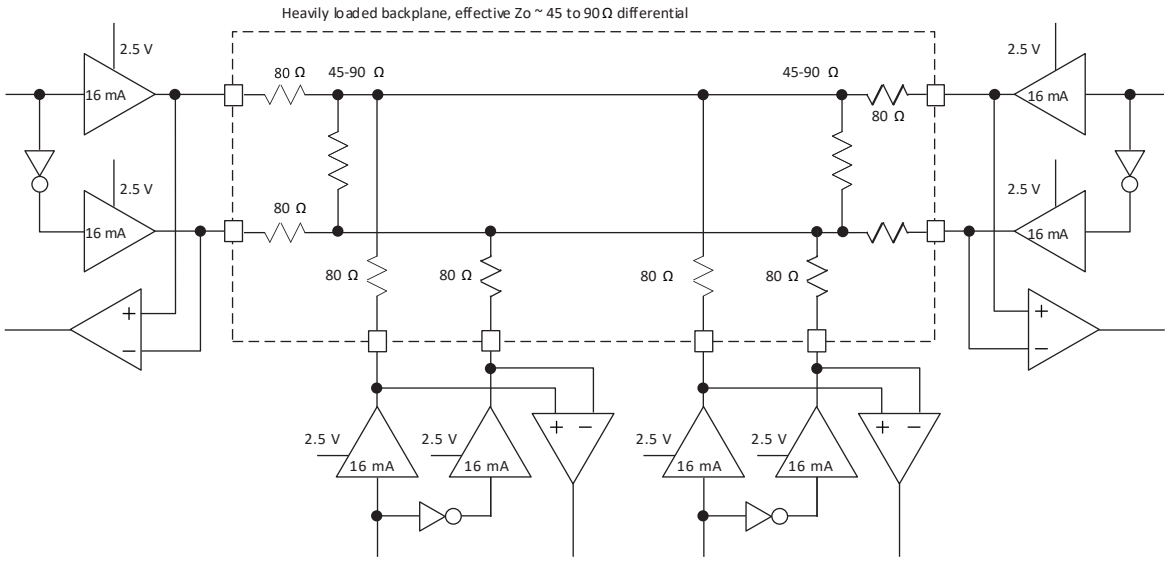

Figure 5.3. BLVDS Multi-point Output Example

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Table 5.23. BLVDS DC Conditions

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	10	10	Ω
R_S	Driver series resistance	80	80	Ω
R_{TLEFT}	Left end termination	45	90	Ω
R_{TRIGHT}	Right end termination	45	90	Ω
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

Note: For input buffer, see LVDS table.

LVPECL

FPGA section outputs support the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 5.4 is one possible solution for point-to-point signals.

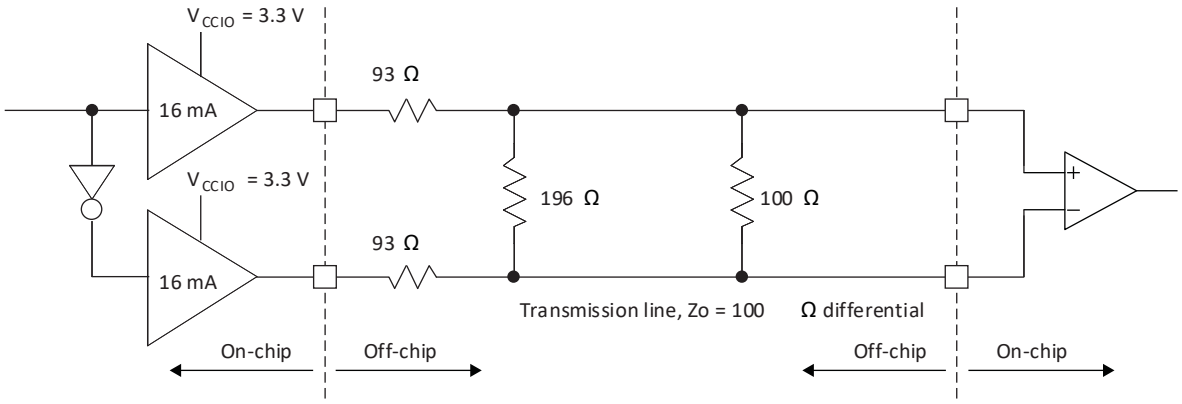

Figure 5.4. Differential LVPECL

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Table 5.24. LVPECL DC Conditions

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	10	Ω
R_S	Driver series resistor	93	Ω
R_P	Driver parallel resistor	196	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	12.11	mA

Note: For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

FPGA section outputs support the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 5.5 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 5.5 are industry standard values for 1% resistors.

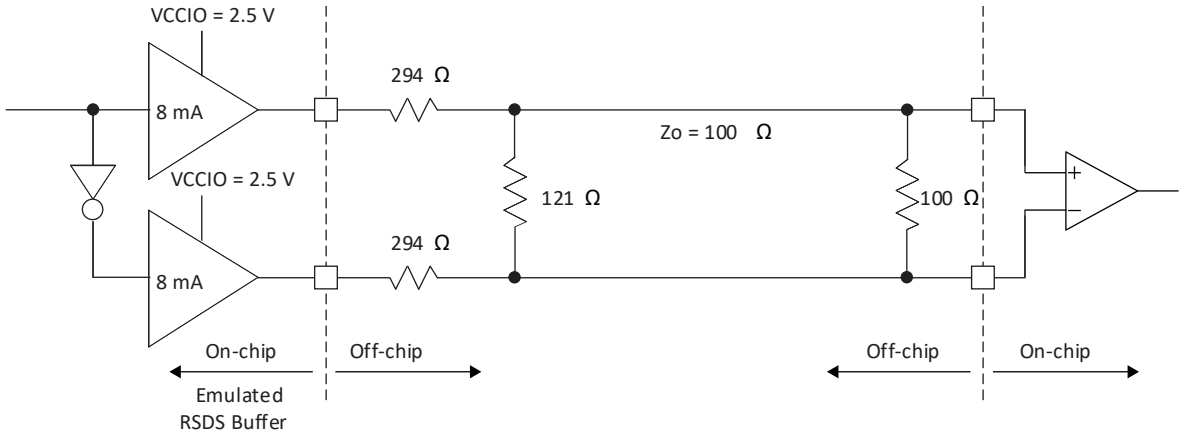

Figure 5.5. RSDS (Reduced Swing Differential Standard)

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Table 5.25. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	294	Ω
R_P	Driver parallel resistor	121	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ω
I_{DC}	DC output current	3.66	mA

5.23. Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Table 5.26. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Table 5.27. Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

Note: The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

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5.24. FPGA Section External Switching Characteristics

Over Recommended Operating Conditions

Table 5.28. FPGA Section External Switching Characteristics[1, 2, 3]

Symbol	Parameter	Min	Max.	Units
Primary Clocks				
f_{MAX_PR}[4]	Frequency for Primary Clock Tree		388	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	0.5		ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device		868	ps
Pin-LUT-Pin Propagation Delay				
t_{PD}	Best case propagation delay through one LUT-4		6.72	ns
General I/O Pin Parameters				
t_{CO}	Clock to Output – PIO Output Register		7.44	ns
t_{SU}	Clock to Data Setup – PIO Input Register	–0.17		ns
t_{H}	Clock to Data Hold – PIO Input Register	1.88		ns
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	1.63		ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	–0.24		ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register		388	MHz

Notes:

1. Exact performance may vary with device and design implementation.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load.
3. The tSU_DEL and tH_DEL values use the SCLK_ZERHOLD default step size. Each step is 105 ps.
4. This number for general purpose usage. Duty cycle tolerance is +/–10%.

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5.25. sysCLOCK PLL Timing

Over Recommended Operating Condition

Table 5.29. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)	—	1.5625	400	MHz
f_{OUT}[2]	Output Frequency (CLKOS3 cascaded from CLKOS2)	—	0.0122	400	MHz
f_{VCO}	PLL VCO Frequency	—	200	800	MHz
f_{PFD}	Phase Detector Input Frequency	—	7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected3	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy	—	–75	75	%
t_{PH}[4]	Output Phase Accuracy	—	–6	6	%
t_{OPJIT}[1,8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	150	ps p-p
		f_{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	180	ps p-p
		f_{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2,5]	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable	—	—	15	ms
t_{RST}	RST/RESETM Pulse Width	—	1	—	ns
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width	—	10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time	—	1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time	—	10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width	—	4	—	VCO Cycles

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Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See MachXO2 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02157) for more details.
5. At minimum fPFD. As the fPFD increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

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5.26. Analog Sense and Control Propagation Delays

Table 5.30. Analog Sense and Control Propagation Delays

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Voltage Monitors						
$t_{VMONtoFPGA}$	Propagation delay VMON input to signal update at FPGA	Glitch Filter Off		48		µs
		Glitch Filter ON		96		µs
$t_{VMONtoOCB}$[2]	Propagation delay VMON input to output update at OCB	Glitch Filter Off			16	µs
		Glitch Filter ON			64	µs
Current Monitors						
$t_{IMONtoFPGA}$	Propagation delay IMON input to signal update at FPGA	Glitch Filter Off		48		µs
		Glitch Filter ON		96		µs
$t_{IMONtoOCB}$[2]	Propagation delay IMON input to output update at OCB	Glitch Filter Off			16	µs
		Glitch Filter ON			64	µs
$t_{IMONFtoOCB}$[2]	Propagation delay IMONF input to output update at OCB	—			1	µs
Temperature Monitors						
$t_{TMONtoFPGA}$	Propagation delay TMON input to signal update at FPGA[1]	Monitor Alarm Filter Depth = 1		15		ms
		Monitor Alarm Filter Depth = 16		240		ms
GPIO – Inputs						
$t_{GPIOtoFPGA}$	Propagation delay GPIO input to signal update at FPGA	—		32		µs
$t_{GPIOtoOCB}$[3]	Propagation delay GPIO input to output update at OCB	—			50	ns
GPIO – Outputs						
$t_{FPGAtoGPIO}$	Propagation delay FPGA signal update to GPIO output	—		32		µs
$t_{OCBtoGPIO}$[2]	Propagation delay OCB input to output update at GPIO	—			50	ns
HVOUT						
$t_{FPGAtoHVOUT}$	Propagation delay FPGA signal update to HVOUT output	—		32		µs
$t_{OCBtoHVOUT}$[4]	Propagation delay OCB input to output update at HVOUT	—			110	ns
TRIM DAC						
$t_{FPGAtoTrimOE}$	Propagation delay FPGA signal update to TRIM-OE update	—		32		µs

Notes:

1. Propagation delay based on one TMON enabled. For multiple TMONs, propagation delay can be multiplied by the number of enabled TMON channels.
2. OCB output propagation delays measured using time delay to GPIO output from OCB. Propagation delay is measured on falling GPIO outputs. Rising output propagation will be dependent on external pull-up resistor.
3. OCB input propagation delays measured using time delay from GPIO input to OCB.
4. HVOUT propagation delay measured with HVOUT in open-drain mode, with switched mode disabled. Propagation delay in charge pump mode is dependent on external load and HVOUT settings.

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5.27. JTAG Port Timing Specifications

Table 5.31. JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

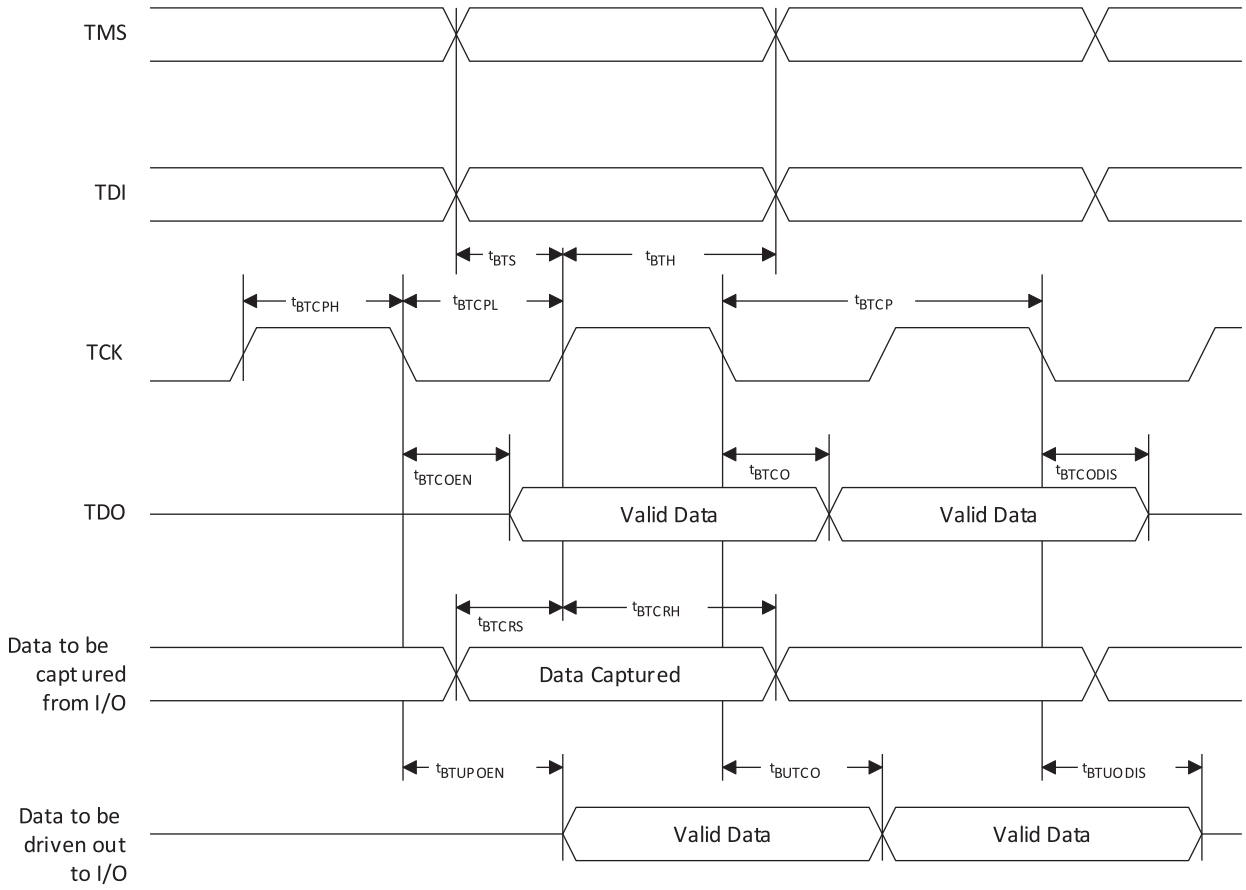

Figure 5.6. JTAG Port Timing Waveforms

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5.28. I²C Port Timing Specifications

Table 5.32. I²C Port Timing Specifications[1, 2]

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

Notes:

1. Platform Manager 2 supports the following modes:
   - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

5.29. Switching Test Conditions — FPGA Section

Figure 5.7 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 5.33.

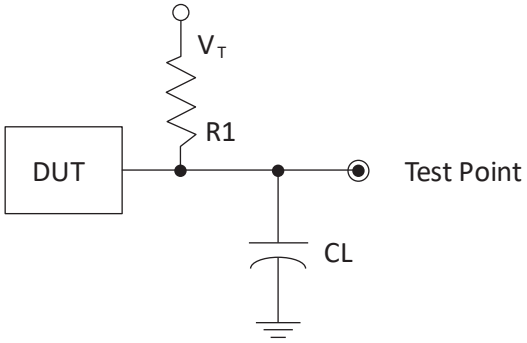

Figure 5.7. Output Test Load, LVTTL and LVCMOS Standards

Table 5.33. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

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6. Theory of Operation

6.1. Hardware Management System

The Platform Manager 2 is a fast-reacting, programmable logic based hardware management controller. The Platform Manager 2 includes an Analog Sense and Control (ASC) section and an FPGA section, allowing it to address the Power Management, Thermal Management and Digital Control Plane requirements of a circuit board.

The Platform Manager 2 FPGA section includes the hardware management control logic and other plug-in IP components to support functions like Fan Control, Voltage by Identification (VID), and time stamped fault logging to internal or external memory. The FPGA section also includes the ASC Interface logic (ASC-I/F) used to communicate with the ASC section (internal to the device) and additional hardware management expanders (L-ASC10 or LPTM21L).

The Platform Manager 2 supports a scalable, star-architecture implementation with centralized sequencing and control. This is accomplished by adding additional hardware management expanders to the circuit board. The basic system concept is shown in Figure 6.1. The necessary connections are shown in detail in the System Connections section.

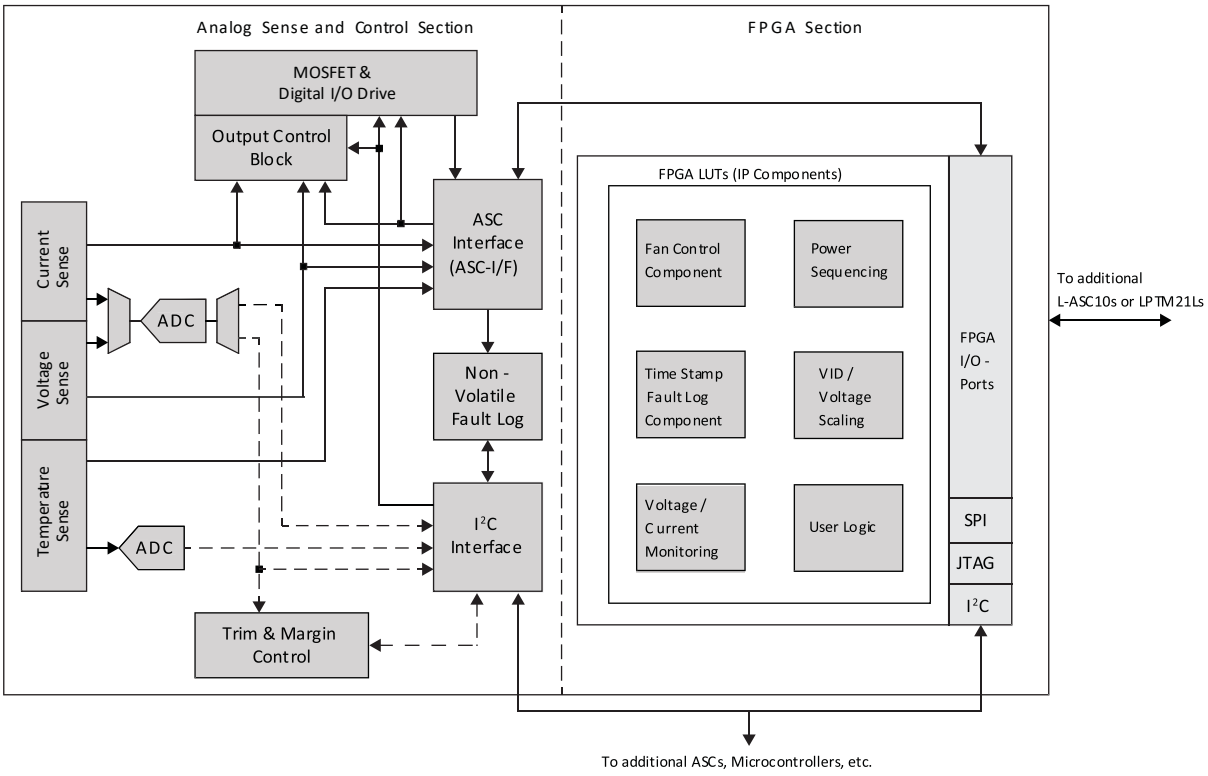

Figure 6.1. Hardware Management System

The Hardware Management System is configured using Platform Designer, a part of Lattice Diamond software. Platform Designer provides an easy to use graphical and spreadsheet based interface. Platform Designer automatically generates the device memory configuration based on the options selected in the software. See the For Further Information section for more details

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6.2. Voltage Monitor Inputs

The ASC provides ten independently programmable voltage monitor input circuits. There are nine standard voltage channels and one high voltage channel. The standard voltage channels are shown in Figure 6.2, while the high voltage channel is described in the High Voltage Monitor section. Two individually programmable trip-point comparators are connected to each voltage monitoring input. Each comparator reference has programmable trip points over the range of 0.075 V to 5.734 V. The 75 mV 'zero-detect' threshold allows the voltage monitors to determine if a monitored signal has dropped to ground level. This feature is especially useful for determining if a power supply's output has decayed to a substantially inactive condition after it has been switched off.

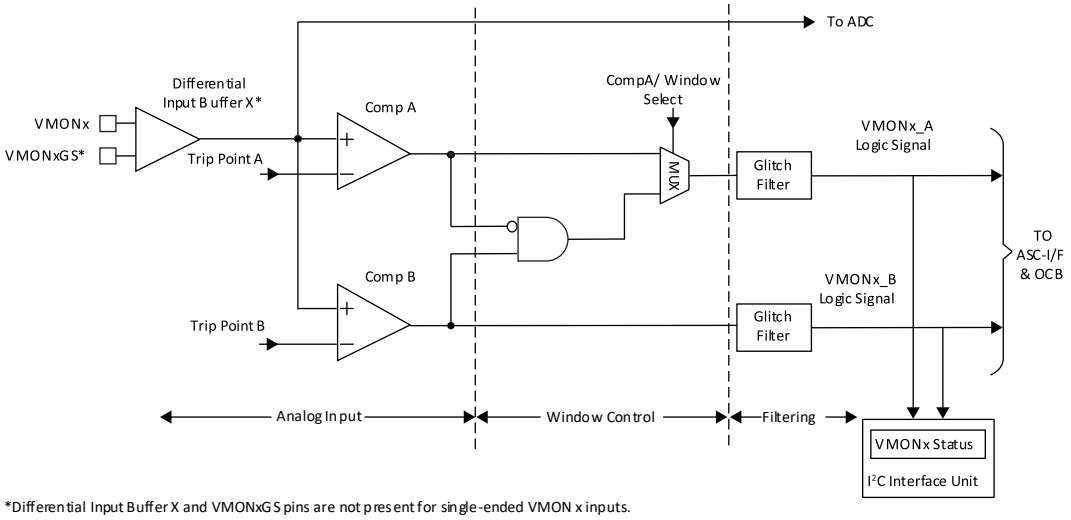

Figure 6.2. ASC Voltage Monitors

Figure 6.2 shows the functional block diagram of one of the nine voltage monitor inputs - 'x' (where x = 1...9). Each voltage monitor can be divided into three sections: Analog Input, Window Control, and Filtering. The first section provides a differential input buffer to monitor the power supply voltage through VMONx (to sense the positive terminal of the supply) and VMONxGS (to sense the power supply ground). Differential voltage sensing minimizes inaccuracies in voltage measurement with ADC and monitor thresholds due to the potential difference between the Platform Manager 2 device ground and the ground potential at the sensed node on the circuit board.

The voltage output of the differential input buffer is monitored by two individually programmable trip-point comparators, shown as Comp A and Comp B. The differential input buffer shown above is not present for any of the single-ended VMON inputs. VMON1-4 are differential inputs, while VMON5-9 are single-ended.

Each comparator outputs a HIGH signal to the ASC-I/F if the voltage at its positive terminal is greater than its programmed trip point setting; otherwise it outputs a LOW signal. The VMON4A and VMON9A comparators also output their status signals to the OCB.

Hysteresis is provided by the comparators to reduce false triggering as a result of input noise. The hysteresis provided by the voltage monitor is a function of the input divider setting. Table 6.1 lists the typical hysteresis versus voltage monitor trip-point.

AGOOD Logic Signal

All the VMON, IMON and TMON comparators auto-calibrate following a power-on reset event. During this time, the digital glitch filters are also initialized. This process completion is signaled by an internally generated logic signal: AGOOD. The ASC-I/F will not begin communicating valid VMON status bits or receiving GPIO control signals until the AGOOD signal is initialized.

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Programmable Over-Voltage and Under-Voltage Thresholds

Figure 6.3 shows the power supply ramp-up and ramp-down voltage waveforms. Because of hysteresis, the comparator outputs change state at different thresholds depending on the direction of excursion of the monitored power supply.

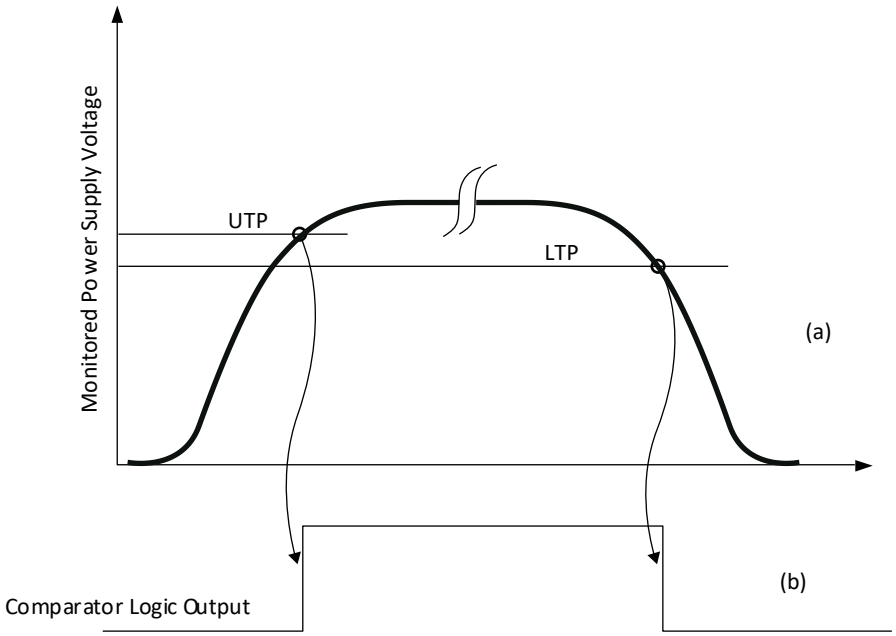

Figure 6.3. Power Supply Voltage Ramp-up and Ramp-down Waveform and the Resulting Comparator Output (a) and Corresponding to Upper and Lower Trip Points (b)

During power supply ramp-up the comparator output changes from logic zero to one when the power supply voltage crosses the upper trip point (UTP). During ramp down the comparator output changes from logic state one to zero when the power supply voltage crosses the lower trip point (LTP). To monitor for over voltage fault conditions, the UTP should be used. To monitor under-voltage fault conditions, the LTP should be used. The upper and lower trip points are automatically selected in software depending on whether the user is monitoring for an over-voltage condition or an under-voltage condition. Table 6.1 shows the comparator hysteresis versus the trip-point range.

Table 6.1. Voltage Monitor Comparator Hysteresis vs. Trip-Point

Trip-point Range (V)		Hysteresis (mV)
Low Limit	High Limit	
0.66	0.79	8
0.79	0.9	10
0.94	1.12	12
1.12	1.33	14
1.33	1.58	17
1.58	1.88	20
1.88	2.24	24
2.24	2.66	28
2.66	3.16	34
3.16	3.76	40
4.05	4.82	51
4.82	5.73	61
0.075	0.57	0 (Disabled)

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The window control section of the voltage monitor circuit is an AND gate (with inputs: an inverted COMPA "ANDed" with COMPB signal) and a multiplexer that supports the ability to develop a 'window' function in hardware. Through the use of the multiplexer, voltage monitor's 'A' output may be set to report either the status of the 'A' comparator, or the window function of both comparator outputs. The voltage monitor's 'A' output indicates whether the input signal is between or outside the two comparator thresholds. Important: This windowing function is only valid in cases where the threshold of the 'A' comparator is set to a value higher than that of the 'B' comparator. Table 6.2 shows the operation of window function logic.

Table 6.2. Voltage Monitoring Window Logic

Input Voltage	Comp A	Comp B	Window (B and Not A)	Comment
V_{IN} < Trip-Point B < Trip-Point A	0	0	0	Outside window, low
Trip-Point B <V_{IN} < Trip-Point A	0	1	1	Inside window
Trip-Point B < Trip-Point A < V_{IN}	1	1	0	Outside window, high

Note that when the 'A' output of the voltage monitor circuit is set to windowing mode, the 'B' output continues to monitor the output of the 'B' comparator. This can be useful in that the 'B' output can be used to augment the windowing function by determining if the input is above or below the windowing range.

The third section in the voltage monitor circuit is a glitch filter. When enabled, glitches of less than 64 µs will not result in the comparator output changing. This results in a comparator output delay of 64 µs (typical) for all comparator transitions. This is especially useful for reducing the possibility of false triggering from noise that may be present on the voltages being monitored. When the filter is disabled, the comparator output will be delayed by 16 µs (typical). See the Analog Sense and Control Propagation Delays section for more details.

The comparator status can be read from the I^2C interface. For details on the I^2C interface, please refer to the I2C Interface section of this data sheet.

6.3. Current Monitor Inputs

The ASC provides two current monitor circuits as shown in Figure 6.12. This includes a low-voltage current monitor (with a common mode voltage up to around 6 V, see VIN_IMONP in Recommended Operating Conditions section) and a high-voltage current monitor (with a common mode voltage range of up to around 13 V, see VIN_HIMONP in Recommended Operating Conditions section). The low-voltage and high-voltage current monitors share the same basic functional blocks, which are described in this section. Only the low-voltage current monitor supports the lowside sensing mode (shown in Figure 6.12). The high voltage current monitor shares input pins with the high voltage monitor described in the next section.

The current monitor circuits have a differential input that is connected to an external shunt resistor. The differential input goes to a pair of programmable gain amplifiers (PGA) and a fast comparator. The output of PGA A is connected to the ADC and the programmable trip point comparator A. The output of PGA B is connected to the programmable trip point comparator B. The output of the fast comparator is routed to the on-chip Output Control Block (OCB). This signal is useful for fast overcurrent or short circuit shutdown scenarios.

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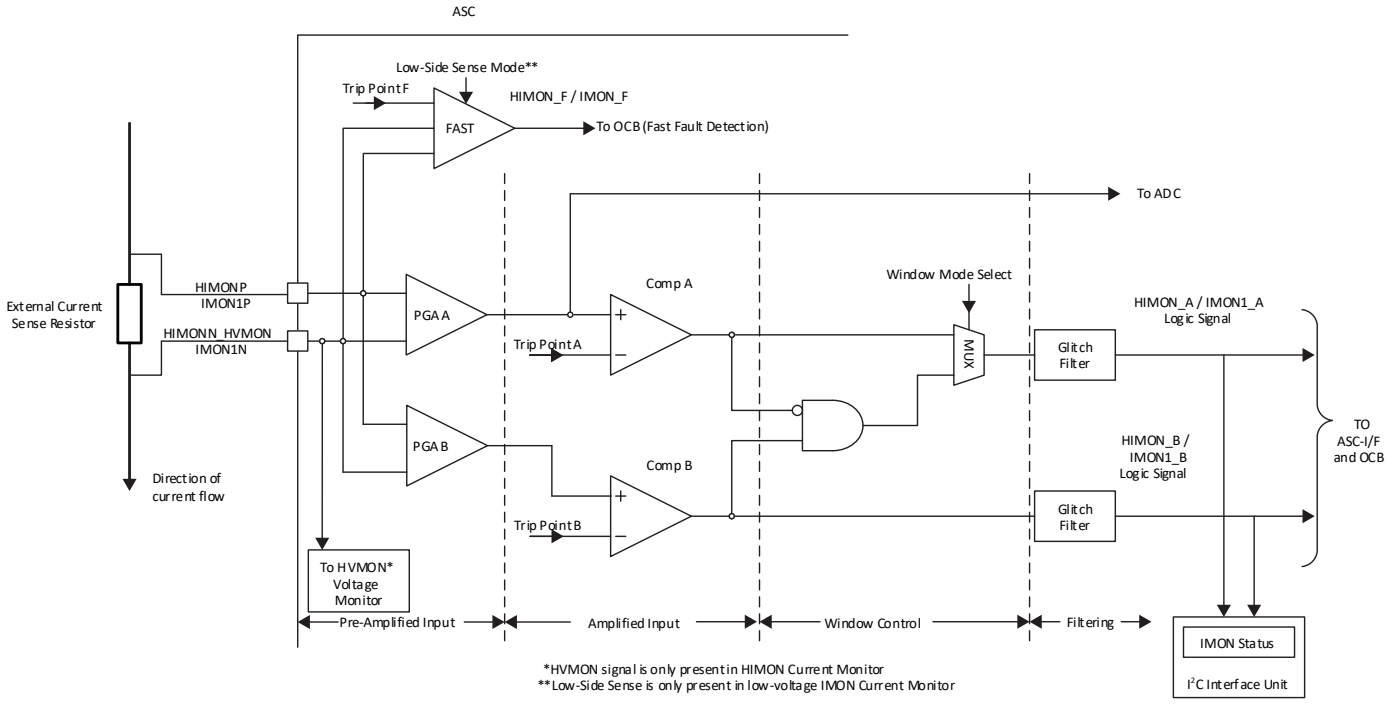

Figure 6.4. ASC Current Monitor

The Current Monitors can be divided into four sections: Pre-Amplified Input, Amplified Input, Window Control, and Filtering. The first section includes the differential input pins IMON1P and IMON1N (low voltage current monitor) or HIMONP and HIMONN_HVMON (high voltage current monitor). These pins are connected to the PGA circuits as well as the direct differential connection to the Fast Fault Detector.

The differential input is monitored by the fast fault detector. The fast fault detector has coarse accuracy and eight programmable trip points. The key feature of the fast fault detector is its response time. The fast fault detector outputs a HIGH signal to the OCB if the differential voltage across the current sensing shunt exceeds the programmed trip point setting. The current shunt is normally connected on the high-side of the input voltage. However, the low voltage current monitor also supports low-side sensing. The low-side sensing mode should be enabled when sensing negative voltage supplies (such as –48 V) or if the current sense resistor is placed in the return line between the load and ground. This insures proper operation of the fast comparator in a low-side sensing circuit.

Table 6.3 shows the available trip points for the fast fault detector vs. three frequently used sense resistor values.

Table 6.3. Fast Fault Detector Current Trip Points vs. Frequently Used Sense Resistor Values

Trip Point Setting	Frequently Used Sense Resistor Value		
	1 Milliohm	5 Milliohm	10 Milliohm
50 mV	50 A	10 A	5 A
100 mV	100 A	20 A	10 A
150 mV	150 A	30 A	15 A
200 mV	200 A	40 A	20 A
250 mV	250 A	50 A	25 A
300 mV	300 A	60 A	30 A
400 mV	400 A	80 A	40 A
500 mV	500 A	100 A	50 A

The Programmable Gain Amplifiers have gain settings of 10x, 25x, 50x, and 100x. The PGA circuits amplify the voltage differential across the current shunt and pass the results to the amplified input section of the current monitor.

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The Amplified Input section provides two individually programmable trip-point comparators, shown as Comp A and Comp B above. Each comparator supports four different trip points. Combining these trip points with the respective PGA settings, 16 unique threshold levels are selected for each current monitor.

Table 6.4 shows the available voltage differential trip points.

Table 6.4. Comparator Trip Points

Trip Point Setting	Programmable Gain Amplifier Setting (V/V)			
	10 x	25 x	50 x	100 x
1	75 mV	30.5 mV	15.5 mV	8 mV
2	100 mV	40.5 mV	20.5 mV	10.5 mV
3	140 mV	56.5 mV	28.5 mV	14.5 mV
4	190 mV	77 mV	39 mV	20 mV

The output of PGA A is also passed to the on-chip ADC. The current is measured and averaged by the ADC at regular intervals, as described in the Current Measurement with ADC section of the datasheet.

The window control section of the current monitor circuit is an AND gate (with inputs: an inverted COMPA “ANDed” with COMPB signal) and a multiplexer that supports the ability to develop a ‘window’ function in hardware, similar to the voltage monitor window function. Through the use of the multiplexer, the current monitor’s ‘A’ output may be set to report either the status of the ‘A’ comparator, or the window function of both comparator outputs. The current monitor’s ‘A’ output indicates whether the input signal is between or outside the two comparator thresholds. Important: This windowing function is only valid in cases where the threshold of the ‘A’ comparator is set to a value higher than that of the ‘B’ comparator. Table 6.5 shows the operation of window function logic.

Table 6.5. IMON Window Mode Behavior

Input Voltage	Comp A	Comp B	Window (B and Not A)	Comment
IIN < Trip-Point B < Trip-Point A	0	0	0	Outside window, low
Trip-Point B <IIN < Trip-Point A	0	1	1	Inside window
Trip-Point B < Trip-Point A < IIN	1	1	0	Outside window, high

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Note that when the 'A' output of the current monitor circuit is set to windowing mode, the 'B' output continues to monitor the output of the 'B' comparator. This can be useful in that the 'B' output can be used to augment the windowing function by determining if the input is above or below the windowing range.

The fourth section in the current monitor circuit is a glitch filter. When enabled, glitches of less than 64 µs will not result in the comparator output changing. This results in a comparator output delay of 64 µs (typical) for all comparator transitions. This is especially useful for reducing the possibility of false triggering from noise that may be present on the currents being monitored. When the filter is disabled, the comparator output will be delayed by 16 µs (typical). See the Analog Sense and Control Propagation Delays section for more details.

The comparator status can be read from the I^2C interface. For details on the I^2C interface, please refer to the I2C Interface section of this data sheet.

6.4. High Voltage Monitor

The High Voltage Monitor circuit is a single-ended high voltage monitor (HVMON) which is connected to the same input pin as the High Voltage Current Monitor (HIMONN_HVMON). Figure 6.5 shows the single-ended monitor circuit, which monitors the voltage on the HIMONN_HVMON pin. The HIMONP pin should be left unconnected or tied to the HIMONN_HVMON pin (never tied to ground) when the HIMONN_HVMON is only used to monitor High Voltage. Extending the input voltage range with an external voltage divider as described in Extending the VMON Input Range of Power/Platform Management Devices (AN6041) is not recommended for the HVMON inputs.

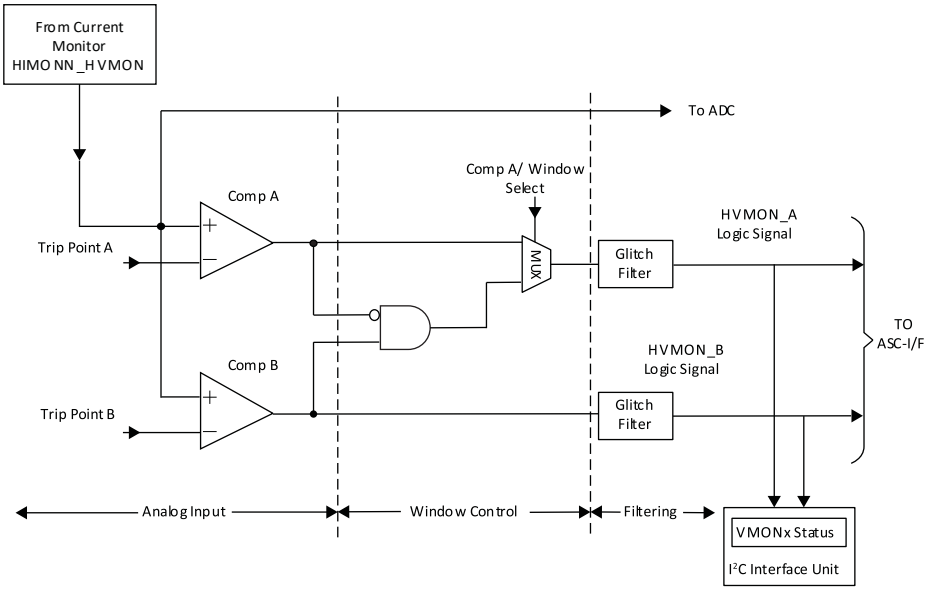

Figure 6.5. HVMON Monitor Circuit

The HVMON follows the same structure as the Voltage Monitor circuits. Two individually programmable trip-point comparators are connected to the HIMONN_HVMON pin voltage. Each of the comparator references has 408 programmable trip points, over a range of 0.227 V to 13.226 V.

The functional block diagram, shown in Figure 6.5, is a similar structure to the other single-ended Voltage Monitor circuits. Each comparator outputs a HIGH signal to the ASC-I/F if the voltage at its positive terminal is greater than its programmable trip point setting. A hysteresis of approximately 1% of the setpoint is provided by the comparators to reduce false triggering. Table 6.6 shows a typical hysteresis versus voltage monitor trip point.

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Table 6.6. HVMON Hysteresis vs Trip Point Range

Trip-point Range (V)		Hysteresis (mV)
Low Limit	High Limit	
1.91	2.27	22
2.27	2.7	28
2.69	3.2	30
3.16	3.76	38
3.72	4.43	44
4.40	5.24	52
5.18	6.17	61
6.04	7.20	72
7.08	8.43	84
8.29	9.87	99
9.68	11.52	115
11.17	13.2	133
0.23	1.28	0 (Disabled)

The Over-Voltage and Under-Voltage thresholds, along with the window mode and glitch filter, are identical to the features described in the voltage monitor section.

6.5. VMON and IMON Measurement with the On-Chip Analog to Digital Converter (ADC)

The ASC section of Platform Manager 2 has an on-chip analog to digital converter that can be used for measuring the voltages at the VMON inputs or the currents at the IMON inputs. This ADC is also used in closed loop trimming of DC-DC converters. Closed loop trimming is covered later in this document.

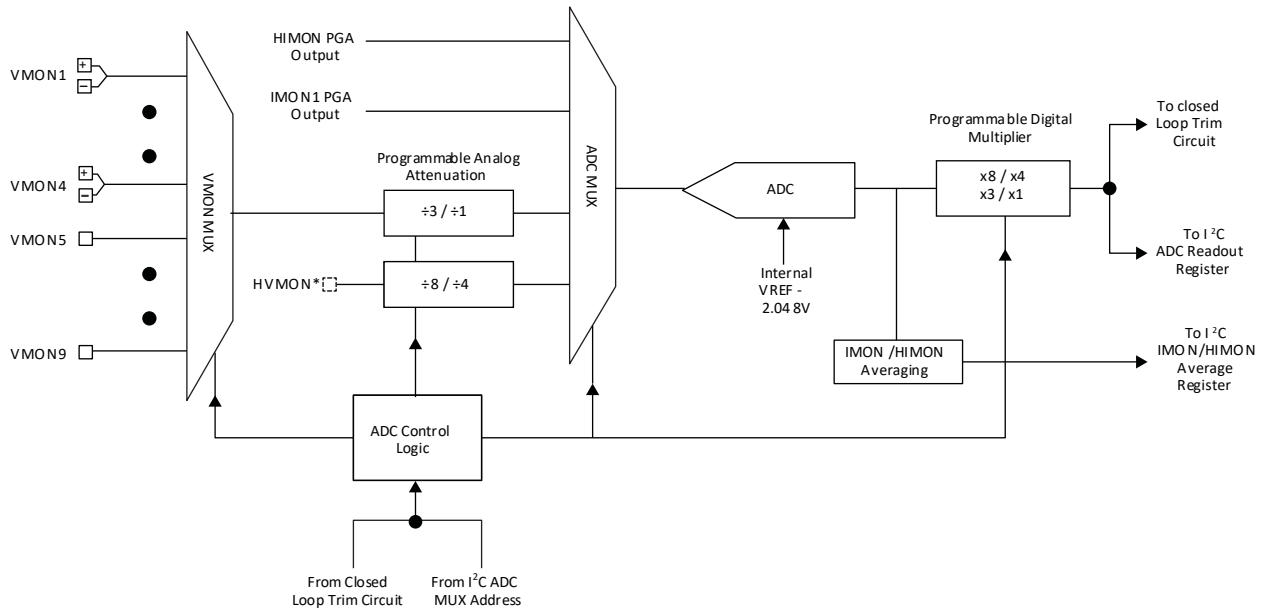

Figure 6.6. ADC Monitoring VMON and IMON

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Figure 6.6 shows the ADC circuit arrangement within the ASC device. The ADC can measure all analog input voltages up to 2.048 V through the multiplexer, ADC MUX. The ADC MUX receives inputs from the High Voltage IMON Programmable Amplifier (PGA), the IMON1 PGA, the High Voltage Monitor (HVMON) at the HIMONN_HVMON pin, and the VMON MUX. The VMON voltages can be attenuated (divided by three) or unattenuated (divided by one). The divided-by-three setting is used to measure voltages from 0 V to 6 V range and divided-by-one setting is used to measure the voltages from 0 V to 2 V range. The HVMON voltage requires attenuation, with settings for divided by eight (voltages between 8 V and 13.2 V) or divided by four (voltages between 8 V and 0 V). The HIMON and IMON1 PGA output voltages must be kept below 2.0 V for proper ADC operation since they are not attenuated.

The ADC control logic manages the MUX and attenuation settings. The control logic manages conversion requests from I^2C and the Closed Loop Trim Circuit. The control logic also schedules regular IMON1 and HIMON conversions, which are subsequently averaged and stored for user access. These IMON conversions are configured through the I^2C bus and filtered using an eight sample, weighted averaging scheme.

The control logic also sets the digital multiplication factor. This results in VMON and HVMON voltages, regardless of attenuation setting, maintaining a 2 mV per LSB scale. (See Calculation section for more details). The IMON1/HIMON voltages are not multiplied.

A microcontroller or FPGA IP can place a request for any VMON or IMON voltage measurement at any time through the I^2C bus. After the receipt of an I^2C command, the control logic will connect the ADC to the I^2C selected VMON or IMON through the ADC MUX. The ADC output is then latched into the I^2C readout registers.

6.6. Calculation

The algorithm to convert the ADC code to the corresponding VMON / HVMON voltage takes into consideration the relevant attenuation setting. In other words, if the attenuation is set to divide-by-eight, then the 10-bit ADC result is automatically multiplied by eight to calculate the actual voltage at that VMON input. Thus, the I^2C readout register is 13 bits instead of 10 bits. The other attenuator settings are also automatically compensated using the digital multiplier. The following formula can always be used to calculate the actual voltage from the ADC code.

Voltage at the VMONx Pins

VMON= ADC code (13 bits, converted to decimal) * 2 mV

The ADC code includes the ADC_VALUE_HIGH (8 bits) and ADC_VALUE_LOW (5 bits) read from I^2C interface

Calculating the HIMON or IMON1 current is slightly more complex, and requires knowledge about the current PGA setting and the resistance value of the current sense shunt resistor. The PGA has four settings (x10, x25, x50, and x100), while the current sensing resistance is chosen by the customer.

Current at the HIMON / IMON1 Pins

IMON current = ADC code (13 bits, converted to decimal) * 2 mV / (PGAsetting x Rsense)

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6.7. Temperature Monitor Inputs

The ASC section of the Platform Manager 2 provides two external temperature monitor inputs and one internal temperature monitor as shown in Figure 6.7.

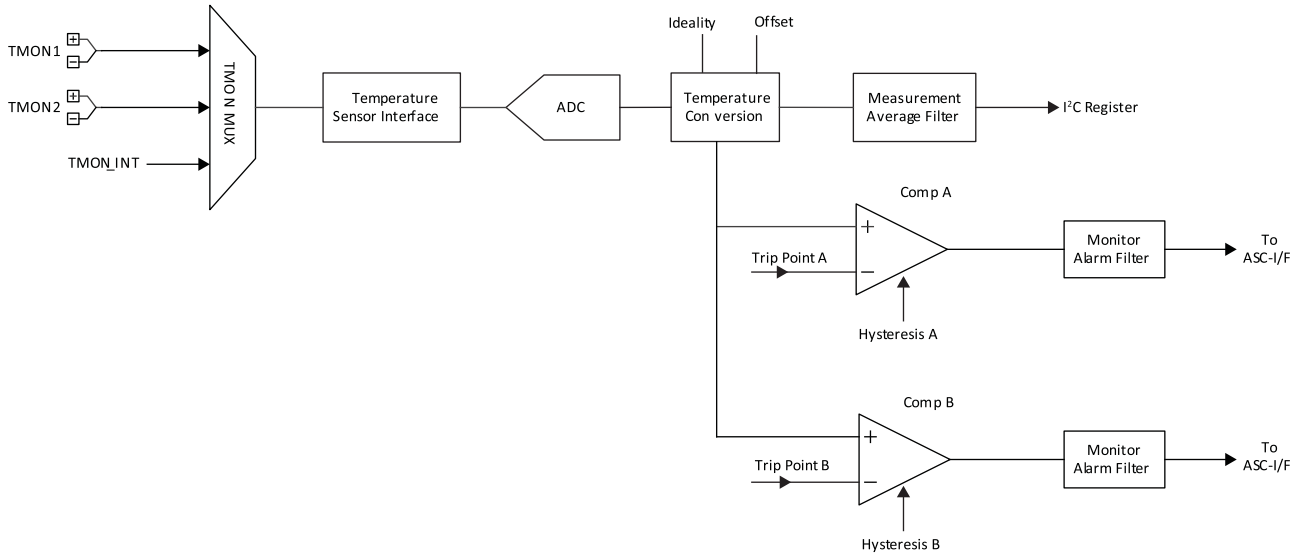

Figure 6.7. Temperature Monitor

The independently programmable temperature monitor inputs can be used with internal substrate diodes on microprocessors, FPGAs, ASICs, or with low cost external NPN or PNP transistors. The temperature sensor interface block includes programmable support for a variety of sensor configurations as shown in Figure 6.8. The sensor configuration settings available in the design software are described in Table 6.7.

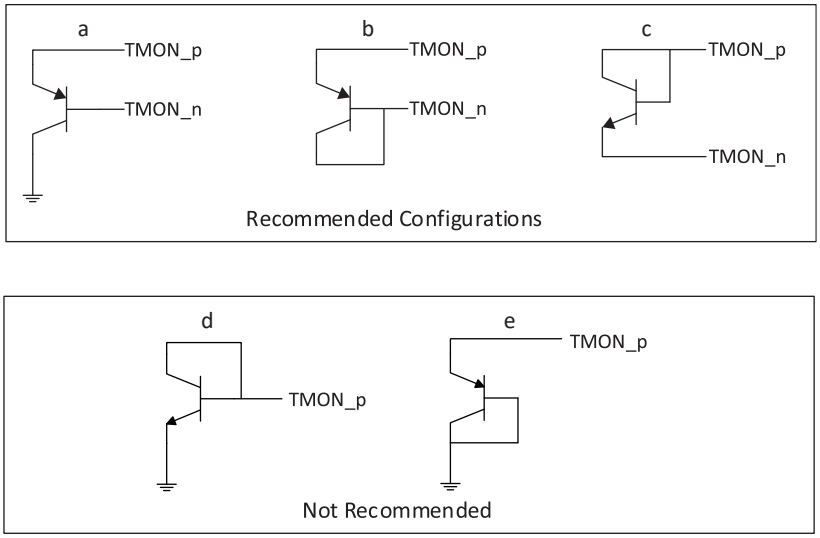

Figure 6.8. Remote TMON Diode Configurations

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Table 6.7. Remote TMON Diode Configurations

Sensor Configuration	Figure Number	Auto-β Compensation	Series Resistance Compensation	Accuracy
Beta Compensated PNP	16-a	Effective	Effective	Specified in recommended operating conditions
Differential PNP or NPN or Diode	16-b / 16-c	Not effective	Effective	Dependent on β variance
Single Ended	16-d / 16-e	Not effective	Not Effective	Not specified

Note: When using any of the Recommended Configurations (shown in Figure 6.8), low-voltage differential-signal layout practices should be followed. Furthermore, the TMON_n pin must not be grounded. The minimum impedance from TMON_n to ground is 200 kΩ. An impedance lower than 200 kΩ can cause significant temperature measurement errors.

The temperature sensor interface block also has built-in circuits to automatically compensate for the series resistance of the PCB traces to the sensor as well as the intrinsic device resistance. In addition, the interface block has circuits to compensate for the variable Beta (β) of the transistor sensor when it is connected in the configuration shown in. Figure 6.8 (In order for the variable β compensation circuit to be effective it must be able to measure the base current separately from the collector current.) For a discrete PNP or NPN transistor with high β (approximately 100 or greater) the effect of variable beta is typically negligible. However, most substrate diode temperature sensors will have a low β value which can vary considerably over temperature and current density making this a very useful feature.

The temperature signal information is converted to digital data by the dedicated TMON ADC. The digital data is scaled and converted to a two's complement, 11-bit temperature reading by the Temperature Conversion block. The measurement resolution is 0.25 °C per bit. The temperature conversion block takes into account the user entered ideality factor and offset value.

The ideality factor (also known as the emission coefficient or the N-factor) is a measure of how closely a real diode follows the ideal diode equation. In a real diode imperfections allow some recombination to occur in the junctions or by other methods which are not accounted for in the ideal equation. The ASC temperature conversion block is optimized for an ideality factor of 1 so any errors in the actual ideality factor of the sensor will produce a proportional error in the temperature value (in Kelvins). The diode ideality factor can be programmed in the range from 0.9 to 2.0 to match the actual ideality factor of the sensor.

An approximate value for the ideality factor for a 2N3904 NPN transistor is 1.004 and for a 2N3906 PNP transistor is 1.008. A substrate diode temperature sensor will typically have an ideality factor published in its data sheet.

Uncertainty can be introduced in temperature measurement by using an approximate value rather than the actual value for a 2N3904 or a 2N3906 transistor. This can lead to an error of around 0.4 °C. If the ideality factor for the transistor being used is not published, it can be determined by the ASC using the following procedure.

1. Force the system temperature to a known value (Tref).
2. With the ASC ideality factor set to 1.000, record the temperature value calculated (Tnocal).
3. Convert the Tref and Tnocal to Kelvin.
4. Divide the Tnocal (K) by Tref (K).

The result will be the actual ideality factor to be entered for the given TMON channel in the design software.

Note: The calibration is only as accurate as the Tref value. Any errors in the test equipment used will be transferred to the ASC readings.

The temperature conversion block also provides user programmable temperature offset from –64°C to 63.75°C for each channel's digital data to mitigate errors due to self-heating of the sensor, systematic offset and other unforeseen errors.

The conversion block also includes programmable output values for detected short or open conditions at the monitor input. The output levels are shown in Table 6.8.

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Table 6.8. Temperature Measurement Fault Readings

Fault	Short	Open
0	–255.75 °C	255.75 °C
1	255.75 °C	–255.75 °C

The converted temperature data for each channel is stored in two registers and can be read out through I^2C, after the programmable Measurement Averaging filter. See the Measurement and Control Register Access section for more details about the data register format.

The programmable measurement filter performs exponential averaging. Data is available immediately after one update cycle and is continually averaged using the programmable filter coefficients of 1, 8, or 16 per channel. The filtering equation is shown below:

$$\text{TempAve[x]} = \frac{\text{TempMeas[x]}}{\text{FiltCo}} + \text{TempAve[x} - 1\text{]} \text{ x } \frac{\text{FiltCo} - 1}{\text{FiltCo}}$$

When the temperature input changes it will require some settling time for the new value to be fully reflected in the results register due to the averaging filter. The settling time will vary depending upon how many channels are enabled and the programmed averaging coefficient. The settling time for various averaging coefficients and number of channels is shown in Table 6.9.

Table 6.9. Temperature Measurement Settling Time

Measurement Averaging Coefficient	Number of Channels Enabled	Average Settling Time (ms)
1	1	14.2
8	1	114
16	1	228
1	2	28.4
8	2	227
16	2	454
1	3	42.6
8	3	341
16	3	682

Note: Values are approximate and are not guaranteed by characterization.

In addition to the direct temperature measurement, the ASC has a temperature comparison function. The digital data of each channel is monitored by two trip-point comparators, shown as Comp A and Comp B in Figure 6.7. The digital temperature data monitored at the comparators is not processed by the measurement averaging filters. Each comparator reference has programmable trip points over the range of –64°C to 155°C with resolution of 1°C. Whenever the monitored temperature is above the trip point, the comparator output is set to one. The comparator outputs are transmitted over the ASC-I/F to the FPGA, depending on the setting of the Alarm Filter.

The two comparators each support programmable Hysteresis of 0°C to 63°C. When a comparator is used for overtemperature monitoring, the programmed hysteresis value is subtracted from the trip point and when the comparator is used for under-temperature monitoring, the programmed hysteresis value is added to the trip point. The hysteresis behavior is displayed in Figure 6.9 (Overtemperature setting with Hysteresis) and Figure 6.10 (Undertemperature setting with Hysteresis).Each comparator can be individually selected as either over-temperature or under-temperature operation.

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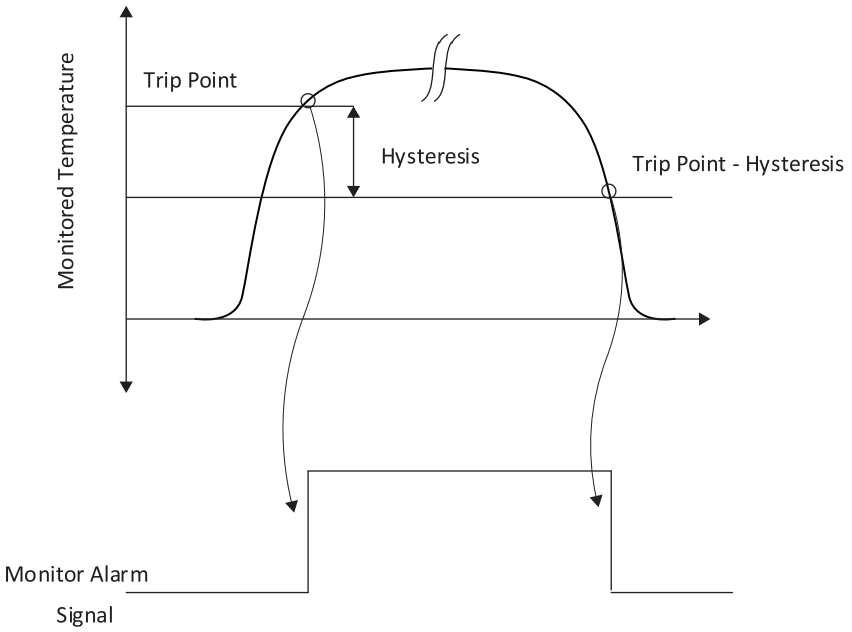

Figure 6.9. Monitor Alarm Signal Behavior - Overtemperature (OT) Setting

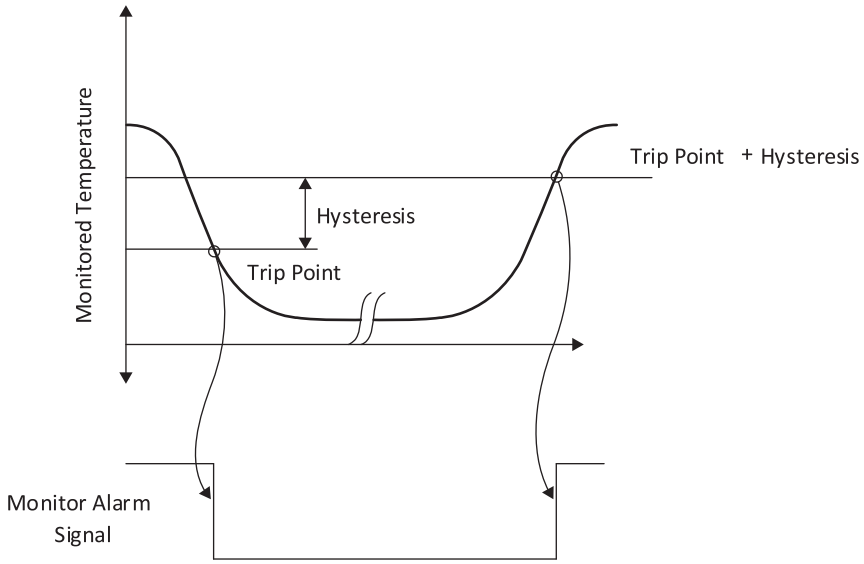

Figure 6.10. Monitor Alarm Signal Behavior - Undertemperature (UT) Setting

A programmable Alarm Filter (separate from the measurement averaging filter) is available at the output of the comparators. The depth of this filter is programmable from one to 16. The filter monitors the comparator alarm output each time the temperature measurement is refreshed. The filter counts up each time the comparator alarm value is 1, and down each time the comparator alarm value is 0. When the filter counter reaches the programmed filter depth, the TMONx_A or TMONx_B signal are set to one.

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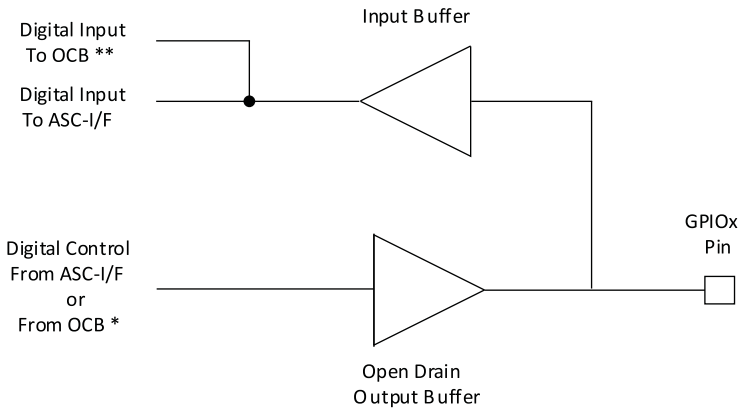
6.8. Digital Inputs/Outputs

The ASC section of Platform Manager 2 has four dedicated digital outputs (HVOUTs) and ten General Purpose Input/Output (GPIO) pins. The four HVOUT pins can be configured as high-voltage FET drivers or Open Drain outputs. This provides a high degree of flexibility when interfacing to power supply control inputs or other external logic signals.

The ten GPIO pins can be configured as inputs or Open Drain outputs. Figure 6.11 shows a block diagram of the GPIO circuitry. When configured as inputs, GPIO1 through GPIO10 inputs are registered and made available to the FPGA using the ASC-I/F. GPIO5 through GPIO10 are also made available to the Output Control Block (OCB) directly without being registered. Table 6.10 shows a summary of the input and output sources for each GPIO pin.

Table 6.10. GPIO Input and Output Sources

GPIO	ASC-I/F Input	OCB Input	ASC-I/F output	OCB output	Hysteretic control
GPIO1	Y	N	Y	N	N
GPIO2	Y	N	Y	Y	Y
GPIO3	Y	N	Y	Y	Y
GPIO4	Y	N	Y	N	N
GPIO5	Y	Y	Y	N	N
GPIO6	Y	Y	Y	N	N
GPIO7	Y	Y	Y	N	N
GPIO8	Y	Y	Y	N	N
GPIO9	Y	Y	Y	N	N
GPIO10	Y	Y	Y	N	N



* Digital Control comes from OCB for GPIO 2 and 3.
Digital Control comes from ASC-I/F for remaining GPIO.
** Only available for GPIO 5, 6, 7, 8, 9 and 10.

Figure 6.11. GPIO Block Diagram

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6.9. Output Control Block

The ASC Output Control Block (OCB) is used to control GPIO2, GPIO3, and the four HVOUTs. The Output Control Block has two modes of operation available; Direct Output control and Hysteretic Feedback control as shown in Figure 6.12.

Direct Output control is supported by various inputs which include the I^2C registers, GPIO pins 5-10 (when configured as inputs), the VMON4A and VMON9A comparator output signals, and the Fast IMON1 and Fast HIMON comparator output signals. These inputs are individually selectable for each of the outputs. When these inputs are used with the Direct Output control mode they provide a fast path for control which has very low propagation delay. The outputs in the OCB can also be controlled from the FPGA Logic over the ASC Interface (ASC-I/F) with the normal propagation delays. See the Analog Sense and Control Propagation Delays section for more details.

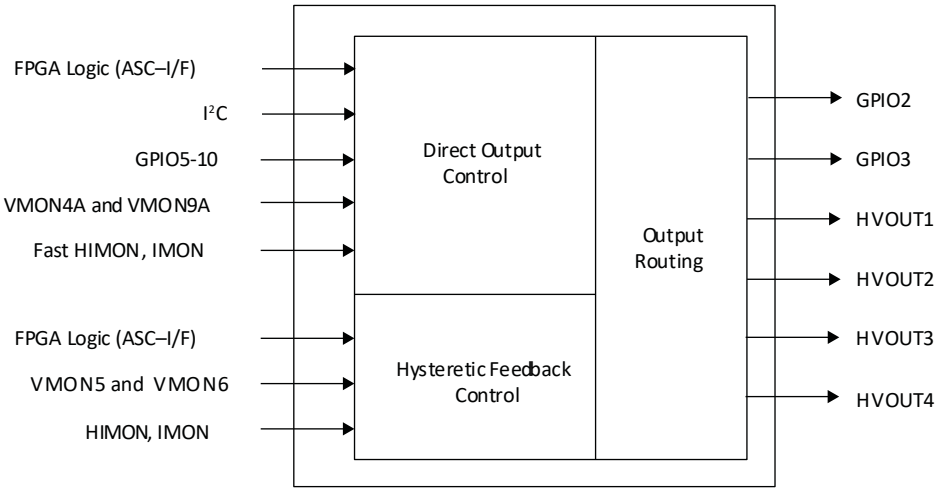

Figure 6.12. Output Control Block – Simplified Diagram

The OCB outputs can also be configured for Hysteretic Feedback control if desired. In the Hysteretic Feedback control mode the output will be switched on and off based upon the feedback signal chosen. The available feedback signals are the HIMON, IMON1, VMON5, or VMON6 trip points. As the feedback signal changes it will turn the output on or off depending upon whether it is above or below the chosen set-point and depending upon the output polarity. The user logic can switch between the high and low trip points of a signal to provide additional flexibility. In addition, the FPGA Logic can be dynamically selected to provide the feedback signal over the ASC-I/F which allows the user logic to change from a conditional output to a static value.

One example of how the Hysteretic feedback control feature can be used is to modulate a high-voltage FET driver using the FPGA logic and the trip points to control the rate of modulation over different voltage ranges - such as in a Hot Swap application. The design software provides an easy to use interface for configuring the device as a hot swap controller. The software will generate the required device settings and control algorithm automatically.

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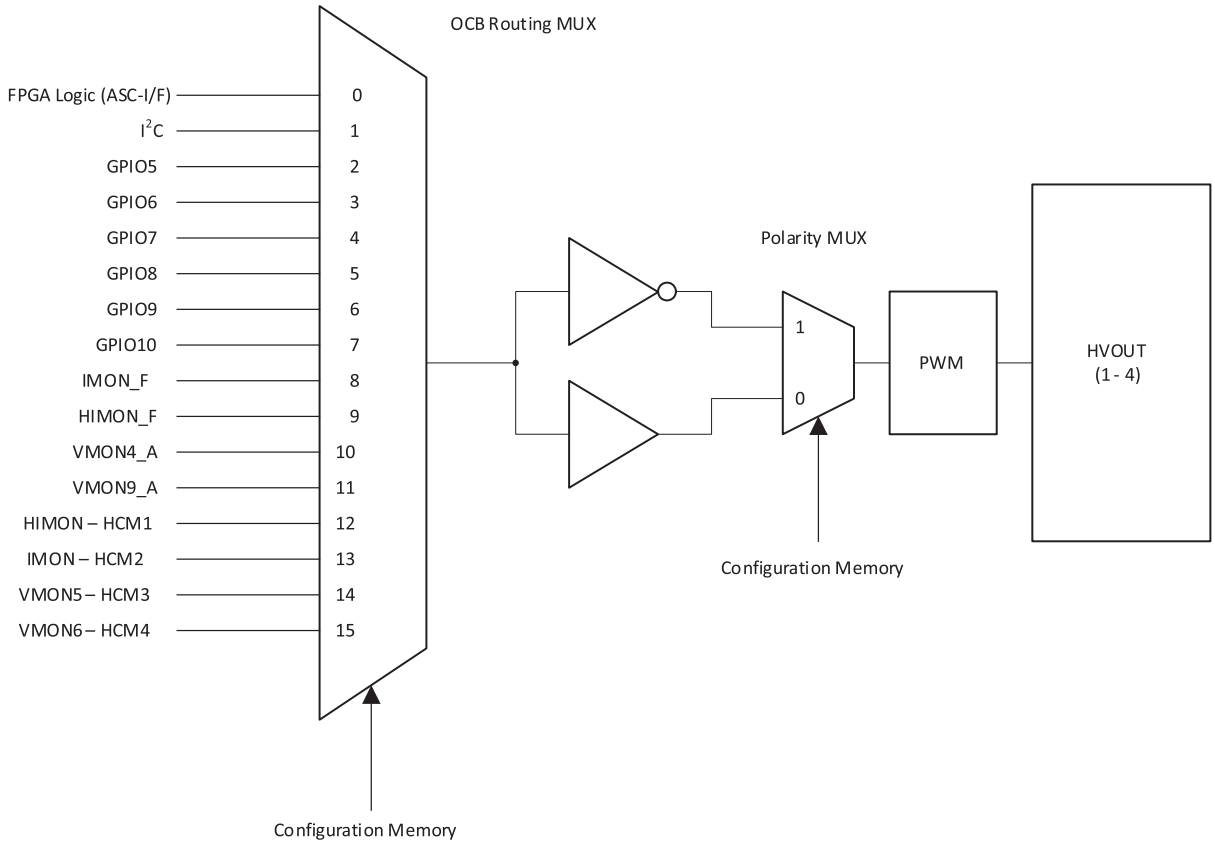

Figure 6.13. HVOUT Output Routing MUX Block Diagram

Figure 6.13 is a generic HVOUT routing diagram that applies to all the HVOUTs and provides a bit more detail than the simplified diagram in Figure 6.12. The MUX on the left is configured by Platform Designer software and selects from either the 12 direct control signals at the top or the four Hysteretic Control Module (HCM) signals at the bottom. The software is also used to select normal or inverted control. The features and configuration of the PWM and HVOUT blocks are covered in the High Voltage Outputs section. If PWM is enabled then the output of the Polarity MUX will enable or disable the PWM; otherwise the HVOUT will be on or off based on the Polarity Mux output signal.

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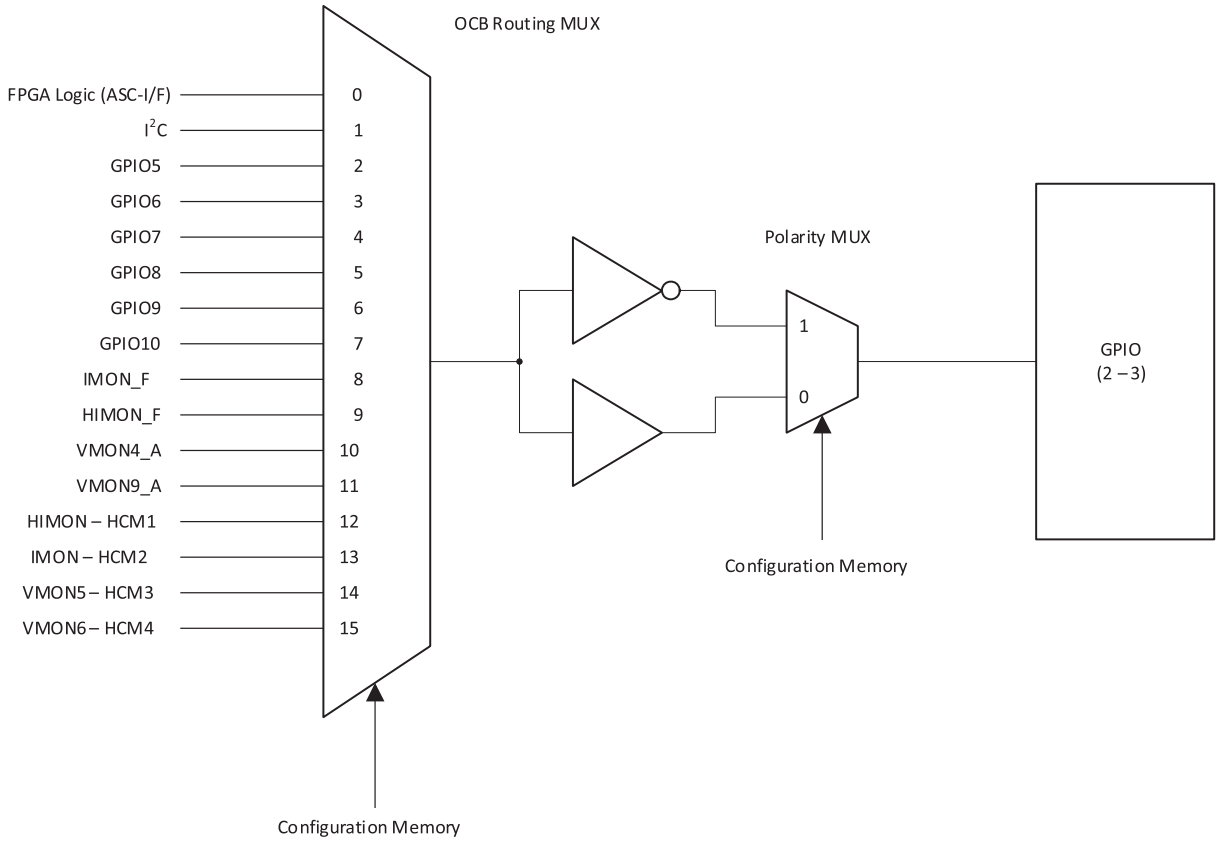

Figure 6.14. GPIO Output Routing MUX Block Diagram

Figure 6.14 is a generic GPIO routing diagram that applies to GPIO2 & GPIO3 and it provides a bit more detail than the simplified diagram in Figure 6.12. The MUX on the left is configured by Platform Designer software and selects from either the 12 direct control signals at the top or the four Hysteretic Control Module (HCM) signals at the bottom. The software is also used to select normal or inverted control. The GPIO pin will be on or off based on the Polarity Mux output signal.

Figure 6.15 is a diagram of Hysteretic Control Module #1 (HCM1) which is a little more complex than the other HCMs in the device. It is unique in that it is the only HCM that supports a dynamic selection of the Trip Point from the table; while the other HCMs can only dynamically switch between two comparator outputs (for example a low and high setting). The software configures the Trip Point MUX to either use a fixed configuration HIMON trip point or the dynamic HIMON trip point which is set by the FPGA Logic based upon the operating conditions. The output of the HIMON comparator is inverted before sending it to the Hysteretic Enable MUX.

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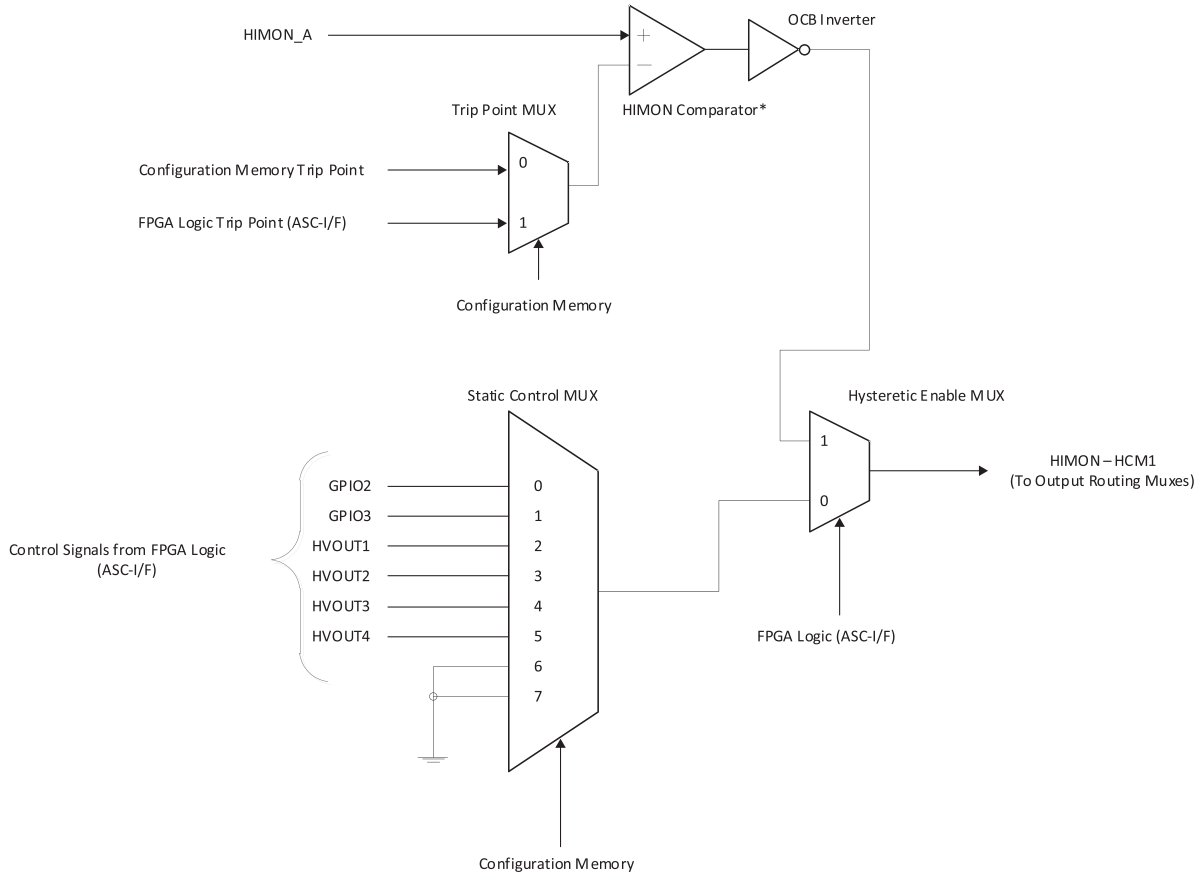

Figure 6.15. OCB HIMON HCM1 Block Diagram

The Hysteretic Enable MUX is controlled by the FPGA Logic over the ASC-I/F. The HIMON comparator signal is selected when the Hysteretic mode is enabled and the HVOUT or GPIO is controlled based on the voltage sensed at the HIMON input pins. When the Hysteretic mode is disabled the HVOUT or GPIO is controlled by the output of the Static Control MUX. All the input signals to the Static Control MUX come from the FPGA Logic over the ASCI/F. Typically the Static Control MUX is configured by the software to connect to the corresponding output being controlled by the HCM. For example, if HCM1 is selected for HVOUT2, then the Static Control MUX would also be set to HVOUT2. In this manner when Hysteretic Mode is disabled it is just like setting the OCB Routing MUX to zero where the FPGA Logic controls the HVOUT or GPIO over the ASC-I/F.

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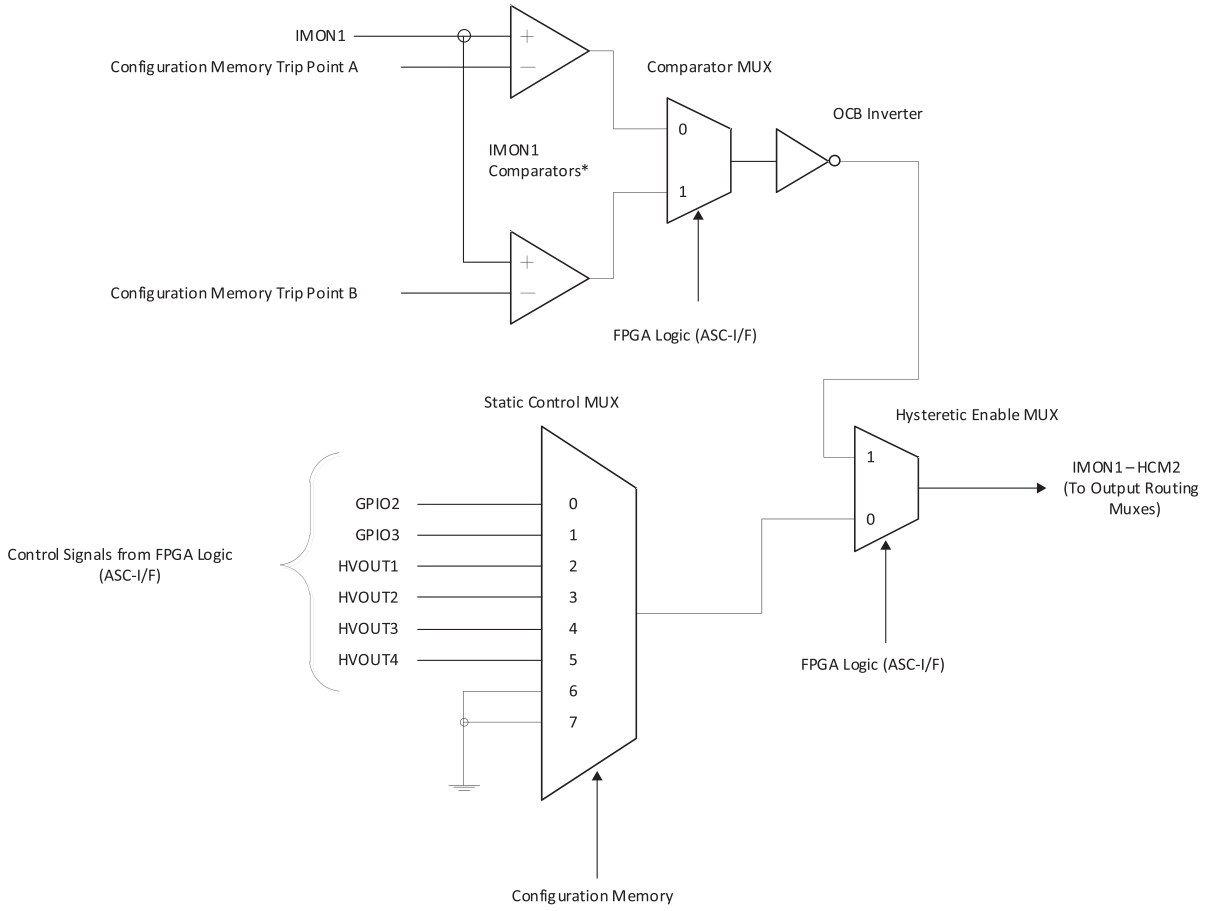

* IMON Windowing and Glitch Filters are not shown in this diagram for clarity.
The input to the comparator MUX is from the glitch filters.

Figure 6.16. OCB IMON1 HCM2 Block Diagram

Figure 6.16 is a diagram of Hysteretic Control Module #2 (HCM2) which is also an IMON based HCM. The software is used to select both the A and B trip points, while the FPGA Logic is used to dynamically switch between the two comparator outputs. The output of the Comparator MUX is inverted before sending it to the Hysteretic Enable MUX.

The Hysteretic Enable MUX is controlled by the FPGA Logic over the ASC-I/F. The Comparator MUX output signal is selected when the Hysteretic mode is enabled and the HVOUT or GPIO is controlled based on the voltage sensed at the IMON1 input pins. When the Hysteretic mode is disabled the HVOUT or GPIO is controlled by the output of the Static Control MUX. All the input signals to the Static Control MUX come from the FPGA Logic over the ASC-I/F. Typically the Static Control MUX is configured by the software to connect to the corresponding output being controlled by the HCM.

When using the hysteretic mode in hot swap applications, the design software will automatically configure the muxes and generate the control algorithm. See the For Further Information section for more details.

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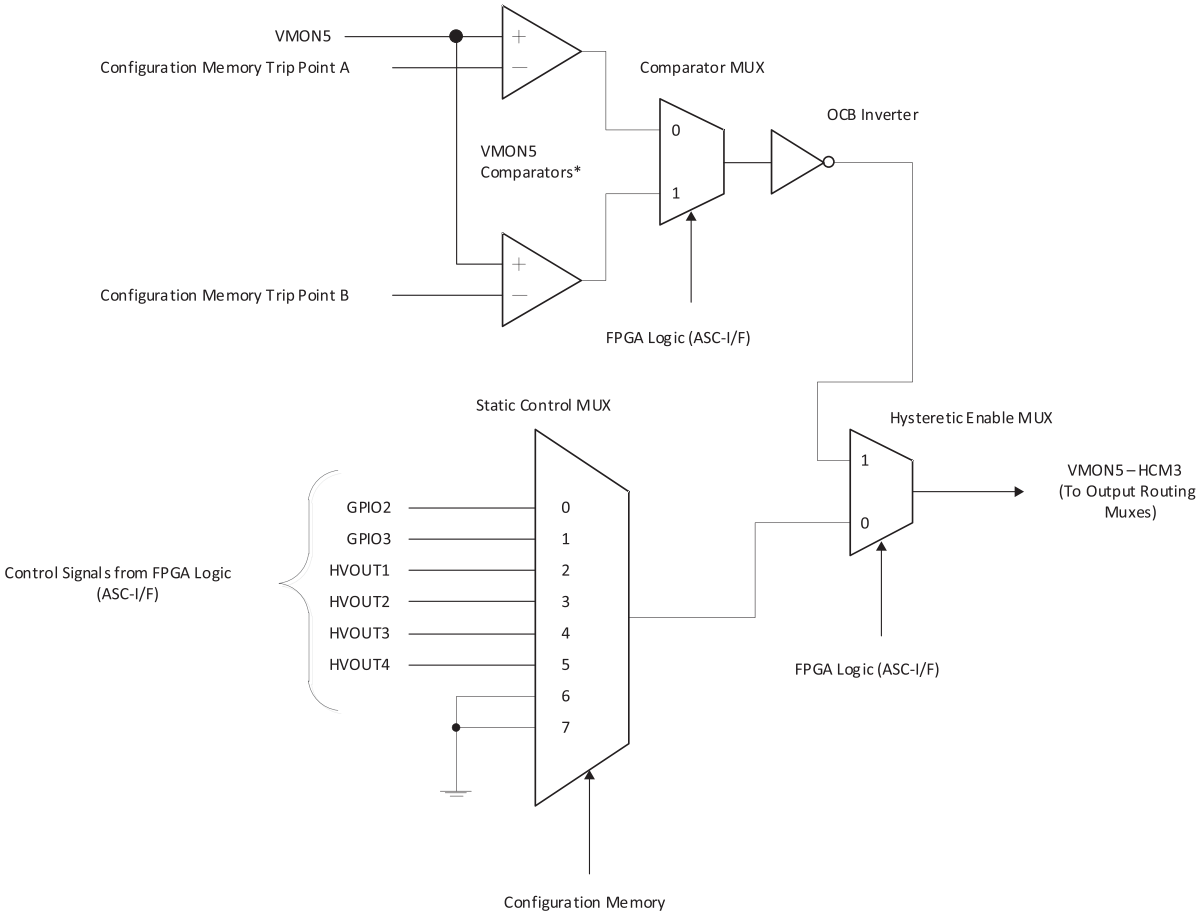

Figure 6.17. OCB VMON5 HCM3 Block Diagram

Figure 6.17 is a diagram of Hysteretic Control Module #3 (HCM3) which is a VMON based HCM. The software is used to select both the A and B trip points, while the FPGA Logic is used to dynamically switch between the two comparator outputs. The output of the Comparator MUX is inverted before sending it to the Hysteretic Enable MUX.

The Hysteretic Enable MUX is controlled by the FPGA Logic over the ASC-I/F. The Comparator MUX output signal is selected when the Hysteretic mode is enabled and the HVOUT or GPIO is controlled based on the voltage sensed at the VMON5 input pins. When the Hysteretic mode is disabled the HVOUT or GPIO is controlled by the output of the Static Control MUX. All the input signals to the Static Control MUX come from the FPGA Logic over the ASC-I/F. Typically the Static Control MUX is configured by the software to connect to the corresponding output being controlled by the HCM.

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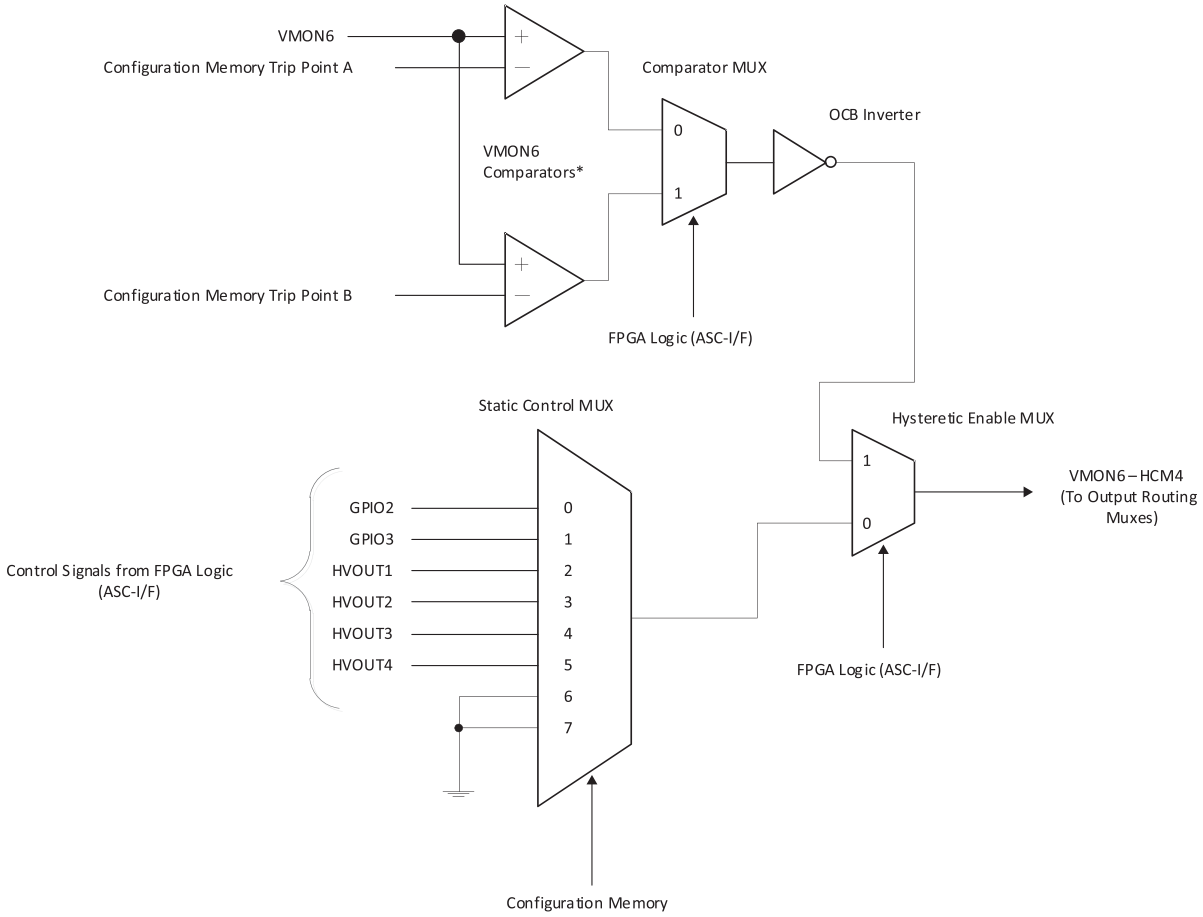

Figure 6.18. OCB VMON6 HCM4 Block Diagram

Figure 6.18 is a diagram of Hysteretic Control Module #4 (HCM4) which is a second VMON based HCM. The software is used to select both the A and B trip points but, the FPGA Logic is used to dynamically switch between the two comparator outputs. The output of the Comparator MUX is inverted before sending it to the Hysteretic Enable MUX.

The Hysteretic Enable MUX is controlled by the FPGA Logic over the ASC-I/F. When the Comparator MUX output signal is selected the Hysteretic mode is enabled and the HVOUT or GPIO is controlled based on the voltage sensed at the VMON6 input pins. When the Hysteretic mode is disabled the HVOUT or GPIO is controlled by the output of the Static Control MUX. All the input signals to the Static Control MUX come from the FPGA Logic over the ASC-I/F. Typically, the Static Control MUX is configured by the software to connect to the corresponding output being controlled by the HCM.

The Platform Designer software has component interfaces that are used to simplify the task of configuring the OCB blocks discussed in this section. For example, the Hot Swap component provides a functional interface for the designer while setting the trip points for VMONs and IMONs, and routing them to HVOUTs using OCB paths.

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6.10. High Voltage Outputs

In addition to being usable as digital Open Drain outputs the four HVOUT pins can be configured as high-voltage FET drivers. Figure 6.19 shows the details of the HVOUT circuitry.

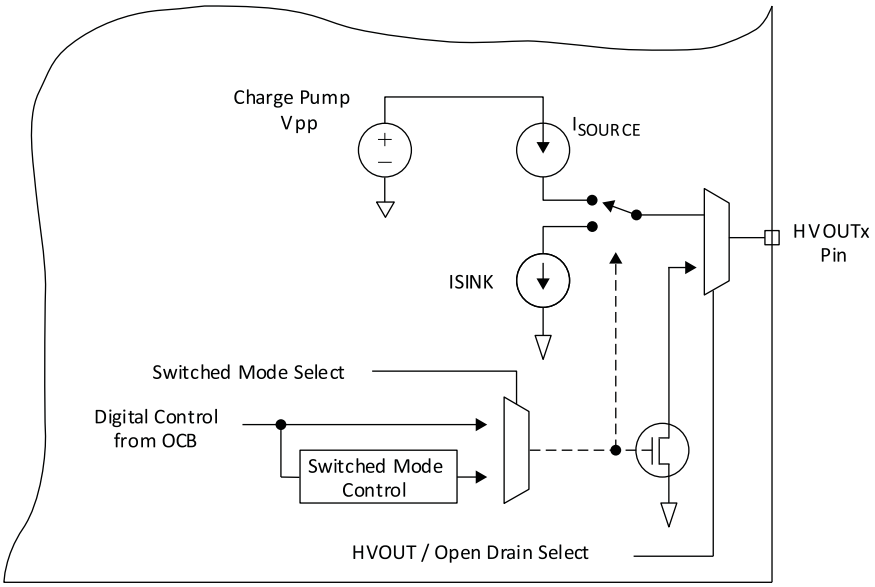

Figure 6.19. HVOUT Block Diagram

When the HVOUT is configured as a high-voltage FET driver, the output either sources current from a charge pump or sinks current. The output level at the pin can rise to a configurable maximum voltage. The maximum voltage levels that are required depend on the gate-to-source threshold of the FET being driven and the power supply voltage being switched. The maximum voltage level needs to be sufficient to bias the gate-to-source threshold on and also accommodate the load voltage at the FET's source with the source pin of the FET tied to the supply of the target board. Using this arrangement allows the system to provide a wide range of ramp rates for the FET driver.

The HVOUT FET driver outputs a configurable source current (I_{SOURCE}) in order to charge the FET gate. When the driver is turned off, it outputs a configurable sink current (I_{SINK}) to discharge the FET gate. The Isink setting also includes a fast turn off setting. See the High Voltage FET Drivers section in DC and Switching Characteristics for more details.

The four HVOUT pins can also be configured as switched mode outputs in either the high-voltage FET driver or Open Drain mode. This is useful when the HVOUT is driving a High side MOSFET controlling a supply greater than 6 V. This feature is also useful for driving a MOSFET in a charge pump circuit to generate voltages above 12 volts. The switched output duty cycle can be configured from 6.25 % up to 93.75 % in step sizes of 6.25 % and the frequency can be configured as either 15.625 kHz or 31.25 kHz. This flexibility allows the output to be configured to drive a wide variety of circuit components for a design. The rise and fall of the switched mode outputs may not complete with certain combinations of the charge pump settings (V_{PP}, I_{SOURCE}, I_{SINK}) and the switched mode settings (Duty Cycle and Frequency). The configuration should be chosen with the output circuit in mind.

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6.11. Safe State

During power-up the ASC GPIO will be configured as outputs and will be in the “Safe-State” as defined in Table 6.11. The HVOUTs will be configured in the FET driver mode during power-up. When the ASC completes the power up sequence, then the HVOUT and GPIO control is transferred to the ASC-I/F or OCB depending upon the configuration. The ASC will indicate that it has completed the power up sequence by asserting the AGOOD signal to the FPGA section using the ASC-I/F.

Note: After power-up, if the ASC-I/F is interrupted (specifically WRCLK and WDAT), the ASC outputs will revert to the Safe State.

Table 6.11. ASC GPIO and HVOUT Safe-State Definitions

I/O	SAFE-STATE
HVOUT1	Low
HVOUT2	Low
HVOUT3	Low
HVOUT4	Low
GPIO1	Low
GPIO2	Low
GPIO3	Low
GPIO4	Low
GPIO5	Low
GPIO6	Low
GPIO7	Hi-Z
GPIO8	Hi-Z
GPIO9	Hi-Z
GPIO10	Low

6.12. Controlling Power Supply Output Voltage by Trim and Margin Block

One of the key features of the ASC is its ability to make adjustments to the power supplies that it may also be monitoring and/or sequencing. This is accomplished through the Trim and Margin Block of the device.

As shown in Figure 6.20 the Trim and Margin Block can adjust voltages of up to four different power supplies through the DACs built-in the Trim Cells. The DC-DC blocks in the figure represent virtually any type of DC power supply that has a trim or feedback input. This can be an off-the-shelf unit or custom circuit designed around a switching regulator IC. The interface between ASC and the power supply shown in diagram by a resistor actually represents a resistor network.

The individual ASC-I/F control signals for each Trimcell are:

- ASCx_TRIMx_CLTE — This is a closed loop trim enable signal of a TrimCell. When ASCx_TRIMx_CLTE =1 the closed loop trimming for the DC-DC power supply connected to the TrimCell is enabled.
- ASCx_TRIMx_P0 and ASCx_TRIMx_P1 — These are two closed loop Trim Profile select signals used to select the active voltage profile of a TRIM cell.
- ASCx_TRIMx_OE — This control signal enables the DAC output of a TrimCell. When ASCx_TRIMx_OE=1 the DAC output of the Trim cell is active.

Other inputs to the TrimCell are:

- ADC — This input to the Trim cell is from the ADC which converts each VMON voltage into digital. The ADC input is used by the Trim Cell for controlling the closed loop trim operation.
- I^2C interface — Internal registers of the TrimCell can be accessed via I^2C interface. The Platform Designer software provides control signals which can be programmed to restrict I^2C access to the ASC.

Next to each DC-DC converter, three example voltages are shown. These example voltages correspond to the operating voltage profile of the corresponding TrimCell. As shown in Figure 6.20, the active operating profile for each TrimCell is selected independently (of other TrimCells) using TRIMx_P0 and TRIMx_P1 signals.

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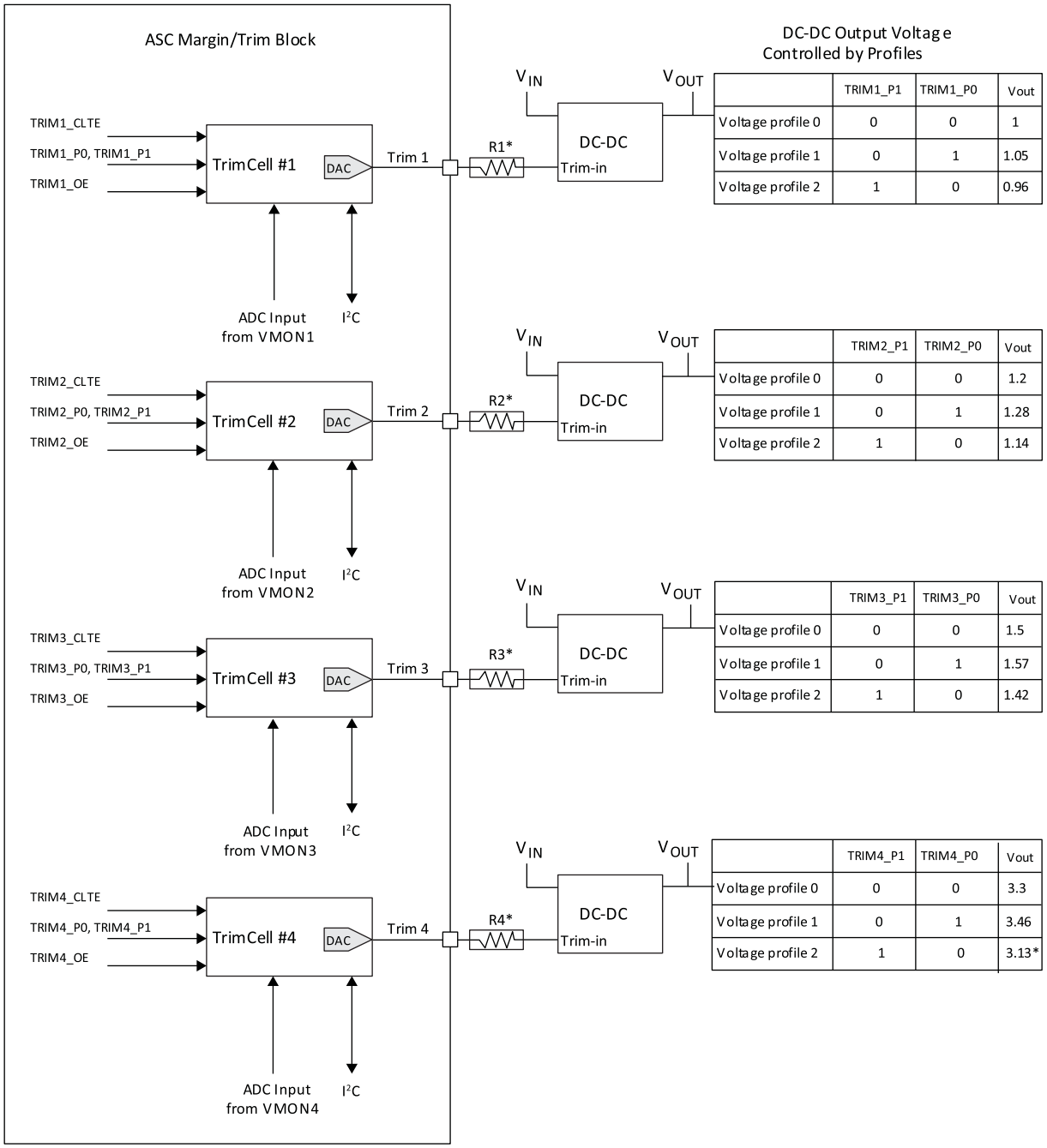

	TRIM1_P1	TRIM1_P0	Vout
Voltage profile 0	0	0	1
Voltage profile 1	0	1	1.05
Voltage profile 2	1	0	0.96

	TRIM2_P1	TRIM2_P0	Vout
Voltage profile 0	0	0	1.2
Voltage profile 1	0	1	1.28
Voltage profile 2	1	0	1.14

	TRIM3_P1	TRIM3_P0	Vout
Voltage profile 0	0	0	1.5
Voltage profile 1	0	1	1.57
Voltage profile 2	1	0	1.42

	TRIM4_P1	TRIM4_P0	Vout
Voltage profile 0	0	0	3.3
Voltage profile 1	0	1	3.46
Voltage profile 2	1	0	3.13*

*Indicates resistor network, see Figure 6.21.

Figure 6.20. ASC Margin/Trim Block

There are four independently enabled TrimCells in the ASC section of the Platform Manager 2 for controlling individual power supplies. Each Trimcell can generate up-to three trimming voltages to control the output voltage of the DC-DC converter.

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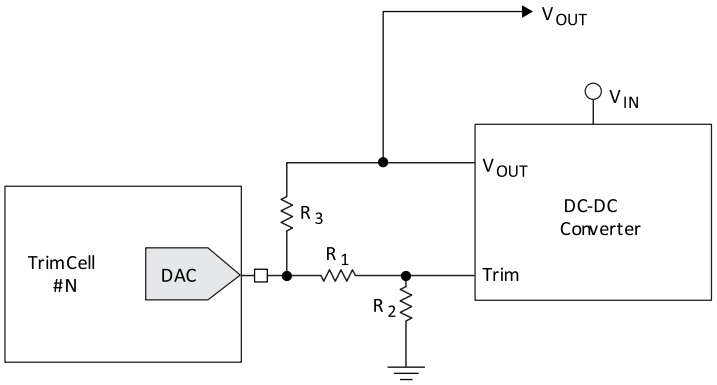

Figure 6.21. TrimCell Driving a Typical DC-DC Converter

Figure 6.21 shows an example resistor network between the TrimCell #N in the ASC and the DC-DC converter. The values of these resistors depend on the type of DC-DC converter used and its operating voltage range. The calculation to determine the values of the resistors R1, R2, and R3 is performed automatically in the Platform Designer software.

TrimCell Architecture

The TrimCell block diagram is shown in Figure 6.22. Each TrimCell can be used in either of two modes to control an 8-bit DAC. The output of the DAC can be used to apply a voltage to trim an external power supply or DC-DC converter. The **Trim Configuration Mode** is selected in the Platform Designer software; the default mode is **Trim Calculator**, and the optional mode is **Manual**. Manual mode applies the user specified DAC Codes directly to the DAC Register. The Trim Calculator mode is the Closed Loop Trim Mode where feedback from the corresponding VMON is compared to a programmable Voltage Setpoint Register and the result is used to update the DAC register.

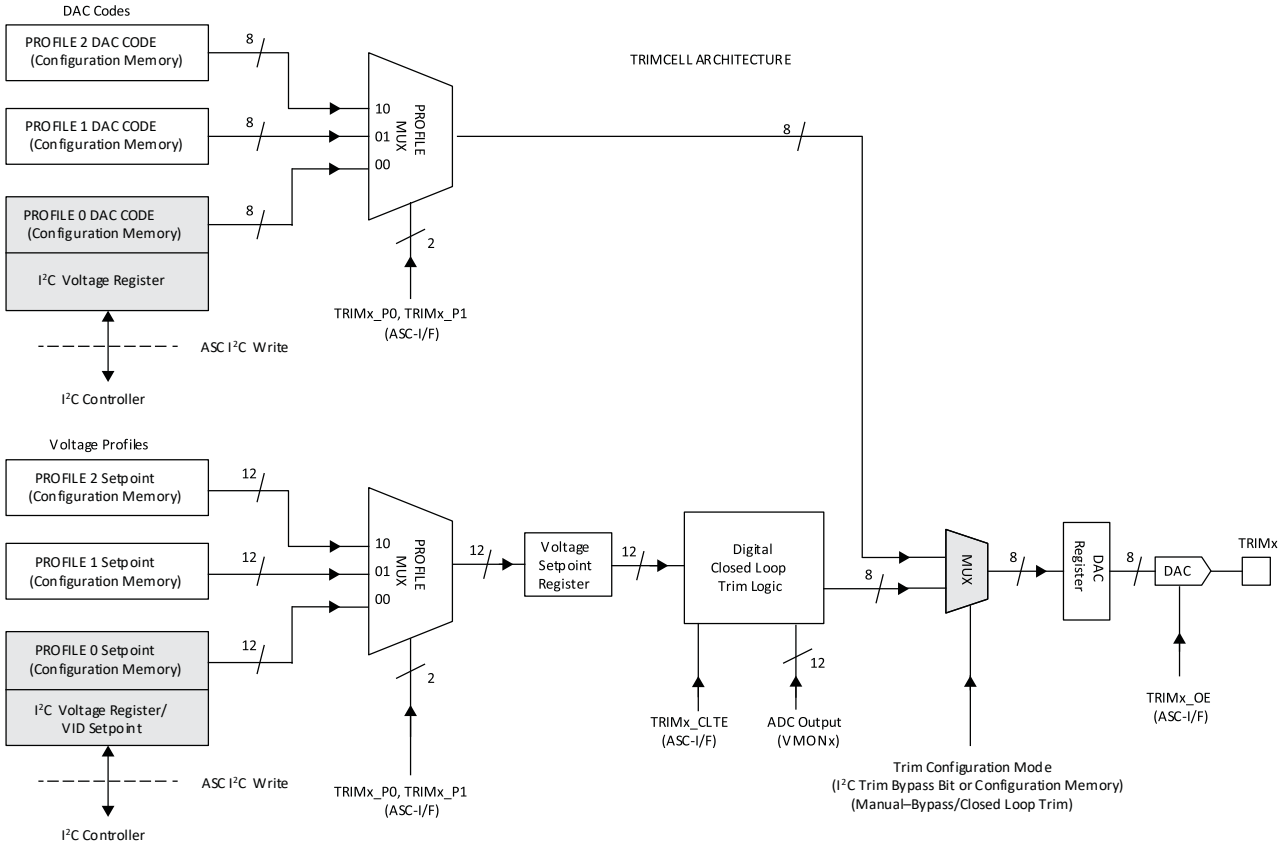

Figure 6.22. TrimCell Architecture

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Manual Mode

Shown in the upper portion of Figure 6.22, PROFILE 0, PROFILE 1, PROFILE 2 are 8-bit DAC Codes that are written in the EEPROM memory during programming. The active DAC Code for each TrimCell is independently chosen based on ASC-I/F signals TRIMx_P0 / TRIMx_P1. The active DAC Code is written to the DAC Register whenever the TRIMx_P0, TRIMx_P1 signals change. As shown, the PROFILE 0 DAC Code written in configuration memory can be overwritten by I^2C commands during run-time. The I^2C access to the PROFILE 0 DAC Code can be restricted based on the ASC I^2C write protect feature that can be enabled during configuration (see the I2C Interface section for more details).

Closed Loop Trim Mode

Shown in the lower portion of Figure 6.22, PROFILE 0, PROFILE 1, and PROFILE 2 are 12-bit Setpoints, which are written in the EEPROM memory during programming. The active Setpoint for each TrimCell is independently chosen based on ASC-I/F signals TRIMx_P0 / TRIMx_P1. This Setpoint is copied to the Voltage Setpoint Register whenever the TRIMx_P0, TRIMx_P1 signals change. As shown, the PROFILE 0 Setpoint written in configuration memory can be overwritten by I^2C commands during run-time. The I^2C access to the PROFILE 0 Setpoint can be restricted based on the ASC I^2C write protect feature that can be enabled during configuration (see the I2C Interface section for more details). The Digital Closed Loop Trim Logic (near the center of Figure 6.22) compares the Voltage Setpoint Register with the corresponding VMON voltage (digitized by the ADC) to make active adjustments to the 8-bit DAC Register. The Closed Loop Trim is enabled on a per channel basis, depending on the ASC-I/F signal TRIMx_CLTE. See the Digital Closed Loop Trim Mode section for additional details on this mode of operation.

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DAC Output Control

The DAC output of the TrimCell is enabled using ASC-I/F signal TRIMx_OE. When enabled, the DAC register value is converted to an analog voltage and output on the TRIMx pin. When disabled, the DAC output is high impedance. The Trim Configuration Mode sets how the DAC Register is controlled (either Manual or Closed Loop Trim) and is programmed into the EEPROM memory. The Trim Configuration Mode is set by the user in the Trim/Margin view of Platform Designer software based on the selection of either Manual or Trim Calculator. The DAC output values versus configuration settings are shown in Table 6.12.

Table 6.12. DAC Output Value vs. Configuration Settings

Trim Configuration Mode (Platform Designer Software)	CLTE (ASC –I/F)	TRIMx_OE (ASC- I/F)	DAC Output Value
x	x	0	Hi-Z
Manual (Bypass)	x	1	DAC Code
Trim Calculator (Closed Loop Trim Mode)	0	1	Held at last updated value by Closed Loop Trim Logic. Reset value is 80h.
Trim Calculator (Closed Loop Trim Mode)	1	1	Dynamically updated based on measured VMONx voltage and Digital Closed Loop Trim Logic.

VID Selection

The ASC can be configured to support VID (Voltage Identification) control using the TRIM block. The control signals and VID tables are created using the Platform Designer software. As shown in Figure 6.22, the VID mechanism uses the I^2C interface to control the VID Setpoint (duplicated as PROFILE 0 Setpoint). The I^2C access to the VID Setpoint can be restricted based on the ASC I^2C write protection feature that can be set during configuration.

6.13. Digital Closed Loop Trim Mode

Closed loop trim mode operation can be used when tight control over the DC-DC converter output voltage at a desired value is required. The closed loop trim mechanism operates by comparing the measured output voltage of the DC-DC converter with the internally stored Voltage Setpoint. The difference between the Voltage Setpoint and the actual DC-DC converter voltage generates an error voltage. This error voltage adjusts the DC-DC converter output voltage toward the Voltage Setpoint. This operation iterates until the Voltage Setpoint and the DC-DC converter voltage are equal. The closed loop trim hardware then continues monitoring the converter voltage and adjusts the converter output voltage as necessary. Figure 6.23 shows the closed loop trim operation of a TrimCell. At regular intervals (as determined by the Update Rate Control register) the ASC device initiates the closed loop power supply voltage correction cycle through the following blocks.

- Volatile Voltage Setpoint Register stores the desired output voltage (set by the TRIMx_P0 and TRIMx_P1 ASC-I/F signals)
- On-chip ADC is used to measure the voltage of the DC-DC converter
- Three-state comparator is used to compare the measured voltage from the ADC with the Voltage Setpoint Register contents. The output of the three state comparator can be one of the following:
  - +1 if the setpoint voltage is greater than the DC-DC converter voltage
  - –1 if the setpoint voltage is less than the DC-DC converter voltage
  - 0 if the setpoint voltage is equal to the DC-DC converter voltage
- Channel polarity control determines the polarity of the error signal (Polarity is set on a per channel basis in configuration memory)
- Closed loop trim register is used to compute and store the DAC code corresponding to the error voltage. The contents of the Closed Loop Trim will be incremented or decremented depending on the channel polarity and the three-state comparator output. If the three-state comparator output is 0, the closed loop trim register contents are left unchanged.
- The DAC in the TrimCell is used to generate the analog error voltage that adjusts the attached DC-DC converter output voltage.

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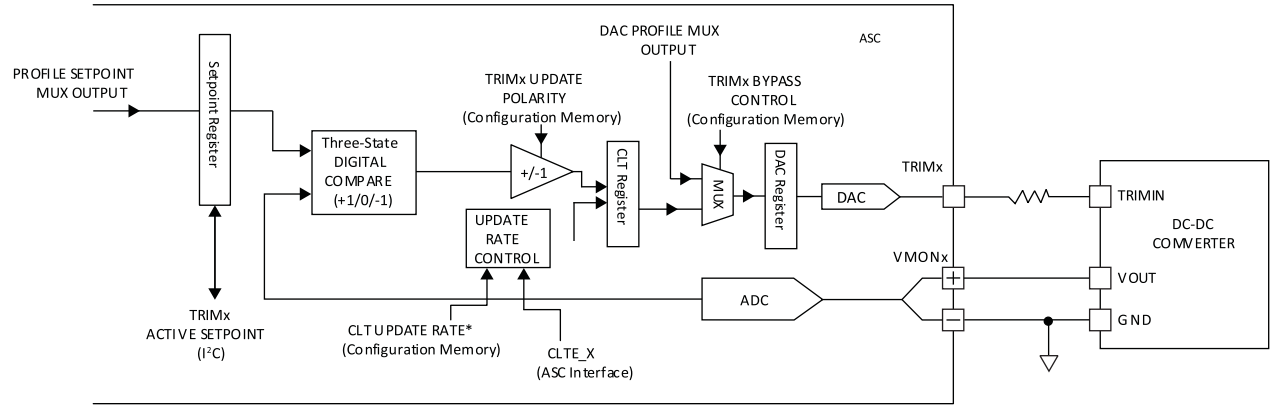

* CLT UPDATE RATE parameter is shared between all four TRIM Cells

Figure 6.23. Digital Closed Loop Trim Operation

The closed loop trim cycle interval is programmable and is set by the update rate control register. Table 6.13 lists the programmable update interval that can be selected by the update rate register. The update rate register is set in configuration memory and is shared between all TRIM cells.

Table 6.13. Closed Loop Trim Update Rates

CLT Update Rate Settings
860 µs
1.72 ms
13.8 ms
27.6 ms

There is a one-to-one relationship between the selected TrimCell and the corresponding VMON input for the closed loop operation. For example, if TrimCell 3 is used to control the power supply in the closed loop trim mode, VMON3 must be used to monitor its output power supply voltage. The closed loop operation can only be started by asserting the TRIMx_CLTE ASC-I/F signal.

TrimCell at Start-up

The status of registers and the TrimCell output during start-up or POR of the ASC is as follows.

1. The TRIM DAC output is High-Z.
2. DAC register is based on Trim configuration Mode.

Trim Configuration Mode for TRIMx channel (Platform Designer Software)	TRIMx DAC register
Manual	Profile 0 DAC code is copied to the DAC register.
Trim Calculator	Value of 80h (Bipolar-zero) is copied to the DAC register.

3. The Closed Loop Trim Logic is disabled.
4. Profile 0 Setpoint is copied to the Voltage Setpoint Register.

The DAC output mode can be enabled (TRIMx_OE) at any time by the user logic, depending on the application requirements. Normally the chosen profile (TRIMx_P0, TRIMx_P1) setpoint should be loaded and the DAC output enabled when the application is ready for trimming. If closed loop trimming is to be used, the user logic should enable the closed loop trim (TRIMx_CLTE) after the DAC output and trim profile have already been configured.

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6.14. Details of the Digital to Analog Converter (DAC)

Each trim cell has an 8-bit bipolar DAC to set the trimming voltage as shown in Figure 6.24. The full-scale output voltage of the DAC is +/– 320 mV. A code of 80H results in the DAC output set at its bi-polar zero value.

The voltage output from the DAC is added to a programmable offset value and the resultant voltage is then applied to the trim output buffer. The offset voltage is typically selected to be approximately equal to the DC-DC converter open circuit trim node voltage. This results in maximizing the DC-DC converter output voltage range.

The programmed offset value can be set to 0.6 V, 0.8 V, 1.0 V or 1.25 V. This value selection is stored in configuration memory. The configuration memory is loaded with the value set in EEPROM memory at power-on. It can be updated during runtime via I^2C commands.

The combined offset and DAC output is applied to the TRIM cell output buffer. Each output buffer is controlled by a unique TRIMx_OE signal via the ASC-I/F. When TRIMx_OE = 0, the corresponding TRIMx Pad will be placed in a high impedance state. Setting TRIMx_OE = 1 will enable the output buffer, resulting in the combined offset and DAC output being applied to the TRIM output pin.

The default state at power-on reset is TRIMx_OE = 0. The TRIM cell will maintain this setting until the ASC-I/F communication is successfully established. This ensures that the TRIM function will remain in a passive, high impedance state, until it is enabled the user control logic.

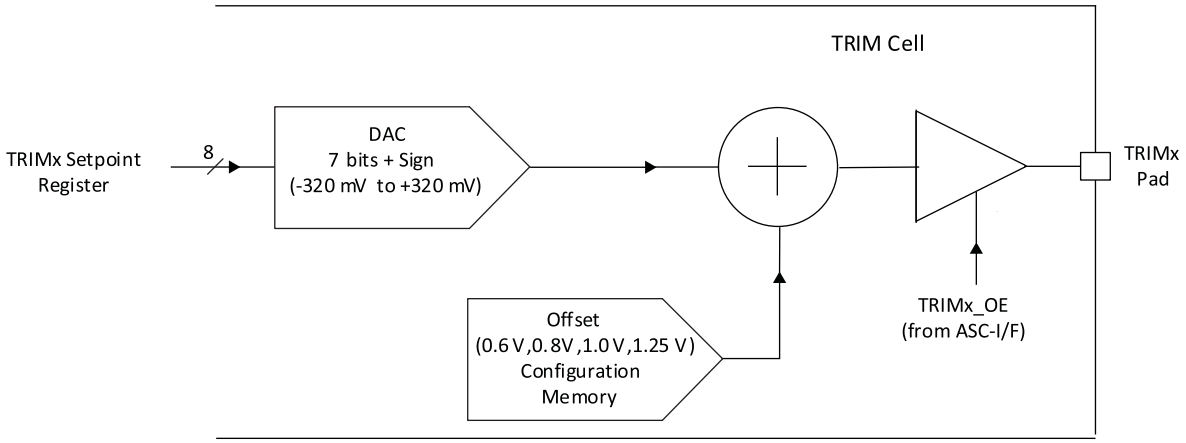

Figure 6.24. Offset Voltage is Added to DAC Output Voltage to Derive Trim Pad Voltage

6.15. Fault Logging and User Tag Memory

The ASC contains the following storage space used with Fault Logging or User Tag operation:

- Non-volatile EEPROM memory array which has 16 rows where each row stores 7 bytes of data.
- A volatile memory register which stores 7 bytes of data.

The ASC can be configured to choose this memory, either for User Tag Operation or Fault Log Operation through Platform Designer Software. Figure 6.25 shows the interface to the EEPROM memory and Volatile register for data access.

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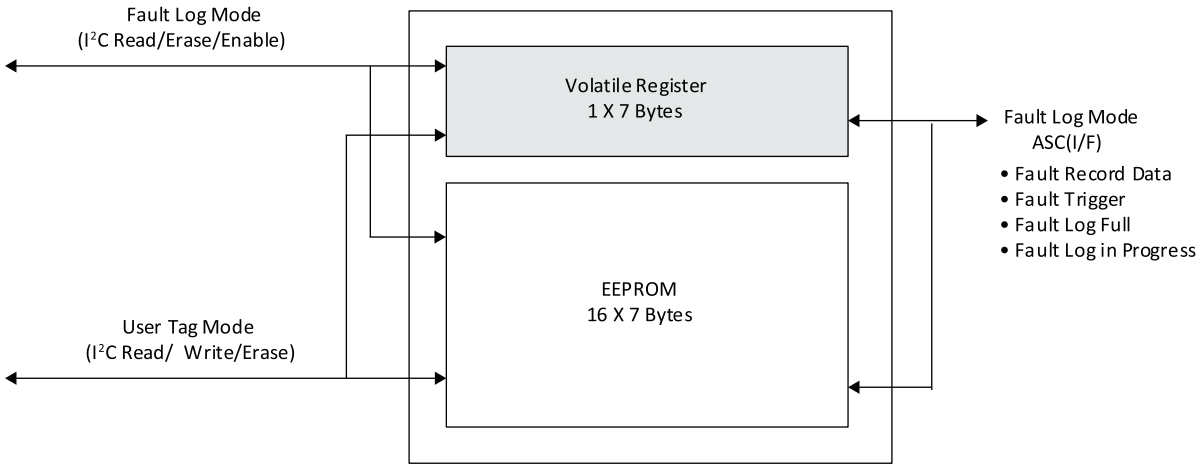

Figure 6.25. Access to EEPROM and Volatile Memory for Fault Logging/User Tag Operation

User Tag Memory

When the ASC is configured for User Tag Mode, the memory block can be used as a scratch pad memory for critical data, board serialization, board revision logs, programmed pattern identification or as general data storage in EEPROM.

As shown in Figure 6.25, in the User Tag Mode, data can be read, written or erased from the EEPROM or Volatile Register via the I²C interface of the ASC. For more details, please refer to User Tag Memory Access section of this data sheet.

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Fault Log Memory

When the ASC is configured for Fault Log Mode, the memory block is used to record the status of the ASC GPIOs, VMON, IMON, TMON and other significant logic signals on the occurrence of the user defined fault trigger condition. The ASC can also be used with Platform Manager 2 or MachXO2 devices to log faults to User Flash Memory (UFM) or external SPI flash. See Fault Logging Using Platform Manager 2 (TN1277) for more details.

Each fault record has seven bytes, six bytes of ASC specific data and one byte of user specified FPGA signals. The ASC Fault Log Record Memory Map is shown in Table 6.14. Erased fault records and fault records which have not been written yet will read all zeros.

Table 6.14. Fault Log Record Memory Map

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	User bit7	User bit6	User bit5	User bit4	User bit3	User bit2	User bit1	User bit0
1	AGOOD	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4
2	GPIO3	GPIO2	GPIO1	HVOUT4	HVOUT3	HVOUT2	HVOUT1	HIMONB
3	HIMONA	IMON1B	IMON1A	HVMONB	HVMONA	VMON9B	VMON9A	VMON8B
4	VMON8A	VMON7B	VMON7A	VMON6B	VMON6A	VMON5B	VMON5A	VMON4B
5	VMON4A	VMON3B	VMON3A	VMON2B	VMON2A	VMON1B	VMON1A	TMON2B
6	TMON2A	TMON1B	TMON1A	TMONINB	TMONINA	1	0	1

The ASC can be configured to store fault log data either in the EEPROM array or the Volatile register.

The EEPROM memory array can store up to 16 fault log records. When the fault log memory is full no further fault log records can be stored in the EEPROM and any future trigger signals will be ignored.

The volatile register can also be used to store faults. The volatile fault log contains only one record of 7 bytes and each time the trigger signal is asserted the current data will be stored in the register overwriting any previous data. In order to preserve the volatile register fault log data it must be read back prior to the next assertion of the trigger signal.

The following control signals for ASC based Fault Logging are defined in the Platform Designer software for use in the FPGA logic:

- Fault_Log_Trigger: This user defined signal is used to initiate fault log recording. Recording is initiated by toggling the fault log trigger signal high based on the FPGA logic. The Fault log trigger signal should be set high for a minimum period (see Recommended Operating Conditions section). The fault log trigger signal initiates fault log recording for all ASCs in the system. Readback must be disabled for the fault log recording to begin.
- ASCx_Fault_Log_Full: This ASC-I/F signal reports to the user logic when the EEPROM for the given ASC is full.
- ASCx_Fault_Log_In_Progress: This ASC-I/F signal reports to the user logic when a fault log operation for the given ASC is in progress.

When the ASC is configured for Fault Log Operation, the Fault Record Data frame, as shown in Table 6.14, is captured every 16 us. When the fault log trigger signal is asserted, the captured data is stored in the selected memory. This includes the user bits in the fault record. These user bits are not used for any other ASC functions.

The read-back function of the Fault Log must be enabled in order to read or erase the Fault Log. The read-back is enabled using the I^2C interface. As shown in Figure 6.25, the Fault Log contents can be read or erased from the EEPROM or the volatile register via the I^2C interface of the ASC.

When the user enables the read-back of the fault log contents, the fault log recording is disabled and must be re-enabled by the user after the read-back is completed in order to store future fault log events. For more information about reading, erasing and enabling the fault log recording refer to Fault Log Memory Access section.

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7. FPGA Section Architecture Overview

The Platform Manager 2 family architecture is based on the MachXO2 family architecture. This architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The Platform Manager 2 also includes blocks of sysMEM Embedded Block RAM (EBRs). Figure 7.1 shows the block diagram of the FPGA section of the Platform Manager 2.

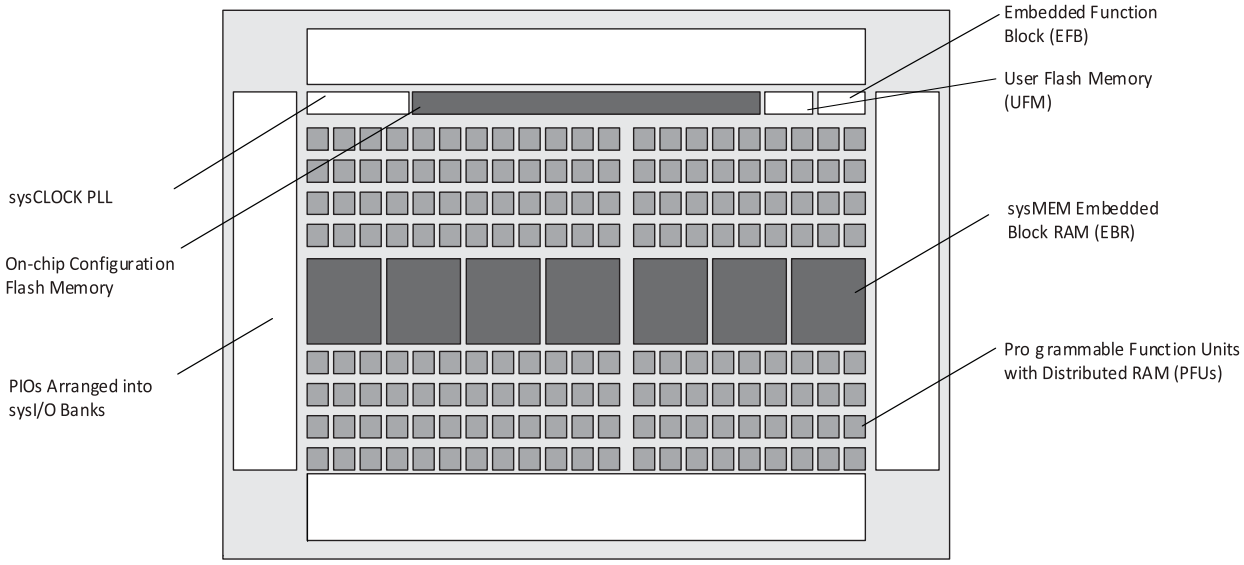

Figure 7.1. Platform Manager 2 FPGA Section Block Diagram

The Programmable Functional Unit (PFU) logic blocks, and sysMEM EBR blocks are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in four sysI/O banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The PFU, EBR, and PIO blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocate these routing resources.

The FPGA section provides one sysCLOCK Phase Locked Loop (PLL). The PLL has multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks. The Platform Manager 2 devices provide commonly used hardened functions such as SPI controller, I^2C controller, timer/counter, and User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I^2C and JTAG ports. The Platform Manager 2 family devices have a JTAG port that supports programming and configuration of the device as well as access to the user logic.

The Platform Manager 2 operates on a 3.3 V power supply.

7.1. PFU Blocks

The Platform Manager 2 uses a Lookup Table (LUT) architecture. The core of the Platform Manager 2 consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM, and distributed ROM functions. Each PFU consists of four interconnected slices and each slice contains two LUTs and 2 registers. The LUTs in each slice can be configured as 4-input combinatorial lookup tables and can be used to implement 4-input logic functions. Larger input functions are implemented by combining LUTs together. The slices can also be configured to operate as Distributed RAM or ROM memory if desired. The Diamond software design tool will automatically place the logic functions for the design and route the connections required between the PFUs and to other resources. See MachXO2 Family Data Sheet (FPGA-DS-02056) for more details on the PFU Blocks.

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7.2. Clock Resources

There are eight dedicated primary clock routing lines available in the Platform Manager 2 architecture which allows the software to route the clocks in the most efficient manner. The input clock signals should be connected to the primary clock input pins (PCLK) for the most efficient use of the primary clock resources. There are six PCLK input pins available for user logic in the LPTM21 (237-Ball ftBGA package) and a seventh PCLK pin is reserved for system use by the ASCCLK signal (An eighth PCLK pin is used by the primary I^2C port). The LPTM21L (100-Ball caBGA package) has only four PCLK input pins available for user logic. When using a single-ended clock input only the true clock pin (PCLKT) can directly drive the primary clock lines. The primary clock lines can also be driven by internal resources such as the PFU connections for added flexibility.

The eight primary clock lines in the primary clock network can drive throughout the entire device to provide clocks for all the resources within the device. For the most efficient designs, the clock signals that are used by the largest number of resources (LUTs, EBRs, or I/O cells) should utilize the primary clock routing resources. Each of the primary clock routing lines has a Dynamic Clock enable feature which can be utilized if desired. In addition, two of the eight primary clock lines have dynamic clock switches to allow switching between two different clock sources. Any of the primary clock input pins can drive any of the eight primary clock lines so the user does not have to be concerned about which clock pin to use in order to use the dynamic clock switches.

There are also eight secondary high fan-out routing lines available for signals which go to many PFUs such as local resets or clock enables. These secondary routing lines can be driven by internal logic or from a PCLK pin.

There is one programmable Phase Locked Loop available, sysCLOCK PLL, which can be used to generate higher or lower clock frequencies for the design if desired. The PLL can be driven by the system clock input, from an external PLL clock input pin, or from internal routing. The PLL has 4 outputs available and each has its own output divider, thus allowing the PLL to generate different frequencies for each output. The outputs can be used to drive the clock distribution network, other internal routing resources, or external output pins. The PLL provides a wide range of configurable features - for more information see MachXO2 sysClock PLL Design and Usage Guide (FPGA-TN-02157).

There is one programmable internal Oscillator available in the Platform Manager 2 FPGA section which can be used to generate a clock source for internal logic or other uses. The internal oscillator frequency ranges from 2.08 MHz up to 133 MHz.

7.3. sysI/O Resources

The FPGA section of Platform Manager 2 has four I/O banks. The I/O buffers in each bank can support single-ended and differential I/O standards. The VCCIO voltage for each I/O bank can be independent to allow the designer to use different I/O standards in different banks if desired. Multiple input standards can be supported in a bank as shown in Table 7.1. The output standards used in each bank must match the bank VCCIO voltages shown in Table 7.2.

The I/O resources in each bank are arranged in groups called a Programmable I/O Cell (PIC) block. Each PIC block has four programmable I/Os, grouped into two pairs. Each pair can form a pair of complementary output drivers. One pair is labeled as the A and B pins while the other is labeled as the C and D pins. The pins within the pair are also designated as a True and a Complementary pin for use with the differential I/O standards. In some cases not all the pins within a PIC are available as package pins.

The I/O buffers support individually configurable drive strength and bus maintenance (weak pull-up, weak pulldown, or bus keeper) circuits for most standards. See MachXO2 sysI/O Usage Guide (FPGA-TN-02158) for more detailed information about the use of the I/O resources in the FPGA sections.

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Table 7.1. Supported Input Standards

VCCIO (Typical)					
Input Standard	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V
Single-Ended Interfaces	—	—	—	—	—
LVTTL	Y	Y2	Y2	Y2	—
LVCMOS33	Y	Y2	Y2	Y2	—
LVCMOS25	Y2	Y	Y2	Y2	—
LVCMOS18	Y2	Y2	Y	Y2	—
LVCMOS15	Y2	Y2	Y2	Y	Y2
LVCMOS12	Y2	Y2	Y2	Y2	Y
PCI1	Y	—	—	—	—
SSTL25 (Class I, Class II)	—	Y	—	—	—
SSTL18 (Class I, Class II)	—	—	Y	—	—
HSTL18 (Class I, Class II)	—	—	Y	—	—
Differential Interfaces	—	—	—	—	—
LVDS	Y	Y	—	—	—
BLVDS, MLVDS, LVPECL, RSDS	Y	Y	—	—	—
Differential SSTL25 Class I, II	—	Y	—	—	—
Differential SSTL18 Class I, II	—	—	Y	—	—
Differential HSTL18 Class I, II	—	—	Y	—	—

Notes:

1. Bank 2 of FPGA section only.
2. Reduced functionality. Refer to MachXO2 sysI/O Usage Guide (FPGA-TN-02158) for more details.

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Table 7.2. Supported Output Standards

Output Standard	VCCIO (Typical)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
PCI33	3.3
SSTL25 (Class I)	2.5
SSTL18 (Class I)	1.8
HSTL18 (Class I)	1.8
Differential Interfaces	
LVDS[1, 2]	2.5, 3.3
BLVDS, MLVDS, RSDS2	2.5
LVPECL[2]	3.3
Differential SSTL25	2.5
Differential SSTL18	1.8
Differential HSTL18	1.8

Notes:

1. The FPGA section has dedicated LVDS output buffers in bank 0 only.
2. These interfaces can be emulated with external resistors in all banks of the FPGA section.

7.4. sysMEM Embedded Block RAM Memory (EBR)

The Platform Manager 2 contains sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM with dedicated input and output registers. These EBRs can implement single port, dual port, or First-In First-Out (FIFO) memories in a variety of depths and widths. Larger and deeper blocks of RAM can be created by cascading the EBRs together. Typically the Lattice design software will cascade memory transparently based upon the specific design inputs.

If desired, the contents of the EBR RAM can be pre-loaded during device configuration. The EBR can also be used as ROM if required. The FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize the LUT usage. For further information on the sysMEM EBR block, please refer to Memory Usage Guide for MachXO2 Devices (FPGA-TN-02159).

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7.5. Embedded Hardened IP Functions and User Flash Memory

The Platform Manager 2 provides embedded hardened functions such as SPI, I²C, Timer/Counter and User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 7.2.

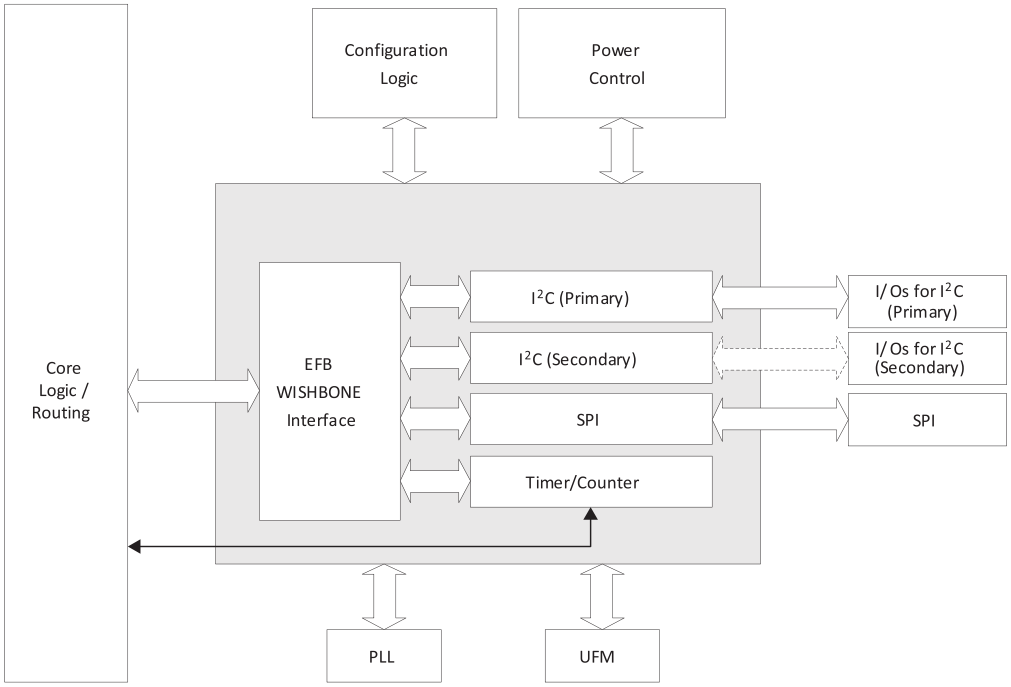

Figure 7.2. Embedded Blocks Interface

The Platform Manager 2 contains two I²C IP cores, the primary and secondary I²C IP cores. Each core can be configured either as an I²C master or as an I²C slave. The main difference between the two IP cores is that the primary core has pre-assigned I/O pin whereas users can assign I/O pins for the secondary core.

The hardened SPI core can be configured as either a SPI master or slave. The Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. For details on these embedded functions, please refer to Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162).

7.6. User Flash Memory (UFM)

The Platform Manager 2 provides a User Flash Memory block (UFM) which contains up to 64 Kbits of non-volatile memory. The UFM can be used for a variety of applications including storing the time stamped fault log, storing EBR initialization data, or as general purpose user flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. The UFM can also be accessed through the JTAG, SPI, and the primary I²C ports of the device. For more information on the UFM, please refer to Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162).

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7.7. System Resources Usage

The Platform Manager 2 can be configured for different functions as required by the customer's requirements. The Lattice Diamond software and Platform Designer tool provide a flexible interface to configure the hardware management functions of the device. The device configuration that is produced by the software will automatically assign certain device resources. As a result, certain resources in the device may not be available for general use.

The following resources may be fully or partially assigned depending on the selected functions in the design software.

- EBRs
- Timer / Counter
- Primary I^2C
- PLL
- SPI
- UFM

For more details on the programmable logic architecture, see MachXO2 Family Data Sheet (FPGA-DS-02056).

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8. System Connections

The Platform Manager 2 is a fast-reacting, programmable logic based hardware management controller. The Platform Manager 2 can be paired with the L-ASC10 (ASC) hardware management expander to expand the number of resources available to the hardware management system. In order for the Platform Manager 2 to function properly as a hardware management controller, there are a number of mandatory system connections. The overall set of required connections between the Platform Manager 2 and ASC hardware expanders are shown in Figure 8.1 and Figure 8.2 below. The required connections include Clock, Reset, ASC Interface (ASC-I/F) and I^2C. These connections are assigned and managed using Diamond software and the Platform Designer tool. Each of the connection requirements is described below.

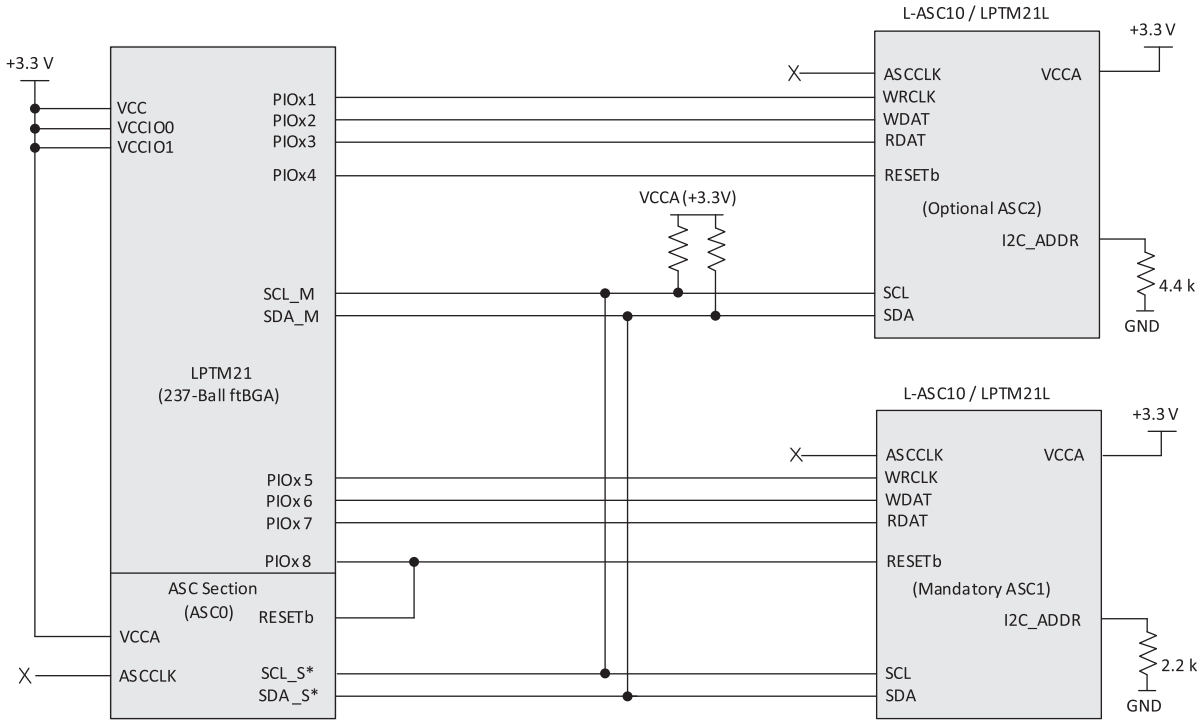

Figure 8.1. System Connections - LPTM21 and ASCs or LPTM21Ls

Note: Hardware connections may require additional passive components not shown, see L-ASC10 and Platform Manager 2 Hardware Checklist (FPGA-TN-02175) for more details.

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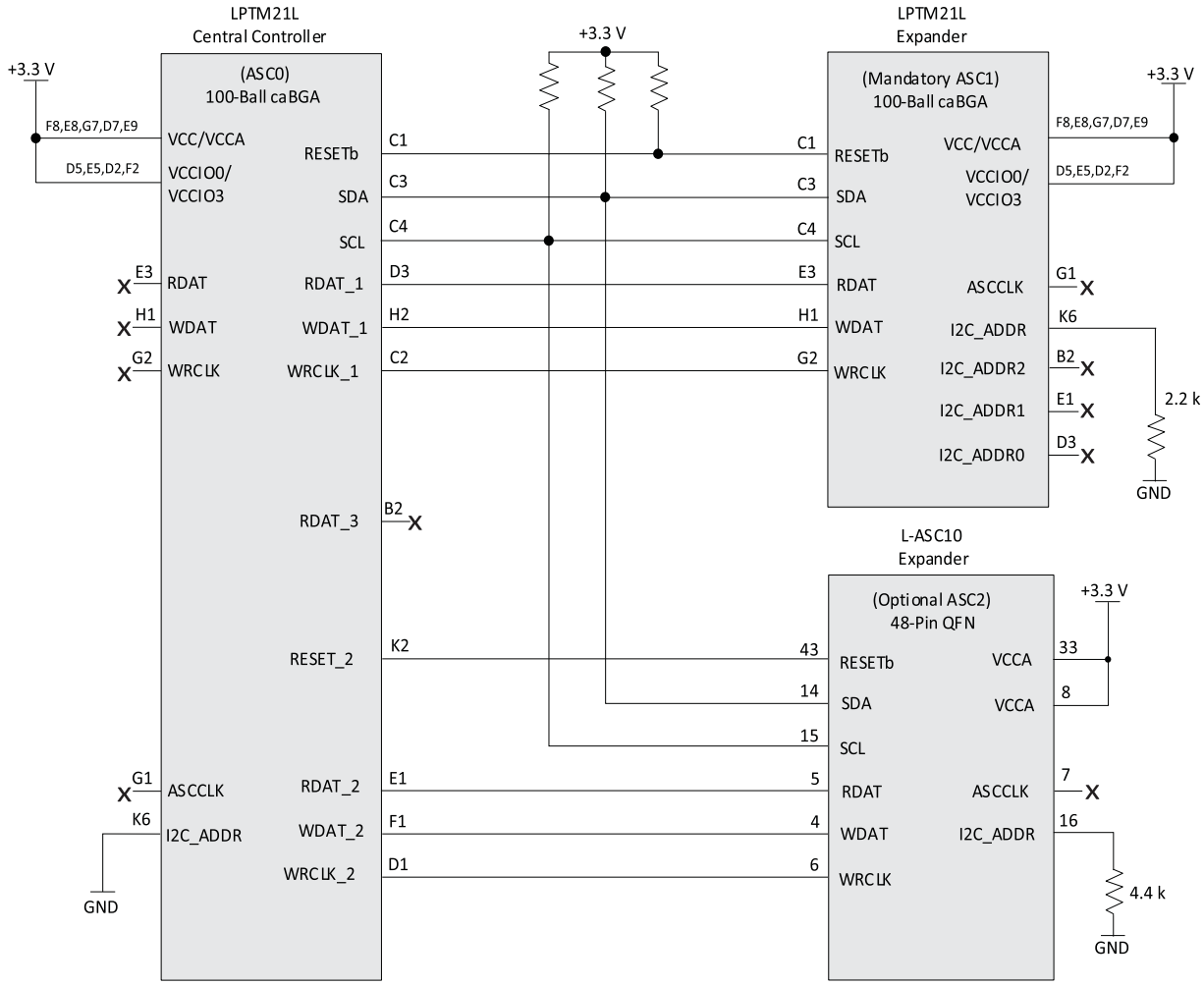

Figure 8.2. System Connections - LPTM21L and LPTM21Ls or ASCs

Note: Hardware connections may require additional passive components not shown, see L-ASC10 and Platform Manager 2 Hardware Checklist (FPGA-TN-02175) for more details.

8.1. Clock requirements

The ASC has an internal 8 MHz clock source which is used by the device during startup. Once startup has successfully completed, the ASC will switch to the ASC-I/F system clock signal (WRCLK) for operation. The Platform Manager 2 provides the WRCLK signal for each ASC in the system. This ensures that the system is fully synchronized to a common clock source to minimize any differences in timing.

The ASC has a built-in detection circuit for WRCLK loss. If a loss of WRCLK is detected, the ASC will reset itself and pull RESETb low. The device I/O will return to safe state, as described in the Safe State section.

The ASC clock signal connected internally in the Platform Manager 2 device (see Figure 8.1), making the ASCCLK pin a no-connect in Platform Manager 2 systems. All ASC devices (both optional and mandatory) in the system will disable their ASCCLK output signal and this pin should be treated as a no connect.

An external 8 MHz clock source can be used as the system clock instead of the ASCCLK. In this case, the ASCCLK output will be disabled and the external clock should be connected to the ASCCLK pin on Platform Manager 2. The user must specify that an external clock source is being used in software.

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8.2. RESET Requirements

The ASC RESETb pin is used for synchronizing the ASC section with the Platform Manager 2 FPGA section and other ASC hardware management expanders. The RESETb pin should not be driven by any external device as this will adversely affect the system operation. A software reset signal for the internal logic can be created using a PIO pin on the Platform Manager 2.

The ASC section RESETb must be externally connected to a PIO signal from the FPGA section of Platform Manager 2. This PIO must be assigned as the ASC0_RSTN signal in the design software.

External ASCs used in a system can be designated as either Mandatory or Optional. The Mandatory or Optional designation determines how the RESETb pins must be connected and how the system will treat the Reset signal from each ASC. The Mandatory or Optional designation must be specified in the design software.

A Mandatory ASC is required to be present at system start-up. The RESETb pins for all mandatory ASCs must be connected to the RESETb pin on the Platform Manager 2 (as shown in Figure 8.1). The internal ASC section of Platform Manager 2 is always designated as ASC0 and is always mandatory. If any one of the mandatory ASCs cannot be detected by the hardware management controller, the system will be held in reset. Any of the mandatory ASCs which experience a critical issue (such as loss of WRCLK signal) will hold the Reset signal low, keeping the system in reset.

An Optional ASC is not required to be present at system start-up. This designation can be used for ASCs placed on plug in modules or optional boards in a system. The RESETb pin of each optional ASC should be connected to a unique PIO pin on the Platform Manager 2. Each reset signal is treated individually, so that only the registers associated with a particular Optional ASC will reset when the reset input is driven low. The rest of the system, both Mandatory and other Optional ASCs, will continue to operate normally without interruption.

8.3. ASC Interface and I^{2}C Connections

The ASC uses two communication links to transfer information between the ASC and the Platform Manager 2. These are the ASC Interface (ASC-I/F) and I^{2}C bus. These two links are used for different types of information and both must be connected properly for the system to operate correctly.

The ASC-I/F bus uses three signals: WRCLK, WDAT, and RDAT. The ASC-I/F bus operates at 8 MHz and includes error checking and reporting capabilities. The ASC and FPGA sections of Platform Manager 2 have an internal ASC-I/F connection which is automatically setup by the design software. The ASC-I/F pins on external ASC or LPTM21L devices must be connected to three PIO pins on the Platform Manager 2. These three PIO pins are assigned in the design software. The design software will automatically instantiate the interface for communicating with the ASC devices. Each expander device requires its own unique ASC-I/F link, as shown in Figure 8.1 and Figure 8.2. The ASC-I/F uses the LVCMOS 3.3/LVTTL standard for both ASC and PIO pins, as listed in Table 5.20.

For the LPTM21 237-Ball ftBGA package, the VCCA, VCC, VCCIO0, and VCCIO1 pins should be connected to the same power supply. VCCA can be separately filtered for improved performance of the analog monitors. Care should be taken that Bank 1 (the bank used for the internal connection of the FPGA and ASC sections) is not exposed to significant SSO noise, as this can degrade the performance of the analog monitors. See L-ASC10 and Platform Manager 2 Hardware Checklist (FPGA-TN-02175) for more details.

For the LPTM21L 100-Ball caBGA package, the VCCA, VCC, VCCIO0, and VCCIO3 pins should be connected to the same power supply. VCCA can be separately filtered for improved performance of the analog monitors. Care should be taken that Bank 3 (the bank used for the internal connection of the FPGA and ASC sections) is not exposed to significant SSO noise, as this can degrade the performance of the analog monitors. See L-ASC10 and Platform Manager 2 Hardware Checklist (FPGA-TN-02175) for more details.

The I^{2}C bus uses the SDA and SCL pins and operates at 100 kHz to 400 kHz. When using the 237-Ball ftBGA device, the user must connect the SDA and SCL pins on the ASC to the SDA_M/SCL_M pins on the Platform Manager 2 (as shown in Figure 8.1). The LPTM21L (100-Ball caBGA package) Platform Manager 2 makes the connections internally so only two pins are needed to connect to the I^{2}C bus (as shown in Figure 8.2). Table 8.1 details the I2C_ADDR pin connections based how many hardware expanders are included in the system. External pull-up resistors from SDA and SCL to VCCA are required in all configurations. See the I2C Interface section for full details.

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When using the LPTM21L (100-Ball caBGA package) Platform Manager 2 as a hardware expander, the FPGA section I²C device address can be changed to avoid bus conflicts. Three pins are sampled at power up to determine the address range occupied by the FPGA section, as listed in Table 8.2 and shown in Figure 8.2.

Table 8.1. R_{addr} Value vs. ASC Section Device Number

R_{addr} Value[1] (on I²C_ADDR pin)	3 LSB of I²C Slave Address	ASC Section Device Number
None (Tie to GND)[2]	000	0
2.2 kΩ	001	1
4.4 kΩ[3]	010	2
7 kΩ[4]	011	3
10 kΩ	100	4
13.7 kΩ	101	5
17.8 kΩ	110	6
None (Tie to V_{CCA})	111	7

Notes:

1. All resistor values should be +/- 1% tolerance or better.
2. The LPTM21 (237-Ball ftBGA package) makes this connection to GND internally.
3. For designs that utilize E-96 resistors a value of 4.42 kΩ can also be used.
4. For designs that utilize E-96 resistors a value of 7.15 kΩ can also be used.

Table 8.2. LPTM21L (100-Ball caBGA Package) Setting the FPGA Section I²C Address Range

Logical State of Input at Power Up[1]			FPGA Section I²C Address Used
B2 I2C_ADDR2	E1 I2C_ADDR1	D3 I2C_ADDR0	
0	0	0	0x20 – 0x23
0	0	1	0x24 – 0x27
0	1	0	0x28 – 0x2B
0	1	1	0x2C – 0x2F
1	0	0	0x30 – 0x33
1	0	1	0x34 – 0x37
1	1	0	0x38 – 0x3B
1	1	1	0x3C – 0x3F

Note: Install a 1 kΩ pull up resistor to VCC to set the input to logic 1.

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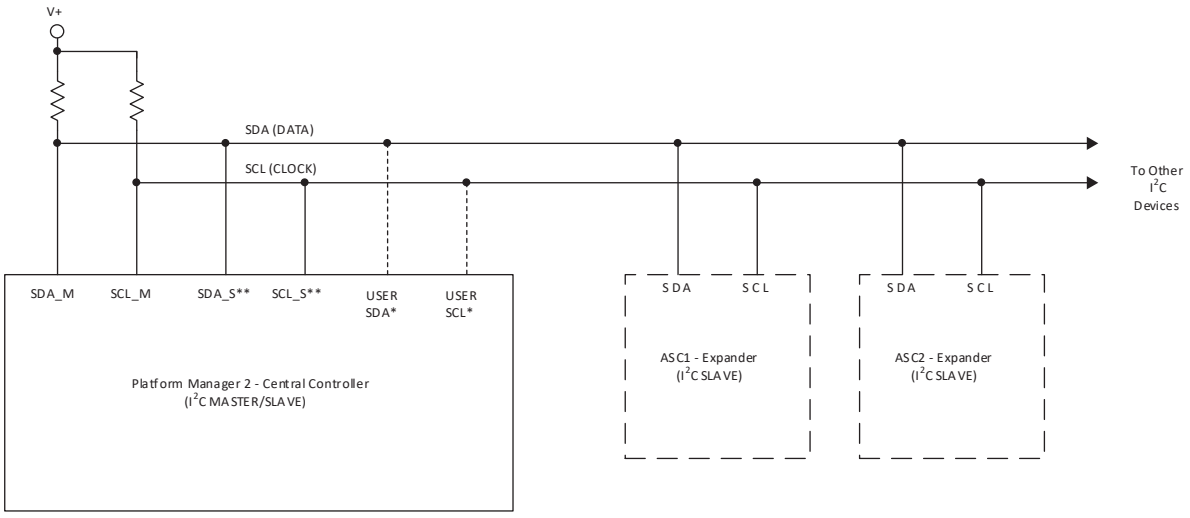
9. I²C Interface

I²C is a low-speed serial interface protocol designed to enable communications among a number of devices on a circuit board. The ASC section of Platform Manager 2 supports the I²C communications protocol 7-bit addressing. The I²C interface of the ASC section is used for programming by the Platform Manager 2 or other system processor. The interface is also used for accessing measurement and control functions and fault log memory on the device. Figure 9.1 shows a typical I²C configuration, in which the Platform Manager 2 I²C master and slave ports are connected together. Additional ASC hardware management expanders may be connected to a Platform Manager 2 Hardware Management Central Controller as shown in Figure 9.1. SDA is used to carry data signals, while SCL provides a synchronous clock signal. The 7-bit address of the ASC is formed by the 4 most significant bits which are programmable in EEPROM, while the bottom 3 bits of the address are set based on the connection to the I2C_ADDR pin, as listed in Table 8.2.

The LPTM21L (100-Ball caBGA Package) also provides a method of setting the I²C address of the FPGA section. The LPTM21L is configured from the factory with an algorithm in the FPGA section that reads the logic level of three pins at power up. Based on the decoding of the three pins, a unique I²C address is written into EEPROM, as listed in Table 9.2. The FPGA section I²C address remains in effect even after the user flash memory (UFM) or configuration array (CFG) is erased.

WARNING: If the entire FPGA section is erased, then both the algorithm and the unique I²C address will be removed and the FPGA section will only respond to the default I²C address of 0x40.

Figure 9.2 shows the required connections for an LPTM21L central controller with three LPTM21L hardware expanders. At power up, the rdat signal from each hardware expander will be low so that the FPGA section I²C address of the central controller will be set to 0x20 (see Table 9.2). The three hardware expanders use the same three pins (D3, E1, and B2) of each device, with 1 kΩ pull-up resistor used to set the I²C address of their respective FPGA sections. The pins are configured with an internal weak pull-down so that unconnected pins are a logic zero (0).



* Adding a USER_SDA and USER_SCL is application dependent and not required for all systems. This port is for accessing FPGA logic resources over I²C.
**LPTM21L (100-ball caBGA package) has master and slave connected internally (see Table 92 and Table 93).

Figure 9.1. Platform Manager 2 Device on an I²C Bus

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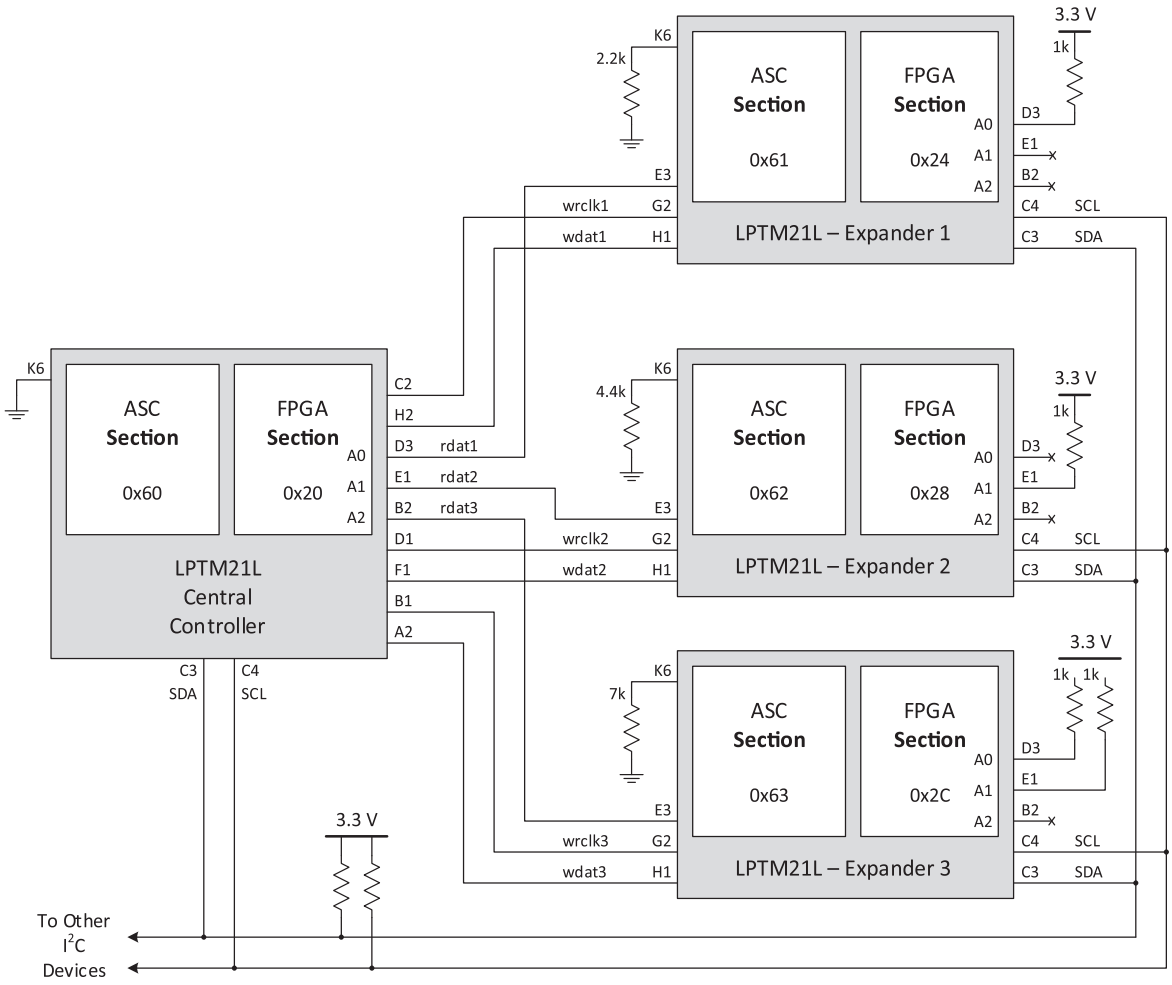

Figure 9.2. LPTM21L I²C and ASC-I/F Connections with Three Expander Devices

In the I²C protocol, the bus is controlled by a single MASTER device at any given time. This master device generates the SCL clock signal and coordinates all data transfers to and from a number of slave devices. The ASC section of the Platform Manager 2 is designed as an I²C slave. In a multiple ASC system configuration, all ASCs share the same I²C bus. This shared I²C bus is used by the Platform Manager 2 master to program the ASC devices. Each slave device is assigned a unique address. Any 7-bit address can be assigned to the ASC section, however one should note that several addresses are reserved by the I²C standard and should not be assigned to the ASC to ensure bus compatibility. These are shown in Table 9.1.

Table 9.1. I²C Reserved Slave Device Addresses

Address	R/W bit	I²C Function Description
0000 000	0	General Call Address
0000 000	1	Start Byte
0000 001	X	CBUS Address
0000 010	X	Reserved
0000 011	X	Reserved
0000 1xx	X	HS-mode master code
1111 0xx	1	10-bit addressing
1111 1xx	X	Device ID

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The ASC supports a dedicated 8-bit instruction set. These instructions are divided as follows among device programming instructions, measurement and control access, and fault log/user tag memory access. The ASC also supports configuration memory protection.

The ASC's I^2C interface allows data to be both written to and read from the device. A data write transaction, as shown in Figure 9.3, consists of the following operations:

1. Start the bus transaction
2. Transmit the slave address (7 bits) along with a low write bit
3. Transmit the instruction code as described in Table 9.2 (8 bits)
4. Transmit the first data byte to be written (8 bits). Note some instructions do not include data bytes, while others support multiple data bytes. For information on which instructions support multiple data bytes, see individual instruction details
5. Stop the bus transaction

To start the transaction, the master device holds the SCL line high while pulling SDA low. Address, instruction code and data bits are then transferred on each successive SCL pulse, in consecutive byte frames of 9 SCL pulses. Data is transferred on the first 8 SCL clocks in each frame, while an acknowledge signal is asserted by the slave device on the 9th clock in each frame. The first frame contains the 7-bit slave address, with bit 8 held low to indicate a write operation. The second frame contains the instruction code indicating the type of data to be written. The remaining frames contain the actual data to be written. The number of allowed or required data frames is determined by the instruction code used and is described in the Instruction Codes section.

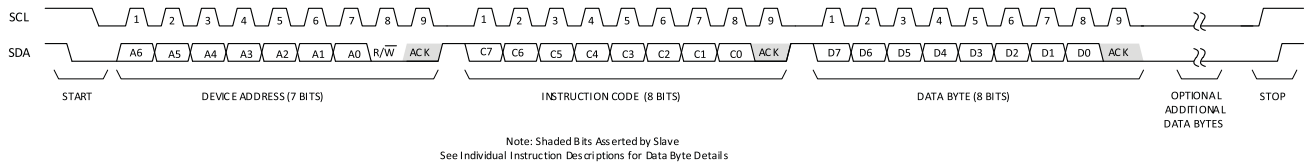

Figure 9.3. I^2C Write Operation

Reading a data byte from the ASC requires two separate bus transactions, as shown in Figure 9.4. The first transaction writes the device address with write bit, and then the instruction code indicating the type of data to be read. This transaction typically ends after the second frame since no data is being written to the slave. However, some instruction codes include additional frames, such as address information for the type of data to be read. See the Instruction Codes section for more information about the number of allowed or required data frames. No stop condition is issued at the end of the first step, to ensure that the full read operation is completed properly.

The second transaction performs the actual read, beginning with the issuing of a repeated start condition. A repeated start is a start condition issued by the master which does not follow a stop condition. This prevents the bus from being released by the master. The first frame contains the 7-bit slave address with the R/W bit held high. In the second frame, the ASC asserts data out on the bus in response to the SCL signal. Note that the acknowledge signal in the second frame is asserted by the master device and not the ASC. Depending on the instruction code, the ASC may assert additional data bytes in response to additional SCL frames depending on the instruction as detailed in the Instruction Codes section. The master completes the transaction by issuing a stop condition.

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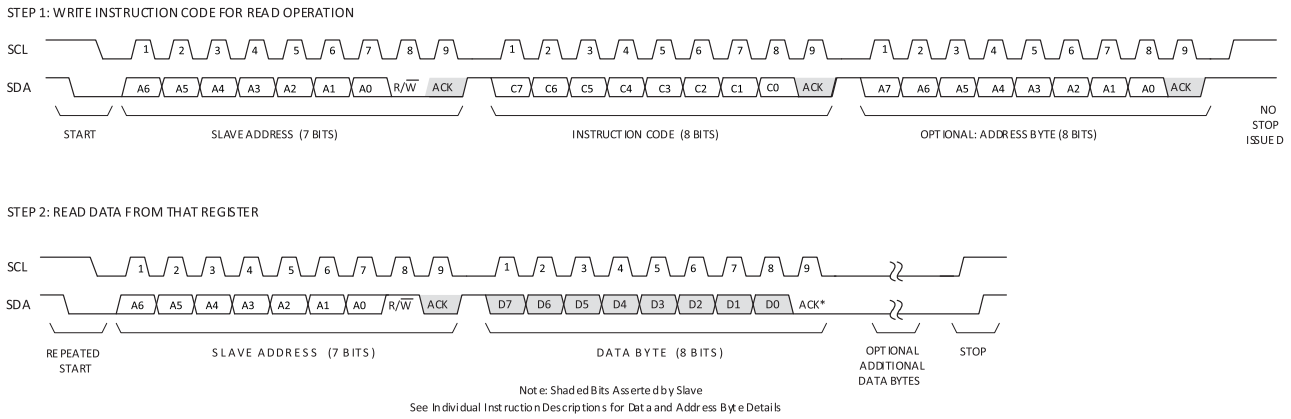

* After final data byte read, master should NACK before issuing the STOP command

Figure 9.4. I²C Read Operation

9.1. Instruction Codes

The ASC device supports a set of 8-bit instruction codes. These instructions are used to access EEPROM programming functions, shadow register programming functions, measurement and control functions, and User Tag or Fault Log memories. The instruction space is shown in Table 9.2. Each set of instructions is described in more detail in the following sections. Do not read or write to instruction codes marked reserved.

Table 9.2. I²C Instruction Summary

Instruction Code	Instruction Name	Instruction Group
0x01	RESERVED	N/A
0x02	READ_ID	Device Status and Mode Management
0x03	READ_STATUS	
0x04	ENABLE_PROG	
0x05	ENABLE_USER	
0x06-0x24	RESERVED	N/A
0x25	READ_CFG_EEPROM	ASC Configuration Memory Access
0x26-0x30	RESERVED	N/A
0x31	WRITE_CFG_REG	ASC Configuration Memory Access
0x32	WRITE_CFG_REG_wMASK	
0x33	READ_CFG_REG	
0x34	READ_ALL_CFG_REG	
0x35	LOAD_CFG_REG	
0x36-0x40	RESERVED	N/A
0x41	TRIM1_CLT_P0_SET	Closed Loop Trim Setpoint Access
0x42	TRIM2_CLT_P0_SET	
0x43	TRIM3_CLT_P0_SET	
0x44	TRIM4_CLT_P0_SET	
0x45-0x50	RESERVED	N/A
0x51	WRITE_MEAS_CTRL	Measurement and Control Register Access
0x52	READ_MEAS_CTRL	
0x53-0x60	RESERVED	N/A
0x61	ERASE_USER_TAG_EEPROM	User Tag Memory Access
0x62	WRITE_USER_TAG_REG	
0x63	READ_USER_TAG_REG	

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Instruction Code	Instruction Name	Instruction Group
0x64	PROG_USER_TAG_EEPROM	
0x65	READ_USER_TAG_EEPROM	
0x66-0x70	RESERVED	N/A
0x71	ERASE_FAULT_EEPROM	Fault Log Memory Access
0x72	RESERVED	N/A
0x73	READ_FAULT_VOLATILE_REG	Fault Log Memory Access
0x74	READ_FAULT_ENABLE	
0x75	READ_FAULT_RECORD_EEPROM	
0x76	READ_ALL_FAULT_EEPROM	
0x77-0xFF	RESERVED	N/A

Each instruction is described in detail in the following sections. The description includes information about the individual instruction code, the instruction format and any associated write or read addresses or data. The instruction format uses the following notation:

I²C Instruction Format Key (See Figure 6.8 for details of each condition or bit):

- S – Start Condition
- A[6:0] – Slave Address
- W – Write Bit (Logic 0)
- A – Acknowledge Bit
- NA – Not Acknowledge Bit
- Sr – Repeated Start Condition
- R – Read Bit (Logic 1)
- P – Stop Bit
- Shaded Bits (A) – Bits asserted by the slave

9.2. Device Status and Mode Management

There are several miscellaneous registers from the programming flow which are useful or required for completing separate operations (such as entering the programming mode to enable the User Tag memory access). These are shown in Table 9.3.

Table 9.3. Device Status and Mode Management Instruction Codes

Instruction Code	Instruction Name	Read/Write	Description
0x01	RESERVED		N/A
0x02	READ_ID	R	Read the device ID Code
0x03	READ_STATUS	R	Read the ASC Status Register
0x04	ENABLE_PROG	W	Enable the programming mode (correct two byte key required)
0x05	ENABLE_USER	W	Enable the device user mode

The READ_ID instruction is used to verify that the slave device is an ASC or the ASC section of Platform Manager 2. The device IDCODES are shown in Table 9.4. The format for the READ_ID instruction is shown in Figure 9.5.

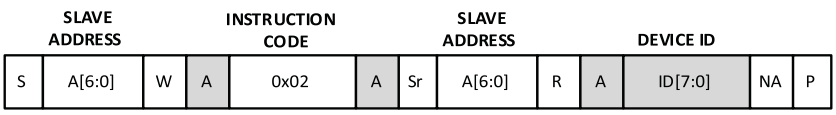

Figure 9.5. READ_ID Instruction Format

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Table 9.4. ASC ID Codes

Device	ID Code
ASC Hardware Management Expander	0x88
ASC Section of LPTM21	0x8A
ASC Section of LPTM21L	0x8A

The READ_STATUS instruction provides readout access to the two byte status register of the ASC. The READ_STATUS instruction provides information about the status of the ASC fault log memory, the current chip mode (Programming Mode or User Mode), and the status of the DONE bit of the I²C address resolution and the configuration memory. The READ_STATUS instruction format is shown in Figure 9.6. The ASC_Status_Register bit mapping is shown in Figure 9.7.

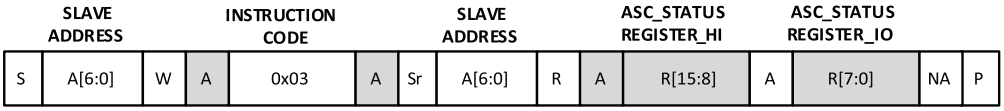

Figure 9.6. READ_STATUS - I²C Instruction Format

ASC_STATUS_REGISTER_LO (Read)

DUALBOOT_CRC _ERROR	CFGARRAY_ DONE	I2CSA_DONE	PROG_MODE	RESERVED	CFG_SHADOW_ REG_REFRESH	RESERVED	ERASE
b7	b6	b5	b4	b3	b2	b1	b0

ASC_STATUS_REGISTER_HI (Read)

PROGRAM	FAULT_UT_ ERASE	FAULT_PROG	FAULT_LOG_ FULL	FAULT_CNT[3]	FAULT_CNT[2]	FAULT_CNT[1]	FAULT_CNT[0]
b15	b14	b13	b12	b11	b10	b9	b8

Figure 9.7. ASC_Status Register

The individual status bits are described below:

- DUALBOOT_CRC_ERROR – Reset to logic 0 at power up and at the beginning of a dual-boot configuration write I²C instruction. Logic 1 when a CRC error is encountered during dual-boot configuration.
- CFGARRAY_DONE – Logic 1 if the configuration memory done bit has been programmed (set to 1 at the proper completion of an EEPROM programming operation)
- I2CSA_DONE – Logic 1 if the chip I²C slave address I2CSADone has been programmed (set to 1 at the proper completion of an EEPROM programming operation)
- PROG_MODE – Logic 1 if the chip is in programming mode, Logic 0 if the chip is in user mode
- RESERVED
- CFG_SHADOW_REG_REFRESH –Set to Logic 1 if Configuration EEPROM data was copied into corresponding shadow registers just after a Reset or after the shadow register refresh I²C instruction is given. This bit is cleared just after the status register is read out.
- ERASE – Logic 1 if any EEPROM Erase operation is in progress
- PROGRAM – Logic 1 if any EEPROM Program operation is in progress
- FAULT_UT_ERASE – Logic 1 if the ASC Fault Log or User Tag memory is currently being erased
- FAULT_PROG – Logic 1 if the ASC Fault Log data is being programmed into Fault Log EEPROM array
- FAULT_LOG_FULL – Logic 1 if all rows of the ASC Fault Log EEPROM have been programmed
- FAULT_CNT [3:0] – 4-bit value that is equal to the last row of ASC Fault Log EEPROM that has been programmed with fault log data. Row 0 up to Row FAULT_CNT have been programmed with Fault Log Data.

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The ENABLE_PROG instruction places the ASC into the programming mode. The instruction requires that a specific key code is written along with it in order to ensure that the programming mode is not entered unintentionally. The ENABLE_PROG instruction should only be used by the Lattice delivered programming algorithms or to write or erase the User Tag memory. The ASC_PROG_KEY is a two byte value of 0xE53D. The ENABLE_PROG instruction format is shown in Figure 9.8.

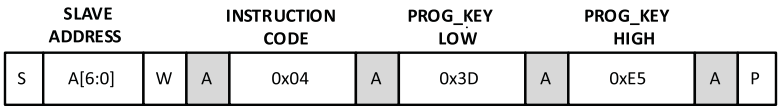

Figure 9.8. ENABLE_PROG - I²C Instruction Format

After completing a user tag operation, it is important to exit the programming mode and return to user mode. This will prevent unintentional programming operations. The ENABLE_USER instruction will return the ASC to the user mode. The ENABLE_USER instruction format is shown in Figure 9.9.

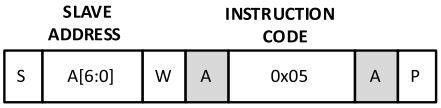

Figure 9.9. ENABLE_USER - I²C Instruction Format

9.3. ASC Configuration Memory Access

The I²C interface is used for programming the ASC device. The ASC device includes an EEPROM configuration memory which stores the device configuration in non-volatile memory. The ASC device also includes a set of shadow registers, which are used during runtime by the device to determine operational thresholds, output controls, etc. At power-on reset, the device automatically copies the EEPROM configuration memory to the shadow registers, provided the EEPROM done bit is set in the ASC Status Register. The EEPROM configuration settings are automatically generated by the Platform Designer software tool.

The I²C interface unit provides access to both the non-volatile EEPROM memory and the configuration shadow registers for erase, programming, and verify operations. The EEPROM memory is background programmed. It can be copied to the configuration shadow registers at the end of programming by an additional I²C instruction. The EEPROM configuration memory map is automatically generated by the Platform Designer software. The flow and usage of the EEPROM instructions is handled by the Lattice Diamond Programmer software (for PC-based programming) or the Lattice deployment tool (for programming the device via a tester or an on-board microcontroller using the I²C embedded solution). Lattice recommends using these software tools to access the EEPROM configuration programming instruction space.

The I²C interface can also be used to re-configure the shadow registers directly. These instructions provide access to individual voltage monitor thresholds, temperature measurement settings, and other device configuration parameters. Some configuration shadow registers are implemented as master/slave pairs. These shadow registers do not update operational parameters immediately after I²C configuration writes to the master shadow register. They support an additional load instruction which updates all slave shadow registers from the master shadow registers at the same time. Other shadow registers are implemented as a single master-only register. These registers update their operation (or reset the associated circuit) immediately after an I²C configuration write. The configuration memory architecture is shown in Figure 9.10. The ASC Configuration Registers section details which registers support the additional load instruction. The configuration registers can be accessed in user mode, although overwriting the registers can be protected through additional device settings. The configuration register access instructions are shown in Table 9.5.

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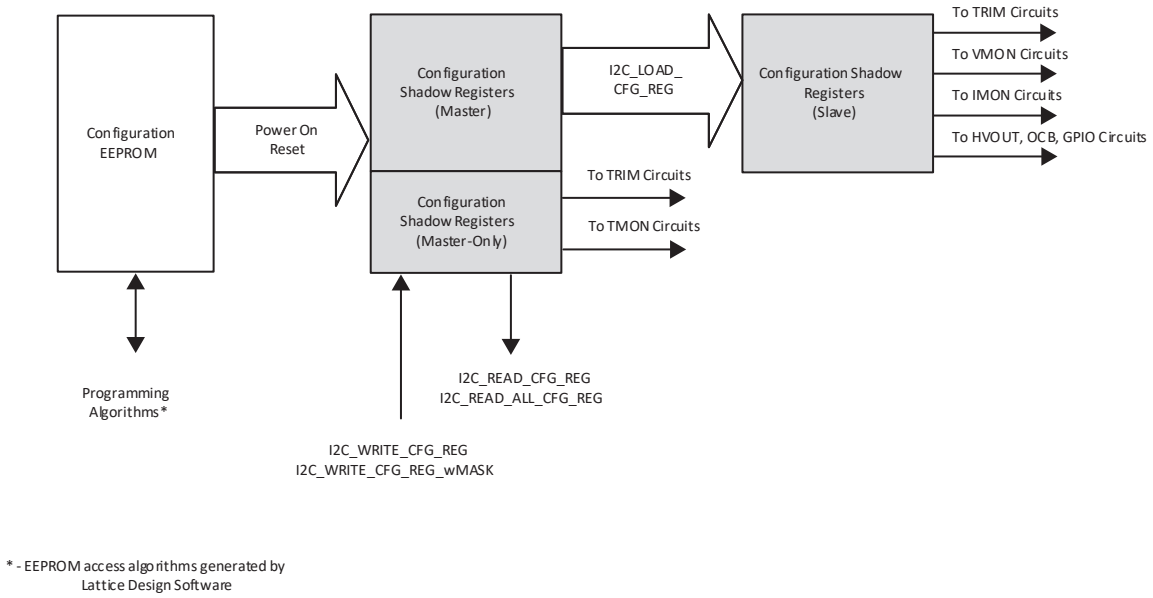

Figure 9.10. Configuration Memory Architecture

Table 9.5. Configuration Register Instruction Codes

Instruction Code	Instruction Name	Read/Write	Description
0x25	READ_CFG_EEPROM	R	Read out the selected configuration EEPROM byte or bytes
0x31	WRITE_CFG_REG	W	Write configuration data byte to addressed register
0x32	WRITE_CFG_REG_wMASK	W	Write masked configuration data bits to addressed register
0x33	READ_CFG_REG	R	Read addressed configuration register
0x34	READ_ALL_CFG_REG	R	Read all configuration registers, starting at address 0x00
0x35	LOAD_CFG_REG	W	Load the slave shadow configuration registers from the I^2C master shadow configuration registers (not all registers supported, see Table 9.6)

The configuration registers and address map are shown in the tables in the ASC Configuration Registers section. The tables in this section also describe which registers support the LOAD_CFG_REG instruction.

Special configuration memory parameters (such as the Write Protect setting, User Tag / Fault Log mode, and UES bits) can only be modified in EEPROM. They cannot be modified using configuration register instructions. This increases the reliability of the device operation.

The READ_CFG_EEPROM instruction is used to readout the contents of an addressed byte or bytes of configuration EEPROM. This instruction will readout the configuration data stored in the EEPROM memory – this is not necessarily the current device configuration. The current device configuration can be readout using the READ_CFG_REG or READ_ALL_CFG_REG commands. The address map for the configuration EEPROM is the same as the configuration register map. The READ_CFG_EEPROM instruction is the only mechanism for reading out the User Electronic Signature (described in Table 9.54). The READ_CFG_EEPROM is a two-step transaction operation, as shown in Figure 9.11. In the first step, a write transaction is performed with the 0x25 instruction, and an 8-bit address code corresponding to a specific memory address (defined in the ASC Configuration Registers section).

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In the second step, a read transaction is used to read the EEPROM memory contents. The memory address will auto-increment to support reading multiple bytes in a single transaction. This means a single transaction can support reading the entire configuration address map (120 bytes), if the starting address of 0x00 is used. A stop condition will complete the read transaction, this can be issued after any number of bytes have been read.

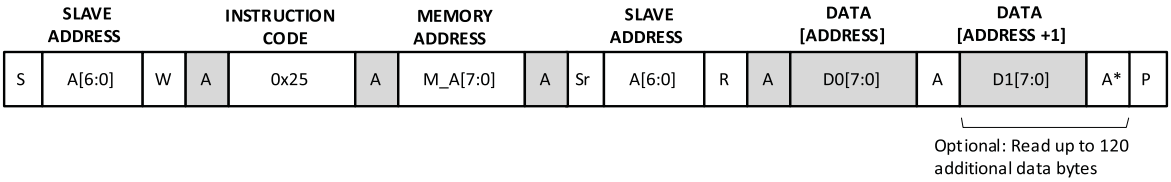

Figure 9.11. READ_EEPROM - I²C Instruction Format

The WRITE_CFG_REG instruction is used to write configuration data to an addressed register. The instruction format includes an address byte and at least one data byte, as shown in Figure 9.12. Additional data bytes can be written in a single transaction as the configuration register address will increment automatically. A stop condition will complete the write transaction, this can be issued after any number of bytes have been written. The WRITE_CFG_REG instruction should be used with caution, as many of the configuration registers are used to define multiple device options. In many cases, the WRITE_CFG_REG_wMASK instruction is a more reliable method for updating a single configuration parameter. For configuration registers which support the LOAD_CFG_REG instruction, the slave shadow registers will not be updated until the LOAD_CFG_REG instruction is executed. Master-only shadow registers will be updated immediately, and in some cases will reset their circuitry (see the ASC Configuration Registers section).

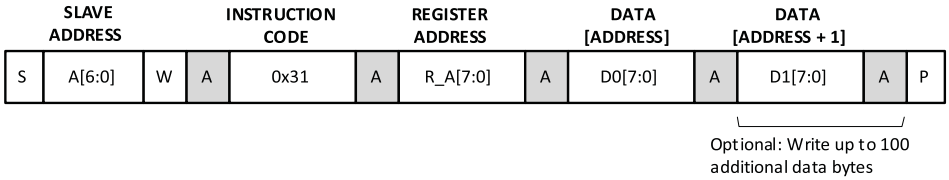

Figure 9.12. WRITE_CFG_REG - I²C Instruction Format

The WRITE_CFG_REG_wMASK instruction is used to write the masked configuration data bits to an addressed master register. The instruction format includes an address byte and at least one mask byte / data byte pair, as shown in Figure 9.13. Additional mask and data byte pairs can be written in a single transaction as the configuration register address will increment automatically. A stop condition will complete the write transaction, this can be issued after any number of data and mask pairs have been written. This instruction will not modify the configuration bits set to 1 in the mask byte. Those configuration bits will keep their current value. Bit locations set to 0 in the mask byte will be modified by the data byte. For configuration registers which support the LOAD_CFG_REG instruction, the slave shadow registers will not be updated until the LOAD_CFG_REG instruction is executed. Master-only shadow registers will be updated immediately, and in some cases will reset their circuitry.

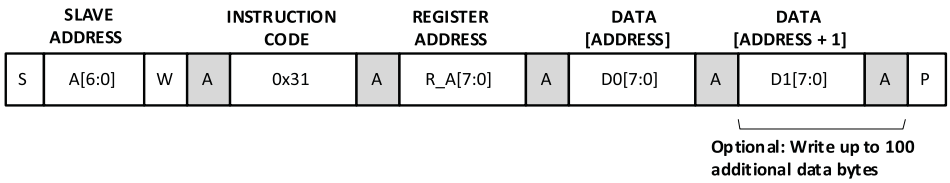

Figure 9.13. WRITE_CFG__REG_wMASK - I²C Instruction Format

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Using the WRITE_CFG_REG_wMASK Instruction Format

The WRITE_CFG_REG_wMASK instruction is the preferred instruction for updating a single programmable device parameter. As an example, the following I²C write transaction can be used to update only the VMON4_A threshold. The example will update the A_TRIP_FINE to a value of hex 0x0A (binary 001010) See Table 9.12 for more details.

1. Start the bus transaction.
2. Transmit the device address (7 bits) along with a low write bit.
3. Transmit the 0x32 instruction code (WRITE_CFG_REG_wMASK.)
4. Transmit the 0x1F address byte (VMON4_CFG0 register as defined by Table 9.12).
5. Transmit 0x3F as the MASK0 byte (only A_TRIP_FINE[1:0] will be modified, B_TRIP_SELECT[5:0] will maintain its current configuration).
6. Transmit the data to be written to the two highest bits of VMON4_CFG0 (0x80 corresponds to A_TRIP_FINE[1:0] = 10).
7. Transmit 0xF0 as the next mask byte (address will auto-increment to 0x20, the VMON4_CFG1 register). Only A_TRIP_FINE[5:2] will be modified. Other VMON4_CFG1 parameters will be unchanged.
8. Transmit the data to be written to the four lowest bits of VMON4_CFG1 (0x02 corresponds to A_TRIP_FINE[5:2] = 0010).
9. Stop the bus transaction.
10. Start an additional bus transaction using the LOAD_CFG_REG instruction (see Figure 9.15).

The configuration register settings can also be readout over I²C. This is accomplished using the READ_CFG_REG instruction and the READ_ALL_CFG_REG instruction. The READ_CFG_REG is a two-step transaction operation, as shown in Figure 9.14. In the first step, a write transaction is performed with the 0x33 instruction, and an 8-bit address code corresponding to a specific register address (defined in the ASC Configuration Registers section). In the second step, a read transaction is used to read the register contents. The register address will auto-increment to support reading multiple registers in a single transaction. This means a single transaction can support reading the entire configuration address map (102 bytes), if the starting address of 0x00 is used. A stop condition will complete the read transaction, this can be issued after any number of bytes have been read.

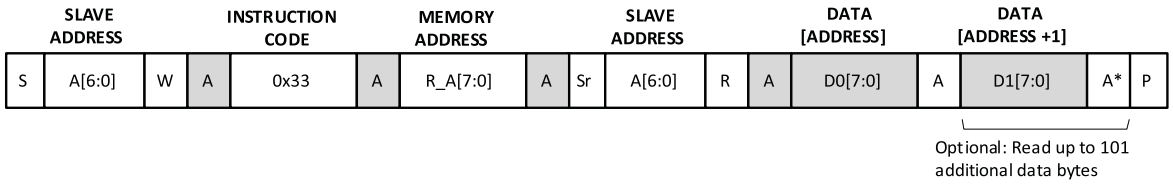

Figure 9.14. READ_CFG_REG - I²C Instruction Format

The READ_ALL_CFG instruction works in a similar way to the READ_CFG_REG. The difference is that the READ_ALL_CFG instruction always starts at register address 0x00. Multiple data bytes can be read out in a single transaction, with the register address auto-incrementing after each byte is read. The entire configuration register memory space can be read out with a single transaction (102 data bytes). A stop condition will complete the read transaction, this can be issued after any number of bytes have been read. The format for the READ_ALL_CFG_REG instruction is shown in Figure 9.15.

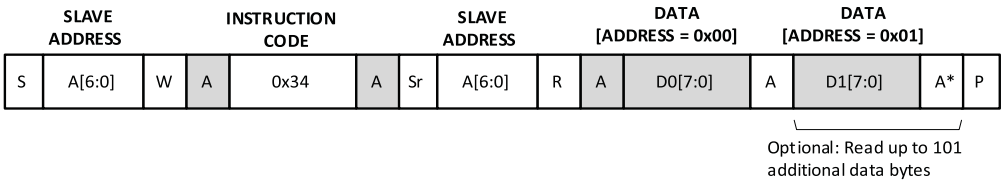

Figure 9.15. READ_ALL_CFG_REG - I²C Instruction Format

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The LOAD_CFG_REG instruction is used to load the data from the I²C master shadow registers to the slave shadow registers. All the slave shadow registers are loaded at once when the instruction is received. The LOAD_CFG_REG instruction should be used after WRITE_CFG_REG and WRITE_CFG_REG_wMask updates to the I²C configuration registers are completed. This instruction is useful for updating multiple parameters which affect the operation of a single circuit (such as a VMON or IMON), as these parameters are often spread across multiple configuration addresses. Note that certain configuration registers (such as temperature monitor or trim profiles) do not support this instruction. These master-only shadow registers are updated immediately by a WRITE_CFG_REG instruction, they do not require a LOAD_CFG_REG instruction. The format for the LOAD_CFG_REG instruction is shown in Figure 9.16.

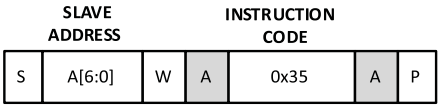

Figure 9.16. LOAD_CFG_REG - I²C Instruction Format

9.4. ASC Configuration Registers

The ASC Configuration registers are grouped below by function and shown in the following tables:

- Table 9.6, Trim Configuration Register Summary
- Table 9.12, Voltage Monitor Configuration Register Summary
- Table 9.21, Current Monitor Configuration Register Summary
- Table 9.27, Temperature Monitor Configuration Register Summary
- Table 9.35, High Voltage Output Configuration Register Summary
- Table 9.44, Output Control Block Configuration Register Summary
- Table 9.49, GPIO Input Configuration Register Summary
- Table 9.51, Write Protect and User Tag Configuration Register
- Table 9.54, UES Memory Summary
- Table 9.55, Reserved Configuration Addresses

The configuration register address space is 8-bits (0x00-0xFF). The registers contain the configuration information for all the analog blocks in the ASC. These registers are automatically populated with their configuration information at power on reset, either from the ASC EEPROM memory or external memory through Dual Boot algorithm. These registers should not be confused with the “Measurement and Control” registers described in a later section. The measurement and control registers are used to read voltage, current, and temperature measurements and are accessed with a different set of instructions.

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Table 9.6. Trim Configuration Register Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x00	Trim1_P1_Lo*	Trim1_P1_Set [7:0]								Master-Only (Immediate Update)
0x01	Trim1_Trim2_P1_Hi	Trim1_P1_Set[11:8]				Trim2_P1_Set[11:8]				
0x02	Trim2_P1_Lo*	Trim2_P1_Set [7:0]								
0x03	Trim3_P1_Lo*	Trim3_P1_Set [7:0]								
0x04	Trim3_Trim4_P1_Hi	Trim3_P1_Set [11:8]				Trim4_P1_Set [11:8]				
0x05	Trim4_P1_Lo*	Trim4_P1_Set [7:0]								
0x06	Trim1_P2_Lo*	Trim1_P2_Set [7:0]								
0x07	Trim1_Trim2_P2_Hi	Trim1_P2_Set[11:8]				Trim2_P2_Set[11:8]				
0x08	Trim2_P1_Lo*	Trim2_P2_Set [7:0]								
0x09	Trim3_P2_Lo*	Trim3_P2_Set [7:0]								
0x0A	Trim3_Trim4_P2_Hi	Trim3_P2_Set [11:8]				Trim4_P2_Set [11:8]				
0x0B	Trim4_P1_Lo*	Trim4_P1_Set [7:0]								
0x0C	Trim1_P0_Lo*	Trim1_P0_Set [7:0]								Master/Slave (LOAD_CFG_REG supported)
0x0D	Trim1_P0_Hi_Cfg	POL	BYP	ATT	x	Trim1_P0_Set[11:8]				
0x0E	Trim2_P0_Lo*	Trim2_P0_Set [7:0]								
0x0F	Trim2_P0_Hi_Cfg	POL	BYP	ATT	x	Trim2_P0_Set[11:8]				
0x10	Trim3_P0_Lo*	Trim3_P0_Set [7:0]								
0x11	Trim3_P0_Hi_Cfg	POL	BYP	ATT	x	Trim3_P0_Set[11:8]				
0x12	Trim4_P0_Lo*	Trim4_P0_Set [7:0]								
0x13	Trim4_P0_Hi_Cfg	POL	BYP	ATT	x	Trim4_P0_Set[11:8]				
0x14	Trim_CLT_Rate	—		—		—		RATE[1:0]		
0x15	Trim_DAC_BPZ	D4_BPZ[1:0]		D3_BPZ[1:0]		D2_BPZ[1:0]		D1_BPZ[1:0]		

***Note:** When the bypass bit (manual mode) is set, the lower 8-bits of the profile set-point are the profile DAC registers shown in Figure 6.22.

Closed Loop Trim Configuration Registers

The ASC configuration memory specifies the operation of the closed loop trim circuitry, described in the Controlling Power Supply Output Voltage by Trim and Margin Block section. Each of the configurable parameters, shown in Table 9.6, are described in the following section.

Trimx_Py_Set [11:0] (Trim1_P0 … Trim4_P2) – Trim Channel Profile Setpoints 0, 1 and 2

The Trim profile setpoints are configured as 12 bit numbers, where each bit corresponds to 2 mV. The equation below (which is a reversal of the calculation equation found in the ADC section) describes how to calculate the trim target.

TRIM_SETPOINT_CODE (12_bits, converted to binary) = ROUND (Target Voltage / 2 mV)

Each of the 4 Trim channels supports three separate programmable setpoints, as shown in Table 9.6. The P1 and P2 setpoints for each channel do not support the LOAD_CFG_REG instruction and are updated immediately after being written by I^2C instructions. It is not recommended to update these registers during operation. Updating the trim setpoint is best accomplished using the Closed Loop Trim Register Access instructions.

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POL – Polarity

The Polarity setting for each trim channel determines the closed loop trim behavior of trim voltage control versus output voltage feedback, as shown in Figure 6.23. The polarity settings are described in Table 9.7.

Table 9.7. POL Setting vs Closed Loop Trim Polarity

POL	Closed Loop Trim Polarity
0	Positive
1	Negative

BYP – Bypass

The Bypass setting for each trim channel determines whether the trim output voltage is controlled by the closed loop trim circuitry or by the stored profile DAC codes, as shown in Figure 6.22. When the Trim-DAC circuitry is in bypass mode, the lower 8-bits of the profile set-point are the profile DAC registers shown in Figure 6.22. The bypass settings are described in Table 9.8.

Table 9.8. BYP Setting vs Trim Voltage Source

BYP	Trim Voltage Source
0	Closed Loop Trim Logic (Trim Calculator)
1	Profile DAC Code (Manual)

ATT – Attenuator Enable

The Attenuator Enable setting for each trim channel determines whether the monitored DC-DC output voltage needs to be attenuated before ADC measurement, as shown in Figure 6.6. DC-DC output voltages above 2 V need to be attenuated. The attenuator settings are described in Table 9.9.

Table 9.9. ATT Setting vs Attenuation Value

ATT	Attenuation Value
0	÷ 1 (no attenuation)
1	÷ 3

RATE[1:0] – Closed Loop Trim Update Rate

The Closed Loop Trim update rate is a common setting for all four trim channels. The available settings are shown in Table 9.10.

Table 9.10. RATE[1:0] Setting vs Closed Loop Trim Update Rate

RATE[1:0]	Update Rate
00	860 µs
01	1.72 ms
10	13.8 ms
11	27.6 ms

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Dx_BPZ (DAC1_BPZ … DAC4_BPZ) – DAC Bi-Polar Zero Output Voltage

The DAC Bi-Polar Zero Output Voltage for each channel determines the Trim outputs Bi-Polar Zero voltage as shown in Figure 6.24. There are four available settings shown in Table 9.11.

Table 9.11. Dx_BPZ[1:0] Setting vs DAC Bi-Polar Zero Output Voltage

Dx_BPZ[1:0]	DAC BPZ Voltage
00	0.6 V
01	0.8 V
10	1.0 V
11	1.25 V

Voltage Monitor Configuration Registers

Table 9.12. Voltage Monitor Configuration Register Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x16	VMON1_Config0	V1_ATF[1:0]		V1_BTF[5:0]						Master/Slave (LOAD_CFG_REG supported)
0x17	VMON1_Config1	1	1	GBP	WM	V1_ATF[5:2]				
0x18	VMON1_Config2	V1_ATC[3:0]				V1_BTC[3:0]				
0x19	VMON2_Config0	V2_ATF[1:0]		V2_BTF[5:0]						
0x1A	VMON2_Config1	1	1	GBP	WM	V2_ATF[5:2]				
0x1B	VMON2_Config2	V2_ATC[3:0]				V2_BTC[3:0]				
0x1C	VMON3_Config0	V3_ATF[1:0]		V3_BTF[5:0]						
0x1D	VMON3_Config1	1	1	GBP	WM	V3_ATF[5:2]				
0x1E	VMON3_Config2	V3_ATC[3:0]				V3_BTC[3:0]				
0x1F	VMON4_Config0	V4_ATF[1:0]		V4_BTF[5:0]						
0x20	VMON4_Config1	1	1	GBP	WM	V4_ATF[5:2]				
0x21	VMON4_Config2	V4_ATC[3:0]				V4_BTC[3:0]				
0x22	VMON5_Config0	V5_ATF[1:0]		V5_BTF[5:0]						
0x23	VMON5_Config1	1	1	GBP	WM	V5_ATF[5:2]				
0x24	VMON5_Config2	V5_ATC[3:0]				V5_BTC[3:0]				
0x25	VMON6_Config0	V6_ATF[1:0]		V6_BTF[5:0]						
0x26	VMON6_Config1	1	1	GBP	WM	V6_ATF[5:2]				
0x27	VMON6_Config2	V6_ATC[3:0]				V6_BTC[3:0]				
0x28	VMON7_Config0	V7_ATF[1:0]		V7_BTF[5:0]						
0x29	VMON7_Config1	1	1	GBP	WM	V7_ATF[5:2]				
0x2A	VMON7_Config2	V7_ATC[3:0]				V7_BTC[3:0]				
0x2B	VMON8_Config0	V8_ATF[1:0]		V8_BTF[5:0]						
0x2C	VMON8_Config1	1	1	GBP	WM	V8_ATF[5:2]				
0x2D	VMON8_Config2	V8_ATC[3:0]				V8_BTC[3:0]				
0x2E	VMON9_Config0	V9_ATF[1:0]		V9_BTF[5:0]						
0x2F	VMON9_Config1	1	1	GBP	WM	V9_ATF[5:2]				
0x30	VMON9_Config2	V9_ATC[3:0]				V9_BTC[3:0]				
0x31	HVMON_Config0	HV_ATF[1:0]		HV_BTF[5:0]						
0x32	HVMON_Config1	1	1	GBP	WM	HV_ATF[5:2]				
0x33	HVMON_Config2	HV_ATC[3:0]				HV_BTC[3:0]				

The ASC configuration memory specifies the operation of the voltage monitor (VMON), described in the Voltage Monitor Inputs section. The voltage monitor (VMON1-VMON9 and HVMON) trip points, glitch filter setting, and window mode are configurable over I^2C. The configuration registers are summarized in Table 9.12.

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Vx_ATF[5:0], Vx_ATC[3:0], Vx_BTF[5:0], Vx_BTC[3:0] (V1_ATF … V9_BTC) – Voltage Monitor Fine and Coarse, A and B Trip Points

Each voltage monitor includes programmable trip points A and B, corresponding to the two comparators for each voltage monitor input pin. The A and B trip points of the Differential Voltage Monitors (VMON1 - VMON4) are defined based on the fine and coarse settings shown in Table 9.14 (for over-voltage monitoring) and Table 9.15 (for under-voltage monitoring). The A and B trip points of the Single-Ended Voltage Monitors (VMON5-VMON9) are defined based on the fine and coarse settings shown in Table 9.16 (for over-voltage monitoring) and Table 9.17 (for under-voltage monitoring). Fine and Coarse settings outside of the table range are prohibited. There is no programmable setting for over or under voltage. Based on the type of voltage monitoring, choose the applicable table. For more details on over and under voltage monitoring, see the Programmable Over-Voltage and Under-Voltage Thresholds discussion in the Voltage Monitor Inputs section. Setting the trip point to the Low-Voltage sense row (Fine Range 0x21) disables hysteresis for that voltage monitor input for both under and over voltage detection.

Table 9.13. Trip Point for Over-Voltage Detection (Differential VMON1-VMON4)

Fine Range Setting	Coarse Range Setting											
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB
0x00	0.795	0.947	1.127	1.341	1.589	1.897	2.259	2.677	3.172	3.779	4.848	5.775
0x01	0.790	0.942	1.121	1.334	1.581	1.887	2.247	2.663	3.156	3.759	4.822	5.744
0x02	0.786	0.937	1.115	1.327	1.572	1.876	2.235	2.648	3.139	3.739	4.797	5.713
0x03	0.782	0.931	1.109	1.320	1.564	1.866	2.223	2.634	3.122	3.719	4.771	5.683
0x04	0.778	0.926	1.103	1.313	1.555	1.856	2.211	2.620	3.105	3.699	4.746	5.652
0x05	0.773	0.921	1.097	1.306	1.547	1.846	2.199	2.605	3.088	3.679	4.720	5.621
0x06	0.769	0.916	1.091	1.299	1.538	1.836	2.187	2.591	3.071	3.658	4.694	5.590
0x07	0.765	0.911	1.085	1.291	1.530	1.826	2.175	2.577	3.055	3.638	4.668	5.559
0x08	0.761	0.906	1.079	1.284	1.521	1.816	2.163	2.563	3.038	3.618	4.642	5.529
0x09	0.756	0.901	1.073	1.277	1.513	1.806	2.151	2.548	3.021	3.598	4.616	5.498
0x0A	0.752	0.896	1.067	1.270	1.504	1.796	2.139	2.534	3.004	3.578	4.590	5.468
0x0B	0.748	0.891	1.061	1.263	1.497	1.786	2.127	2.520	2.987	3.558	4.565	5.437
0x0C	0.744	0.886	1.055	1.256	1.488	1.775	2.115	2.505	2.970	3.537	4.539	5.406
0x0D	0.739	0.881	1.049	1.249	1.480	1.765	2.103	2.492	2.953	3.517	4.513	5.375
0x0E	0.735	0.876	1.043	1.241	1.472	1.755	2.091	2.478	2.936	3.497	4.487	5.345
0x0F	0.731	0.871	1.037	1.234	1.463	1.745	2.079	2.464	2.919	3.478	4.462	5.314
0x10	0.727	0.866	1.031	1.227	1.455	1.735	2.066	2.449	2.902	3.458	4.436	5.283
0x11	0.723	0.861	1.025	1.220	1.446	1.725	2.054	2.435	2.885	3.438	4.410	5.252
0x12	0.718	0.856	1.019	1.213	1.438	1.715	2.042	2.421	2.868	3.417	4.384	5.221
0x13	0.714	0.851	1.013	1.206	1.429	1.705	2.030	2.406	2.851	3.397	4.359	5.191
0x14	0.710	0.846	1.007	1.199	1.421	1.695	2.018	2.392	2.835	3.377	4.333	5.160
0x15	0.706	0.841	1.001	1.191	1.412	1.685	2.006	2.378	2.819	3.357	4.307	5.130
0x16	0.701	0.836	0.995	1.184	1.404	1.674	1.994	2.364	2.802	3.337	4.281	5.099
0x17	0.697	0.831	0.989	1.177	1.395	1.664	1.982	2.349	2.785	3.317	4.255	5.068
0x18	0.693	0.826	0.983	1.170	1.387	1.654	1.970	2.335	2.768	3.296	4.229	5.038
0x19	0.689	0.821	0.977	1.163	1.378	1.644	1.958	2.321	2.751	3.276	4.203	5.007
0x1A	0.684	0.816	0.971	1.156	1.370	1.634	1.946	2.307	2.734	3.256	4.178	4.976
0x1B	0.680	0.810	0.965	1.149	1.362	1.624	1.934	2.292	2.717	3.236	4.153	4.945
0x1c	0.676	0.805	0.959	1.141	1.353	1.614	1.922	2.278	2.700	3.216	4.127	4.914
0x1d	0.672	0.800	0.953	1.134	1.345	1.604	1.910	2.264	2.683	3.196	4.101	4.884
0x1e	0.668	0.795	0.947	1.127	1.336	1.594	1.898	2.249	2.666	3.176	4.075	4.853
Low-Voltage Sense												
0x21	0.075	0.089	0.106	0.126	0.150	0.178	0.212	0.252	0.300	0.356	0.457	0.545

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Table 9.14. Trip Point for Under-Voltage Detection (Differential VMON1-VMON4)

Fine Range Setting	Coarse Range Setting											
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB
0x00	0.786	0.937	1.115	1.327	1.572	1.876	2.235	2.648	3.139	3.739	4.797	5.713
0x01	0.782	0.931	1.109	1.320	1.564	1.866	2.223	2.634	3.122	3.719	4.771	5.683
0x02	0.778	0.926	1.103	1.313	1.555	1.856	2.211	2.620	3.105	3.699	4.746	5.652
0x03	0.773	0.921	1.097	1.306	1.547	1.846	2.199	2.605	3.088	3.679	4.720	5.621
0x04	0.769	0.916	1.091	1.299	1.538	1.836	2.187	2.591	3.071	3.658	4.694	5.590
0x05	0.765	0.911	1.085	1.291	1.530	1.826	2.175	2.577	3.055	3.638	4.668	5.559
0x06	0.761	0.906	1.079	1.284	1.521	1.816	2.163	2.563	3.038	3.618	4.642	5.529
0x07	0.756	0.901	1.073	1.277	1.513	1.806	2.151	2.548	3.021	3.598	4.616	5.498
0x08	0.752	0.896	1.067	1.270	1.504	1.796	2.139	2.534	3.004	3.578	4.590	5.468
0x09	0.748	0.891	1.061	1.263	1.497	1.786	2.127	2.520	2.987	3.558	4.565	5.437
0x0A	0.744	0.886	1.055	1.256	1.488	1.775	2.115	2.505	2.970	3.537	4.539	5.406
0x0B	0.739	0.881	1.049	1.249	1.480	1.765	2.103	2.492	2.953	3.517	4.513	5.375
0x0C	0.735	0.876	1.043	1.241	1.472	1.755	2.091	2.478	2.936	3.497	4.487	5.345
0x0D	0.731	0.871	1.037	1.234	1.463	1.745	2.079	2.464	2.919	3.478	4.462	5.314
0x0E	0.727	0.866	1.031	1.227	1.455	1.735	2.066	2.449	2.902	3.458	4.436	5.283
0x0F	0.723	0.861	1.025	1.220	1.446	1.725	2.054	2.435	2.885	3.438	4.410	5.252
0x10	0.718	0.856	1.019	1.213	1.438	1.715	2.042	2.421	2.868	3.417	4.384	5.221
0x11	0.714	0.851	1.013	1.206	1.429	1.705	2.030	2.406	2.851	3.397	4.359	5.191
0x12	0.710	0.846	1.007	1.199	1.421	1.695	2.018	2.392	2.835	3.377	4.333	5.160
0x13	0.706	0.841	1.001	1.191	1.412	1.685	2.006	2.378	2.819	3.357	4.307	5.130
0x14	0.701	0.836	0.995	1.184	1.404	1.674	1.994	2.364	2.802	3.337	4.281	5.099
0x15	0.697	0.831	0.989	1.177	1.395	1.664	1.982	2.349	2.785	3.317	4.255	5.068
0x16	0.693	0.826	0.983	1.170	1.387	1.654	1.970	2.335	2.768	3.296	4.229	5.038
0x17	0.689	0.821	0.977	1.163	1.378	1.644	1.958	2.321	2.751	3.276	4.203	5.007
0x18	0.684	0.816	0.971	1.156	1.370	1.634	1.946	2.307	2.734	3.256	4.178	4.976
0x19	0.680	0.810	0.965	1.149	1.362	1.624	1.934	2.292	2.717	3.236	4.153	4.945
0x1A	0.676	0.805	0.959	1.141	1.353	1.614	1.922	2.278	2.700	3.216	4.127	4.914
0x1B	0.672	0.800	0.953	1.134	1.345	1.604	1.910	2.264	2.683	3.196	4.101	4.884
0x1c	0.668	0.795	0.947	1.127	1.336	1.594	1.898	2.249	2.666	3.176	4.075	4.853
0x1d	0.663	0.790	0.941	1.120	1.328	1.584	1.886	2.235	2.649	3.156	4.049	4.822
0x1e	0.659	0.785	0.935	1.113	1.319	1.573	1.874	2.221	2.632	3.136	4.023	4.792
Low-Voltage Sense												
0x21	0.075	0.089	0.106	0.126	0.150	0.178	0.212	0.252	0.300	0.356	0.457	0.545

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Table 9.15. Trip Point for Over-Voltage Detection (Single-Ended VMON5-VMON9)

Fine Range Setting	Coarse Range Setting											
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb
0x0	0.799	0.952	1.133	1.347	1.597	1.907	2.270	2.688	3.185	3.794	4.868	5.798
0x1	0.794	0.947	1.126	1.340	1.589	1.897	2.258	2.674	3.168	3.774	4.842	5.767
0x2	0.790	0.942	1.120	1.333	1.580	1.886	2.246	2.659	3.151	3.754	4.816	5.736
0x3	0.786	0.936	1.114	1.326	1.572	1.875	2.234	2.645	3.134	3.734	4.790	5.706
0x4	0.782	0.931	1.108	1.319	1.563	1.865	2.222	2.631	3.117	3.714	4.765	5.675
0x5	0.777	0.926	1.102	1.312	1.555	1.855	2.210	2.616	3.100	3.694	4.739	5.644
0x6	0.773	0.921	1.096	1.305	1.546	1.845	2.198	2.602	3.083	3.673	4.713	5.613
0x7	0.769	0.916	1.090	1.297	1.538	1.835	2.186	2.588	3.067	3.653	4.687	5.582
0x8	0.765	0.911	1.084	1.290	1.529	1.825	2.174	2.574	3.050	3.633	4.661	5.552
0x9	0.760	0.906	1.078	1.283	1.521	1.815	2.162	2.559	3.033	3.613	4.635	5.521
0xa	0.756	0.901	1.072	1.276	1.512	1.805	2.150	2.545	3.016	3.593	4.609	5.489
0xb	0.752	0.896	1.066	1.269	1.504	1.795	2.138	2.531	2.999	3.573	4.584	5.458
0xc	0.748	0.891	1.060	1.262	1.495	1.784	2.125	2.516	2.982	3.552	4.558	5.427
0xd	0.743	0.886	1.054	1.255	1.487	1.774	2.113	2.501	2.965	3.532	4.532	5.396
0xe	0.739	0.881	1.048	1.247	1.479	1.764	2.101	2.487	2.948	3.512	4.506	5.366
0xf	0.735	0.875	1.042	1.240	1.470	1.754	2.089	2.473	2.931	3.491	4.479	5.335
0x10	0.731	0.870	1.036	1.233	1.462	1.744	2.076	2.458	2.914	3.471	4.453	5.304
0x11	0.727	0.865	1.030	1.226	1.453	1.734	2.064	2.444	2.897	3.451	4.427	5.273
0x12	0.722	0.860	1.024	1.219	1.445	1.724	2.052	2.430	2.880	3.430	4.401	5.242
0x13	0.718	0.855	1.018	1.212	1.436	1.714	2.040	2.415	2.863	3.410	4.376	5.212
0x14	0.714	0.850	1.012	1.205	1.428	1.704	2.028	2.401	2.847	3.390	4.350	5.181
0x15	0.710	0.845	1.006	1.197	1.419	1.694	2.016	2.387	2.830	3.370	4.324	5.150
0x16	0.705	0.840	1.000	1.190	1.411	1.683	2.004	2.373	2.813	3.350	4.298	5.119
0x17	0.701	0.835	0.994	1.183	1.402	1.673	1.992	2.358	2.796	3.330	4.272	5.088
0x18	0.697	0.830	0.988	1.176	1.394	1.663	1.980	2.344	2.779	3.309	4.246	5.058
0x19	0.693	0.825	0.982	1.169	1.385	1.653	1.968	2.330	2.762	3.289	4.220	5.027
0x1a	0.688	0.820	0.976	1.162	1.376	1.643	1.956	2.316	2.745	3.269	4.195	4.996
0x1b	0.684	0.814	0.970	1.155	1.368	1.633	1.944	2.301	2.728	3.249	4.169	4.965
0x1c	0.680	0.809	0.964	1.147	1.359	1.622	1.932	2.287	2.711	3.229	4.143	4.934
0x1d	0.676	0.804	0.958	1.140	1.351	1.612	1.920	2.273	2.694	3.209	4.117	4.904
0x1e	0.672	0.799	0.952	1.133	1.342	1.602	1.908	2.258	2.677	3.189	4.091	4.873
Low-Voltage Sense												
0x21	0.080	0.093	0.110	0.132	0.155	0.186	0.220	0.262	0.310	0.370	0.475	0.565

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Table 9.16. Trip Point for Under-Voltage Detection (Single-Ended VMON5-VMON9)

Fine Range Setting	Coarse Range Setting											
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb
0x0	0.790	0.942	1.120	1.333	1.580	1.886	2.246	2.659	3.151	3.754	4.816	5.736
0x1	0.786	0.936	1.114	1.326	1.572	1.875	2.234	2.645	3.134	3.734	4.790	5.706
0x2	0.782	0.931	1.108	1.319	1.563	1.865	2.222	2.631	3.117	3.714	4.765	5.675
0x3	0.777	0.926	1.102	1.312	1.555	1.855	2.210	2.616	3.100	3.694	4.739	5.644
0x4	0.773	0.921	1.096	1.305	1.546	1.845	2.198	2.602	3.083	3.673	4.713	5.613
0x5	0.769	0.916	1.090	1.297	1.538	1.835	2.186	2.588	3.067	3.653	4.687	5.582
0x6	0.765	0.911	1.084	1.290	1.529	1.825	2.174	2.574	3.050	3.633	4.661	5.552
0x7	0.760	0.906	1.078	1.283	1.521	1.815	2.162	2.559	3.033	3.613	4.635	5.521
0x8	0.756	0.901	1.072	1.276	1.512	1.805	2.150	2.545	3.016	3.593	4.609	5.489
0x9	0.752	0.896	1.066	1.269	1.504	1.795	2.138	2.531	2.999	3.573	4.584	5.458
0xa	0.748	0.891	1.060	1.262	1.495	1.784	2.125	2.516	2.982	3.552	4.558	5.427
0xb	0.743	0.886	1.054	1.255	1.487	1.774	2.113	2.501	2.965	3.532	4.532	5.396
0xc	0.739	0.881	1.048	1.247	1.479	1.764	2.101	2.487	2.948	3.512	4.506	5.366
0xd	0.735	0.875	1.042	1.240	1.470	1.754	2.089	2.473	2.931	3.491	4.479	5.335
0xe	0.731	0.870	1.036	1.233	1.462	1.744	2.076	2.458	2.914	3.471	4.453	5.304
0xf	0.727	0.865	1.030	1.226	1.453	1.734	2.064	2.444	2.897	3.451	4.427	5.273
0x10	0.722	0.860	1.024	1.219	1.445	1.724	2.052	2.430	2.880	3.430	4.401	5.242
0x11	0.718	0.855	1.018	1.212	1.436	1.714	2.040	2.415	2.863	3.410	4.376	5.212
0x12	0.714	0.850	1.012	1.205	1.428	1.704	2.028	2.401	2.847	3.390	4.350	5.181
0x13	0.710	0.845	1.006	1.197	1.419	1.694	2.016	2.387	2.830	3.370	4.324	5.150
0x14	0.705	0.840	1.000	1.190	1.411	1.683	2.004	2.373	2.813	3.350	4.298	5.119
0x15	0.701	0.835	0.994	1.183	1.402	1.673	1.992	2.358	2.796	3.330	4.272	5.088
0x16	0.697	0.830	0.988	1.176	1.394	1.663	1.980	2.344	2.779	3.309	4.246	5.058
0x17	0.693	0.825	0.982	1.169	1.385	1.653	1.968	2.330	2.762	3.289	4.220	5.027
0x18	0.688	0.820	0.976	1.162	1.376	1.643	1.956	2.316	2.745	3.269	4.195	4.996
0x19	0.684	0.814	0.970	1.155	1.368	1.633	1.944	2.301	2.728	3.249	4.169	4.965
0x1a	0.680	0.809	0.964	1.147	1.359	1.622	1.932	2.287	2.711	3.229	4.143	4.934
0x1b	0.676	0.804	0.958	1.140	1.351	1.612	1.920	2.273	2.694	3.209	4.117	4.904
0x1c	0.672	0.799	0.952	1.133	1.342	1.602	1.908	2.258	2.677	3.189	4.091	4.873
0x1d	0.667	0.794	0.946	1.125	1.334	1.592	1.896	2.244	2.660	3.168	4.065	4.842
0x1e	0.663	0.789	0.940	1.118	1.325	1.581	1.884	2.230	2.643	3.148	4.039	4.811
Low-Voltage Sense												
0x21	0.080	0.093	0.110	0.132	0.155	0.186	0.220	0.262	0.310	0.370	0.475	0.565

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GBP – Glitch Filter Bypass

Each of the voltage monitors include a glitch filter at each of the trip point comparator outputs as shown in Figure 6.2. This glitch filter can be bypassed dependent on the GBP setting shown in Table 9.17.

Table 9.17. GBP Setting vs Glitch Bypass Behavior

GBP	Glitch Filter Setting
0	Glitch Filter On
1	Glitch Filter Bypassed

WM – Window Mode

Each of the voltage monitors include a selectable window mode, as described in Table 5.2. The window mode setting is shown in Table 9.18.

Table 9.18. WM Setting vs Window Mode Value

WM	Window Mode
0	Off
1	On

HV_ATF[5:0], HV_ATC[3:0], HV_BTF[5:0], HV_BTC[3:0] – High Voltage Monitor Fine and Coarse, A and B Trip Points

The High Voltage Monitor (HVMON) is configured in a similar fashion to the low voltage monitor inputs. The key difference from the low voltage monitor inputs is the trip point table. The HVMON range is up to 13.2 V, as reflected in Table 9.19 (Over-Voltage Trip Points) and Table 9.20 (Under-Voltage Trip Points). Setting the trip point to the Low-Voltage sense row (Fine Range 0x21) disables hysteresis for that voltage monitor input for both under and over voltage detection.

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Table 9.19. Trip-Point for Over-Voltage Detection (HVMON)

Fine Range Setting	Coarse Range Setting											
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb
0x0	2.269	2.694	3.193	3.748	4.421	5.207	6.137	7.160	8.382	9.819	11.455	13.218
0x1	2.257	2.680	3.176	3.729	4.398	5.179	6.104	7.121	8.337	9.767	11.394	13.147
0x2	2.245	2.666	3.159	3.709	4.374	5.152	6.071	7.083	8.293	9.714	11.333	13.077
0x3	2.233	2.651	3.142	3.689	4.351	5.124	6.039	7.045	8.248	9.662	11.272	13.007
0x4	2.221	2.637	3.125	3.669	4.327	5.096	6.006	7.007	8.204	9.610	11.212	12.936
0x5	2.208	2.623	3.108	3.649	4.304	5.068	5.974	6.969	8.159	9.558	11.151	12.866
0x6	2.196	2.608	3.091	3.629	4.280	5.041	5.941	6.931	8.114	9.505	11.090	12.796
0x7	2.184	2.594	3.074	3.609	4.257	5.013	5.908	6.893	8.070	9.453	11.029	12.725
0x8	2.172	2.580	3.057	3.589	4.233	4.985	5.876	6.855	8.025	9.401	10.968	12.655
0x9	2.160	2.565	3.040	3.569	4.210	4.958	5.843	6.817	7.981	9.349	10.907	12.585
0xa	2.148	2.551	3.023	3.549	4.186	4.930	5.810	6.779	7.936	9.297	10.846	12.515
0xb	2.136	2.537	3.006	3.529	4.163	4.902	5.778	6.741	7.891	9.244	10.785	12.444
0xc	2.124	2.522	2.989	3.509	4.139	4.875	5.745	6.703	7.847	9.192	10.724	12.374
0xd	2.112	2.508	2.972	3.489	4.116	4.847	5.712	6.664	7.802	9.140	10.663	12.304
0xe	2.100	2.494	2.955	3.469	4.092	4.819	5.680	6.626	7.758	9.088	10.602	12.233
0xf	2.088	2.479	2.938	3.449	4.069	4.791	5.647	6.588	7.713	9.035	10.541	12.163
0x10	2.076	2.465	2.921	3.429	4.045	4.764	5.614	6.550	7.669	8.983	10.480	12.093
0x11	2.064	2.451	2.904	3.410	4.021	4.736	5.582	6.512	7.624	8.931	10.419	12.022
0x12	2.052	2.436	2.887	3.390	3.998	4.708	5.549	6.474	7.579	8.879	10.358	11.952
0x13	2.040	2.422	2.870	3.370	3.974	4.681	5.517	6.436	7.535	8.826	10.298	11.882
0x14	2.027	2.408	2.853	3.350	3.951	4.653	5.484	6.398	7.490	8.774	10.237	11.811
0x15	2.015	2.393	2.836	3.330	3.927	4.625	5.451	6.360	7.446	8.722	10.176	11.741
0x16	2.003	2.379	2.819	3.310	3.904	4.598	5.419	6.322	7.401	8.670	10.115	11.671
0x17	1.991	2.365	2.803	3.290	3.880	4.570	5.386	6.284	7.356	8.618	10.054	11.601
0x18	1.979	2.350	2.786	3.270	3.857	4.542	5.353	6.246	7.312	8.565	9.993	11.530
0x19	1.967	2.336	2.769	3.250	3.833	4.515	5.321	6.207	7.267	8.513	9.932	11.460
0x1a	1.955	2.322	2.752	3.230	3.810	4.487	5.288	6.169	7.223	8.461	9.871	11.390
0x1b	1.943	2.307	2.735	3.210	3.786	4.459	5.255	6.131	7.178	8.409	9.810	11.319
0x1c	1.931	2.293	2.718	3.190	3.763	4.431	5.223	6.093	7.134	8.356	9.749	11.249
0x1d	1.919	2.279	2.701	3.170	3.739	4.404	5.190	6.055	7.089	8.304	9.688	11.179
0x1e	1.907	2.264	2.684	3.150	3.716	4.376	5.157	6.017	7.044	8.252	9.627	11.108
Low-Voltage Sense												
0x21	0.220	0.260	0.308	0.361	0.425	0.504	0.593	0.692	0.810	0.949	1.108	1.28

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Table 9.20. Trip-Point for Under-Voltage Detection (HVMON)

Fine Range Setting	Coarse Range Setting											
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xa	0xb
0x0	2.245	2.666	3.159	3.709	4.374	5.152	6.071	7.083	8.293	9.714	11.333	13.077
0x1	2.233	2.651	3.142	3.689	4.351	5.124	6.039	7.045	8.248	9.662	11.272	13.007
0x2	2.221	2.637	3.125	3.669	4.327	5.096	6.006	7.007	8.204	9.610	11.212	12.936
0x3	2.208	2.623	3.108	3.649	4.304	5.068	5.974	6.969	8.159	9.558	11.151	12.866
0x4	2.196	2.608	3.091	3.629	4.280	5.041	5.941	6.931	8.114	9.505	11.090	12.796
0x5	2.184	2.594	3.074	3.609	4.257	5.013	5.908	6.893	8.070	9.453	11.029	12.725
0x6	2.172	2.580	3.057	3.589	4.233	4.985	5.876	6.855	8.025	9.401	10.968	12.655
0x7	2.160	2.565	3.040	3.569	4.210	4.958	5.843	6.817	7.981	9.349	10.907	12.585
0x8	2.148	2.551	3.023	3.549	4.186	4.930	5.810	6.779	7.936	9.297	10.846	12.515
0x9	2.136	2.537	3.006	3.529	4.163	4.902	5.778	6.741	7.891	9.244	10.785	12.444
0xa	2.124	2.522	2.989	3.509	4.139	4.875	5.745	6.703	7.847	9.192	10.724	12.374
0xb	2.112	2.508	2.972	3.489	4.116	4.847	5.712	6.664	7.802	9.140	10.663	12.304
0xc	2.100	2.494	2.955	3.469	4.092	4.819	5.680	6.626	7.758	9.088	10.602	12.233
0xd	2.088	2.479	2.938	3.449	4.069	4.791	5.647	6.588	7.713	9.035	10.541	12.163
0xe	2.076	2.465	2.921	3.429	4.045	4.764	5.614	6.550	7.669	8.983	10.480	12.093
0xf	2.064	2.451	2.904	3.410	4.021	4.736	5.582	6.512	7.624	8.931	10.419	12.022
0x10	2.052	2.436	2.887	3.390	3.998	4.708	5.549	6.474	7.579	8.879	10.358	11.952
0x11	2.040	2.422	2.870	3.370	3.974	4.681	5.517	6.436	7.535	8.826	10.298	11.882
0x12	2.027	2.408	2.853	3.350	3.951	4.653	5.484	6.398	7.490	8.774	10.237	11.811
0x13	2.015	2.393	2.836	3.330	3.927	4.625	5.451	6.360	7.446	8.722	10.176	11.741
0x14	2.003	2.379	2.819	3.310	3.904	4.598	5.419	6.322	7.401	8.670	10.115	11.671
0x15	1.991	2.365	2.803	3.290	3.880	4.570	5.386	6.284	7.356	8.618	10.054	11.601
0x16	1.979	2.350	2.786	3.270	3.857	4.542	5.353	6.246	7.312	8.565	9.993	11.530
0x17	1.967	2.336	2.769	3.250	3.833	4.515	5.321	6.207	7.267	8.513	9.932	11.460
0x18	1.955	2.322	2.752	3.230	3.810	4.487	5.288	6.169	7.223	8.461	9.871	11.390
0x19	1.943	2.307	2.735	3.210	3.786	4.459	5.255	6.131	7.178	8.409	9.810	11.319
0x1a	1.931	2.293	2.718	3.190	3.763	4.431	5.223	6.093	7.134	8.356	9.749	11.249
0x1b	1.919	2.279	2.701	3.170	3.739	4.404	5.190	6.055	7.089	8.304	9.688	11.179
0x1c	1.907	2.264	2.684	3.150	3.716	4.376	5.157	6.017	7.044	8.252	9.627	11.108
0x1d	1.895	2.250	2.667	3.130	3.692	4.348	5.125	5.979	7.000	8.200	9.566	11.038
0x1e	1.883	2.236	2.650	3.110	3.669	4.321	5.092	5.941	6.955	8.148	9.505	10.968
Low-Voltage Sense												
0x21	0.220	0.260	0.308	0.361	0.425	0.504	0.593	0.692	0.810	0.949	1.108	1.28

Current Monitor Configuration Registers

The ASC configuration memory defines the operation of the current monitor (IMON/HIMON) circuitry, described in the Theory of Operation section. The low and high voltage current monitor trip points, glitch filter setting, and window mode are configurable over I^2C. The IMON1 (low voltage) also includes a Low-Side bit, which configures the low-side sense setting on IMON1.

The configuration registers are described in Table 9.21.

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Table 9.21. Current Monitor Configuration Register Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x34	IMON1_Config0	FAST_TH[2:0]			GBP	WM	LSS	0	0	Master/Slave (LOAD_CFG_REG supported)
0x35	IMON1_Config1	A_TH[1:0]		B_TH[1:0]		A_GAIN[1:0]		B_GAIN[1:0]		
0x36	HIMON_Config0	FAST_TH[2:0]			GBP	WM	X	0	0	
0x37	HIMON_Config1	A_TH[1:0]		B_TH[1:0]		A_GAIN[1:0]		B_GAIN[1:0]		

A_TH[1:0], B_TH[1:0], A_GAIN[1:0], B_GAIN[1:0] – Threshold and Gain Setting for A and B Comparators

The A and B current monitor trip points are defined by the combination of the threshold and gain settings. Table 9.22 shows the trip point settings for both the IMON1 and HIMON current monitor circuits.

Table 9.22. Current Monitor Trip Points (Differential Voltage)

A_TH/B_TH[1:0]	GAIN[1:0]			
	00 (GAIN = 100V/V)	01 (GAIN = 50V/V)	10 (GAIN = 25V/V)	11 (GAIN = 10V/V)
00	8 mV	15.5 mV	30.5 mV	75 mV
01	10.5 mV	20.5 mV	40.5 mV	100 mV
10	14.5 mV	28.5 mV	56.5 mV	140 mV
11	20 mV	39 mV	77 mV	190 mV

GBP – Glitch Filter Bypass

Each of the current monitors include a glitch filter at each of the trip point comparator outputs as shown in Figure 6.4. This glitch filter can be bypassed dependent on the GBP setting shown in Table 9.23.

Table 9.23. GBP Setting vs Glitch Bypass Behavior

GBP	Glitch Filter Setting
0	Glitch Filter On
1	Glitch Filter Bypassed

WM – Window Mode

Each of the current monitors include a selectable window mode, as described in Table 6.5. The window mode setting is shown in Table 9.24.

Table 9.24. WM Setting vs Window Mode Value

WM	Window Mode
0	Off
1	On

LSS – Low Side Sense Mode

The IMON1 current monitor includes a low side sense mode, as shown in Figure 6.4. The low side sense settings are shown in Table 9.25.

Table 9.25. LSS Setting vs Low Side Sensing Mode

LSS	Low Side Sense Mode
0	Disabled
1	Enabled

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FAST_TH[2:0] - Fast Comparator Threshold

The fast trip point for both IMON1 and HIMON is set according to the FAST_TH[2:0] code. Table 9.26 shows the fast trip point settings vs the FAST_THRESH code for both IMON1 and HIMON current monitor circuits.

Table 9.26. Fast Current Monitor Trip Points (Differential Voltage)

FAST_TH[2:0]	Trip Point
000	50 mV
001	100 mV
010	150 mV
011	200 mV
100	250 mV
101	300 mV
110	400 mV
111	500 mV

Temperature Monitor Configuration Registers

Table 9.27. Temperature Monitor Configuration Register Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x38	TMON1_Config0	Ideality_Code[13:6]								Master-Only (TMON circuit resets after each time configuration update)
0x39	TMON1_Config1	Ideality_Code[5:0]						Cfg[1:0]		
0x3A	TMON1_Config2	Off[8:1]								
0x3B	TMON1_Config3	Th_A[8:2]							Off[0]	
0x3C	TMON1_Config4	Th_B[8:3]						Th_A[1:0]		
0x3D	TMON1_Config5	X	X	FLT	AVE[1:0]		Th_B[2:0]			
0x3E	TMON1_Config6	FilterA[3:0]				FilterB[3:0]				
0x3F	TMON1_Config7	X	HystA[6:0]							
0x40	TMON1_Config8	X	HystB[6:0]							
0x41	TMON2_Config0	Ideality_Code[13:6]								
0x42	TMON2_Config1	Ideality_Code[5:0]						Cfg[1:0]		
0x43	TMON2_Config2	Off[8:1]								
0x44	TMON2_Config3	Th_A[8:2]							Off[0]	
0x45	TMON2_Config4	Th_B[8:3]						Th_A[1:0]		
0x46	TMON2_Config5	X	X	FLT	AVE[1:0]		Th_B[2:0]			
0x47	TMON2_Config6	FilterA[3:0]				FilterB[3:0]				
0x48	TMON2_Config7	X	HystA[6:0]							
0x49	TMON2_Config8	X	HystB[6:0]							
0x4A	TMONint_Config0	Ideality_Code[13:6]								
0x4B	TMONint_Config1	Ideality_Code[5:0]						Cfg[1:0]		
0x4C	TMONint_Config2	Off[8:1]								
0x4D	TMONint_Config3	Th_A[8:2]							Off[0]	
0x4E	TMONint_Config4	Th_B[8:3]						Th_A[1:0]		
0x4F	TMONint_Config5	X	X	FLT	AVE[1:0]		Th_B[2:0]			
0x50	TMONint_Config6	FilterA[3:0]				FilterB[3:0]				
0x51	TMONint_Config7	X	HystA[6:0]							
0x52	TMONint_Config8	X	HystB[6:0]							

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The temperature monitor circuit (TMON) configuration registers can be updated over I^2C. The definition and function of these parameters is described in the Temperature Monitor Inputs section. There are nine configuration registers per TMON channel (TMON1, TMON2, and TMON_int). The diode ideality factor, transducer configuration, temperature offset, A and B monitor characteristics (threshold, filter, hysteresis) and measurement averaging and fault behavior are all configurable according to the format in Table 9.27. A description of how to calculate each parameter follows the register format. The temperature monitor circuit will reset each time a configuration parameter is updated over I^2C.

Ideality_Code[13:0] - Ideality Factor Setting

The Temperature Monitor inputs support a programmable ideality factor (emission coefficient) for interfacing to different remote transistor diodes. The programmable ideality factor is calculated based on a 14-bit code. The allowed range of ideality factors is 0.9 to 2.0, values outside this range are not allowed. Calculating the code for a given ideality factor is done using the following calculation:

Ideality_Code (14 bits, converted to binary) = ROUND (4572 / ideality factor)

Table 9.28 shows some common ideality factors and their corresponding codes.

Table 9.28. Ideality Factor vs Ideality_Code Setting

Ideality_Code[13:0]	Ideality Factor
0x08EE	2.0000

0x11B6	1.0083
0x11B7	1.0082
0x11B8	1.0079

0x11C8	1.0044
0x11C9	1.0042
0x11CA	1.0039

0x11D9	1.0007
0x11DA	1.0004
0x11DB	1.0002
0x11DC	1.0000
0x11DD	0.9998
0x11DE	0.9996
0x11DF	0.9993

0x13D8	0.9000

Cfg[1:0] - Temperature Monitor Diode Configuration

As described in the Temperature Monitor Inputs section, the TMON supports different transistor-based diode configurations for connection to the ASC Temperature Monitors. The two bit value Tran_cfg[1:0], corresponds to the supported configurations as shown in Table 9.29.

Table 9.29. Temperature Monitor Diode Configuration Settings

Cfg[1:0]	Diode Configuration
00	TMON disabled
01	Beta Compensated PNP
10	Differential PNP or NPN
11	Single-Ended (Not recommended)

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Off[8:0] - Temperature Monitor Offset

The TMON supports a 9-bit programmable temperature offset, which is applied to the temperature measurement for both readout and the A and B monitor comparison. The programmable offset range is from –64°C to 63.75°C, with a resolution of 0.25°C. The offset is stored as a 2's complement number, with the 9th bit as the signed bit. Table 9.30 shows the settings associated with several different offset temperatures.

Table 9.30. Temperature Monitor Offset Settings

Off[8:0]	Offset Temperature oC
0x0FF	63.75
0x0FE	63.50

0x002	0.50
0x001	0.25
0x000	0.00
0x1FF	–0.25
0x1FE	–0.50

0x101	–63.75
0x100	–64.00

Th_A[8:0], Th_B[8:0] - Comparator Thresholds for A and B alarms

The TMON includes two individually programmable comparators, TMONA and TMONB. The 9-bit alarm thresholds range for each of these monitors is –64°C to 155°C, with a resolution of 1°C. The thresholds are stored as 2's complement numbers, with the 9th bit as the signed bit. Values above 155°C or below –64°C are not valid threshold settings. Table 9.31 shows the settings associated with several different threshold temperatures.

Table 9.31. Temperature Monitor Thresholds Settings

Th_A / Th_B[8:0]	Threshold Temperature °C
0x09B	155
0x09A	154

0x002	2
0x001	1
0x000	0
0x1FF	–1
0x1FE	–2

0x1C1	–63
0x1C0	–64

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FLT - Fault Reading Setting

The TMON circuit includes open and short fault detection circuitry for the remote diode channels. (The fault detect is not applicable for the internal temperature monitor, TMON_INT). The 1-bit programmable fault setting determines the measurement readout behavior of both open and short faults. The readout values compared to the fault setting is shown in Table 9.32.

Table 9.32. Temperature Monitor Fault Setting

FLT	Short Condition Reading		Open Condition Reading	
	°C	Code	°C	Code
0	–255.75	0x401	255.75	0x3FF
1	255.75	0x3FF	–255.75	0x401

AVE[1:0] - Average Filter Coefficient

The TMON temperature measurement can be read out over I^2C. The TMON circuit includes a programmable exponential averaging filter that is applied before the measurement readout. The Average parameter can be programmed to three different averaging coefficients, as shown in Table 9.33.

Table 9.33. Temperature Monitor Measurement Average Settings

AVE[1:0]	Coefficient
00	1
01	8
10	16
11	N/A

FilterA[3:0] / FilterB[3:0] - Monitor Alarm Filter

The TMONA and TMONB comparators each support programmable monitor alarm filters. The depth of the alarm filter can be programmed between 1 and 16, based on the Filter[3:0] setting. The relationship between the filter code and the filter depth is given by the following equation:

DEPTH = Filter[3:0] + 1

HystA[6:0] / HystB[6:0] - Temperature Monitor Hysteresis

The TMONA and TMONB comparators each support programmable temperature hysteresis. The 7-bit hysteresis range for each of these monitors is –64°C to 63°C, with a resolution of 1°C. (The negative hysteresis range should be applied to over-temperature comparisons, while the positive hysteresis should be applied to under-temperature comparisons) The hysteresis settings are stored as 2's complement numbers, with the 7th bit as the signed bit. Table 9.34 shows the settings associated with several different hysteresis temperatures.

Table 9.34. Temperature Monitor Hysteresis Settings

Hyst[6:0]	Temperature Hysteresis °C
0x3F	63
0x3E	62

0x02	2
0x01	1
0x00	0
0x7F	–1
0x7E	–2

0x41	–63
0x40	–64

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High Voltage Output (HVOUT) Configuration Registers

Table 9.35. High Voltage Output Configuration Register Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x53	HVOUT1_Config0	OCB	1	I_SRC[1:0]		I_SNK[1:0]		VPP[1:0]		Master/Slave (LOAD_CFG_REG supported)
0x54	HVOUT1_Config1	SW	FR	OD	X	DUTY[3:0]				
0x55	HVOUT2_Config0	OCB	1	I_SRC[1:0]		I_SNK[1:0]		VPP[1:0]		
0x56	HVOUT2_Config1	SW	FR	OD	X	DUTY[3:0]				
0x57	HVOUT3_Config0	OCB	1	I_SRC[1:0]		I_SNK[1:0]		VPP[1:0]		
0x58	HVOUT3_Config1	SW	FR	OD	X	DUTY[3:0]				
0x59	HVOUT4_Config0	OCB	1	I_SRC[1:0]		I_SNK[1:0]		VPP[1:0]		
0x5A	HVOUT4_Config1	SW	FR	OD	X	DUTY[3:0]				

The High Voltage Output pins (HVOUT) configuration registers can be updated over I^2C. The definition and function of these parameters is described in the High Voltage Outputs section. There are two configuration registers per HVOUT (HVOUT1, HVOUT2, HVOUT3, HVOUT4). The open-drain/charge pump setting, charge pump voltage, source and sink current, switched/static mode, and switched mode duty cycle and frequency are all configurable according to the format in Table 9.35. A description of how to calculate each parameter follows the register format.

OCB - Output Control Block Source

The OCB parameter is used to select the control signal source for the HVOUT pin from either the Output Control Block (OCB) or the ASC-I/F. Table 9.36 shows the available settings.

Table 9.36. OCB Setting vs HVOUT Source Selection

OCB	HVOUT Source
0	ASC-I/F Signal
1	OCB

I_SRC[1:0] - HVOUT Source Current

The I_SRC[1:0] setting is used to choose between the four supported source currents for the HVOUT in charge pump mode. The available choices are shown in Table 9.37.

Table 9.37. HVOUT Source Current Settings

I_SRC[1:0]	Output Source Current
00	12.5 uA
01	25 uA
10	50 uA
11	100 uA

I_SNK[1:0] - HVOUT Sink Current

The I_SNK[1:0] setting is used to choose between the four supported sink currents for the HVOUT in charge pump mode. The available choices are shown in Table 9.38.

Table 9.38. HVOUT Sink Current Settings

I_SNK[1:0]	Output Sink Current
00	100 uA
01	250 uA
10	500 uA
11	3000 uA

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VPP[1:0] - Charge Pump Output Voltage Settings

The VPP[1:0] setting is used to choose between the four programmable output voltage levels for the HVOUT in charge pump mode. The available choices are shown in Table 9.39.

Table 9.39. HVOUT Output Voltage Settings

VPP[1:0]	Output Voltage
00	6 V
01	8 V
10	10 V
11	12 V

SW - Switched Output Setting

The SW parameter configures the HVOUT pin for either static drive mode (on or off) or switched mode (either switched at the programmed frequency and duty, or off). Table 9.40 shows the available settings.

Table 9.40. SW Setting vs HVOUT Mode

SW	HVOUT Mode
0	On/Off
1	Switched

FR - Output Frequency Select (Switched Mode Only)

The FR parameter configures the output frequency of the HVOUT when the device is placed in switched mode. Table 9.41 shows the available settings.

Table 9.41. FR Setting vs HVOUT Output Frequency (Switched Mode only)

FR	Frequency
0	31.25 kHz
1	15.625 kHz

OD - Open Drain Output Mode Setting

The OD parameter is used to configure the output mode of the device. Table 9.42 shows the available settings.

Table 9.42. OD Setting vs HVOUT Output Mode

OD	HVOUT Output Mode
0	Charge-Pump Mode
1	Open-Drain Mode

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DUTY[3:0] - Duty Cycle Selection (Switched Mode Only)

The Duty_Cycle[3:0] setting is used to choose between the sixteen programmable duty cycles for the HVOUT in switched mode. The available choices are shown in Table 9.43.

Table 9.43. HVOUT Switched Output Duty Cycle Settings

Duty_Cycle[3:0]	Duty Cycle%
0x0	6.25%
0x1	12.5%
0x2	18.75%
0x3	25%
0x4	31.25%
0x5	37.55%
0x6	43.75%
0x7	50.00%
0x8	56.25%
0x9	62.50%
0xA	68.75%
0xB	75.00%
0xC	81.25%
0xD	87.50%
0xE	93.75%
0xF	50.00%

Output Control Block Configuration Registers

Table 9.44. Output Control Block Configuration Register Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x5B	OCB_Config0	GPIO3_src[3:0]				GPIO2_src[2:0]				Master/Slave (LOAD_CFG_REG supported)
0x5C	OCB_Config1	HVOUT2_src[3:0]				HVOUT1_src[3:0]				
0x5D	OCB_Config2	HVOUT4_src[3:0]				HVOUT3_src[3:0]				
0x5E	OCB_Config3	X	X	IM_HCM_CTRL[2:0]		HI_HCM_CTRL[2:0]				
0x5F	OCB_Config4	X	X	V6_HCM_CTRL[2:0]		V5_HCM_CTRL[2:0]				
0x60	OCB_Config5	X	HI_T	H4i	H3i	H2i	H1i	G3i	G2i	

The Output Control Block (OCB) configuration registers can be updated over I^2C. The definition and function of these parameters is described in the Output Control Block section. There are 6 total configuration registers for the output control block. The settings in the six registers define the operation of the output control block output muxes, the hysteretic control muxes, and the dynamic threshold management. Registers 0x5B-0x5D define the out control muxes according to the format shown in Table 9.44.

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OUTPUT_src[3:0] - Output Channel Source Signal Select

The output control source for each of the six OCB based outputs is defined by the four bit _src[3:0] code. The outputs selected by each code are shown in Table 9.45.

Table 9.45. Output Control Block – Output Source Signals

OUTPUT_src[3:0]	Source Signal
0x0	ASC-I/F
0x1	I^2C
0x2	GPIO5
0x3	GPIO6
0x4	GPIO7
0x5	GPIO8
0x6	GPIO9
0x7	GPIO10
0x8	HIMON_F
0x9	IMON1_F
0xA	VMON_4A
0xB	VMON_9A
0xC	HIMON_HCM
0xD	IMON1_HCM
0xE	VMON5_HCM
0xF	VMON6_HCM

HCM_CTRL - Hysteretic Mux Configuration for IMON1, HIMON, VMON6 and VMON5

Registers 0x5E and 0x5F define the control signal inputs for the 4 Hysteretic Control Muxes (HCM). The register format is shown in Table 9.44. The control signals selected by the _HCM_CTRL[2:0] code are shown in Table 9.46.

Table 9.46. Output Control Block – Hysteretic Control Mux Settings

HCM_CTRL[2:0]	ASC-I/F Source Signal
000	GPIO2
001	GPIO3
010	HVOUT1
011	HVOUT2
100	HVOUT3
101	HVOUT4
110	N/A
111	N/A

H4i / H3i / H2i / H1i/ G3i / G2i - Output Invert Control

The OCB outputs can be inverted with respect to their control signals. As shown in Table 9.44, the register 0x60 defines the programmable invert option for each of the outputs.The invert setting parameter is shown in Table 9.47.

Table 9.47. H4i … G2i Setting vs OCB Output Behavior

H4i / H3i / H2i / H1i/ G3i / G2i	OCB Output
0	Normal
1	Inverted

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HI_T - HIMON_A Threshold Source

Register 0x60 also defines the programmable threshold source select for the HIMON circuit. The threshold source can be selected as either the configuration memory or the ASC-I/F, as shown in Table 9.48.

Table 9.48. HI_T Setting vs HIMONA Threshold Source

HI_T	HIMONA Threshold Source
0	Configuration Memory
1	ASC-I/F

GPIO Input Configuration Registers

Table 9.49. GPIO Input Configuration Register Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x62	GPIO_Config0	X	G4in	X	G3in	X	G2in	X	G1in	Master/Slave (LOAD_CFG_REG supported)
0x63	GPIO_Config1	X	G8in	X	G7in	X	G6in	X	G5in	
0x64	GPIO_Config2	X	X	X	X	X	G10in	X	G9in	

The GPIO pins can be configured as input or output. The GPIO configuration registers can be updated over I^2C. The registers at addresses 0x62, 0x63, and 0x64 include single configuration bit for each of the GPIO. When the device is configured as an input, the GPIO pin is put into a Hi-Z state and a weak pulldown is enabled. The input setting is described in Table 9.50. The input status can still be read at the pin, regardless of the Gxin setting. The format for registers 0x62, 0x63, and 0x64 is shown in Table 9.49.

Table 9.50. Gxin Setting vs GPIO Input Setting

Gxin	GPIO Setting
0	Output – Weak Pulldown Disabled
1	Input – Weak Pulldown Enabled

Write Protect and User Tag Configuration Register

Table 9.51. Write Protect and User Tag Configuration Register

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x66	WRITEPROTECT_USERTAG	X	X	X	X	X	UT_EN	WP[1:0]		Read Only

The Write Protect and User Tag modes are defined by the bit settings in register 0x66 (shown in Table 9.51). This register cannot be written using the configuration register commands. It can only be overwritten in the EEPROM memory.

UT_EN - User Tag Enable

The UT_EN bit configures the device for either User Tag Memory mode or Fault Logging mode, as described in Table 9.52. The User Tag and Fault Log features are described in more details in the Fault Logging and User Tag Memory section.

Table 9.52. UT_EN vs Fault Log / User Tag Mode

UT_EN	Fault Log / User Tag Mode
0	Fault Log Enabled / User Tag Disabled
1	User Tag Enabled / Fault Log Disabled

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WP[1:0] - Write Protect Setting

The write protect setting bits are defined in Table 9.53. The write protect function is described in detail later in the I2C Write Protection section.

Table 9.53. Write Protect Settings

WP[1:0]	Write Protect Settings
00	No protection
01	No protection
10	Protection based on GPIO1 level
11	I^2C write disabled

User Electronic Signature (UES) Registers

Table 9.54. UES Memory Summary

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x70	UES0	UES[7:0]								EEPROM Read Only
0x71	UES1	UES[15:8]								
0x72	UES2	UES[23:16]								
0x73	UES3	UES[31:24]								
0x74	UES4	UES[39:32]								
0x75	UES5	UES[47:40]								
0x76	UES6	UES[55:48]								
0x77	UES7	UES[63:56]								

The ASC includes a User Electronic Signature feature in the EEPROM memory of the device. This consists of 64 bits that can be configured by the user to store unique data such as ID codes, revision numbers, or inventory control data. The UES code can only be written and readout using the EEPROM memory access commands. The UES storage format is shown in Table 9.54.

Reserved Configuration Addresses

The configuration memory map includes several reserved addresses, which should not be read or written to. The reserved addresses are shown in Table 9.55 below.

Table 9.55. Reserved Configuration Addresses

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reconfiguration Details
0x61	RESERVED	RESERVED								Do not read or write to these addresses
0x65	RESERVED	RESERVED								
0x67-0x6F	RESERVED	RESERVED								
0x78-0xFF	RESERVED	RESERVED								

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9.5. Closed Loop Trim Register Access

The Trim and Margin block provides for I²C access to write closed loop trim profile 0 target values for each Trim channel on-chip as shown in Table 9.56. The 12 bits of each closed trim setpoint register can be updated and read back atomically using the dedicated instructions below.

Table 9.56. Closed Loop Trim Access Instructions

Instruction Code	Instruction Name	Read/Write	Description
0x41	TRIM1_CLT_P0_SET	R/W	Update and readback of TRIM1 closed loop trim profile 0 setpoint register[11:0]
0x42	TRIM2_CLT_P0_SET	R/W	Update and readback of TRIM2 closed loop trim profile 0 setpoint register[11:0]
0x43	TRIM3_CLT_P0_SET	R/W	Update and readback of TRIM3 closed loop trim profile 0 setpoint register[11:0]
0x44	TRIM4_CLT_P0_SET	R/W	Update and readback of TRIM4 closed loop trim profile 0 setpoint register[11:0]

The format for these instructions is shown in Figure 9.17 below.

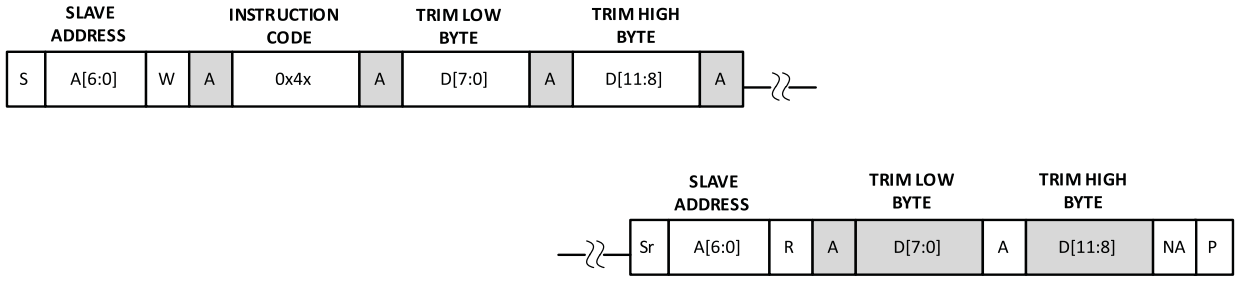

Figure 9.17. TRIMx_CLT_P0_SET - I²C Instruction Format

The new trim target is latched in the hardware at the completion of the write sequence, the LOAD_CFG_REG command is not needed.

In Closed Loop Trim mode, the Trim targets are 12-bit positive numbers where each bit corresponds to 2 mV. See Closed Loop Trim Configuration Registers for details on calculating the trim target voltage. In Manual mode, the DAC targets are 8-bit signed numbers (low byte) where each bit corresponds to 2.5 mV (see the Table 5.16) and the high byte is ignored. Both bytes have to be written for the new value to take effect.

9.6. Measurement and Control Register Access

The measurement and control section of the ASC is accessed via two different I²C instructions. The WRITE_MEAS_CTRL instruction is used to write the measurement selection for voltage and current measurements, the selection for reading the monitor status, and the control selection for the output control block. The READ_MEAS_CTRL is used to read the measurement result selected by the WRITE_MEAS_CTRL instruction. The instructions are used to access the register set shown in Table 9.57. The instructions use the register addresses in Table 9.57 and follow the format shown in Figure 9.18 for WRITE_MEAS_CTRL and Figure 9.19 for READ_MEAS_CTRL.

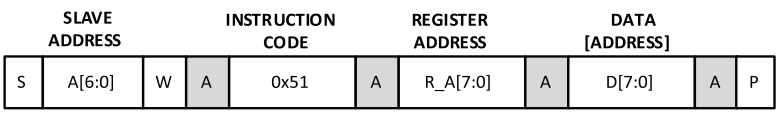

Figure 9.18. WRITE_MEAS_CTRL - I²C Instruction Format

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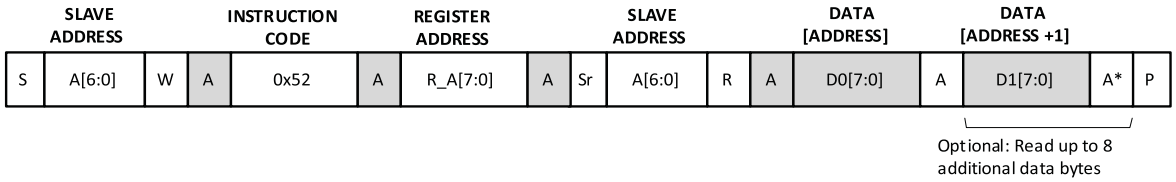

Figure 9.19. READ_MEAS_CTRL - I²C Instruction Format

The measurement and control register address map is shown in Table 9.57. These register are used to read voltage and current measurements from the ADC, read temperature measurements from the TMON circuit, and control I/Os configured for I²C control. These registers should not be confused with the configuration registers, which are accessed with a different set of instructions and comprise a completely separate 8-bit address space.

Table 9.57. Measurement and Control Register Overview

Register Address	Register Name	Read/Write	Description	Value after POR
0x00	adc_mux	R/W	ADC Attenuator and SEL[4:0]	0000 0000
0x01	adc_value_low	R	ADC Result [4:0] and status	0000 0000
0x02	adc_value_high	R	ADC Result [12:5]	0000 0000
0x03	imon_average_ctrl	R/W	Average Control [3:0]	0000 0000
0x04	imon_average_select	R/W	IMON MUX[1:0]	0000 0000
0x05	imon_average_result_low	R	IMON moving average [7:0]	0000 0000
0x06	imon_average_result_high	R	IMON moving average [9:8]	0000 0000
0x07	monitor_select	R/W	Monitor Select[3:0]	0000 0000
0x08	monitor_ record	R	Monitor Record[7:0]	0000 0000
0x09-0x6F	RESERVED	—	—	—
0x70	output_control_block	R/W	HVOUT1-4 and GPIO2-3 control	0000 0000
0x71-0x7F	RESERVED	—	—	—
0x80	tmon_meas_1_high	R	TMON_1 Measurement [15:8]	1110 0000
0x81	tmon_meas_1_low	R	TMON_1 Measurement [7:5]	0000 0000
0x82	tmon_meas_2_high	R	TMON_2 Measurement [15:8]	1110 0000
0x83	tmon_meas_2_low	R	TMON_2 Measurement [7:5]	0000 0000
0x84	tmon_meas_int_high	R	TMON_int Measurement [15:8]	1110 0000
0x85	tmon_meas_int_low1	R	TMON_int Measurement [7:5]	0000 0000
0x86	tmon_stat_a1	R	TMON_A Status [2:0]	0000 0000
0x87	tmon_stat_b	R	TMON_B Status [2:0]	0000 0000
0x88-0xFF	RESERVED	—	—	—

Note: Any READ_MEAS_CTRL command which reads addresses 0x85 or 0x86 as the final data byte must be followed by an additional READ_MEAS_CTRL command of a different address (such as 0x70) before issuing any other I²C read command.

The registers shown in Figure 9.20 are provided for interfacing to the ADC.

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0x00 – ADC_MUX (Read/Write)

ATTEN	0	0	SEL4	SEL3	SEL2	SEL1	SEL0
b7	b6	b5	b4	b3	b2	b1	b0

0x01 – ADC_VALUE_LOW (Read)

D4	D3	D2	D1	D0	PENDING	ACTIVE	DONE
b7	b6	b5	b4	b3	b2	b1	b0

0x02 – ADC_VALUE_HIGH (Read)

D12	D11	D10	D9	D8	D7	D6	D5
b7	b6	b5	b4	b3	b2	b1	b0

Figure 9.20. ADC Registers

To perform an A/D conversion, one must set the input attenuator and channel selector. For VMON input voltage conversions, two input ranges may be set using the attenuator, 0-2.048 V and 0-5.9 V. For conversion of the HVMON input voltage, the available attenuator ranges are 0-8.192 V and 0-13.2 V. These settings are shown in Table 9.58.

Table 9.58. ADC Input Attenuator Control

ATTEN(ADC_MUX.b7)	VMON1-VMON9		HVMON	
	Resolution	Full Scale Range	Resolution	Full Scale Range
0	2 mV	0-2.048 V	8 mV	0-8.192
1	6 mV	0-5.9 V	16 mV	0-13.2

The input selector may be set to monitor any of the VMON input voltages, the VCCA supply voltage, or the IMON differential voltages. The selectable input channels are shown in Table 9.59. Do not read or write to ADC_MUX selections not shown in the table.

Table 9.59. ADC Input Selection

SEL[4:0] (ADC_MUX Selection)	Input Channel
0x00	VMON1
0x01	VMON2
0x02	VMON3
0x03	VMON4
0x04	VMON5
0x05	VMON6
0x06	VMON7
0x07	VMON8
0x08	VMON9
0x09	HVMON
0x0C	VCCA
0x0F	VDC (Attenuated by 8)
0x10	IMON1
0x13	HIMON

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Writing a value to the ADC_MUX register using the WRITE_MEAS_CTRL instruction to set the input attenuator and selector will automatically initiate a conversion. The PENDING bit will be set to 1 when a conversion is requested but not yet active. The ACTIVE bit will be set to 1 when the requested conversion is the active conversion. When the conversion is in process, the DONE bit (ADC_VALUE_LOW.b0) will be reset to 0. When the conversion is complete, this bit will be set to 1. When the result from the ADC is copied to the I²C registers, the ACTIVE bit is reset and the result may be read out by performing two I²C read operations using the READ_MEAS_CTRL instruction; one for ADC_VALUE_LOW, and one for ADC_VALUE_HIGH. It is recommended that the I²C master load a second conversion instruction only after the completion of the current conversion operation (Waiting for the DONE bit to be set to 1). The example flow below shows the necessary instructions to complete an ADC read.

Voltage Monitor ADC Readout Over I²C

1. Perform an I²C Write Operation with Instruction 0x51, Register Address 0x00, and the ADC Channel and Attenuator setting from Table 9.59. This will initiate the ADC conversion.
2. Perform an I²C Read Operation with Instruction 0x52, Register Address 0x01 to check that the DONE bit is set and the ACTIVE bit is reset. Repeat if Register 0x01, bit 0 is not set to 1 and bit 1 is not reset to 0. Read ADC Data[4:0] for ADC low byte.
3. Perform an I²C Read Operation with Instruction 0x052, Register Address 0x02 to read ADC Data [12:5] for ADC high byte

The Current Monitor (IMON1 and HIMON) averaging measurement hardware is also accessed through the I²C interface. The IMON1/HIMON averaging is controlled by dedicated hardware and is managed separately from the single conversion IMON1/HIMON access through the ADC registers. The IMON1/HIMON averaging registers are shown in Figure 9.21.

0x03 – IMON_AVG_CTRL (Read/Write)

0	**0**	**HIMON AVG_EN**	**0**	**0**	**IMON1 AVG_EN**	**SMPL_** INT_1	**SMPL_** INT_0
b7	b6	b5	b4	b3	b2	b1	b0

0x04 – IMON_AVG_SELECT (Read/Write)

0	**0**	**0**	**0**	**0**	**0**	**SEL1**	**SEL0**
b7	b6	b5	b4	b3	b2	b1	b0

0x05 – IMON_AVG_RESULT_LOW (Read)

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
b7	b6	b5	b4	b3	b2	b1	b0

0x06 – IMON_AVG_RESULT_HIGH (Read)

0	**0**	**0**	**0**	**0**	**0**	**D9**	**D8**
b7	b6	b5	b4	b3	b2	b1	b0

Figure 9.21. IMON Average Control Registers

To perform a moving average read, first enable the moving average for the given channel in the IMON_AVG_CTRL register. When the averaging is enabled the averaging hardware will begin to compute a binary exponential weighted moving average, as shown below:

$$\text{CurrentAve[x]}\frac{\text{CurrentMeas[x]}}{8} + \text{CurrentAve[x} - 1\text{]}\ \text{x}\ \frac{7}{8}$$

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The IMON_AVG_CTRL register is used to enable the averaging operation and set the sample period of the averaging. The HIMON and IMON1 averaging operations are enabled independently by setting the HIMON_AVG_EN and IMON1_AVG_EN respectively. Setting these bits to 1 enables the 1/8 moving averaging for that input channel. The SMPL_PER[1:0] is used to select the sampling interval from the values shown in Table 9.60.

Table 9.60. IMON Average Sample Interval Values

SMPL_INT[1:0]	Sample Interval
00	1 ms
01	2 ms
10	4 ms
11	8 ms

Once the averaging is enabled, the IMON_AVG_SELECT register is used to select between the HIMON and IMON1 average values for readout (see Table 9.61).

Table 9.61. Selected IMON Average Readout Channel

SELECT[1:0]	Channel
00	IMON1
01	Not Used
10	Not Used
11	HIMON

After writing to the IMON_AVG_SELECT register, the selected channels 10-bit moving average can be read out of the IMON_AVG_RESULT_LOW and IMON_AVG_RESULT_HIGH registers. The value in the IMON_AVG_SELECT register will remain active until overwritten by another I^2C instruction (or power on reset). The updated 10-bit moving average for the previously selected channel can be readout from the result registers without re-writing the SELECT register.

Current Monitor Moving Average Readout Over I^2C

1. Perform an I^2C Write Operation with Instruction 0x51, Register Address 0x03, and enable the HIMON averaging and configure the sampling period. This will enable the HIMON averaging. See Table 9.60 and Table 9.61.
2. Moving average results are available immediately based on limited samples. Waiting additional sample periods ensures that the averaging filter has time to settle. After enough time has elapsed, perform an I^2C Write Operation with Instruction 0x51, Register Address 0x04, and select the HIMON channel for readout.
3. Perform an I^2C Read Operation with Instruction 0x052, Register Address 0x05 to read IMON_AVG_RESULT_LOW[7:0] for HIMON low byte.
4. Perform an I^2C Read Operation with Instruction 0x052, Register Address 0x06 to read IMON_AVG_RESULT_HIGH[9:8] for HIMON high byte.

The status of the voltage, current, and temperature monitor alarms, as well as the GPIO input status, can be read out over I^2C. Access to the alarm signals is controlled by the MONITOR_SELECT register. To read out the alarm or GPIO status over I^2C, write the applicable selection to the MONITOR_SELECT register as shown in Table 9.63. After writing the corresponding value to the MONITOR_SELECT, you can read the monitor signal status from the MONITOR_RECORD register. These registers are shown in Figure 9.22.

The MONITOR_SELECT also includes a valid bit. This bit is set to 1 once the MONITOR_RECORD register includes the monitor signals selected in the MONITOR_SELECT register. The monitor signals are refreshed much faster than the I^2C access time, so normally the valid bit will read as 1. If the device is in safe state and ASC-I/F communication has not started properly, the valid bit will read as 0. The MONITOR_RECORD register will continue to include the latest status of the specified alarm signals, as specified in the MONITOR_SELECT register.

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0x07 – MONITOR_SELECT (Read/Write)

Valid	0	0	0	SEL3	SEL2	SEL1	SEL0
b7	b6	b5	b4	b3	b2	b1	b0

0x08 – MONITOR_RECORD (Read)

D7	D6	D5	D4	D3	D2	D1	D0
b7	b6	b5	b4	b3	b2	b1	b0

Figure 9.22. Monitor Signal Access Registers

The register map of the monitor data is shown in Table 9.62 below. An example for how to read out selected data is shown after the table.

Table 9.62. MONITOR_RECORD Byte Selection

MONITOR_ SELECT [3:0]	MONITOR_RECORD[7:0]							
	D7	D6	D5	D4	D3	D2	D1	D0
0x0	0	Fault_Log_Full	Fault_Log_Busy	0	0	1	X	1
0x1	AGOOD	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4
0x2	GPIO3	GPIO2	GPIO1	HVOUT4	HVOUT3	HVOUT2	HVOUT1	HIMON_b
0x3	HIMON_a	IMON1_b	IMON1_a	HVMON _b	HVMON _a	VMON9_ b	VMON9_ a	VMON8_ b
0x4	VMON8_ a	VMON7_b	VMON7_a	VMON6 _b	VMON6 _a	VMON5_ b	VMON5_ a	VMON4_ b
0x5	VMON4_ a	VMON3_b	VMON3_a	VMON2 _b	VMON2 _a	VMON1_ b	VMON1_ a	TMON2_b
0x6	TMON2_a	TMON1_b	TMON1_a	TMONin t_b	TMONin t_a	1	0	1

Monitor Record Readout Over I²C

1. Perform an I²C Write Operation with Instruction 0x51, Register Address 0x07, and write the selected data byte for readout. This will populate the MONITOR_RECORD register, Address 0x08, with the latest sampled data of the chosen bits as described in Table 9.62.
2. Perform an I²C Read Operation with Instruction 0x52, Register Address 0x08 to read the selected Monitor Record.

The output signals for HVOUT1-4 and GPIO2-3 can be controlled via I²C instruction, dependent on their Output Control Block configuration. The OUTPUT_CONTROL_BLOCK register (shown in Figure 9.23) is used to set the I²C control input to the Output Control Block. Outputs which are not configured for I²C control will ignore the setting in the I²C register. See the Output Control Block section for more details.

0x70 – OUTPUT_CONTROL_BLOCK (Read/Write)

0	0	HVOUT4	HVOUT3	HVOUT2	HVOUT1	GPIO3	GPIO2
b7	b6	b5	b4	b3	b2	b1	b0

Figure 9.23. Output Control Block Register

Several registers are provided for accessing the temperature monitor measurements. Each temperature monitor channel has a TMON_MEAS_CHx_LO and TMON_MEAS_CHx_HI register for accessing the 11-bit temperature reading (shown in Figure 9.24). Provided the temperature monitor is enabled, these registers are updated automatically with the latest temperature reading. The update rate of the temperature reading is dependent on the number of channels enabled (see the Temperature Monitors section for more details).

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The temperature measurement hardware will latch its latest reading after the TMON_MEAS_CHx_HIGH byte is read over I²C. This will ensure that the corresponding TMON_MEAS_CHx_LOW byte is from the same measurement as the TMON_MEAS_CHx_HIGH byte. The HIGH byte should be read first in the I²C transaction, followed by the LOW byte. This will ensure the two bytes are from the same measurement reading.

0x80 – TMON_MEAS_CH1_HIGH (Read)

D10	D9	D8	D7	D6	D5	D4	D3
b7	b6	b5	b4	b3	b2	b1	b0

0x81 – TMON_MEAS_CH1_LOW (Read)

D2	D1	D0	0	0	0	0	0
b7	b6	b5	b4	b3	b2	b1	b0

0x82 – TMON_MEAS_CH2_HIGH (Read)

D10	D9	D8	D7	D6	D5	D4	D3
b7	b6	b5	b4	b3	b2	b1	b0

0x83 – TMON_MEAS_CH2_LOW (Read)

D2	D1	D0	0	0	0	0	0
b7	b6	b5	b4	b3	b2	b1	b0

0x84 – TMON_MEAS_INT_HIGH (Read)

D10	D9	D8	D7	D6	D5	D4	D3
b7	b6	b5	b4	b3	b2	b1	b0

0x85 – TMON_MEAS_INT_LOW (Read)

D2	D1	D0	0	0	0	0	0
b7	b6	b5	b4	b3	b2	b1	b0

Figure 9.24. Temperature Monitor Measurement Registers

The format of the 11-bit temperature measurement is shown in Figure 9.24 along with some example values. The measurement format is 2-complement, with bit D10 used as the sign bit. The measurement resolution is 0.25°C per bit. **Temperature monitor circuits which are reset or disabled will always readout –64°C**.

Any READ_MEAS_CTRL command which reads addresses 0x85 or 0x86 as the final data byte must be followed by an additional READ_MEAS_CTRL command of a different address (such as 0x70) before issuing any other I²C read command.

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Table 9.63. Temperature Measurement Data Format

D[10:0]	Measured Temperature (°C)
0x3FF	160.00*
0x26C	155.00
0x26B	154.75

0x002	0.50
0x001	0.25
0x000	0.00
0x7FF	–0.25
0x7FE	–0.50

0x701	–63.75
0x700	–64.00*

Note: Measurements above 160°C will limit to 0x3FF. There is no lower limit, although the TMON accuracy is unguaranteed below –64°C.

The temperature monitor alarm signals are also available to be read out over I²C directly. The A comparator alarm signals for each temperature monitor can be read out from the TMON_STAT_A register while the B comparator alarm signals can be read out from the TMON_STAT_B. The register format is shown in Figure 9.25.

0x86 – TMON_STAT_A (Read)

0	0	0	0	0	TMONINT_A	TMON2_A	TMON1_A
b7	b6	b5	b4	b3	b2	b1	b0

0x87 – TMON_STAT_B (Read)

0	0	0	0	0	TMONINT_B	TMON2_B	TMON1_B
b7	b6	b5	b4	b3	b2	b1	b0

Figure 9.25. Temperature Monitor Status Registers

Any READ_MEAS_CTRL command which reads addresses 0x85 or 0x86 as the final data byte must be followed by an additional READ_MEAS_CTRL command of a different address (such as 0x70) before issuing any other I²C read command.

9.7. User Tag Memory Access

The I²C interface is used to access the User Tag memory feature of the ASC. The User Tag memory block consists of a 7 byte User Tag register, a programming hardware block, and a 16 row x 7 byte EEPROM memory. The User Tag memory block architecture is shown in Figure 9.26, along with the I²C access instructions.

The User Tag feature cannot be used when the ASC Fault Log is enabled. These features use the same memory array and only one of the two features can be enabled at a given time. The User Tag instructions shown below are only applicable for accessing the memory in User Tag mode. Access to the memory in Fault Log Mode should follow the Fault Log instructions detailed in the next section.

Table 9.64 shows the User Tag access instructions. The instructions are used to access either the User Tag register or the User Tag EEPROM memory block. Accessing the User Tag memory requires that the ASC is placed into programming mode (see the ENABLE_PROG instruction). The format for each instruction is in the section that follows.

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Table 9.64. User Tag Memory Access Instructions

Instruction Code	Instruction Name	Read/Write	Description
0x61	ERASE_USER_TAG_EEPROM	W	Erase the User Tag EEPROM array
0x62	WRITE_USER_TAG_REG	W	Write to the User Tag data register
0x63	READ_USER_TAG_REG	R	Read out the contents of the User Tag data register
0x64	PROG_USER_TAG_EEPROM	W	Program the selected row of EEPROM bits with the tag data register
0x65	READ_USER_TAG_EEPROM	R	Read out the selected row of User Tag EEPROM bits

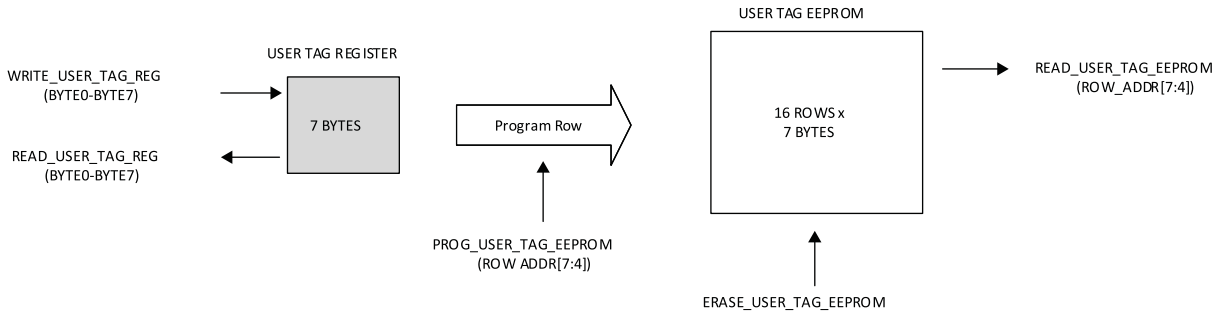

Figure 9.26. User Tag Memory Architecture with I²C Instruction Access

The ERASE_USER_TAG_EEPROM instruction is used to erase the entire User Tag EEPROM array. The User Tag can only be erased as a full block. A row must be erased prior to programming it. The instruction format for ERASE_USER_TAG_EEPROM is shown in Figure 9.27.

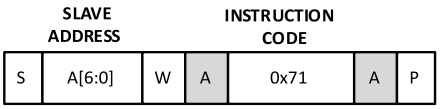

Figure 9.27. ERASE_USER_TAG_EEPROM - I²C Instruction Format

The User Tag EEPROM is programmed in a two-step process. First the data which is to be programmed is written into the User Tag register space, as shown in Figure 9.28. Up to 7 bytes (known as a data "row") can be written into the User Tag register space in a single write transaction. The WRITE_USER_TAG_REG instruction is used for writing the User Tag register space.

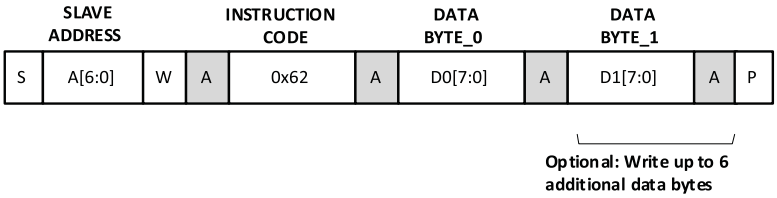

Figure 9.28. WRITE_USER_TAG_REG - I²C Instruction Format

The READ_USER_TAG_REG instruction is used to read out the User Tag register bytes as shown in Figure 9.29. Up to 7 bytes can be read out from the User Tag register space in a single read transaction. The bytes are read back in order from byte 0 to byte 6.

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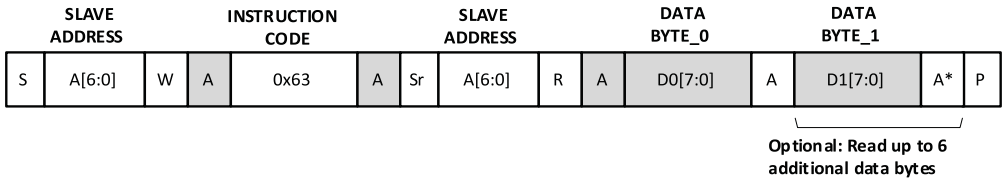
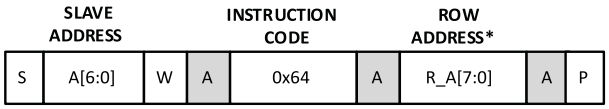


Figure 9.29. READ_USER_TAG_REG - I²C Instruction Format

The second step of the User Tag programming is writing to the EEPROM from the User Tag registers. This is accomplished using the PROGRAM_USER_TAG_EEPROM instruction. The data in the User Tag registers is copied by the programming block to the EEPROM row specified by the R_A[7:4] bits in the data byte as shown in Figure 9.30. The 4-bit code corresponds to Row 0 to Row 15 in the User Tag EEPROM memory block, as shown in the User Tag block diagram in Figure 9.26.



Note: The Row Address R_A[7:0] contains the 4-bit address code in bits [7:4]. Bits [3:0] are always zero.

Figure 9.30. PROG_USER_TAG_EEPROM - I²C Instruction Format

The READ_USER_TAG_EEPROM I²C instruction provides the mechanism to readback data stored in the User Tag memory. The READ_USER_TAG_EEPROM is a two step read transaction operation. In the first step, a write transaction is performed with the 0x65 instruction, and a 4-bit address code [7:4]. The address code corresponds to Row 0 to Row 15 as shown in the User Tag block diagram in Figure 9.26. In the second step, the row can be read out in 7 bytes, from byte 0 to byte 6, using a read transaction. The row address will auto-increment to support reading multiple rows in a single transaction. This means a single transaction can support reading the entire user tag array, if the starting address of Row 0 is used. A stop condition will complete the read transaction, this can be issued after any number of rows and bytes have been read.

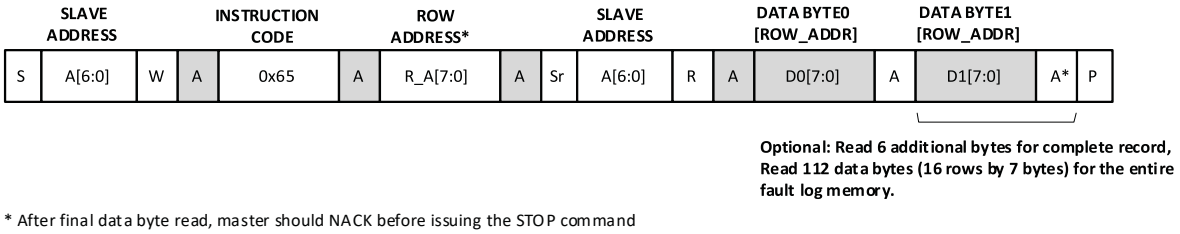


Figure 9.31. READ_USER_TAG_EEPROM - I²C Instruction Format

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User Tag Access Example

This example describes the steps necessary to program 7 Data Bytes to Row 4 of the EEPROM array:

1. Perform an I²C Write with the ENABLE_PROG instruction (0x04), with the 2-byte key code 0xE53D. This will place the chip in programming mode, a required step for User Tag access.
2. (Optional) Perform an I²C Write with the ERASE_USER_TAG_EEPROM instruction (0x61). This is only required if data has already been written to Row 4.
3. Perform an I²C Write with the WRITE_USER_TAG_REG instruction (0x62), with the 7 data bytes to be written.
4. (Optional) Perform an I²C Read with the READ_USER_TAG_REG instruction (0x63) to confirm that the 7 Data Bytes were properly written the USER_TAG_REGISTER.
5. Perform an I²C Write with the PROGRAM_USER_TAG_EEPROM instruction (0x64), with an R_A[0x40], row address 4. This copies the data from the USER_TAG_REG into Row 4 of the USER_TAG_EEPROM array.
6. (Optional) Perform an I²C Read with the READ_USER_TAG_EEPROM instruction (0x65), with an address of 0x04. You can use this operation to verify the EEPROM programming.
7. Perform an I²C Write with the ENABLE_USER instruction (0x05). This operation will place the ASC back in User Mode, in order to prevent accidental programming access.

9.8. Fault Log Memory Access

The ASC includes a fault logging block. The fault logging block consists of fault recording hardware, a volatile memory register which holds one 7 byte fault log record, a programming block, and a 16 row by 7 byte EEPROM memory for fault record storage. The fault logging block, including I²C access instructions is shown in Figure 9.32. The fault logging block is described in detail in the Fault Log section.

The ASC Fault Log cannot be used when the user tag feature is enabled. These features use the same memory array and only one of the two features can be enabled at a given time. The Fault Log instructions shown below are only applicable for accessing the memory in Fault Log mode. Access to the memory in User Tag Mode should follow the User Tag instructions detailed in the previous section.

Table 9.65 shows the Fault Log access instructions. The instructions are used to read out or erase either the fault log register or the fault log EEPROM memory block. The format for each instruction is in the section that follows.

Writing fault logs to the EEPROM memory is triggered by the ASC-I/F. Faults can be recorded in either the fault logging register or in the EEPROM (for more details see the Fault Log section). The fault log recording hardware has priority access to the fault log EEPROM memory, and needs to be disabled via the READ_FAULT_ENABLE instruction prior to accessing the fault log via I²C. The fault log recording process also takes precedence over the reconfiguration/programming of the device. If a fault log record process is active, the device will reject reconfiguration requests. You can avoid that scenario by executing the READ_FAULT_ENABLE instruction prior to starting the reconfiguration process.

The fault log instructions are summarized in Table 9.65 below, with individual instruction details in the following section.

Table 9.65. Fault Log Access Instructions

Instruction Code	Instruction Name	Read/Write	Description
0x71	ERASE_FAULT_EEPROM	W	Erase the entire fault log memory
0x73	READ_FAULT_VOLATILE_REG	R	Read the fault log volatile register contents
0x74	READ_FAULT_ENABLE	R/W	Disables the fault log recording hardware and enables the ERASE and READ instructions
0x75	READ_FAULT_RECORD_EEPROM	R	Read out the selected record of Fault Log Array EEPROM bits
0x76	READ_ALL_FAULT_EEPROM	R	Reads out all records of the Fault Log EEPROM Array

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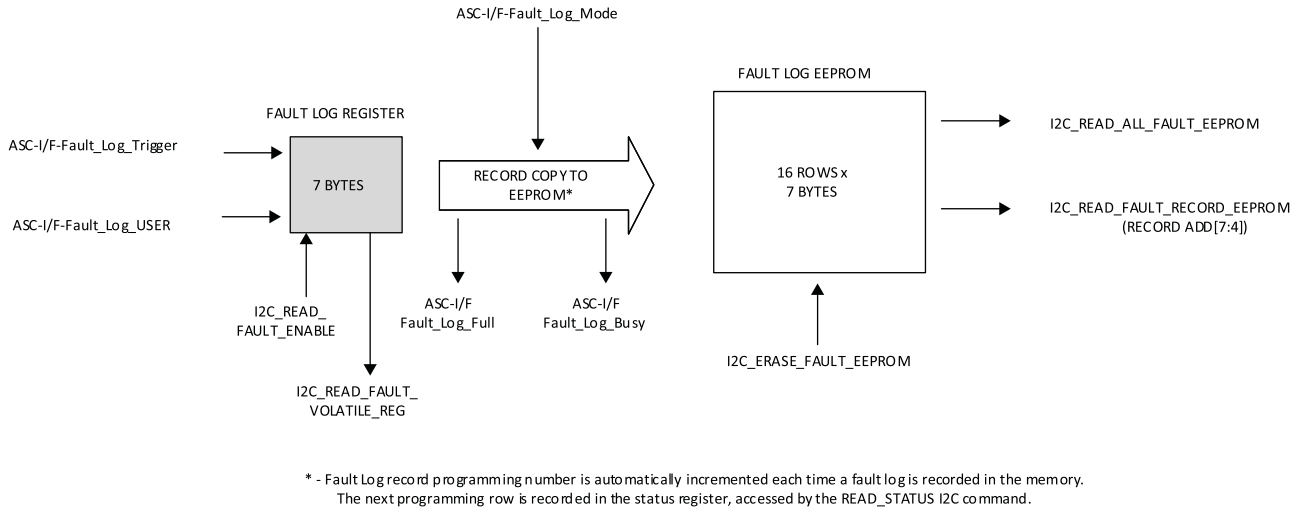

Figure 9.32. Fault Log Memory Block with I²C Access Instructions

The ERASE_FAULT_EEPROM instruction is used to erase the entire fault log EEPROM record storage. The ASC must be in programming mode in order to execute this instruction (See the PROGRAM_MODE instruction). The READ_FAULT_ENABLE instruction must also have been sent to the ASC in order to disable recording of new faults. The format for the ERASE_FAULT_EEPROM is shown in Figure 9.33 below.

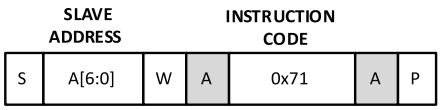

Figure 9.33. ERASE_FAULT_EEPROM - I²C Instruction Format

The READ_FAULT_VOLATILE_REG instruction is used to read back the contents of the fault logging register. The 7 bytes are read back in order from Byte 0 to Byte 7. The READ_FAULT_ENABLE instruction must have been sent to the ASC in order to disable recording of new faults, prior to executing a READ_FAULT_VOLATILE_REG instruction. The format is shown in Figure 9.34.

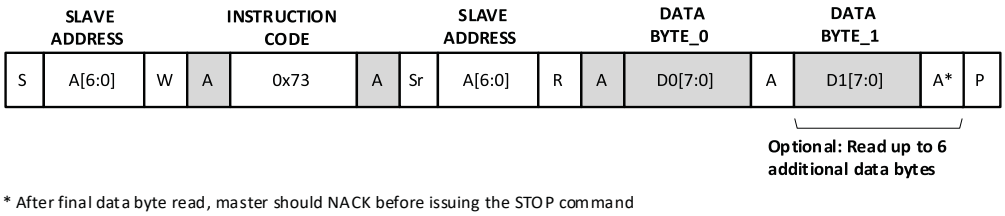

Figure 9.34. READ_FAULT_VOLATILE_REG - I²C Instruction Format

The READ_FAULT_ENABLE instruction is used to disable the fault log recording hardware, and to enable the readback and erase of the fault logging memory block and fault log register. The READ_FAULT_ENABLE instruction is a write instruction with readback. The first transaction is a write transaction, as shown in Figure 9.35 below. The Address Byte with W=0 is sent, followed by the 0x74 instruction byte, followed by a keycode value of 0xAC. This key code is required to enable reading out or erasing of faults and disable fault recording. Sending any other keycode will disable reading and enable fault recording. Sending an incorrect keycode is the mechanism used to reenable fault log recording without resetting the device.

The second transaction is a read transaction, with the Address Byte with R=1 sent, followed by a readback of the Fault Log Status Register. The Fault Log status register is described in Figure 9.36.

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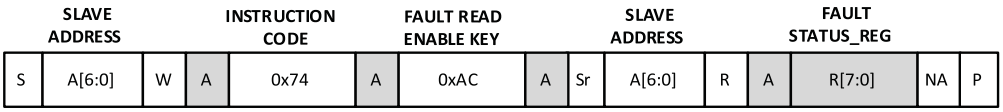

Figure 9.35. READ_FAULT_ENABLE - I²C Instruction Format

Fault Log Status Register (Read Only)

REQ[1]	REQ[0]	EN[1]	EN[0]	0	0	0	0
b7	b6	b5	b4	b3	b2	b1	b0

Figure 9.36. Fault Log Status Register

The Fault Log status register is a read-only register which indicates the status of the fault log hardware. The register bits indicate whether reading of fault logs is enabled or disabled. The possible readout combinations of the register are shown in Table 9.66.

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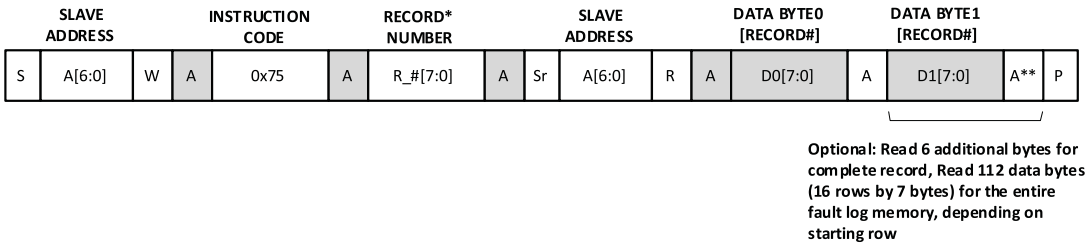
Table 9.66. Fault Log Status Details

REQ[1]	REQ[0]	EN[1]	EN[0]	Fault Log Status
0	0	0	0	ASC device is in safe state, or ERASEFAULT operation is active
0	0	1	1	Fault Logging is active, reading faults is disabled
1	1	0	0	Future fault logging is disabled and fault log read enable is requested. Reading fault logs will be enabled pending completion of in progress fault log recording or other EEPROM erase/program operation on-chip
1	1	1	1	Reading of fault logs via I^2C is now enabled. Fault log recording is disabled
All other values				Invalid reading

The READ_FAULT_RECORD_EEPROM instruction provides the mechanism to readback fault log records stored in the EEPROM memory. The READ_FAULT_RECORD_EEPROM is a two-step read transaction instruction, as shown in Figure 9.37. In the first step, a write transaction is performed with the 0x75 instruction, and a 4-bit address code [7:4]. The address code corresponds to fault log record 0 to 15, as shown in the fault log block diagram in Figure 9.36. In the second step, the fault log record can be read out in 7 bytes, from byte 0 to byte 6, using a read transaction. The record address will auto-increment to support reading multiple records in a single transaction. A stop condition will complete the read transaction, this can be issued after any number of rows and bytes have been read.The fault record is organized according to Table 6.14, in the Fault Logging and User Tag Memory section. This means a single transaction can support reading the all 15 fault log memory records, if the starting address of Record 0 is used.

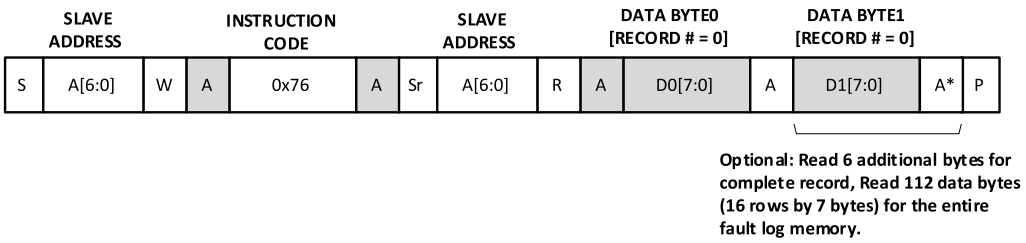
The READ_FAULT_RECORD_EEPROM instruction will be ignored if the READ_FAULT_ENABLE instruction has not been used to disable active fault recording.



*The Record Number R_#[7:0] contains the 4-bit record number code in bits [7:4]. Bits [3:0] are always zero.
** After final data byte read, master should NACK before issuing the STOP command

Figure 9.37. READ_FAULT_RECORD_EEPROM - I^2C Instruction Format

The READ_ALL_FAULT_EEPROM is similar to the READ_FAULT_RECORD_EEPROM instruction and provides an alternative mechanism for reading back fault log records stored in EEPROM memory. The READ_ALL_FAULT_EEPROM instruction always starts the readback at Record 0 and does not support requesting an individual fault log record request. During the read transaction, shown in Figure 9.38, fault log row 0 can be read out in 7 bytes. The row address will auto-increment to allow reading out the entire fault log array in a single transaction. A stop condition will complete the read transaction, this can be issued after any number of rows and bytes have been read. The READ_ALL_FAULT_EEPROM instruction will be ignored if the READ_FAULT_ENABLE instruction has not been used to disable active fault recording.



* After final data byte read, master should NACK before issuing the STOP command

Figure 9.38. READ_ALL_FAULT_EEPROM - I^2C Instruction Format

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Fault Log Memory Readout Example

This example describes the steps necessary to read the fault log EEPROM array over I^2C. Note that the device must be in fault logging mode or it will not respond to these instructions.

1. Perform an I^2C Write with the READ_FAULT_ENABLE instruction (0x74), with the 1-byte key code 0xAC. Complete the READ_FAULT_ENABLE operation by reading back the Fault Log Status Register. Repeat this operation until the Fault Log Status register reads as 0xF0 (Fault Log Reading is Enabled). When reading is enabled, fault log recording will be disabled.
2. Perform an I^2C Read with the READ_STATUS instruction (0x03). The ASC_STATUS_REGISTER_LO[7:4] bits (FAULT_CNT[3:0]) are equal to the number of fault log records which have been written to the EEPROM memory array by the recording hardware. ASC_STATUS_REGISTER_LO[3] (FAULT_LOG_FULL) is set to 1 when all sixteen records have been used for fault logging.
3. Perform an I^2C READ with the READ_ALL_FAULT_EEPROM instruction (0x76). Read out the fault logs starting at Record 0, Byte 0. Continue reading data until you reach the last populated fault record (given by FAULT_CNT[3:0] in step 3), byte 6.
4. Perform an I^2C Write with the READ_FAULT_ENABLE instruction (0x74), with any keycode besides 0xAC. This disables fault log I^2C access and returns the device to fault log recording mode. Repeat this operation until the Fault Log Status register reads as 0x00 (Fault Log Recording is Enabled).

Fault Log Memory Erase Example

This example describes the steps necessary to erase the fault log EEPROM array. Note that the device must be in fault logging mode or it will not respond to these instructions.

1. Perform an I^2C Write with the ENABLE_PROGRAM instruction (0x04), with the 2-byte key code 0xE53D. This will place the chip in programming mode, a required step to erase the fault log EEPROM array.
2. Perform an I^2C Write with the READ_FAULT_ENABLE instruction (0x74), with the 1-byte key code 0xAC. Complete the READ_FAULT_ENABLE operation by reading back the Fault Log Status Register. Repeat this operation until the Fault Log Status register reads as 0xF0 (Fault Log Reading is Enabled).
3. Perform an I^2C Write with the ERASE_FAULT_EEPROM instruction (0x71). This will erase the fault log EEPROM memory.
4. Perform an I^2C Write with the READ_FAULT_ENABLE instruction (0x74), with any keycode besides 0xAC. This disables fault log I^2C access and return the device to fault log recording mode. Repeat this operation until the Fault Log Status register reads as 0x00 (Fault Log Recording is Enabled).
5. Perform an I^2C Write with the ENABLE_USER instruction (0x05). This operation places the ASC back in User Mode in order to prevent accidental programming access.

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9.9. I²C Write Protection

The ASC includes multiple protection mechanisms to prohibit accidental or incorrect access to the active device configuration. The active device configuration access protections are set during the initial programming of the device (also described in Table 9.53). There are three possible protection modes:

- I²C Configuration Write Enabled – The ASC configuration parameters can be freely overwritten by I²C commands
- I²C Configuration Write Disabled – The ASC configuration parameters cannot be overwritten by I²C instructions
- I²C Configuration Write Controlled by GPIO1 Pin State – The ASC configuration parameters can only be overwritten by I²C instructions when GPIO1 is pulled high by an external device (FPGA or Microcontroller)

These protection modes control the configuration access by the following I²C instructions: WRITE_CFG_REG, WRITE_CFG_REG_wMASK, and TRIMx_CLT_P0_SET. This protection does not prevent EEPROM access instructions. EEPROM access is protected by the ENABLE_PROG_MODE instruction and instruction key.

Figure 9.39 shows the typical configuration for working in the "Configuration Write Controlled by GPIO1 pin State" protection mode.

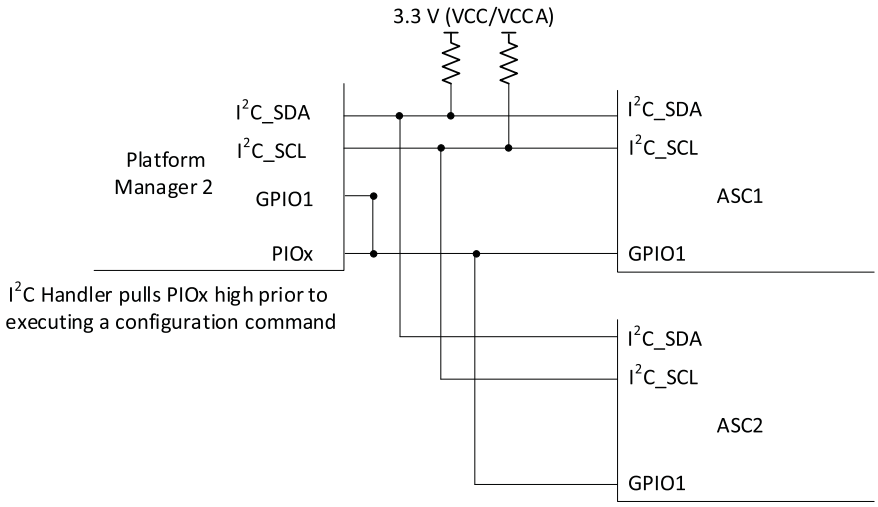

Figure 9.39. I²C Write Protect by GPIO1

The ASC device will still provide ACK bits in I²C write transmissions, even when the configuration write is disabled (by either the GPIO1 state or configuration setting). Even though the device presents ACK bits, the configuration memory will not be overwritten.

When using Write Protect by GPIO1 with WRITE_CFG_REG or WRITE_CFG_REG_wMASK, the GPIO1 signal should be asserted before transmission of the 7-bit slave address. It should be de-asserted after the STOP or RESTART signaling that marks the end of the write access. For TRIMx_CLT_P0_SET access, the GPIO1 signal should be asserted before transmission of the 7-bit slave address of the write phase. It should be de-asserted during or after the transmission of the slave address at the start of the readback phase (See the

Closed Loop Trim Register Access section for more details).

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10. Pin Descriptions

The LPTM21L (100-Ball caBGA package) is designed to be used both as a central controller and as a hardware management expander. Certain logic connections have different functions based on usage as a central controller or expander and are listed in Table 10.1.

Table 10.1. LPTM21L – Central Controller versus Expander Logic Signal Functions

LPTM21L 100-Ball caBGA	Central Controller Function	Expander Function	Comments	Ball Function
K3	DIO1	DIO1	Digital Input / Output	PB11B
K4	DIO2	DIO2	Digital Input / Output	PB11A
J4	DIO3	DIO3	Digital Input / Output	PB20A
H3	DIO4	DIO4	Digital Input / Output	PB9B
G3	DIO5	DIO5	Digital Input / Output	PB9A
F3	DIO6	DIO6	Digital Input / Output	PB15A
E4	DIO7	DIO7	Digital Input / Output	PB15B
A5	DIO8	DIO8	Digital Input / Output	PT12A
B5	DIO9	DIO9	Digital Input / Output	PT12B
D4	DIO10	DIO10	Digital Input / Output	PT11A
C2	DIO11/WRCLK_1	DIO11	ASC-I/F to Expander 1	PL5A
H2	DIO12/WDAT_1	DIO12	ASC-I/F to Expander 1	PL8C
D1	DIO13/WRCLK_2	DIO13	ASC-I/F to Expander 2	PL4B
F1	DIO14/WDAT_2	DIO14	ASC-I/F to Expander 2	PL4D
B1	DIO15/WRCLK_3	DIO15	ASC-I/F to Expander 3	PL3A
A2	DIO16/WDAT_3	DIO16	ASC-I/F to Expander 3	PL3C
D3	RDAT_1/ I2C_ADDR0[1]	I2C_ADDR0[1]	ASC-I/F to Expander 1 / Sets FPGA I^2C Address	PL5B
E1	RDAT_2/ I2C_ADDR1[1]	I2C_ADDR1[1]	ASC-I/F to Expander 2 / Sets FPGA I^2C Address	PL4C
B2	RDAT_3/ I2C_ADDR2[1]	I2C_ADDR2[1]	ASC-I/F to Expander 3 / Sets FPGA I^2C Address	PL3D
K5	DIO17/SI/SISPI/RST_1	DIO17	SPI / ASC-I/F to Optional Expander 1 Reset	PB20D
K2	DIO18/SO/SPISO/RST_2	DIO18	SPI / ASC-I/F to Optional Expander 2 Reset	PB6D
J2	DIO19/CSSPIN/RST_3	DIO19	SPI / ASC-I/F to Optional Expander 3 Reset	PB4C
J3	DIO20/MCLK/CCLK	DIO20	SPI / Digital Input / Output	PB6C
J5	DIO21/SN	DIO21	—	PB20C
A3	DIO22/TDO	DIO22	JTAG / Digital Input / Output	PT10C
A4	DIO23/TCK	DIO23	JTAG / Digital Input / Output	PT11C
B4	DIO24/TMS	DIO24	JTAG / Digital Input / Output	PT11D
B3	DIO25/TDI	DIO25	JTAG / Digital Input / Output	PT10D
E3	DIO26	RDAT2	ASC-I/F to Central Controller	PL8A
H1	NC_FT1	WDAT2	ASC-I/F to Central Controller	NC_FT1
G2	NC_FT2	WRCLK2	ASC-I/F to Central Controller	NC_FT2
J1	NC_FT3	NC_FT3	No Connect Factory Test (RDAT)	NC_FT3
G1	NC_FT4	NC_FT4	No Connect Factory Test (ASCCLK)	ASCCLK
C6	DONE	—	—	PT17D
A6	PROGRAMN	—	—	PT15D
C5	INITN	—	—	PT17C
B6	JTAGENB	JTAGENB	—	PT15C
C4	SCL	SCL	I^2C Clock	SCL
C3	SDA	SDA	I^2C Data	SDA

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LPTM21L 100-Ball caBGA	Central Controller Function	Expander Function	Comments	Ball Function
C1	RESETB	RESETB	Connect all Mandatory Expanders to Central Controller. Connect Optional Expanders to respective ASC-I/F Resets	RESETB

Notes:

1. When the LPTM21L (100-Ball caBGA package) is used as an expander device, connect a pull-up resistor (1k) to set the FPGA I^2C address (as shown in Figure 8.2, Figure 9.2, and Table 8.2).
2. When the LPTM21L (100-Ball caBGA package) is used as an expander device, use these balls to connect to the central Platform Manager 2 control device (as shown in Figure 8.2 and Figure 9.2).

10.1. LPTM21 and LPTM21L

Table 10.2. LPTM21 and LPTM21L – Logic Signal Connections

Ball Function	LPTM21 237-Ball ftBGA	LPTM21L 100-Ball caBGA	Bank	Dual Function	Differential Input / Complementary Output Pairs
PB11A	N6	K4	2	PCLKT2_1	TRUE
PB11B	P6	K3	2	PCLKC2_1	COMP
PB11C	T4	—	2	—	TRUE
PB11D	P5	—	2	—	COMP
PB15A	R5	F3	2	—	TRUE
PB15B	R6	E4	2	—	COMP
PB15C	N7	—	2	—	TRUE
PB15D	M7	—	2	—	COMP
PB18A	T7	—	2	—	TRUE
PB18B	R7	—	2	—	COMP
PB18C	P7	—	2	—	TRUE
PB18D	P8	—	2	—	COMP
PB20A	N8	J4	2	—	TRUE
PB20B	M8	—	2	—	COMP
PB20C	T9	J5	2	SN	TRUE
PB20D	R9	K5	2	SI/SISPI	COMP
PB4A	R1	—	2	—	TRUE
PB4B	P1	—	2	—	COMP
PB4C	P2	J2	2	CSSPIN	TRUE
PB4D	M5	—	2	—	COMP
PB6A	P3	—	2	—	TRUE
PB6B	T2	—	2	—	COMP
PB6C	R3	J3	2	MCLK/CCLK	TRUE
PB6D	T3	K2	2	SO/SPISO	COMP
PB9A	P4	G3	2	PCLKT2_0	TRUE
PB9B	R4	H3	2	PCLKC2_0	COMP
PB9C	N5	—	2	—	TRUE
PB9D	M6	—	2	—	COMP
PL10A	M1	—	3	—	TRUE
PL10B	N1	—	3	—	COMP
PL10C	N2	—	3	—	TRUE
PL10D	M2	—	3	—	COMP
PL2A	E2	—	3	L_GPLLT_FB	TRUE
PL2B	D2	—	3	L_GPLLC_FB	COMP

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Ball Function	LPTM21 237-Ball ftBGA	LPTM21L 100-Ball caBGA	Bank	Dual Function	Differential Input / Complementary Output Pairs
PL2C	D1	—	3	L_GPLLT_IN	TRUE
PL2D	E1	—	3	L_GPLLC_IN	COMP
PL3A	F2	B1	3	PCLKT3_2	TRUE
PL3B	F3	—	3	PCLKC3_2	COMP
PL3C	F1	A2	3	—	TRUE
PL3D	G1	B2	3	—	COMP
PL4A	G2	—	3	—	TRUE
PL4B	G3	D1	3	—	COMP
PL4C	H3	E1	3	—	TRUE
PL4D	H2	F1	3	—	COMP
PL5A	J2	C2	3	PCLKT3_1	TRUE
PL5B	J3	D3	3	PCLKC3_1	COMP
PL8A	K3	E3	3	—	TRUE
PL8B	K2	—	3	—	COMP
PL8C	K1	H2	3	—	TRUE
PL8D	L1	—	3	—	COMP
PL9A	L3	—	3	PCLKT3_0	TRUE
PL9B	L2	—	3	PCLKC3_0	COMP
PR10A	N10	—	1	—	TRUE
PR10B	P10	—	1	—	COMP
PR10C	P9	—	1	—	TRUE
PR10D	R10	—	1	—	COMP
PR2A	D10	—	1	—	TRUE
PR2B	C10	—	1	—	COMP
PR2C	C11	—	1	—	TRUE
PR2D	D11	—	1	—	COMP
PR3A	E10	—	1	—	TRUE
PR3B	E9	—	1	—	COMP
PR4A	E11	—	1	—	TRUE
PR4B	F10	—	1	—	COMP
PR5D	B10	—	1	PCLKC1_0	N/A
PR8D	N9	—	1	—	N/A
PR9A	L10	—	1	—	TRUE
PR9B	T10	—	1	—	COMP
PR9C	M9	—	1	—	TRUE
PR9D	M10	—	1	—	COMP
PT10A	D3	—	0	—	TRUE
PT10B	E4	—	0	—	COMP
PT10C	B3	A3	0	TDO	TRUE
PT10D	A3	B3	0	TDI	COMP
PT11A	D5	D4	0	—	TRUE
PT11B	E6	—	0	—	COMP
PT11C	C4	A4	0	TCK	TRUE
PT11D	B4	B4	0	TMS	COMP
PT12A	A4	A5	0	PCLKT0_1	TRUE
PT12B	C5	B5	0	PCLKC0_1	COMP
PT12C	D6	C4	0	SCL_M	TRUE

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Ball Function	LPTM21 237-Ball ftBGA	LPTM21L 100-Ball caBGA	Bank	Dual Function	Differential Input / Complementary Output Pairs
PT12D	C6	C3	0	SDA_M	COMP
PT15A	B5	—	0	—	TRUE
PT15B	B6	—	0	—	COMP
PT15C	D7	B6	0	JTAGENB	TRUE
PT15D	E7	A6	0	PROGRAMN	COMP
PT16A	A7	—	0	—	TRUE
PT16B	B7	—	0	—	COMP
PT16C	C7	—	0	—	TRUE
PT16D	C8	—	0	—	COMP
PT17A	D8	—	0	—	TRUE
PT17B	E8	—	0	—	COMP
PT17C	C9	C5	0	INITN	TRUE
PT17D	D9	C6	0	DONE	COMP
PT9A	B1	—	0	—	TRUE
PT9B	C1	—	0	—	COMP
PT9C	C2	—	0	—	TRUE
PT9D	B2	—	0	—	COMP

Note: The same balls are listed in both Table 10.2 and Table 10.3 for clarity. They are connected within the LPTM21L (100-Ball caBGA package).

Table 10.3. LPTM21 and LPTM21L – Analog Sense and Control Signals

Ball Function	LPTM21 237-Ball ftBGA	LPTM21L 100-Ball caBGA	Pin Type	Description
I2C_ADDR	—	K6	Analog Input	Connect R to GND to set Address
SCL_S0	P12	C41	Digital I/O	I^2C Serial Clock, Bi-directional Pin
SDA_S0	N12	C31	Digital I/O	I^2C Serial Data, Bi-directional Pin
ASCCLK	P11	G1	Digital I/O	8 MHz ASC Clock Output CMOS
NC_FT1	B11	H1	Digital I/O	Test Point/ASC Interface WDAT2
NC_FT2	F11	G2	Digital I/O	Test Point/ASC Interface WRCLK2
NC_FT3	G11	J1	Digital I/O	Test Point
RESETb	F13	C1	Digital I/O	ASC Reset (Active Low)
HVOUT1	D12	A8	Analog/Digital Out	Current Source / Open Drain Output, reset Low
HVOUT2	C13	A7	Analog/Digital Out	Current Source / Open Drain Output, reset Low
HVOUT3	K11	G5	Analog/Digital Out	Current Source / Open Drain Output, reset Low
HVOUT4	L11	H5	Analog/Digital Out	Current Source / Open Drain Output, reset Low
GPIO1	A14	B7	Digital I/O	Digital Input / Write Protect Input / Open Drain Output, reset Low
GPIO2	F12	C7	Digital I/O	Digital Input / Open Drain Output, reset Low
GPIO3	E13	D6	Digital I/O	Digital Input / Open Drain Output, reset Low
GPIO4	G12	E6	Digital I/O	Digital Input / Open Drain Output, reset Low
GPIO5	B13	F6	Digital I/O	Digital Input / Open Drain Output, reset Low
GPIO6	C12	F5	Digital I/O	Digital Input / Open Drain Output, reset Low
GPIO7	B12	G6	Digital I/O	Digital Input / Open Drain Output, reset Hi-Z
GPIO8	R11	H6	Digital I/O	Digital Input / Open Drain Output, reset Hi-Z
GPIO9	M11	J6	Digital I/O	Digital Input / Open Drain Output, reset Hi-Z
GPIO10	N11	H7	Digital I/O	Digital Input / Open Drain Output, reset Low
VMON1	P16	K8	Analog Input	Voltage Monitor Input
VMON1GS	R16	J8	Analog Input	Voltage Monitor Input Ground Sense

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Ball Function	LPTM21 237-Ball ftBGA	LPTM21L 100-Ball caBGA	Pin Type	Description
VMON2	L15	H8	Analog Input	Voltage Monitor Input
VMON2GS	M15	G8	Analog Input	Voltage Monitor Input Ground Sense
VMON3	K16	J7	Analog Input	Voltage Monitor Input
VMON3GS	L16	K7	Analog Input	Voltage Monitor Input Ground Sense
VMON4	H16	E10	Analog Input	Voltage Monitor Input
VMON4GS	J16	D10	Analog Input	Voltage Monitor Input Ground Sense
VMON5	G15	C10	Analog Input	Voltage Monitor Input
VMON6	E15	B10	Analog Input	Voltage Monitor Input
VMON7	E16	D9	Analog Input	Voltage Monitor Input
VMON8	C16	C9	Analog Input	Voltage Monitor Input
VMON9	B16	B9	Analog Input	Voltage Monitor Input
HIMONP	T13	H9	Analog Input	12 V Current Monitor Input Source
HIMONN_HVMON	T14	G9	Analog Input	12 V Current Monitor Input Return/ Voltage Monitor Input
IMONP	R14	J10	Analog Input	Low Voltage Current Monitor Input source
IMONN	P14	H10	Analog Input	Low Voltage Current Monitor Input return
TMON1P	T15	G10	Analog Input	Temperature Monitor Input source
TMON1N	R15	F10	Analog Input	Temperature Monitor Input Return
TMON2P	P15	K9	Analog Input	Temperature Monitor Input source
TMON2N	N15	J9	Analog Input	Temperature Monitor Input Return
TRIM1	B15	D8	Analog Output	Trim DAC Output
TRIM2	A15	C8	Analog Output	Trim DAC Output
TRIM3	F14	B8	Analog Output	Trim DAC Output
TRIM4	G14	A9	Analog Output	Trim DAC Output
NC	D13	—	N/A	—
NC	A11	—	N/A	—

Notes:

1. The same balls are listed in both Table 10.2 and Table 10.3 for clarity. They are connected within the LPTM21L (100-Ball caBGA package).
2. When the LPTM21L (100-Ball caBGA package) is used as a remote device use these balls to connect to the central Platform Manager 2 control device (as shown in Figure 8.2).

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Table 10.4. LPTM21 and LPTM21L – Power and Ground Connections

Ball Function	LPTM21 237-Ball ftBGA	LPTM21L 100-Ball caBGA	Bank	Description
VCC	G5	D7	N/A	Digital Supply
VCC	G6	G7	N/A	Digital Supply
VCC	G7	—	N/A	Digital Supply
VCC	K5	—	N/A	Digital Supply
VCC	K6	—	N/A	Digital Supply
VCC	K7	—	N/A	Digital Supply
VCCA	G16	E9	N/A	Analog Supply
VCCA	H12	E8	N/A	Analog Supply
VCCA	J12	F8	N/A	Analog Supply
GND	A16	A10	N/A	Device Ground
GND	H14	K10	N/A	Device Ground
GND	J14	F9	N/A	Device Ground
GND	T16	E7	N/A	Device Ground
GND	A13	F7	N/A	Device Ground
GND	H11	G4	N/A	Device Ground
GND	J11	E2	N/A	Device Ground
GND	T12	A1	N/A	Device Ground
GND	A1	K1	N/A	Device Ground
GND	A6	—	N/A	Device Ground
GND	E3	—	N/A	Device Ground
GND	F6	—	N/A	Device Ground
GND	H5	—	N/A	Device Ground
GND	H6	—	N/A	Device Ground
GND	H7	—	N/A	Device Ground
GND	J1	—	N/A	Device Ground
GND	J5	—	N/A	Device Ground
GND	J6	—	N/A	Device Ground
GND	J7	—	N/A	Device Ground
GND	L6	—	N/A	Device Ground
GND	M3	—	N/A	Device Ground
GND	T1	—	N/A	Device Ground
GND	T6	—	N/A	Device Ground
VCCIO0	A5	D5	0	IO-0 Supply
VCCIO0	F4	E5	0	IO-0 Supply
VCCIO0	F5	—	0	IO-0 Supply
VCCIO0	F7	—	0	IO-0 Supply
VCCIO0	F8	—	0	IO-0 Supply
VCCIO1	G8	—	1	IO-1 Supply
VCCIO1	H8	—	1	IO-1 Supply
VCCIO1	J8	—	1	IO-1 Supply
VCCIO1	K8	—	1	IO-1 Supply
VCCIO2	L4	F4	2	IO-2 Supply
VCCIO2	L5	H4	2	IO-2 Supply
VCCIO2	L7	—	2	IO-2 Supply
VCCIO2	L8	—	2	IO-2 Supply
VCCIO2	T5	—	2	IO-2 Supply

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Ball Function	LPTM21 237-Ball ftBGA	LPTM21L 100-Ball caBGA	Bank	Description
VCCIO3	J4	D2	3	IO-3 Supply
VCCIO3	K4	F2	3	IO-3 Supply
NC	A10	—	N/A	Not Used
NC	A2	—	N/A	Not Used
NC	A8	—	N/A	Not Used
NC	A9	—	N/A	Not Used
NC	A12	—	N/A	Not Used (Do not connect)
NC	B14	—	N/A	Not Used
NC	B8	—	N/A	Not Used
NC	B9	—	N/A	Not Used
NC	C14	—	N/A	Not Used
NC	C15	—	N/A	Not Used
NC	C3	—	N/A	Not Used
NC	D14	—	N/A	Not Used
NC	D15	—	N/A	Not Used
NC	D16	—	N/A	Not Used
NC	D4	—	N/A	Not Used
NC	E12	—	N/A	Not Used
NC	E14	—	N/A	Not Used
NC	E5	—	N/A	Not Used
NC	F15	—	N/A	Not Used
NC	F16	—	N/A	Not Used
NC	H15	—	N/A	Not Used
NC	J15	—	N/A	Not Used
NC	K12	—	N/A	Not Used
NC	K14	—	N/A	Not Used
NC	K15	—	N/A	Not Used
NC	L12	—	N/A	Not Used
NC	L14	—	N/A	Not Used
NC	M12	—	N/A	Not Used
NC	M14	—	N/A	Not Used
NC	M16	—	N/A	Not Used
NC	M4	—	N/A	Not Used
NC	N14	—	N/A	Not Used
NC	N16	—	N/A	Not Used
NC	N3	—	N/A	Not Used
NC	N4	—	N/A	Not Used
NC	R12	—	N/A	Not Used
NC	R2	—	N/A	Not Used
NC	R8	—	N/A	Not Used
NC	T11	—	N/A	Not Used
NC	T8	—	N/A	Not Used
NC	H1	—	N/A	Not Used
NC	G4	—	N/A	Not Used
NC	H4	—	N/A	Not Used

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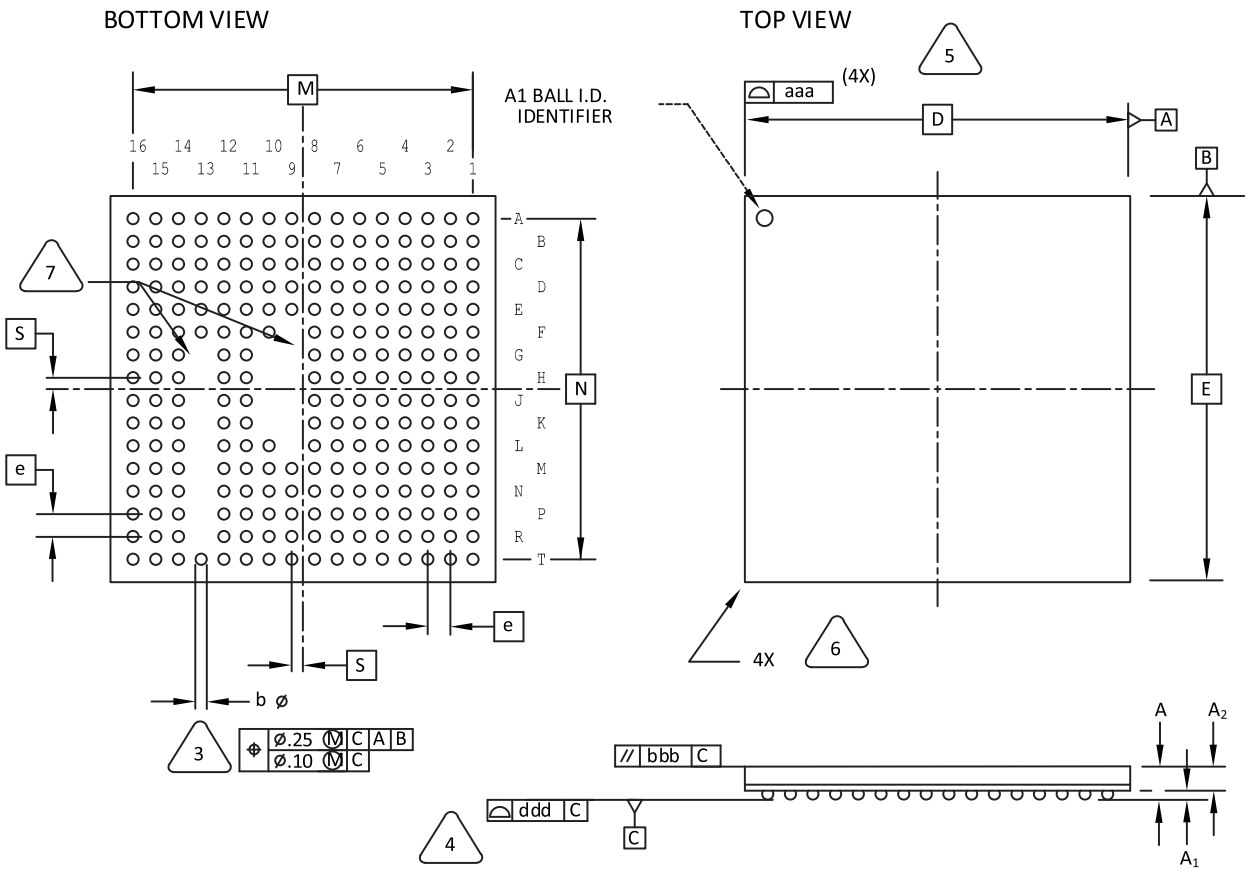
11. Package Diagram

11.1. 237-Ball ftBGA Package

Dimensions in Millimeters



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
4. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. DEPOPULATED 13G TO 13R, 10G TO 10K, AND 9F TO 9L.

SYMBOL	MIN.	NOM.	MAX.
A	1.40	1.55	1.70
A1	0.30	-	
A2	-	-	1.24
D/E	17.0 BSC		
M/N	15.0 BSC		
S	0.50 BSC		
b	0.40	0.50	0. 60
e	1.0 BSC		
aaa	-	-	0.20
bbb	-	-	0.25
ddd	-	-	0.15

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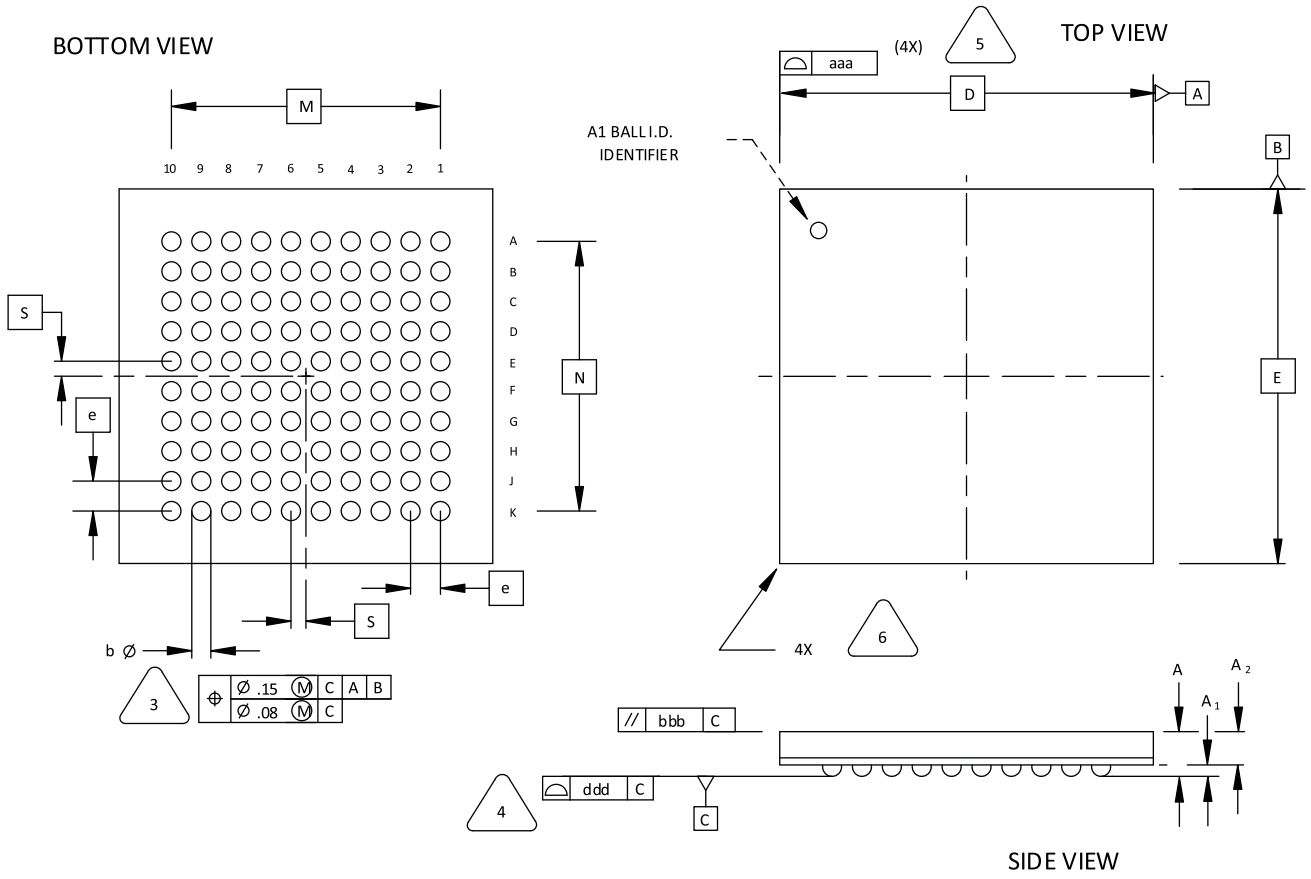
11.2. 100-Ball caBGA Package

Dimensions in Millimeters



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

4. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.

6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	1.30	1.40	1.50
A1	0.31	0.36	0.41
A2	0.99	1.04	1.09
D/E	10.00 BSC		
M/N	7.20 BSC		
S	0.40 BSC		
b	0.40	0.46	0.52
e	0.80 BSC		
aaa	-	-	0.10
bbb	-	-	0.10
ddd	-	-	0.12

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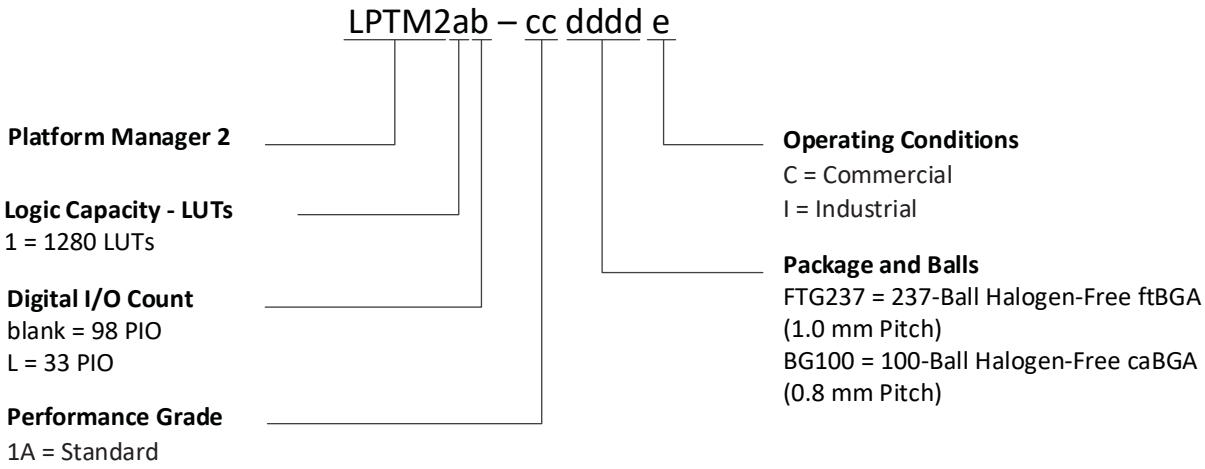
12. Part Number Description



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13. Ordering Information

13.1. Halogen-Free Packaging

Table 13.1. Commercial

Part Number	LUTs	Package	Balls
LPTM21-1A FTG237 C	1280	Halogen-Free ftBGA (17 mm x 17 mm)	237

Table 13.2. Industrial

Part Number	LUTs	Package	Balls
LPTM21-1A FTG237 I	1280	Halogen-Free ftBGA (17 mm x 17 mm)	237
LPTM21L-1A BG100 I	1280	Halogen-Free caBGA (10 mm x 10 mm)	100

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For Further Information

For more information on the Platform Manager 2 family of devices, consult the Platform Manager 2, MachXO2, MachXO3, and ECP5 family data sheets along with related application and technical notes on the Lattice website.

- L-ASC10 Data Sheet (FPGA-DS-02038)
- ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012)
- MachXO2 Family Data Sheet (FPGA-DS-02056)
- MachXO3 Family Data Sheet (FPGA-DS-02032)
- Power Estimation and Management for MachXO2 Devices (TN1198)
- MachXO2 sysI/O Usage Guide (FPGA-TN-02158)
- L-ASC10 and Platform Manager 2 Hardware Checklist (FPGA-TN-02175)
- MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155)
- Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162)
- Platform Manager 2 Evaluation Board User Guide (EB93)

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Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

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Revision History

Revision 2.3, August 2021

Section	Change Summary
All	Updated document template.
Theory of Operation	• Updated information on HIMONP pin in the High Voltage Monitor section. • Added note to Table 6.7. Remote TMON Diode Configurations. • Updated information on Safe State in the Safe State section. • Updated Bit3 value in Table 6.14. Fault Log Record Memory Map.
System Connections	Updated information on power pin connections for the LPTM21 237-Ball ftBGA and the 100-Ball caBGA packages in the ASC Interface and I2C Connections section.
I^2C Interface	• Updated Table 9.6. Trim Configuration Register Summary. • Updated values in Table 9.32. Temperature Monitor Fault Setting. • Updated Temperature Monitor Hysteresis.
All	Updated document numbers in references.

Revision 2.2, September 2019

Section	Change Summary
Multiple	• Removed DC-DC Converter feature from several sections. • Clarified Closed Loop Trim mode and Bypass mode in several sections.
I^2C Interface	• Updated Raddr Values in Table 8.1. • Added footnotes to Table 8.1. • Added clarification to Voltage Monitor ADC Readout Over I^2C.
Pin Descriptions	Added Ball Function to Table 10.1.
Package Diagrams	Added Top and Bottom labels to 237-Ball ftBGA package diagram. Removed corner artwork from 100-Ball caBGA package diagram.
Ordering Information	Removed Commercial part number for LPTM21L 100-Ball caBGA.
Disclaimers	Added this section.

Revision 2.1, March 2019

Section	Change Summary
All	Data sheet status changed from Preliminary to Final.
DC and Switching Characteristics	In Recommended Operating Conditions[1] section, added clarification to footnote 5 (237-ball ftBGA package only).
System Connections	In ASC Interface and I^2C Connections section, added clarification to ASC-I/F and VCCA usage.
Pin Descriptions	Changed LPTM21L 100-ball caBGA balls E8 and F8 from VCC to VCCA.

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Revision 2.0, September 2018

Section	Change Summary
All	Changed document number from DS1043 to FPGA-DS-02036.
Multiple	• Added LPTM21L 100-ball caBGA information. • Added MachXO3 and ECP5 information.
Features	• Updated FPGA Section Resources. • Added devices under Scalable Hardware Management Architecture. • Updated the 12 V DC-DC converter item under System Level Support.
Block Diagram	Updated Table 4.1..
DC and Switching Characteristics	Clarification added to Fault Log table.
System Connections	• Added Figure 8.2Figure 8.2. • Added Table 8.2. • In ASC Interface and I^2C Connections section, added information on using LPTM21L as a hardware expander.
I^2C Interface	• Updated Figure 8.2. • Added figure 9.1. • Updated Table 9.4 with ASC Section of LPTM21L.
Pin Descriptions	• Added information on JTAG pins. • Added Table 10.1. • Updated Table 10.2, Table 10.3, and Table 10.4.
Package Diagrams	Added this section.
Part Number Description	• Added Digital I/O Count. • Added BG100 under Package and Balls.
Ordering Information	Added part numbers for LPTM21L.
For Further Information	• Added MachXO3 and ECP5 information • Updated document numbers in references.
Technical Support Assistance	Updated contact information.

Revision 1.4, May 2016

Section	Change Summary
I^2C Interface	Updated Measurement and Control Register Access section to address restrictions on READ_MEAS_CTRL command with addresses 0x85 and 0x86.

Revision 1.3, April 2015

Section	Change Summary
Multiple	Deleted all references to LPTM20.
System Connections	• Modified Figure 8.1, System Connections - ASC and Platform Manager 2. • Added Table 8.1, Raddr Value vs. ASC Device Number to clarify I2C_ADDR pin connections.
I^2C Interface	• Updated ASC Configuration Registers section. • Updated Polarity bit setting in Table 9.7, POL Setting vs Closed Loop Trim Polarity.

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Revision 1.2, May 2014

Section	Change Summary
All	Data sheet status changed from preliminary to final.
Multiple	• Renamed IMON to IMON1. • Updated ASC-IF TRIM control signal names.
DC and Switching Characteristics	• Populated specifications with characterization results. • Added additional FPGA timing sections.
Theory of Operation	• Removed IMON Hysteresis feature. • Expanded Output Control Block section. • Updated System Connections section.
I^2C Interface	• Corrected error in Table 9.57, ADC Input Selection for IMON1 and HIMON SEL bits. • Update VMON and IMON tables with final device trip points.

Revision 1.1, March 2014

Section	Change Summary
DC and Switching Characteristics	Added preliminary ESD Performance section.

Revision 1.0, December 2013

Section	Change Summary
All	Preliminary release.

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