FSL518H, FSL538H, FSL518A, FSL538A

High Performance Integrated Off-line Switcher with HV Startup and SenseFET

The FSL5x8 is an integrated peak−current−mode controlled pulse width modulation (PWM) power switch, specifically designed for off−line switch−mode power supplies. The PWM controller includes an advanced soft−start, frequency hopping, optimized gate driver, internal transconductance amplifier, temperature−compensated precise current source for loop compensation and enhanced self−protections circuitry as well. Compared to a discrete MOSFET and PWM controller solution, the FSL5x8 allows to reduce total cost, component count, size, and weight, while simultaneously increase efficiency, productivity, and system reliability. This device provides a basic platform for cost−effective design of both isolated and non−isolated Flyback converters.

Features

- Internal 800 V Super−Junction II Rugged MOSFET with SenseFET Technology
- Built−in HV Current Source for Start−up and V_{CC} Regulation
- Peak−current−mode Control with Built−in Slope Compensation
- Line Compensation for Constant Maximum Over−power Limiting
- Advanced Soft−start for Low Electrical Stress
- V_{CC} Regulation for Start−up and Protection Mode
- Pulse−by−pulse Current Limit
- FSL5x8A: 100 kHz and FSL5x8H: 130 kHz
- Line Brown−in, Brown−out Function
- Line Over−voltage Protection (LOVP)
- Fine−tunable Burst Mode Operation
- Frequency Hopping for Low EMI
- All Protections are Auto−Recovery: Brown−out, OLP, V_{CC} OVP, AOCP, TSD, LOVP
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Supplies for White Goods
- Industrial Auxiliary Power Supply, E−metering SMPS
- Consumer Electronics (Chargers, Set−top−boxes, TVs)

ON Semiconductor®

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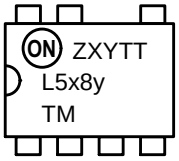
PDIP−7
CASE 626A

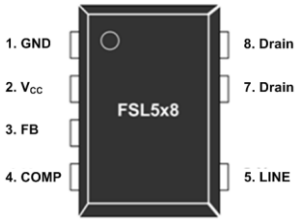
PDIP7 MINUS PIN 6 GW
CASE 707AA

MARKING DIAGRAM



Z	= Plant Code
X	= 1−digit Year Code
Y	= 1−digit Week Code
TT	= 2−digit Die−Run Code
L5x8	= Specific Device Code
x	= Device Option
y	= Frequency Option
T	= Package Type
M	= Manufacture Flow Code

PIN CONNECTIONS



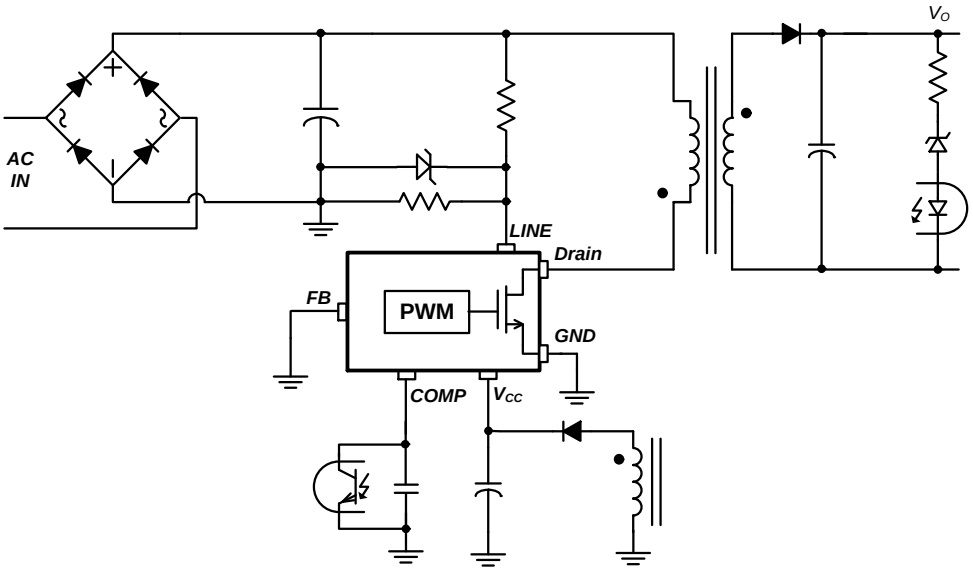
ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

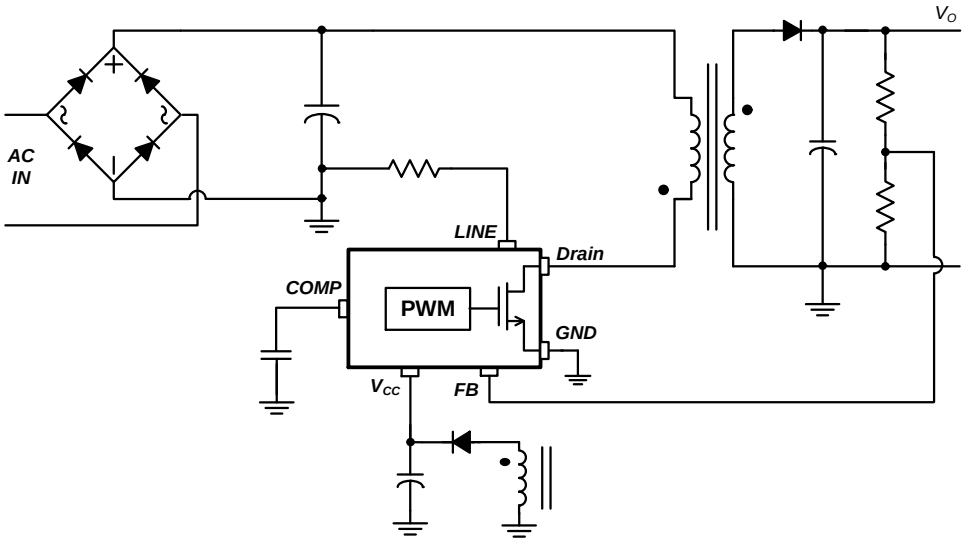
PRODUCT INFORMATION & INDICATIVE RECOMMENDED OUTPUT POWER

Part Number	Operating Junction Temperature	Operation Frequency	Output Power Table (Open Frame) (Notes 1, 2)			
			Current Limit (A)	Max. $R_{DS(ON)}$ (Ω)	230 V_{AC} ± 15%	85 ~ 265 V_{AC}
FSL518H	−40 ~ 125°C	130 kHz	0.46	8.0	15 W	12 W
FSL538H	−40 ~ 125°C	130 kHz	0.66	4.3	21 W	17 W
FSL518A	−40 ~ 125°C	100 kHz	0.61	8.0	17 W	14 W
FSL538A	−40 ~ 125°C	100 kHz	0.86	4.3	25 W	20 W

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open−frame design at 50°C ambient.



(a) Isolated Opto−coupler Feedback (Line detection enable)



(b) Non−isolated Direct Feedback (Line detection disable)

Figure 1. Application Schematic − Isolated or Non−isolated Flyback Converter

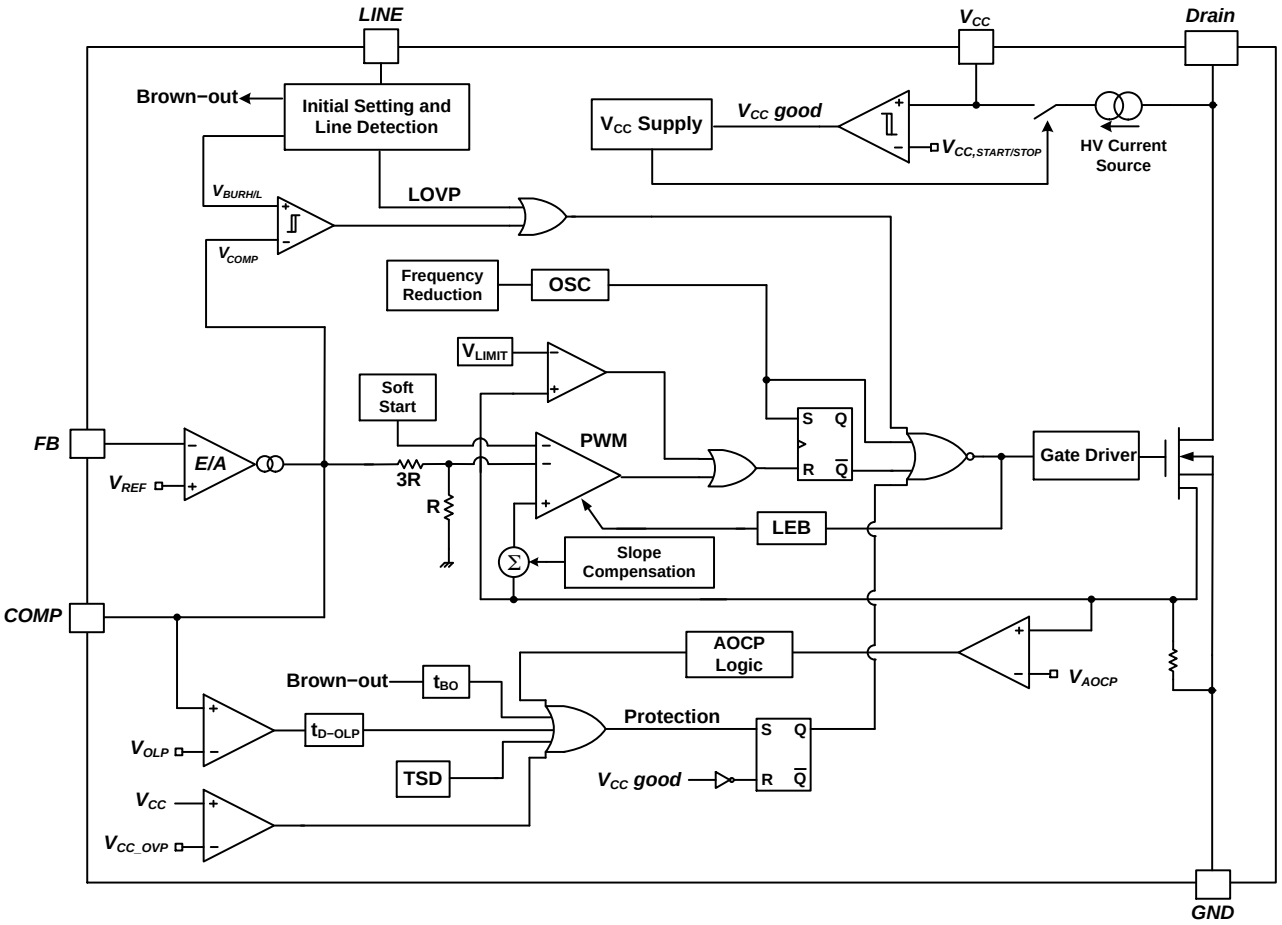


Figure 2. Internal Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Function	Description
1	GND	Ground	Ground reference of the controller.
2	V_{CC}	Power Supply	This pin is the positive supply input, which provides the internal operating current for both startup and steady−state operation.
3	FB	Feedback	This pin is connected to input of built−in transconductance amplifier for regulating output voltage of the power converter. If transconductance amplifier is not used, connect FB to GND.
4	COMP	Feedback−Loop Compensation	Control−loop compensation. For opto−coupler feedback, connect COMP to opto coupler directly.
5	LINE	Brown in/out, LOVP, Burst−Mode Setting	For line detection(Line OVP, Brown in/out), this pin needs to be connected to the high−voltage DC link through voltage divider. And it's also multiple−function pin for Burst Mode adjustment.
7,8	Drain	MOSFET Drain	High−voltage power MOSFET drain connection. In addition, during startup and protection mode, the internal high−voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Drain Pin Voltage	V_{DS}	−0.3 to 800	V
Maximum V_{CC} Pin Voltage	V_{CC}	−0.3 to +26	V
Feedback Pin Voltage	V_{FB}	−0.3 to +5.0	V
Compensation Pin Voltage	V_{COMP}	−0.3 to +5.0	V
Line−detection Pin Voltage	V_{LINE}	−0.3 to V_{CC}	V
Maximum Drain Pin Pulsed Current (Note 3) FSL518H/A FSL538H/A	$I_{D-PULSE}$	 2.1 2.8	A
Maximum Single Pulse Avalanche Energy (Note 4) FSL518H/A FSL538H/A	E_{AS}	 2 18	mJ
Maximum Total Power Dissipation (PDIP−7 & PDIP7 MINUS PIN 6 GW) FSL518H/A & FSL538H/A	P_D	 1.25	W
Maximum Junction Temperature (Note 5)	T_J	150	°C
Operating Junction Temperature (Note 6)	T_J	−40 to +125	°C
Storage Temperature	T_{STG}	−55 to +150	°C
ESD Capability HBM, JESD22−A114 ESD Capability HBM, JESD22−A114 (Except Drain pin)		1600 3000	V
ESD Capability CDM, JESD22−C101		1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty and junction temperature.
4. L=45mH, starting T_J = 25°C.
5. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics
6. Junction temperature can limit maximum output power of power converter controlled by the device.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, PDIP7 MINUS PIN 6 GW and PDIP−7 Thermal Resistance, Junction−to−Air (Note 7) FSL518H/A & FSL538H/A Thermal Reference, Junction−to−Lead (Note 7) FSL518H/A & FSL538H/A	 $R_{\theta JA}$ $R_{\psi JL}$	 100 18	°C/W

7. JEDEC recommended environment, JESD51−2, and test board, JESD51−3, with minimum land pattern.

ELECTRICAL CHARACTERISTICS

T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SenseFET Section						
MOSFET Peak Current Limit	T_J = 25°C, Duty = 60% di/dt = 100 mA/μs FSL518H di/dt = 100 mA/μs FSL518A di/dt = 143 mA/μs FSL538H di/dt = 143 mA/μs FSL538A	I_{LIM}	 428 560 614 790	 460 610 660 860	 492 660 706 930	mA
Drain−to−Source On−State Resistance	MOSFET ON, T_J = 25°C FSL518H/A, I_{DRAIN} = 0.46 A FSL538H/A, I_{DRAIN} = 0.66 A	$R_{DS(ON)}$		 6 3.6	 8.0 4.3	Ω
Output Capacitance	VDS = 480 V, V_{GS} = 0 V, f = 1 MHz, T_J = 25°C FSL518H/A FSL538H/A	C_{OSS}		 3..8 5		pF

ELECTRICAL CHARACTERISTICS (continued)
T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Effective Output Capacitance	VDS = 0 to 480 V, V_{GS} = 0 V, T_J = 25°C FSL518H/A FSL538H/A	$C_{OSS(eff)}$		 31 40		pF
Drain−voltage Rise Time (Note 8)	MOSFET turn off, V_{DRAIN} = 40 V to 360 V, FSL518H/A, I_{DRAIN} = 0.4 A FSL538H/A, I_{DRAIN} = 0.6 A	t_r		 26 35		ns
Drain−voltage Fall Time (Note 8)	MOSFET turn on, V_{DRAIN} = 360 V to 40 V, FSL518H/A, I_{DRAIN} = 0.4 A FSL538H/A, I_{DRAIN} = 0.6 A	t_f		 34 30		ns
Drain to Source Brakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	BV_{DSS}	800			V
Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V, T_J = 25°C V_{DS} = 640 V, V_{GS} = 0 V, T_J = 125°C	I_{DSS}			25 250	μA
V_{CC} Section						
Controller Turn−on Threshold Voltage	Voltage Increasing	$V_{CC-START}$	15	16	17	V
Under−voltage Lockout Thresold Voltage	Voltage Decreasing	$V_{CC-STOP}$	7	8	9	V
V_{CC} Regulation Voltage	During Start−up and Protection	$V_{CC-HVREG}$	9	10	11	V
Restart Time in Protection Mode (Note 9)		t_{AR}		800		ms
Built−in Soft−start Time		t_{SS}	7	10	13	ms
Oscillation Section						
Switching Frequency	V_{CC} = 14 V, V_{COMP} = 3.6 V, T_J = 25°C FSL5x8H FSL5x8A	f_S	 122 94	 130 100	 138 106	kHz
Switching Frequency Variation	T_J = −40 ~ 125°C	Δf_S		±5	±10	%
Frequency Modulation Range	V_{COMP} = 3.6 V	f_M		±6.5		kHz
Frequency Modulation Period	V_{COMP} = 3.6 V	T_{FM}		3.2		ms
Green−Mode Entry Frequency	V_{COMP} = 1.4 V FSL5x8H FSL5x8A	f_N		 115 89		kHz
Green−Mode Ending Frequency	V_{COMP} = 0.4 V	f_G	22	25	28	kHz
Frequency−limiting Voltage (Note 9)		V_{COMP-S}	3.4	3.6	3.8	V
Green−Mode Entry FB Voltage (Note 9)		V_{COMP-N}	1.2	1.4	1.6	V
Green−Mode Ending FB Voltage (Note 9)		V_{COMP-G}	0.35	0.4	0.45	V
Burst−Mode Section						
COMP−pin Threshold Voltage for Entering Burst Mode when Line Detection is Enabled	V_{LINE} in $V_{LINE-SET0}$ during t_{SET} V_{LINE} in $V_{LINE-SET1}$ during t_{SET} V_{LINE} in $V_{LINE-SET2}$ during t_{SET}	V_{BURL}	0.35 0.45 0.55	0.4 0.5 0.6	0.45 0.55 0.65	V
COMP−pin Threshold Voltage for Entering Burst Mode when Line Detection is Disabled	0.9 V < V_{LINE} < 1.2 V 1.2 V < V_{LINE} < 3.6 V	V_{BURL}	0.4 $A_{V-BURST} \times V_{LINE}$			V
COMP−pin Threshold Voltage for Leaving Burst Mode		V_{BURH}	V_{BURL} + 0.1			V
Control Section						
Maximum Duty Ratio	V_{COMP} = 3.6 V	D_{MAX}	68	75	82	%
COMP−pin Output High Voltage	COMP Pin Open	$V_{COMP-OPEN}$		5		V

ELECTRICAL CHARACTERISTICS (continued)
T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
COMP−pin Sourcing Current		I_{COMP}	70	100	125	μA
Transconductance of Internal Error Amplifier		G_M		300		μS
Current−sourcing capability of Internal Error Amplifier	$V_{FB} = V_{REF} - 1$ V	$I_{GM-SOURCE}$	60	90	120	μA
Current−sinking capability of Internal Error Amplifier	$V_{FB} = V_{REF} + 1$ V	$I_{GM-SINK}$	−60	−90	−120	μA
Reference Voltage to Regulate FB−pin Voltage		V_{REF}	2.45	2.5	2.55	V
Leading−edge Blanking Time of Internal SenseFET Current Signal (Note 9)		t_{LEB}		250		ns
Propagation Delay of Turning−off Power MOSFET (Note 9)		t_{PD}		100		ns
LINE Section						
Threshold to Enable Line Detection by Initial Voltage on LINE Pin before V_{CC} is charged to $V_{CC-START}$	$V_{LINE} > V_{LINE-DET}$	$V_{LINE-DET}$	0.15			V
Threshold to Enable Linear Burst Level Adjustment by Initial Voltage on LINE Pin before V_{CC} is charged to $V_{CC-START}$	$V_{LINE} < V_{LINE-ADJ}$	$V_{LINE-ADJ}$			0.05	V
Time Duration for Setting Burst−mode Level when Line Detection is Enabled (Note 9)		t_{SET}		100		μs
LINE−pin sourcing current for Detecting burst−setting zener voltage during t_{SET}	During t_{SET}, V_{CC} = 15 V, V_{LINE} = 10 V	I_{SET}	1.6	2.7	3.8	mA
Burst−setting Zener Voltage for Choosing Burst−mode Level 0	During t_{SET}	$V_{LINE-SET0}$	12.4			V
Burst−setting Zener Voltage for Choosing Burst−mode Level 1	During t_{SET}	$V_{LINE-SET1}$	9.3		10.6	V
Burst−setting Zener Voltage for Choosing Burst−mode Level 2	During t_{SET}	$V_{LINE-SET2}$			7.9	V
LINE−pin Sourcing Current for Setting Burst−mode Level When Line Detection is Disabled	V_{LINE} = 0 V before V_{CC} is charged to $V_{CC-START}$	I_{BURST}	9.4	10	10.6	μA
Line−pin Voltage to Burst−mode Level Attenuation when Line Detection is Disabled (Note 9)		$A_{V-BURST}$		1/3		V/V
Protections: Over−Voltage Protection (OVP)						
Over−Voltage Protection for V_{CC} pin		V_{CC-OVP}	23.0	24.5	26.0	V
Delay time for OVP (Note 9)		t_{D-OVP}		6.0		μs
Protections: Over−Load Protection (OLP)						
OLP−Triggering Threshold Voltage on COMP Pin		V_{OLP}	3.3	3.6	3.9	V
Deley Time of OLP	COMP > V_{OLP} after Soft−start Time	t_{D-OLP}	30	60	90	ms
Abnormal Over−Current Protection (AOCP)						
AOCP Monitoring duration after t_{LEB} (Note 9)		t_{AOCP}		150		ns
Threshold Drain Current for Triggering AOCP (Note 9)		I_{AOCP}		I_{LIM}		mA

ELECTRICAL CHARACTERISTICS (continued)
T_J = −40 to +125°C and V_{CC} = 14 V unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Number of pulse for AOCP to skip switching operation for $N_{AOCP-HALT}$ times (Note 9)	See Figure 29	$N_{AOCP-TRIG}$		2		times
Number of skipped pulses after $N_{AOCP-TRIG}$ is satisfied (Note 9)	See Figure 29	$N_{AOCP-HALT}$		7		times
Times of satisfying $N_{AOCP-TRIG}$ to trigger auto−restart procedure (Note 9)	See Figure 29	$N_{AOCP-COUNT}$		3		times
Protections: Line Detection (BI, BO, LOVP)						
Brown−out (BO) Threshold Voltage on LINE Pin		$V_{LINE-BO}$	0.80	0.85	0.90	V
Brown−in (BI) Threshold Voltage on LINE Pin		$V_{LINE-BI}$	0.95	1	1.05	V
Hysteresis between BI and BO	$V_{LINE-BI} - V_{LINE-BO}$	$\Delta V_{LINE-BIBO}$	0.09	0.15	0.21	V
Brown−out Delay Time (Note 9)		t_{BO}		100		ms
Line−input Over−voltage Protection (LOVP) Triggering Level		$V_{LINE-OVP}$	4.3	4.5	4.7	V
Recovering Level for LOVP		$V_{LINE-OVP-RECOVER}$	4.2	4.4	4.6	V
Hysteresis of Triggering and Recovering of LOVP	$V_{LINE-OVP} - V_{LINE-OVP-RECOVER}$	$\Delta V_{LINE-OVP}$	0.05	0.1	0.15	V
LOVP Delay Time (Note 9)		$t_{LINE-OVP}$		2		μs
Protections: Thermal Shutdown						
Junction Temperature to Trigger Thermal Shutdown (Note 9)		T_{SD}		147		°C
Junction Temperature for Resuming from Thermal Shutdown (Note 9)		$T_{RECOVER}$		95		°C
Total Device Section						
Operating Supply Current, (Control Part in Burst Mode)	V_{COMP} = 0 V, V_{DRAIN} = 12 V, R_{DRAIN} = 500 Ω	I_{OP1}		0.9	1.2	mA
Operating Supply Current	V_{COMP} = 3.2 V, V_{DRAIN} = 12 V	I_{OP2}		1.7	2.0	mA
V_{CC}−pin current at startup condition	V_{CC} = 14.9 V, V_{COMP} = 3.6 V (Before V_{CC} Reaches $V_{CC-START}$)	I_{START}		170	200	μA
Startup Charging Current (JFET saturation current)	V_{CC} = 0 V, V_{DRAIN} = 40 V	I_{CH}	1.4	4	TBD	mA
Minimum DRAIN−pin Voltage to Start Operation (Note 10)	$V_{CC} = V_{COMP}$ = 0 V	V_{START}			40	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. Evaluated in the typical flyback application board, T_A = 25°C
9. This parameter is not tested in production, but verified by design/characterization.
10. It is guaranteed that I_{CH} can charge V_{CC} up to $V_{CC-START}$ if drain−pin voltage is higher than V_{START}.

TYPICAL CHARACTERISTICS

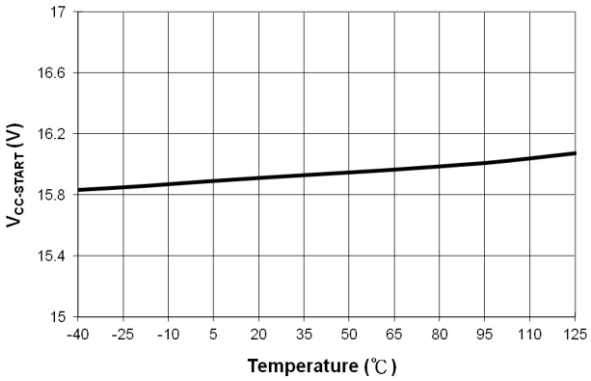


Figure 3. $V_{CC–START}$ vs. Temperature

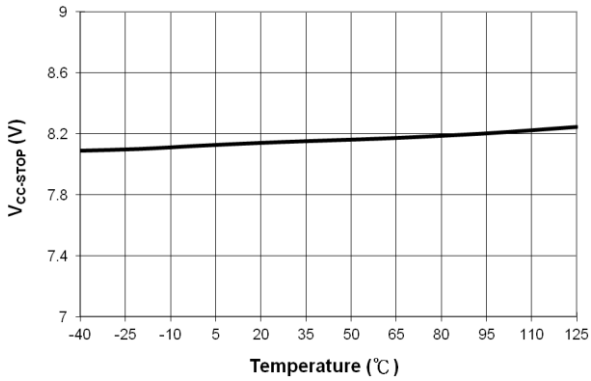


Figure 4. $V_{CC–STOP}$ vs. Temperature

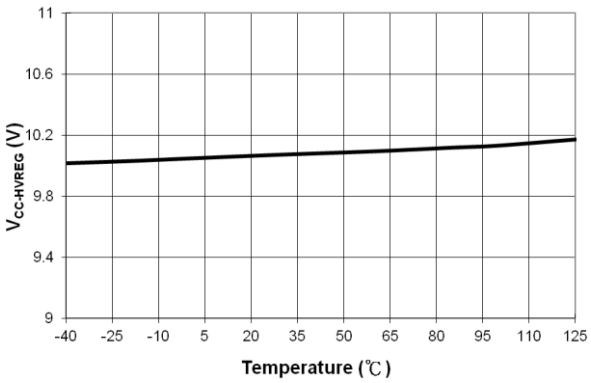


Figure 5. $V_{CC–HVREG}$ vs. Temperature

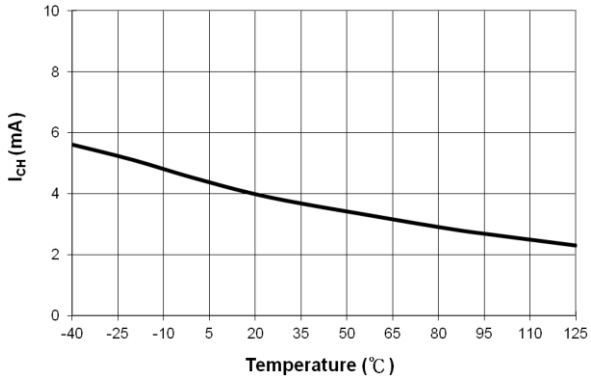


Figure 6. I_{CH} vs. Temperature

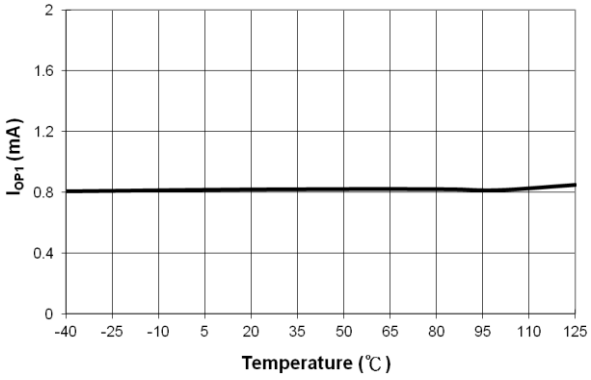


Figure 7. FSL5x8H I_{OP1} vs. Temperature

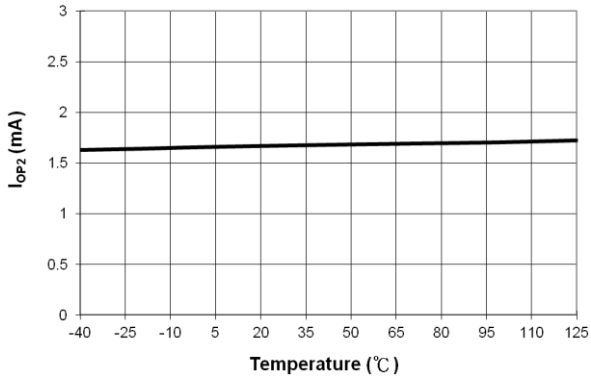


Figure 8. FSL5x8H I_{OP2} vs. Temperature

TYPICAL CHARACTERISTICS

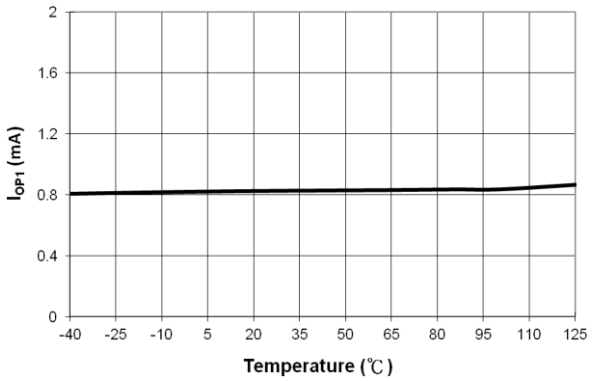


Figure 9. FSL5x8A I_{OP1} vs. Temperature

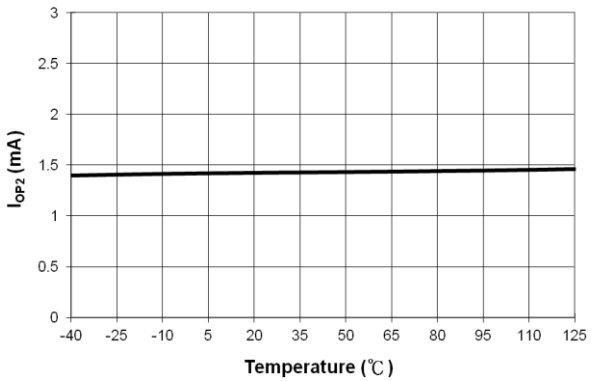


Figure 10. FSL5x8A I_{OP2} vs. Temperature

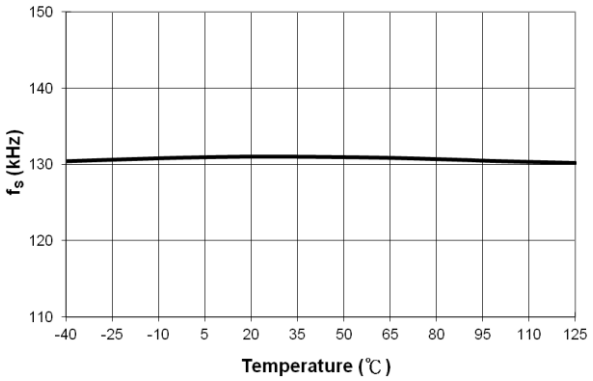


Figure 11. FSL5x8H f_S vs. Temperature

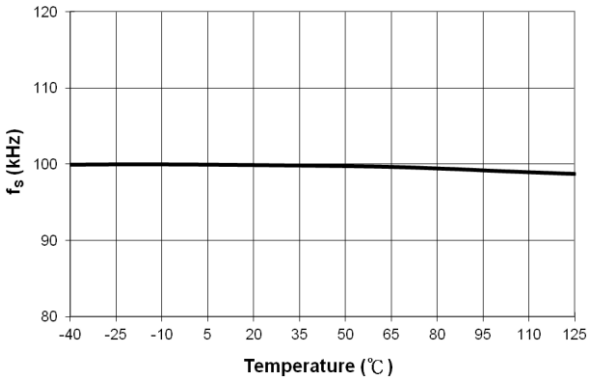


Figure 12. FSL5x8A f_S vs. Temperature

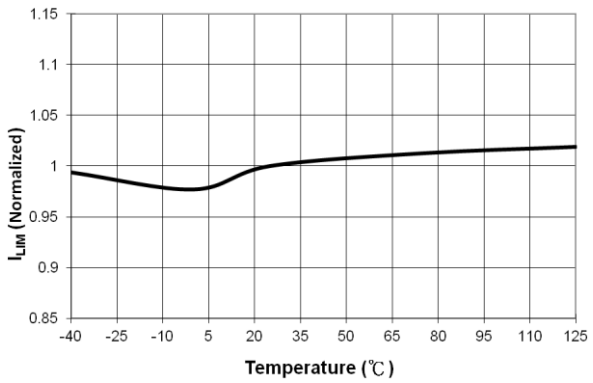


Figure 13. FSL518H I_{LIM} (Normalized to 25°C) vs. Temperature

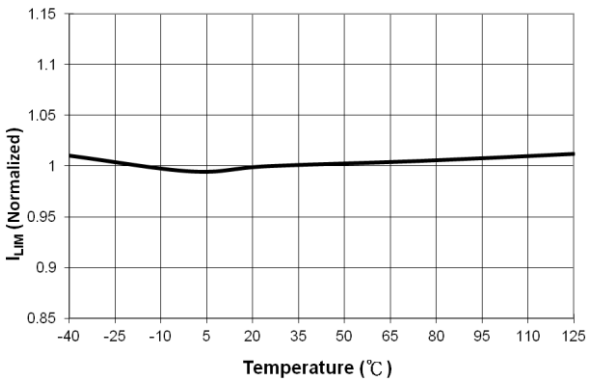


Figure 14. FSL518A I_{LIM} (Normalized to 25°C) vs. Temperature

TYPICAL CHARACTERISTICS

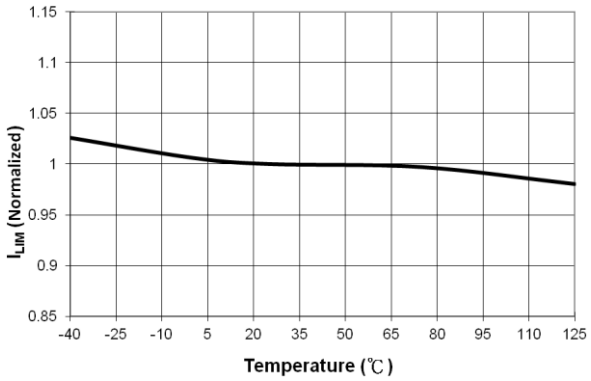


Figure 15. FSL538H I_{LIM} (Normalized to 25°C) vs. Temperature

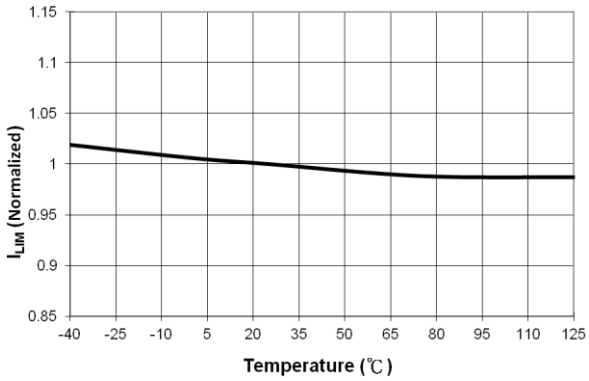


Figure 16. FSL538A I_{LIM} (Normalized to 25°C) vs. Temperature

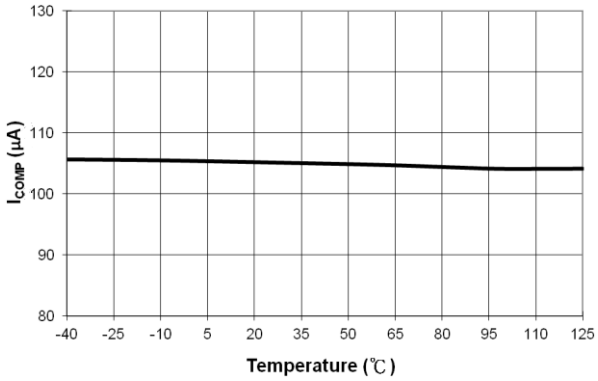


Figure 17. I_{COMP} vs. Temperature

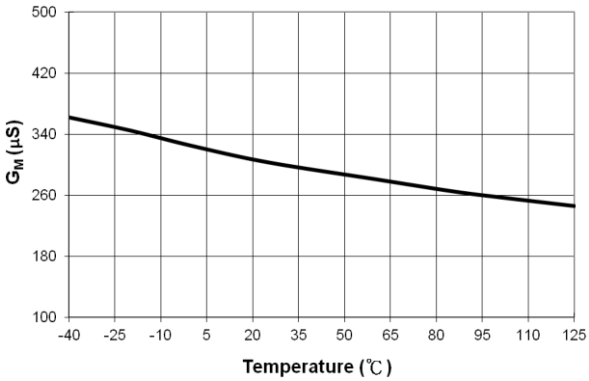


Figure 18. G_M vs. Temperature

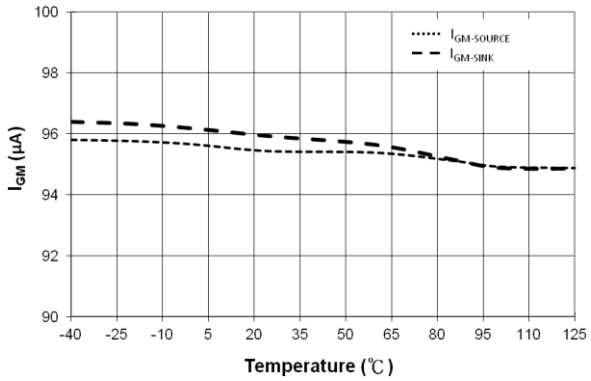


Figure 19. I_{GM} vs. Temperature

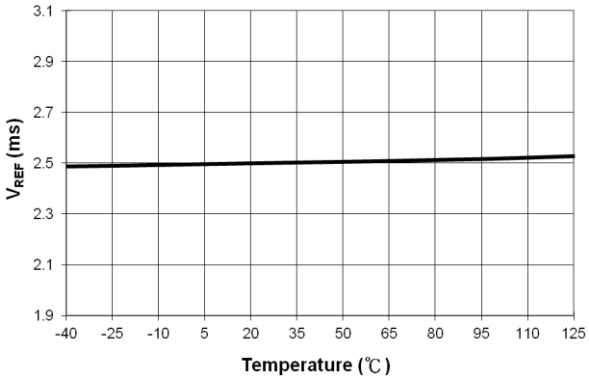


Figure 20. V_{REF} vs. Temperature

TYPICAL CHARACTERISTICS

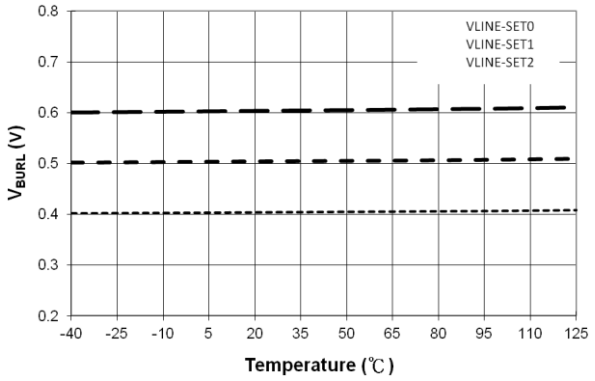


Figure 21. V_{BURL} vs. Temperature

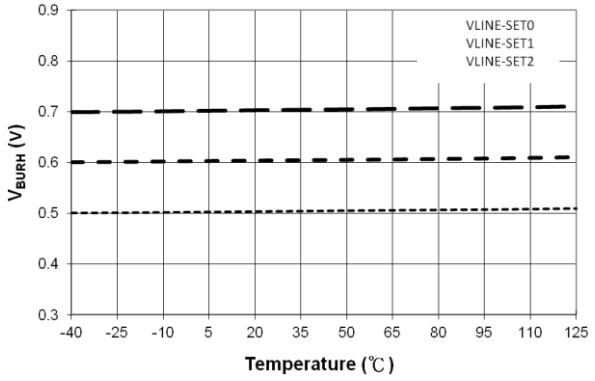


Figure 22. V_{BURH} vs. Temperature

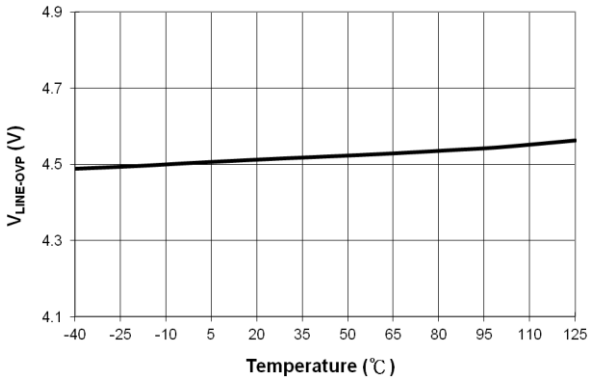


Figure 23. $V_{LINE–OVP}$ vs. Temperature

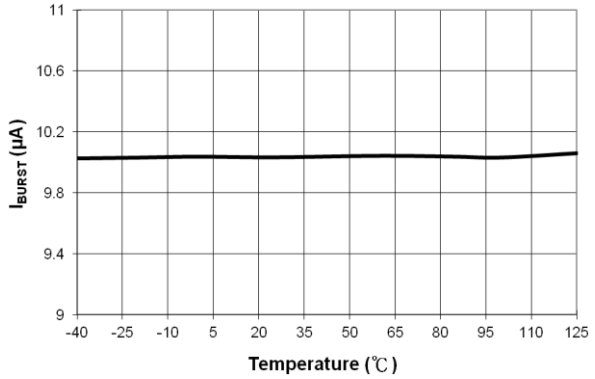


Figure 24. I_{BURST} vs. Temperature

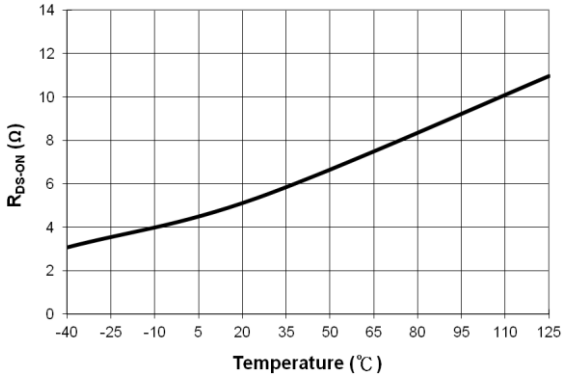


Figure 25. FSL518H/A $R_{DS(ON)}$ vs. Temperature

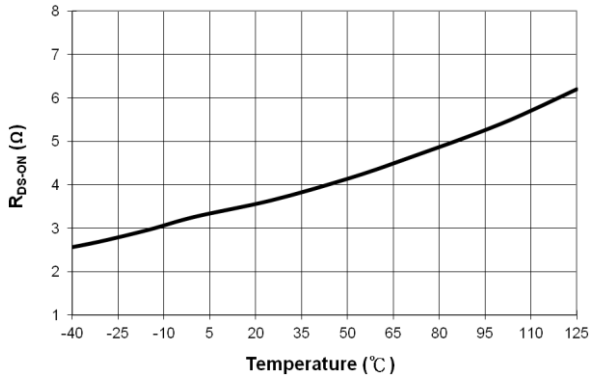


Figure 26. FSL538H/A $R_{DS(ON)}$ vs. Temperature

TYPICAL CHARACTERISTICS

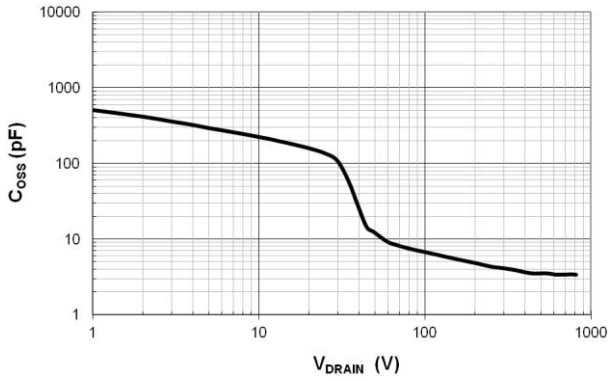


Figure 27. FSL518H/A C_{OSS} vs. V_{DRAIN}

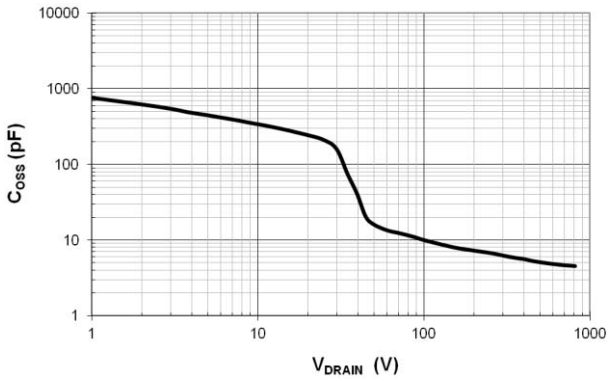


Figure 28. FSL538H/A C_{OSS} vs. V_{DRAIN}

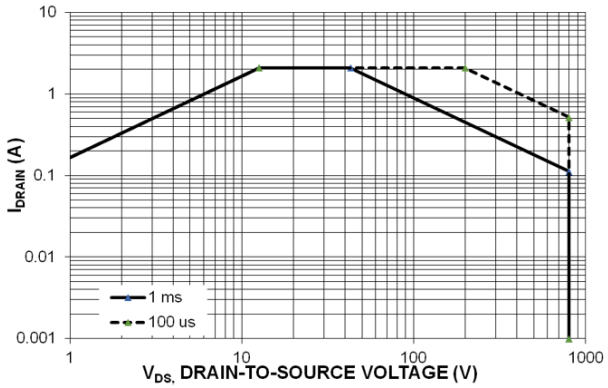


Figure 29. FSL518H/A Safe Operating Range

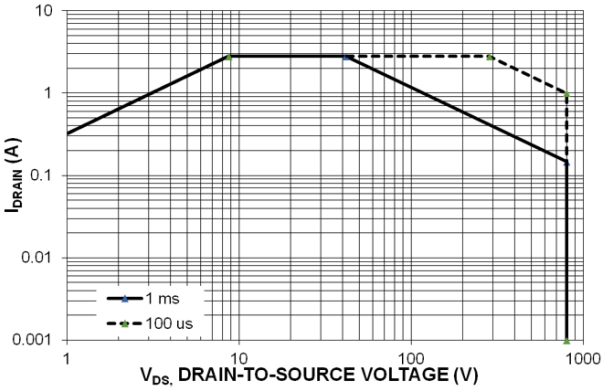


Figure 30. FSL518H/A Safe Operating Range

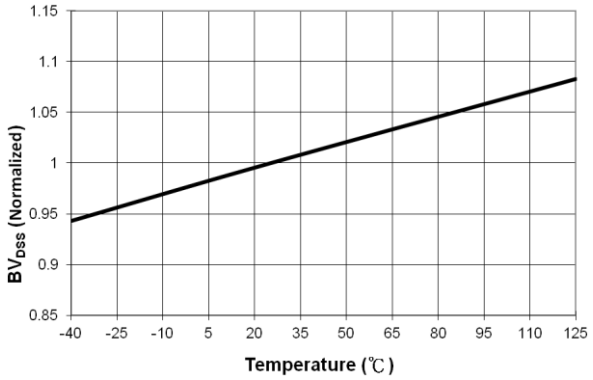


Figure 31. FSL518H/A BV_{DSS} vs. Temperature

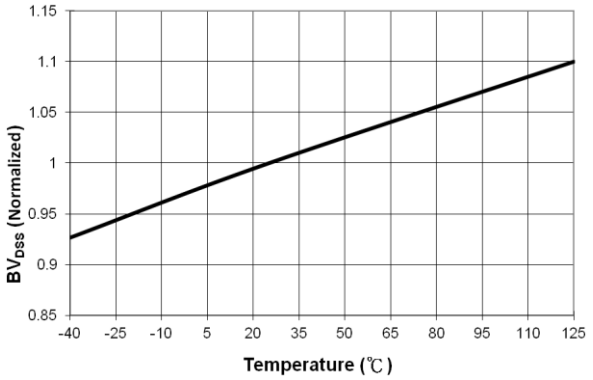


Figure 32. FSL538H/A BV_{DSS} vs. Temperature

TYPICAL CHARACTERISTICS

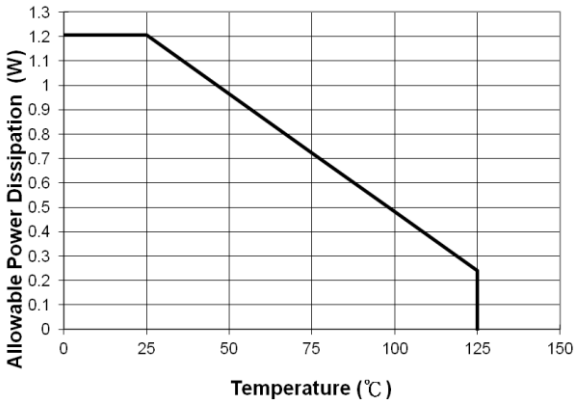


Figure 33. FSL5x8H/A Power Dissipation vs. Temperature

APPLICATION INFORMATION

HV Current Source for V_{CC} Start up and V_{CC} Regulation

An internal current source utilizes voltage on DRAIN pin to charge capacitor on V_{CC} pin. This current source is actived for both V_{CC} start−up and provide operating current when V_{CC} is lower than $V_{CC-HVREG}$. Thanks to V_{CC} start−up function, no external start−up circuitry is needed. The start−up current source is disabled when V_{CC} voltage is charged to $V_{CC-START}$.

V_{CC} regulation also helps avoiding start−up failure during soft−start and keeps FSL5x8 operating for counting auto−restart delay time (t_{AR}) in protection mode, as illustrated in Figure 34. It also enables the use of smaller capacitance for V_{CC} biasing. The V_{CC} regulation is not functional when the external bias is higher than $V_{CC-HVREG}$.

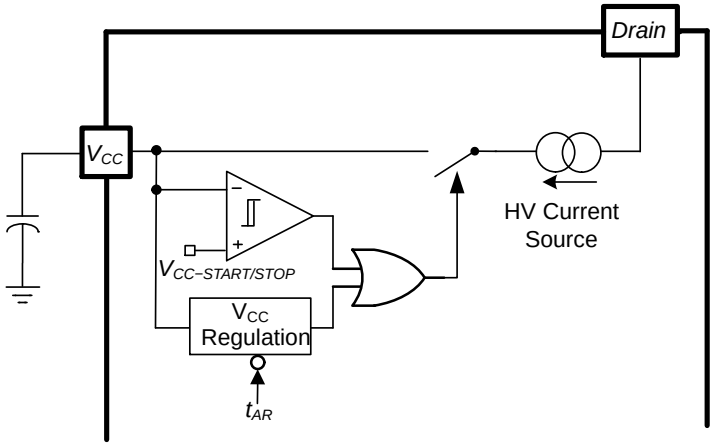


Figure 34. V_{CC} Start Up and V_{CC} Regulation

Initial Setting for Line Detection and Adjusting Burst−Mode Operation

LINE pin is used for both input−voltage detection and burst−mode setting. When a voltage divider connects input bulk capacitor to LINE pin, a zener diode connected to LINE pin can be used to set level of burst−mode operation. If there is no voltage divider, the line−detection function is disabled and burst−mode operation level is set linearly by simply connecting a resistor between LINE pin and GND pin. In order to avoid interference from switching noise, connecting a ceramic capacitor to LINE pin is recommended.

When line detection is enabled, voltage on LINE pin is monitored to offer brown−in (BI), brown−out (BO), and line over−voltage protections (LOVP).

When line detection is disabled, burst−mode operation can be settled by an external resister connecting between LINE and GND pins. With I_{BURST}, V_{LINE} reflects resistance of the external resistor. FSL5x8 adjusts burst−mode operation threshold based on real−time V_{LINE} level.

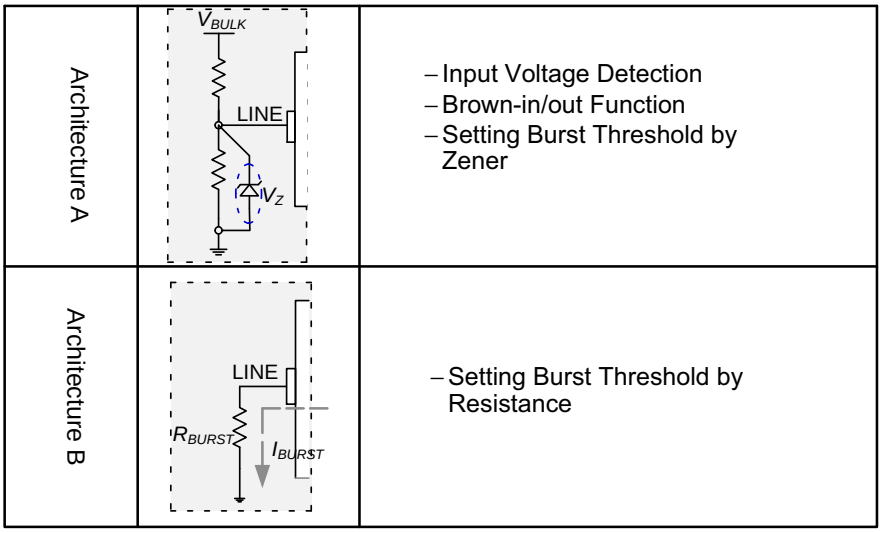


Figure 35. Architecture of LINE−pin Setting

BURST THRESHOLD SETTING TABLE

	Line Detection Enable/Disable	V_{LINE} (V)	V_{BURH}/V_{BURL} (V)
Architecture A	Enable	$12.4\ V < V_Z$	0.5/0.4
		$9.3\ V < V_Z < 10.6\ V$	0.6/0.5
		$V_Z < 7.9\ V$	0.7/0.6
Architecture B	Disable	$0.9\ V < I_{BURST} \times R_{BURST} < 1.2\ V$	0.5/0.4
		$1.2\ V < I_{BURST} \times R_{BURST} < 3.6\ V$	$A_{V-BURST} \times (I_{BURST} \times R_{BURST}) + 0.1$ /$A_{V-BURST} \times (I_{BURST} \times R_{BURST})$

Initial Setting for Configuration of Feedback Regulation

Being simultaneous to the initial setting of LINE−pin functions, configuration of feedback regulation is also decided based on peripheral circuitry to FB pin. If a voltage divider is connected to FB pin, the IC will then do output regulation by regulating voltage on FB pin through internal transconductance error amplifier.

In the case that external error amplifier is used for output regulation, simply connect FB pin to GND pin. The external output regulation circuitry then sinks current with value around I_{COMP} (100 μA) from COMP pin to adjust duty cycle of PWM operation.

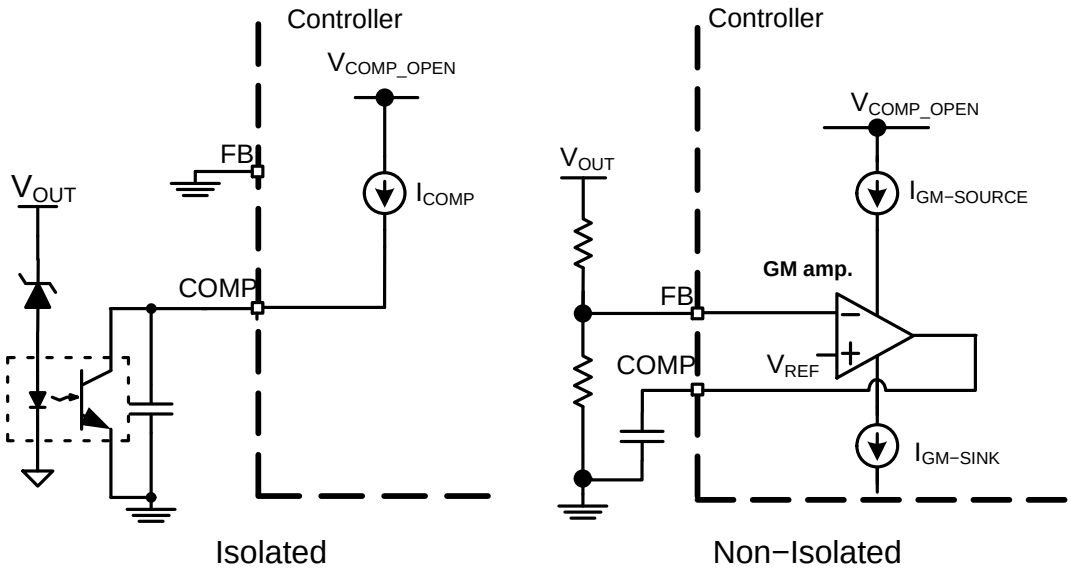


Figure 36. Isolated vs. Non−Isolated Application

Advanced Soft−Start Operation

After V_{CC} is charged to $V_{CC-START}$ and all settings about LINE−pin and FB−pin functions are done, switching operation can be initiated with a soft−start period. The typical soft−start time is 10 ms. During soft−start period, both drain current and switching frequency limits are settled to their target value gradually. Thus, rising waveform of output voltage will be smooth and stresses on semiconductor devices will be under control.

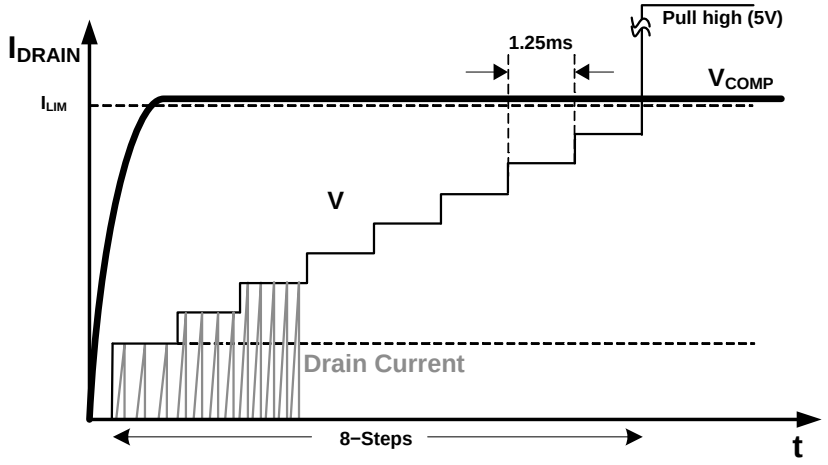


Figure 37. Soft−Start Operation

Main Control Frequency Reduction

Operating frequency of switching operation is modulated by COMP−pin voltage, V_{COMP}. When V_{COMP} drops, operating frequency will also decrease. That help to reduce switching losses and improve light−load efficiency. The operating frequency will not be decreased below 22−kHz so acoustic noise can be avoided.

PWM Control

The FSL5x8 applies peak−current mode pulse−width modulation (PWM) to regulate output of power converters. Duty cycle of PWM signal is based on COMP−pin voltage and drain current of power MOSFET. The COMP−pin voltage can be controlled by either built−in error amplifier or external current−sinking elements such as opto coupler or operational amplifier.

Slope Compensation

Built−in slope compensation is added into the PWM procedure when duty cycle is higher than 45%. It helps to avoid sub−harmonic oscillation of peak−current control.

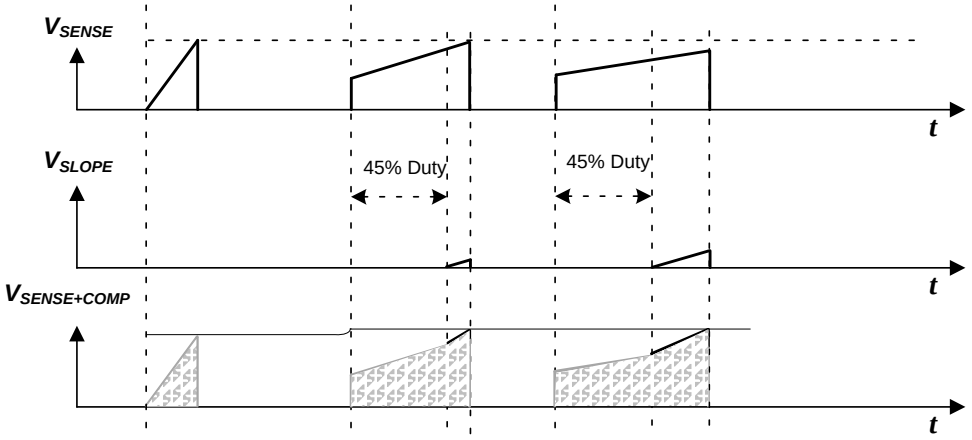


Figure 38. Slope Compensation

Burst Mode Operation

As loading of the power converter decreases, V_{COMP} decreases, thus reducing switching frequency of the oscillator. When minimum operating frequency is reached, to further reduce delivered output power, the device goes into burst mode. In burst mode, switching operation is halted when V_{COMP} is lower than V_{BURL} and resumed when V_{COMP} is higher than V_{BURH}. By skipping un−needed switching cycles, the FSL5x8 drastically reduced the power wasted during light load conditions.

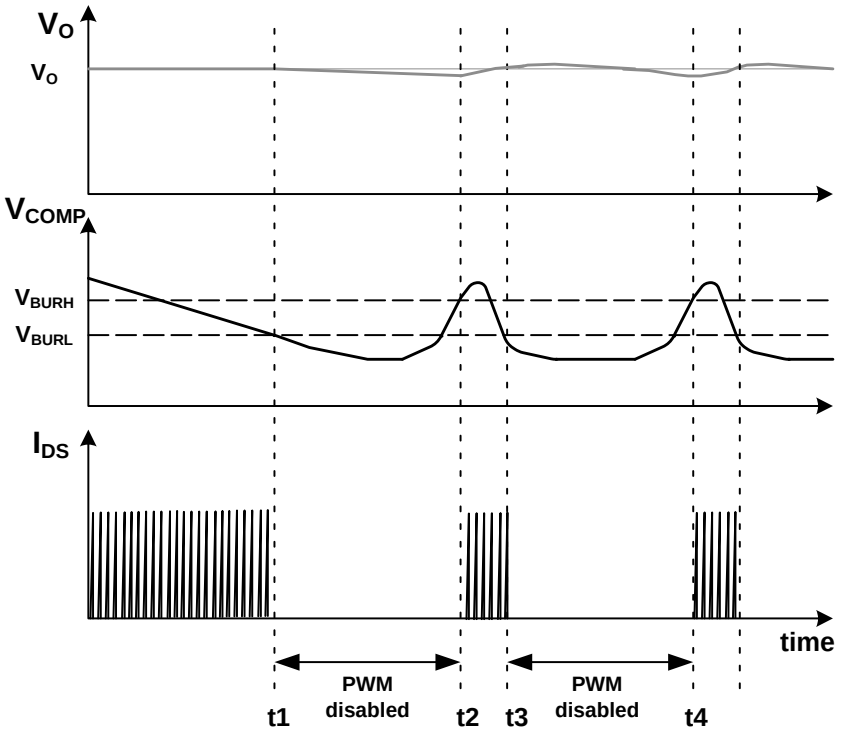


Figure 39. Burst−Mode Behavior

V_{BURL} and V_{BURH} can be adjusted through LINE−pin connection as mentioned in *"Initial Setting for Line Detection"* section. It is provided for tuning light load efficiency and acoustic noise. By adjusting V_{BURL}, minimum peak value of drain current of each switching cycle is adjusted as described in Equation 1.

$$I_{DRAIN.PEAK.BURL} = \frac{V_{BURL}}{4 \cdot 0.6} \cdot I_{LIM} \quad \text{(eq. 1)}$$

Line Compensation

Propagation delay in turning off power MOSFET makes drain current exceed current limit by an amount that related to slope of drain current. The device adjusts its internal current−limit reference voltage according to duty cycle to compensate the effect of propagation delay. As a result, the delivered output power is kept under control across different input voltage conditions.

Protections

Over Load Protection (OLP)

Figure 40 shows the timing chart of triggering OLP. V_{COMP} will be pulled higher than V_{OLP} when drain current hits current limit and switching frequency operates at its highest range. If the condition continues for t_{D-OLP}, OLP will be triggered.

The figure also shows typical protection mode behavior of the IC. Switching operation is stopped when protection is triggered. V_{CC} is then supplied by V_{CC} regulation for a time period t_{AR} to hinder the IC from restart. The t_{AR} can extend restart time to reduce average power dissipation when fault condition is still present. After t_{AR}, V_{CC} drops to $V_{CC-STOP}$ to reset and restart the controller.

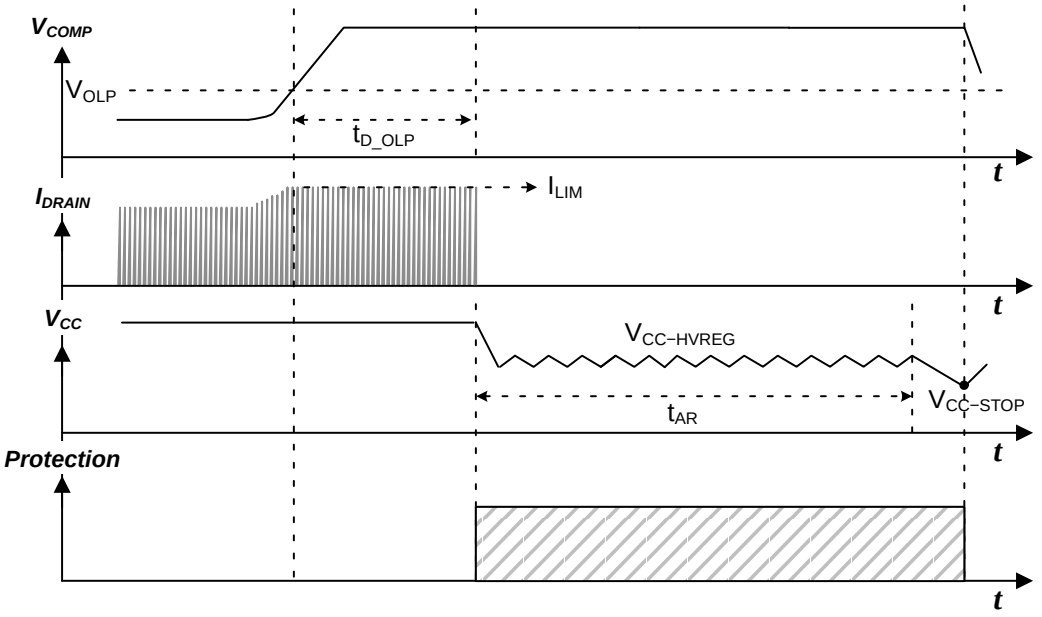


Figure 40. Timing Chart of OLP

Over Voltage Protection (OVP)

A malfunction of voltage−feedback circuitry could result in excessive energy delivered to output by the power converter. Output voltage and V_{CC} would increase under such conditions.

When When V_{CC} rises above V_{CC-OVP}, protection will be triggered after short delay time, t_{D-OVP}.

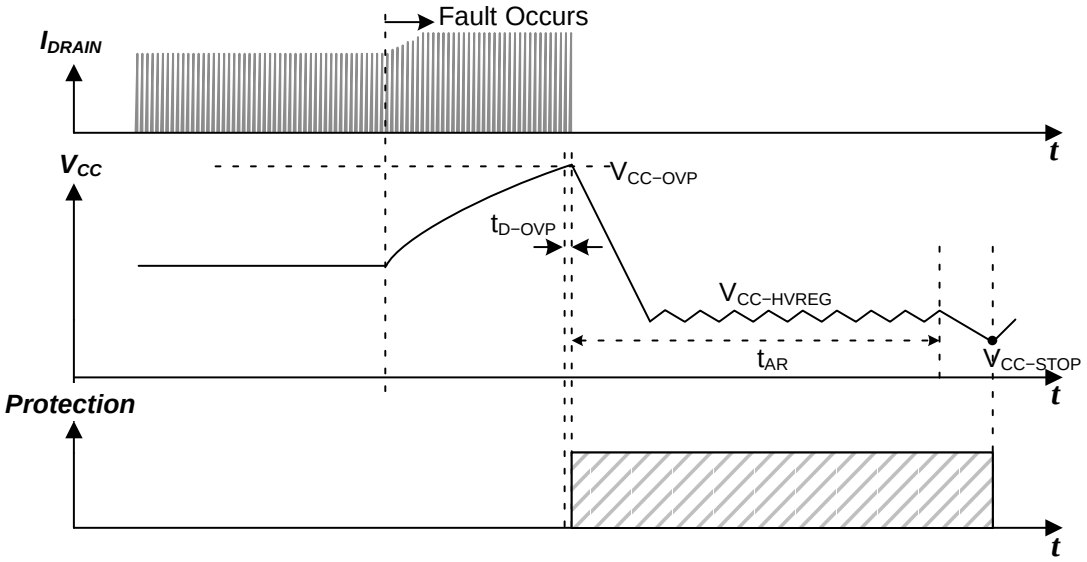


Figure 41. Timing Chart of OVP

Abnormal Over−Current Protection (AOCP)

When the secondary−side rectifier diodes or the transformer windings are shorted, a steep drain current with extremely high di/dt will flow through the MOSFET during the minimum turn−on time. In that condition, each switching cycle makes very high current stress to power MOSFET. The controller monitors current−sense signal within a limited leading−edge time duration t_{LEB} + t_{AOCP} of each switching cycle. If current−sensing signal exceeds current limit for a few consecutive switching cycles, $N_{AOCP-TRIG}$, GATE signal will stop switching for number of pulses, $N_{AOCP-HALT}$. If the faulty condition is met for three times, $N_{AOCP-COUNT}$, the controller goes into protection mode.

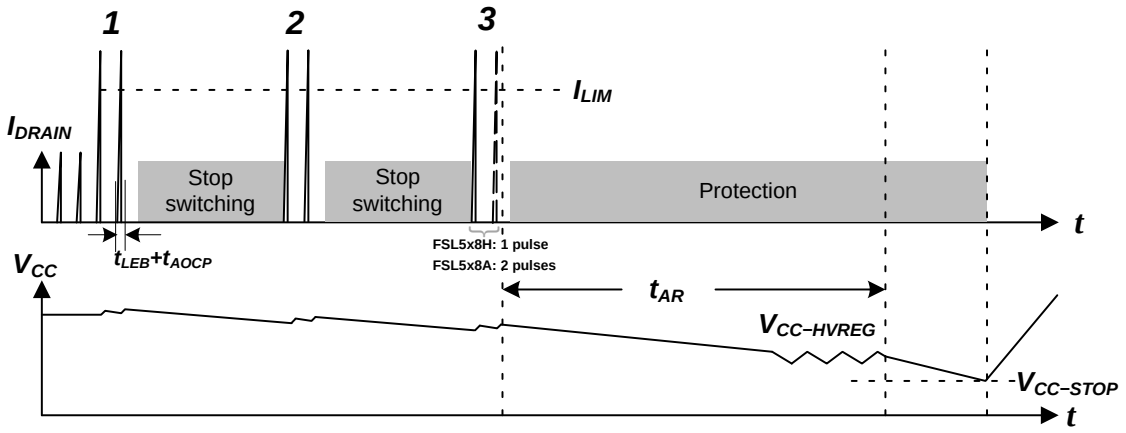


Figure 42. Timing Chart of AOCP

Brown In/Out (BI/BO) and Line Over−Voltage Protection (LOVP)

When voltage divider is connected between LINE pin and input bulk capacitor, line−detection function is enabled and V_{LINE} reflects peak of AC input voltage. If V_{LINE} is below $V_{LINE-BI}$ after initial setting, switching operation will not be initiated until V_{LINE} reaches $V_{LINE-BI}$. If V_{LINE} is lower than $V_{LINE-BO}$ for t_{BO} during normal operation, brown−out will be triggered and the controller will go into protection mode. If V_{LINE} is higher than $V_{LINE-OVP}$, switching operation is halted until V_{LINE} drops down below $V_{LINE-OVP-RECOVER}$. Both recovering from LOVP or after BI, the controller performs a soft start sequence.

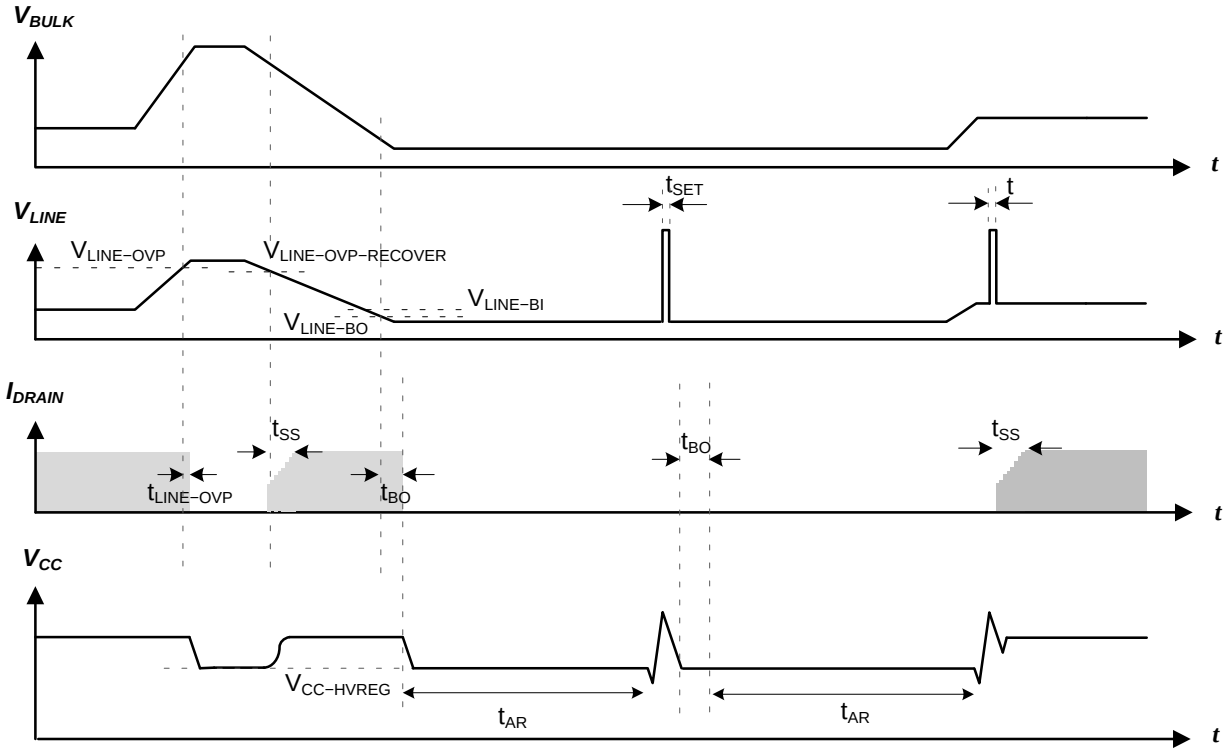


Figure 43. LOVP, Brown−out and Brown−in Behavior

Thermal Shutdown (TSD)

Since SenseFET and controller are integrated on the same package, it is easier for the controller to detect temperature inside the package of the controller. When junction temperature exceeds shut−down temperature, T_{SD}, thermal shutdown is activated. The controller will go into protection mode after thermal shutdown. If temperature is not lower than $T_{RECOVER}$, switching operation will not be resumed.

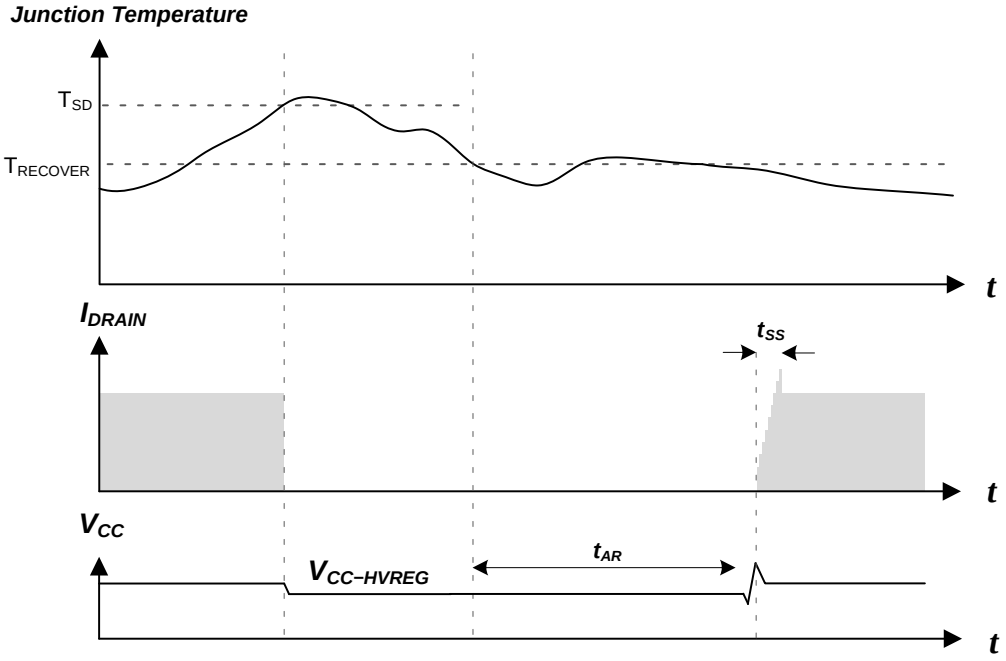


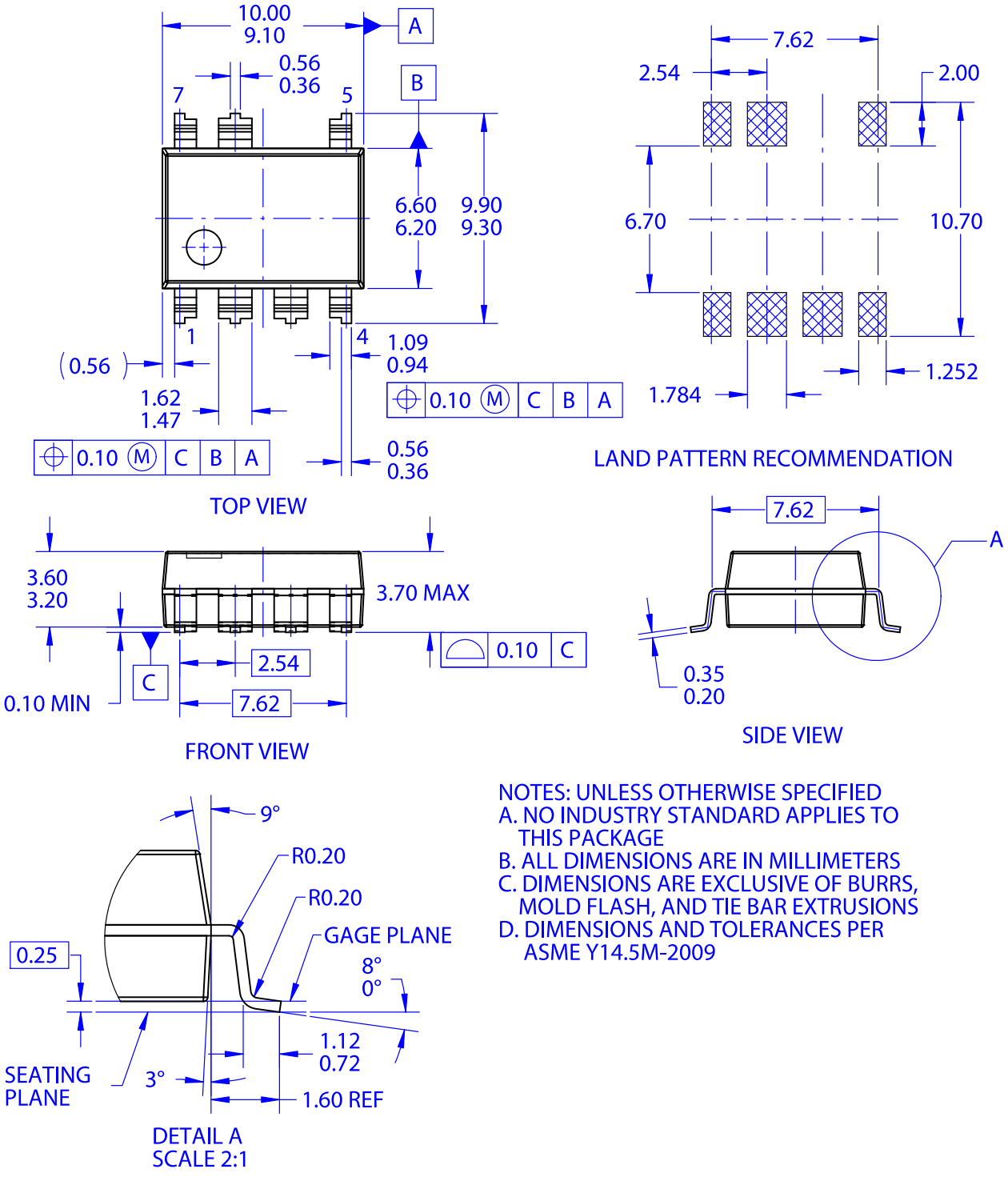
Figure 44. Timing Chart of TSD

ORDERING INFORMATION

Device	Current Limit (A)	$R_{DS.ON,max}$ (Ω)	Package	Shipping
FSL518HPG	0.46	8.0	PDIP−7 (Pb-Free)	Tube
FSL518HPLR2G	0.46	8.0	PDIP7 MINUS PIN 6 GW (Pb-Free)	Tape & Reel
FSL518APG	0.61	8.0	PDIP−7 (Pb-Free)	Tube
FSL518ALR2G	0.61	8.0	PDIP7 MINUS PIN 6 GW (Pb-Free)	Tape & Reel
FSL538HPG	0.66	4.3	PDIP−7 (Pb-Free)	Tube
FSL538HPLR2G	0.66	4.3	PDIP7 MINUS PIN 6 GW (Pb-Free)	Tape & Reel
FSL538APG	0.86	4.3	PDIP−7 (Pb-Free)	Tube
FSL538ALR2G	0.86	4.3	PDIP7 MINUS PIN 6 GW (Pb-Free)	Tape & Reel

PACKAGE DIMENSIONS

PDIP7 MINUS PIN 6 GW
CASE 707AA
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED
A. NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE
B. ALL DIMENSIONS ARE IN MILLIMETERS
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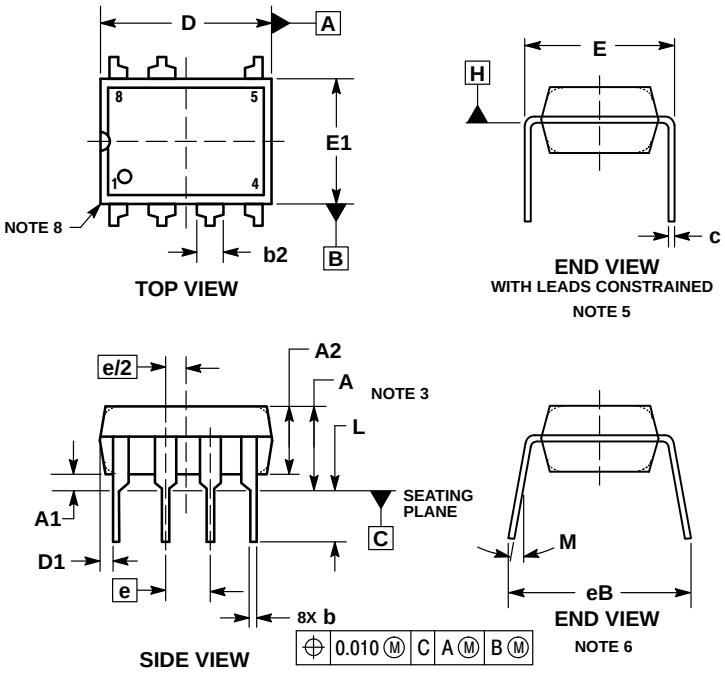
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009

PACKAGE DIMENSIONS

PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	−−−−	0.210	−−−	5.33
A1	0.015	−−−−	0.38	−−−
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	−−−−	0.13	−−−
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	−−−−	0.430	−−−	10.92
L	0.115	0.150	2.92	3.81
M	−−−−	10°	−−−	10°

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