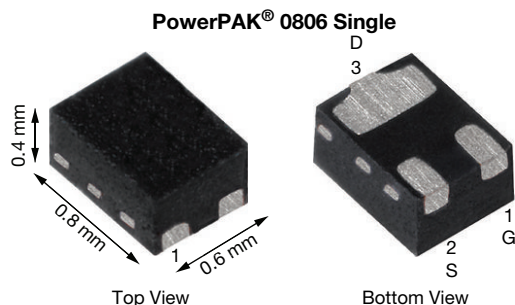


N-Channel 12 V (D-S) MOSFET



FEATURES

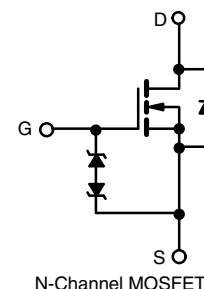
- TrenchFET® power MOSFET
- Ultra small 0.8 mm x 0.6 mm outline
- Ultra thin 0.4 mm max. height
- Typical ESD protection 1500 V (HBM)
- 1.2 V rated $R_{DS(on)}$
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch
- High speed switching
- DC/DC converters
- Battery-operated and mobile devices



PRODUCT SUMMARY	
V_{DS} (V)	12
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.34
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.4
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 1.8$ V	0.55
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 1.5$ V	1.2
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 1.2$ V	2.5
Q_g typ. (nC)	0.47
I_D (A)	0.5 ^{a, f}
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK 0806
Lead (Pb)-free and halogen-free	SiUD412ED-T1-GE3

Note

- The lead finish is NiPdAu and classed as E4 finish

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	12	V
Gate-source voltage	V_{GS}	± 5	
Continuous drain current / $T_J = 150^\circ\text{C}$	I_D	$T_A = 25^\circ\text{C}$	0.5 ^{a, f}
		$T_A = 70^\circ\text{C}$	0.5 ^{a, f}
		$T_A = 25^\circ\text{C}$	0.5 ^b
		$T_A = 70^\circ\text{C}$	0.5 ^b
Pulsed drain current ($t = 100 \mu\text{s}$)	I_{DM}	1.5	A
Continuous source-drain diode current	I_S	$T_A = 25^\circ\text{C}$	0.5 ^{a, f}
		$T_A = 70^\circ\text{C}$	0.37 ^b
Maximum power dissipation	P_D	$T_A = 25^\circ\text{C}$	1.25 ^a
		$T_A = 70^\circ\text{C}$	0.8 ^a
		$T_A = 25^\circ\text{C}$	0.37 ^b
		$T_A = 70^\circ\text{C}$	0.24 ^b
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, d}	R_{thJA}	80	100	$^\circ\text{C}/\text{W}$
Maximum junction-to-ambient ^{b, e}	R_{thJA}	265	335	

Notes

- Surface mounted on 1" x 1" FR4 board with full copper, $t = 5$ s
- Surface mounted on 1" x 1" FR4 board with minimum copper, $t = 5$ s
- Refer to IPC / JEDEC® (J-STD-020), no manual or hand soldering
- Maximum under steady state conditions is 135 $^\circ\text{C}/\text{W}$
- Maximum under steady state conditions is 400 $^\circ\text{C}/\text{W}$
- Package limited



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	12	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	9	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-1	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.35	-	0.9	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V	-	-	± 10	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 12 V, V _{GS} = 0 V	-	-	1	
		V _{DS} = 12 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	1	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 0.5 A	-	0.27	0.34	Ω
		V _{GS} = 2.5 V, I _D = 0.2 A	-	0.31	0.4	
		V _{GS} = 1.8 V, I _D = 0.1 A	-	0.37	0.55	
		V _{GS} = 1.5 V, I _D = 0.1 A	-	0.42	1.2	
		V _{GS} = 1.2 V, I _D = 0.05 A	-	0.55	2.5	
Forward transconductance ^a	g _{fs}	V _{DS} = 6 V, I _D = 0.5 A	-	1.6	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 6 V, V _{GS} = 0 V, f = 1 MHz	-	21	-	pF
Output capacitance	C _{oss}		-	13	-	
Reverse transfer capacitance	C _{rss}		-	7	-	
Total gate charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 0.5 A	-	0.47	0.71	nC
Gate-source charge	Q _{gs}	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 0.5 A	-	0.04	-	
Gate-drain charge	Q _{gd}		-	0.09	-	
Gate resistance	R _g	f = 1 MHz	3	15	30	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 6 V, R _L = 12 Ω, I _D ≅ 0.5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	2	5	ns
Rise time	t _r		-	20	40	
Turn-off delay time	t _{d(off)}		-	17	35	
Fall time	t _f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _A = 25 °C	-	-	0.5 ^c	A
Pulse diode forward current	I _{SM}		-	-	1.5	
Body diode voltage	V _{SD}	I _S = 0.5 A, V _{GS} = 0 V	-	0.7	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 0.5 A, di/dt = 100 A/μs, T _J = 25 °C	-	15	30	ns
Body diode reverse recovery charge	Q _{rr}		-	3	6	nC
Reverse recovery fall time	t _a		-	12.5	-	ns
Reverse recovery rise time	t _b		-	2.5	-	

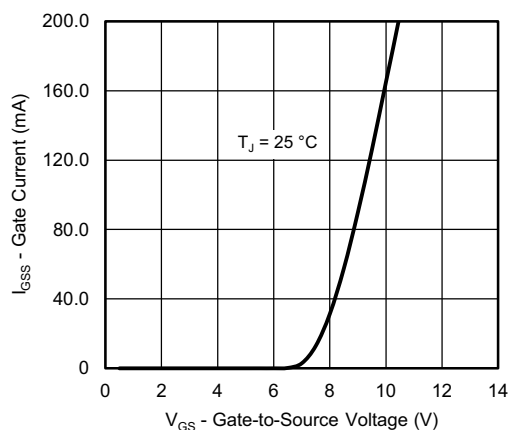
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Surface mounted on 1" x 1" FR4 board with full copper, $t = 5\text{ s}$

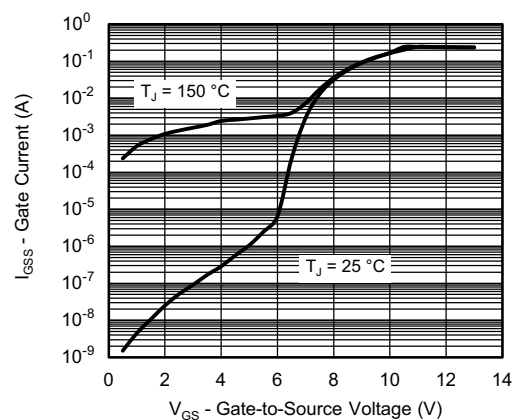
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



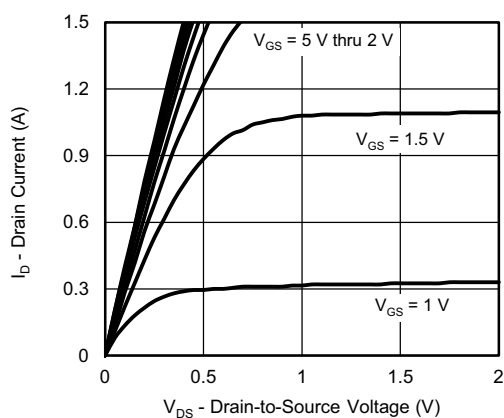
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



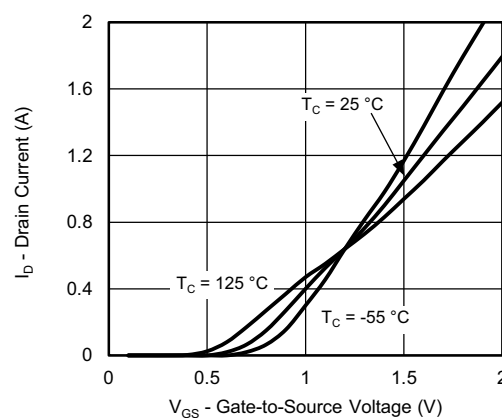
Gate-Current vs. Gate-Source Voltage



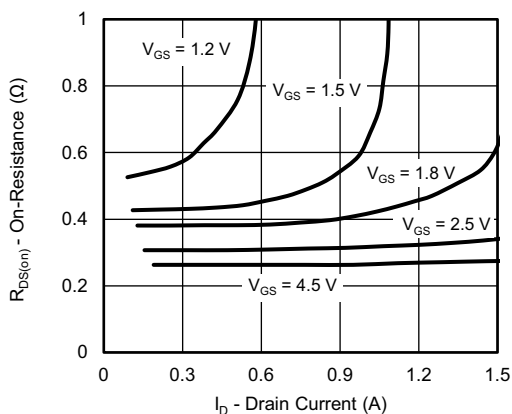
Gate-Current vs. Gate-Source Voltage



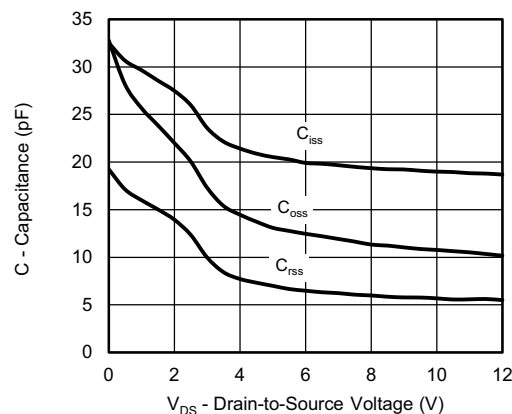
Output Characteristics



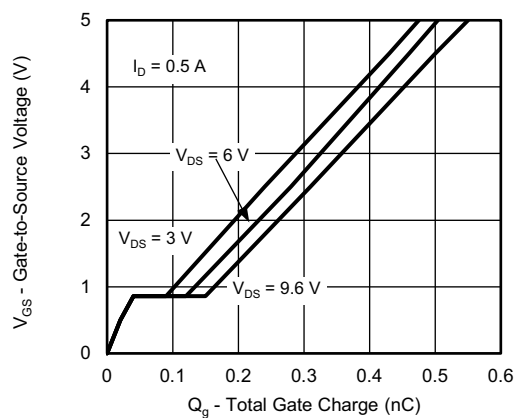
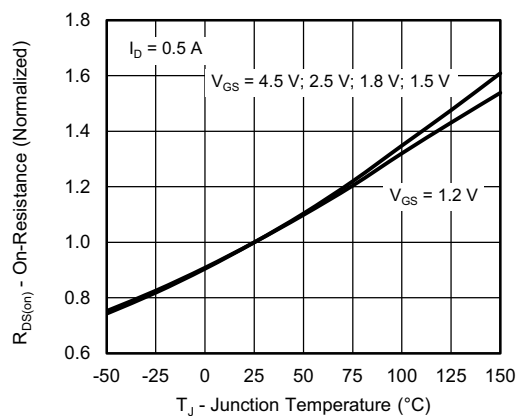
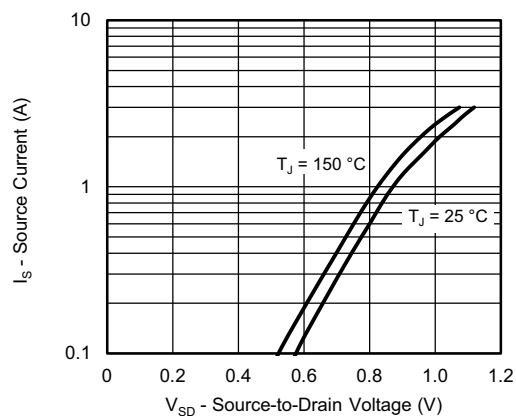
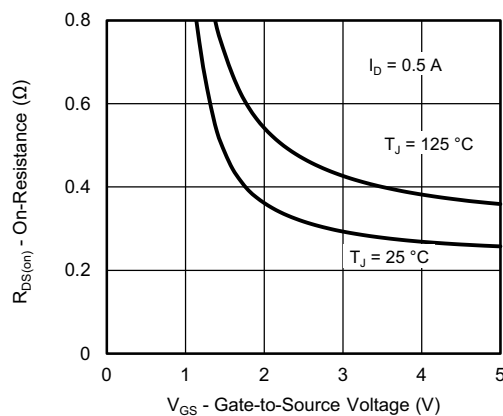
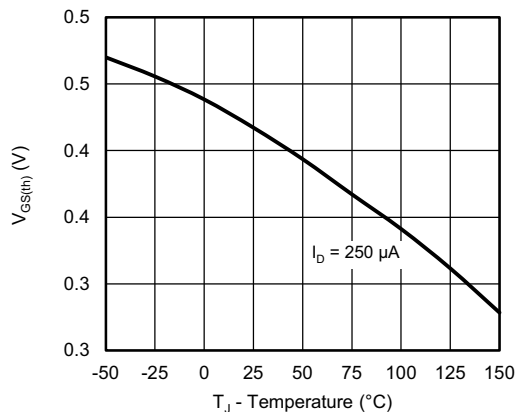
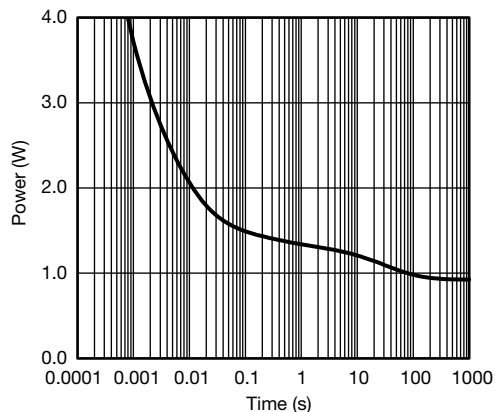
Transfer Characteristics

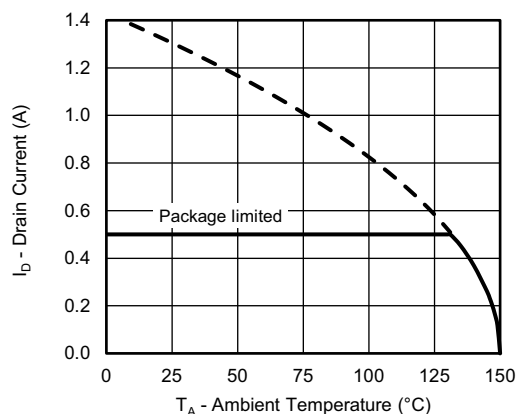
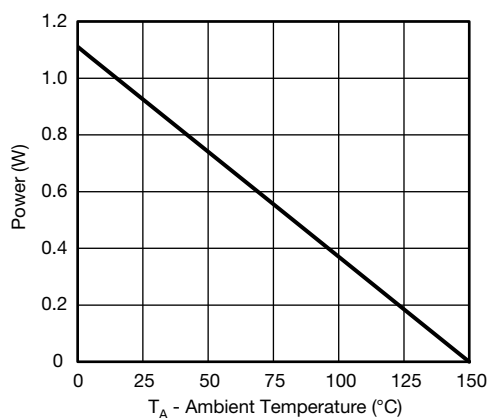
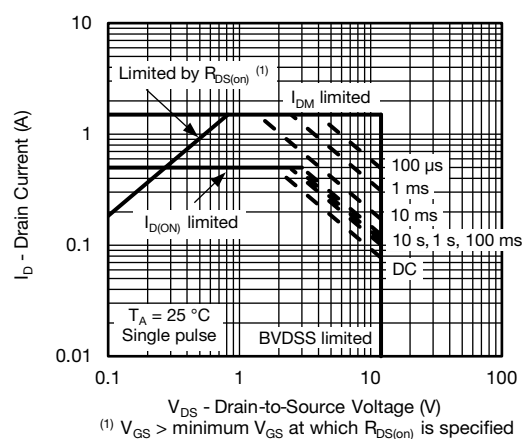


On-Resistance vs. Drain Current and Gate Voltage

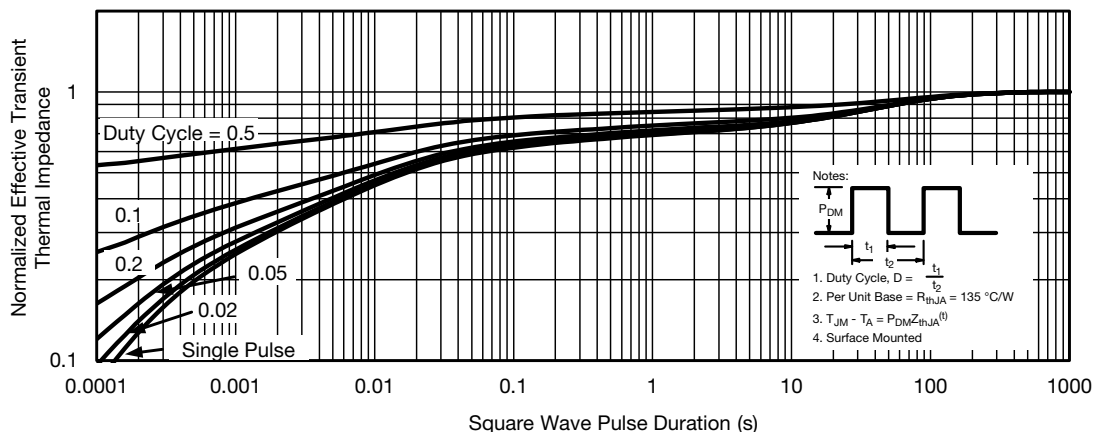
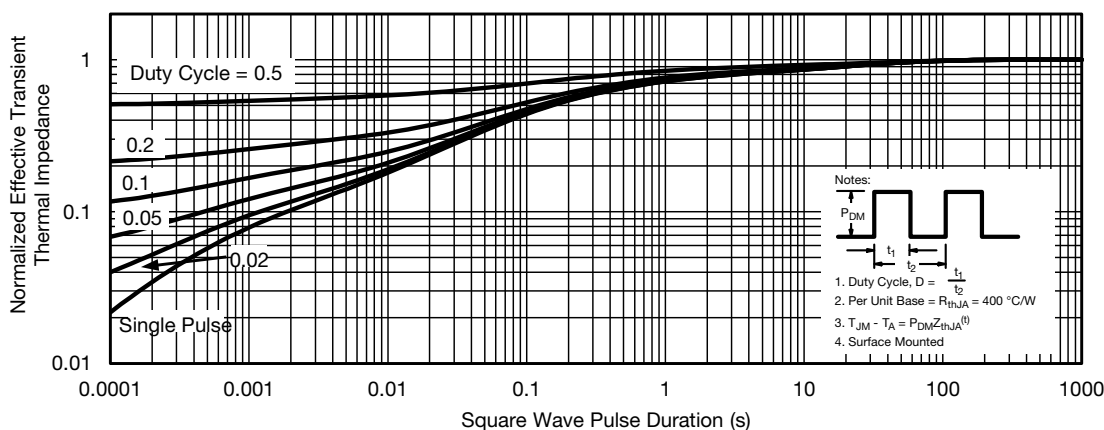


Capacitance

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

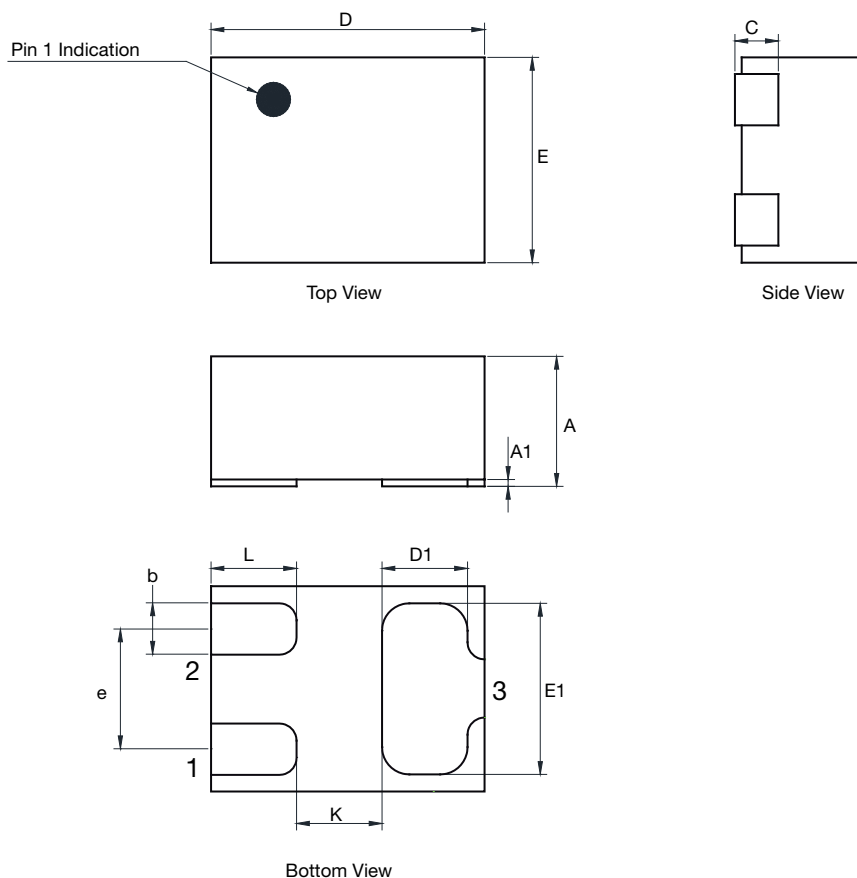
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient
Note

- a. The power dissipation P_D is based on $T_J \text{ max.} = 25^\circ\text{C}$, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)

Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)

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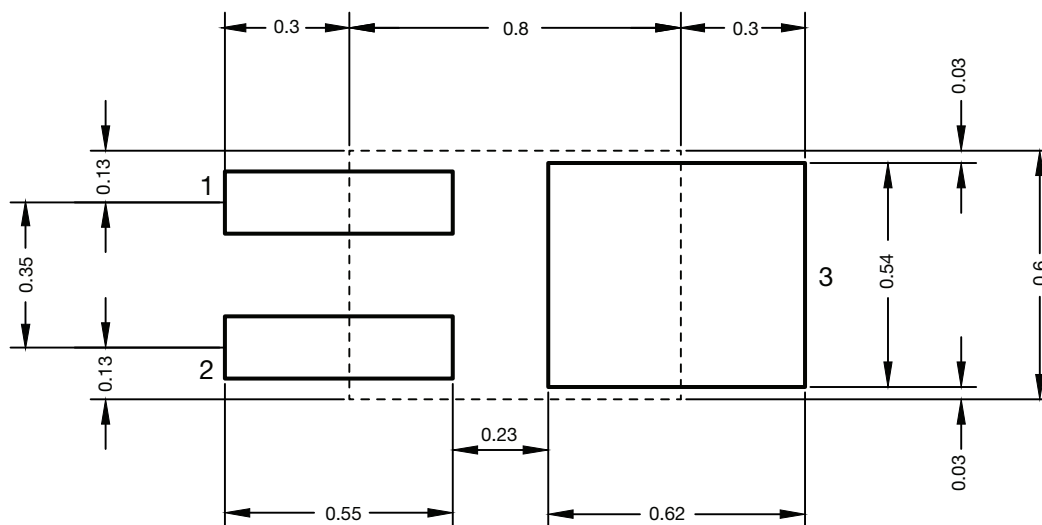
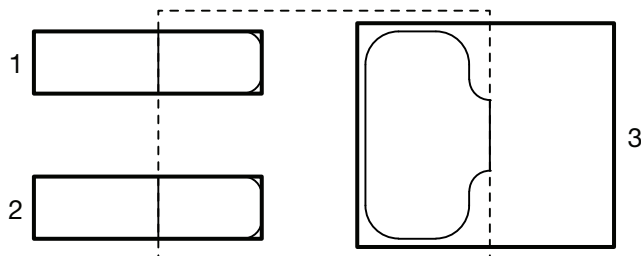
Case Outline for PowerPAK 0.8 mm x 0.6 mm



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.350	0.380	0.400	0.0138	0.0150	0.0157
A1	0	-	0.020	0	-	0.0008
b	0.120	0.150	0.180	0.0047	0.0059	0.0071
C	0.119	0.127	0.135	0.0047	0.0050	0.0053
D	0.750	0.800	0.850	0.0295	0.0315	0.0335
D1	0.200	0.250	0.300	0.0078	0.0098	0.0118
E	0.550	0.600	0.650	0.0217	0.0236	0.0256
E1	0.450	0.500	0.550	0.0177	0.0197	0.0217
e	0.300	0.350	0.400	0.0118	0.0138	0.0158
K	0.150	0.250	0.350	0.0058	0.0098	0.0138
L	0.200	0.250	0.300	0.0078	0.0098	0.0118

ECN: C13-1574-Rev. A, 23-Dec-13
DWG: 6020

Recommended Land Pattern PowerPAK® 0806





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