REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Changes in accordance with NOR 5962-R008-91.	91-10-17	Michael. A. Frye
B	Changes in accordance with NOR 5962-R217-93.	93-08-20	Michael. A. Frye
C	Updated boilerplate. Removed programming specifics from drawing, including table III. Separated source bulletin from body of drawing. - glg	00-08-30	Raymond Monnin
D	Corrected page number count on front page. Updated boilerplate. ksr.	04-11-30	Raymond Monnin
E	5 year review and update. Changed input and output capacitance from 6 pF to 10 pF and 8 pF to 10 pF respectively. ksr	06-06-12	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS															
REV	E	E	E	E	E	E	E	E	E	E	E			
SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

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DRAWING APPROVAL DATE
1988 Sep. 22

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, 2K X 8 REGISTERED UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87529**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87529	01	L	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	1/	2K x 8-registered UVEPROM	45 ns
02	1/	2K x 8-registered UVEPROM	35 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style 2/
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
3	CQCC1-N28	28	square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 3/

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 to +7.0 V dc
DC program voltage	14.0 V
DC input voltage range	-3.0 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D): 4/	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 5/	+150°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Endurance	25 cycles/byte (minimum)
Data retention	10 years minimum

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.
2/ Lid shall be transparent to permit ultraviolet erasure.
3/ Unless otherwise specified, all voltages are referenced to ground.
4/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.
5/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be specified by an altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{IX}	V_{IN} = 5.5 V and GND	1, 2, 3	All	-10	10	µA
Output leakage current 1/	I_{LO}	V_{OUT} = 5.5 V and GND output disabled	1, 2, 3	All		±40	µA
Operating supply current	I_{CC}	$\overline{E}/\overline{E_S}$ = V_{IL}, $\overline{INIT}$ = V_{IH}, addresses cycling between 0 V and 3.0 V, f = $1/2t_{PWC}$	1, 2, 3	All		120	mA
Input high voltage 2/	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All	2.0		V
Input low voltage 2/	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All		0.8	V
High level output voltage	V_{OH}	V_{IL} = 0.8 V, V_{IH} = 2.0 V I_{OH} = -4.0 mA, V_{CC} = 4.5 V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{IL} = 0.8 V, V_{IH} = 2.0 V I_{OL} = 16 mA, V_{CC} = 4.5 V.	1, 2, 3	All		0.4	V
Output short-circuit current 3/ 4/	I_{OS}	V_O = GND	1, 2, 3	All	-20	-125	mA
Input capacitance 4/	C_{IN}	V_{CC} = 5.5V, V_{IN} = 0 V T_C = +25°C	4	All		10	pF
Output capacitance 4/	C_{OUT}	see 4.3.1d, V_{OUT} = 0 V f = 1.0 MHz				10	
Address setup to clock high	t_{SA}	See figures 3 and 4 as applicable	9, 10, 11	01 02	45 35		ns
Address hold from clock	t_{HA}		9, 10, 11	All	0		ns
Clock high to valid output	t_{CO}		9, 10, 11	01 02		25 15	ns
Clock pulse width 4/	t_{PWC}		9, 10, 11	All	20		ns
Valid output from clock high 4/ 5/	t_{COS}		9, 10, 11	01 02		30 20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{E}_S$ setup to clock high 4/	t_{SES}	See figures 3 and 4 as applicable	9, 10, 11	All	15		ns
$\overline{E}_S$ hold from clock high 4/	t_{HES}		9, 10, 11	All	5		ns
Delay from $\overline{INIT}$ to valid output 4/	t_{DI}		9, 10, 11	01		35	ns
				02		20	
$\overline{INIT}$ recovery to clock high 4/	t_{RI}		9, 10, 11	All	20		ns
$\overline{INIT}$ pulse width 4/	t_{PWI}		9, 10, 11	01	25		ns
				02	20		
Inactive output from clock high 4/ 5/ 6/	t_{HZC}		9, 10, 11	01		30	ns
				02		20	
Valid output from $\overline{E}$ low 4/ 7/	t_{DOE}		9, 10, 11	01		30	ns
				02		20	
Inactive output from $\overline{E}$ high 4/ 6/ 7/	t_{HZE}		9, 10, 11	01		30	ns
				02		20	

1/ For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
2/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise.
3/ For test purposes, not more than one output at a time should be shorted. Short-circuit test duration should not exceed 30 seconds.
4/ This parameter tested initially and after any design or process changes which could affect this parameter, therefore, shall be guaranteed to the limits specified in table I.
5/ Applies only when the synchronous $\overline{E}_S$ function is used.
6/ Transition is measured at steady-state high level -500 mV or stead-state low level +500 mV on the output from the 1.5 V level on the input with loads shown on figure 3B.
7/ Applies only when the asynchronous $\overline{E}$ function is used.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMS. All testing requirements and quality assurance provisions herein, shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified by the manufacturer.

3.10.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified by the manufacturer.

3.10.3 Verification of programmed or erased EPROMs. When specified, devices shall be verified as either programmed to a specified program, or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

Device Types	All		
Case Outlines	L, K		3
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	A7	1	NC
2	A6	2	A7
3	A5	3	A6
4	A4	4	A5
5	A3	5	A4
6	A2	6	A3
7	A1	7	A2
8	A0	8	A1
9	O0	9	A0
10	O1	10	NC
11	O2	11	O0
12	GND	12	O1
13	O3	13	O2
14	O4	14	GND
15	O5	15	NC
16	O6	16	O3
17	O7	17	O4
18	CP	18	O5
19	$\overline{E}/\overline{E_S}$	19	O6
		20	O7
20	$\overline{INIT}$	21	NC
21	A10	22	CP
22	A9	23	$\overline{E}/\overline{E_S}$
	A8		
23	VCC	24	$\overline{INIT}$
24	- - -	25	A10
25	- - -		
26	- - -	26	A9
27	- - -	27	A8
28	- - -	28	VCC

FIGURE 1. Terminal connections.

Pins / Mode	CP	$\overline{E}/\overline{E}_S$	$\overline{INIT}$	Outputs
Read 1/ 2/ 3/	X	V_{IL}	V_{IH}	D_{OUT}
Output disable 4/	X	V_{IH}	V_{IH}	High Z

Notes:

1/ X = Input may be high level, low level, or open circuit.

2/ During read operation, the output latches are loaded on a "0" to "1" transition of CP.

3/ In the synchronous mode, pin $\overline{E}_S$ must be low prior to the "0" to "1" transition of CP that loads the register.

4/ In the synchronous mode, pin $\overline{E}_S$ must be high prior to the "0" to "1" transition of CP that loads the register.

FIGURE 2. Truth table.

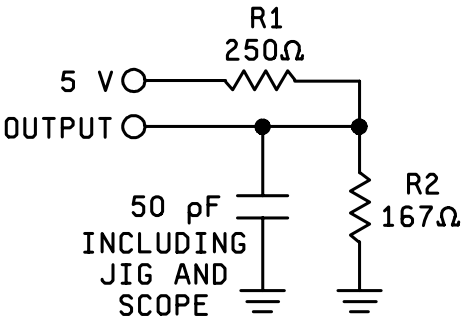


Figure 3A

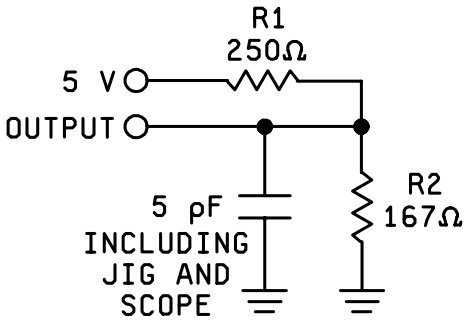


Figure 3B

FIGURE 3. Output load circuit.

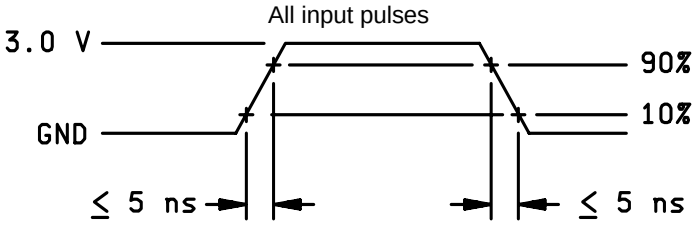
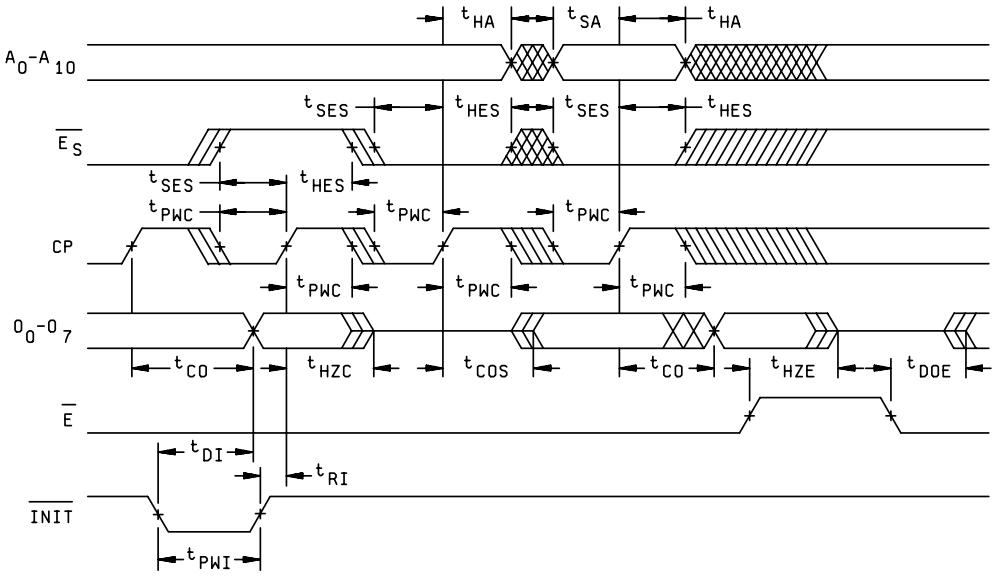


FIGURE 4. Switching waveforms.



NOTES:

1. Ensure that adequate decoupling capacitance is employed across the device VCC and ground terminals. Multiple capacitors are recommended, including a 0.1uF or larger capacitor and a 0.01 µF or smaller capacitor, placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under ac conditions. Large amplitude fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5 V reference levels.
5. Transition is measured at steady-state HIGH level -500 mV or steady-state LOW level +500 mV on output from the 1.5 V level on inputs with load shown on figure 3B.
6. Tests are performed with rise and fall times of 5ns or less.
7. See figure 3A for all switching characteristics except t_{HZC} and t_{HZE}.
8. See figure 3B for t_{HZC} and t_{HZE}.
9. All device test loads should be located within 2 inches of device outputs.

FIGURE 4. Switching waveforms - continued.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9,10,11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, 8***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

1/ * PDA applies to subgroups 1, 7, and 9.
2/ ** See 4.3.1d.
3/ *** See 4.3.1e.
4/ Any subgroups at the same temperature may be combined using a multifunctional tester.
5/ For all electrical tests, the device shall be programmed to the pattern specified.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a checkerboard pattern, or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 5 devices with no failures, and all input and output terminals tested.

e. As a minimum, subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883

c. All devices submitted for testing shall be programmed with a checkerboard pattern, or equivalent. After completion of all testing, the devices shall be erased and verified.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone 614-692-0547.

6.6 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-12

Approved sources of supply for SMD 5962-87529 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-8752901LA	3/	CY7C245-45WMB
	0C7V7	QP7C245A-45WMB
	0C7V7	WS57C45-45TMB
5962-8752901KA	3/	CY7C245-45TMB
	0C7V7	QP7C245A-45TMB
	0C7V7	WS57C45-45FMB
5962-87529013A	0C7V7	QP7C245A-45QMB
	0C7V7	WS57C45-45CMB
5962-87529013C	3/	CY7C245-45QMB
	0C7V7	QP7C245A-45QMB
	0C7V7	WS57C45-45CMB
5962-8752902LA	3/	CY7C245-35WMB
	0C7V7	QP7C245A-35WMB
	0C7V7	WS57C45-35TMB
5962-8752902KA	3/	CY7C245-35TMB
	0C7V7	QP7C245A-35TMB
	0C7V7	WS57C45-35FMB
5962-87529023A	0C7V7	QP7C245A-35QMB
	0C7V7	WS57C45-35CMB
5962-87529023C	3/	CY7C245-35QMB
	0C7V7	QP7C245A-35QMB
	0C7V7	WS57C45-35CMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.