

N-channel 600 V, 0.395 Ω typ., 9 A MDmesh M2 Power MOSFET in a DPAK package

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD12N60M2	600 V	0.450 Ω	9 A

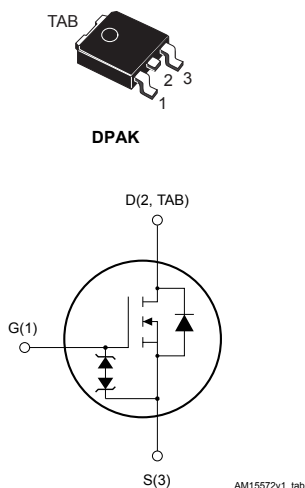
- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.



Product status link

[STD12N60M2](#)

Product summary

Order code	STD12N60M2
Marking	12N60M2
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	9	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	5.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	36	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	85	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 9\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
3. $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.47	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.6	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	117	mJ

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.5\text{ A}$		0.395	0.450	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	538	-	pF
C_{oss}	Output capacitance		-	29	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	106	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	7	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 9\text{ A}$, $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	16	-	nC
Q_{gs}	Gate-source charge		-	2.3	-	nC
Q_{gd}	Gate-drain charge		-	8.5	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 4.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	9.2	-	ns
t_r	Rise time		-	9.2	-	ns
$t_{d(off)}$	Turn-off-delay time		-	56	-	ns
t_f	Fall time		-	18	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 9\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	284		ns
Q_{rr}	Reverse recovery charge		-	2.4		μC
I_{RRM}	Reverse recovery current		-	17		A
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	404		ns
Q_{rr}	Reverse recovery charge		-	3.5		μC
I_{RRM}	Reverse recovery current		-	17.5		A

1. Pulse width is limited by safe operating area
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Characteristics curves

Figure 1. Safe operating area

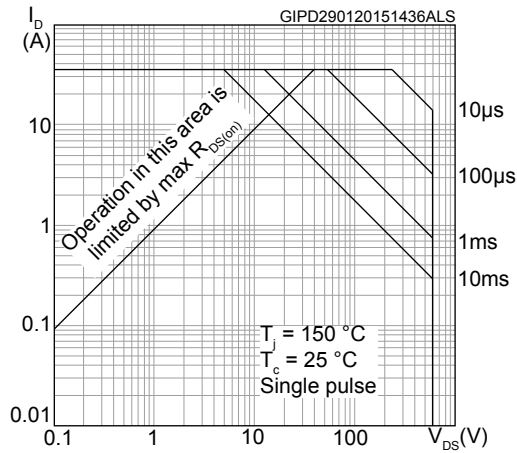


Figure 2. Thermal impedance

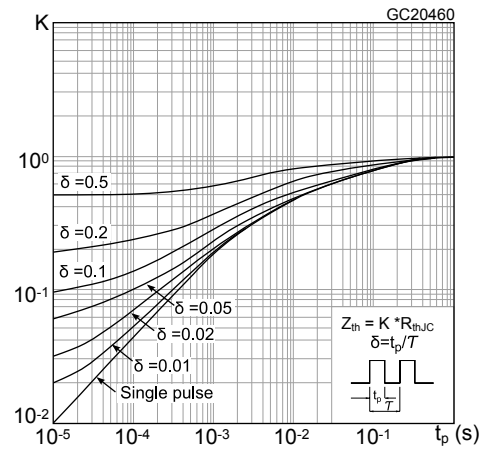


Figure 3. Output characteristics

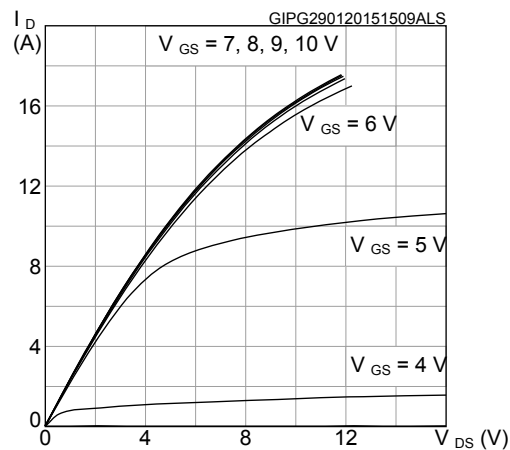


Figure 4. Transfer characteristics

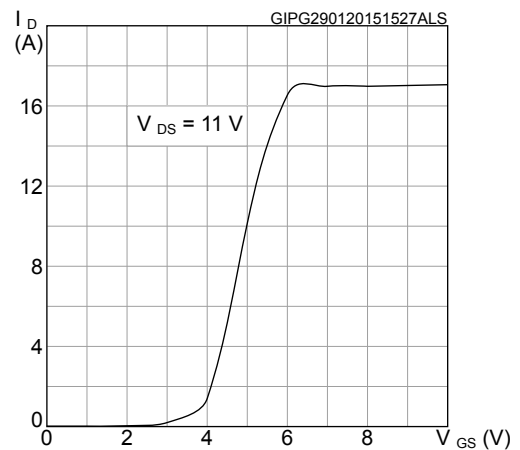


Figure 5. Normalized gate threshold voltage vs temperature

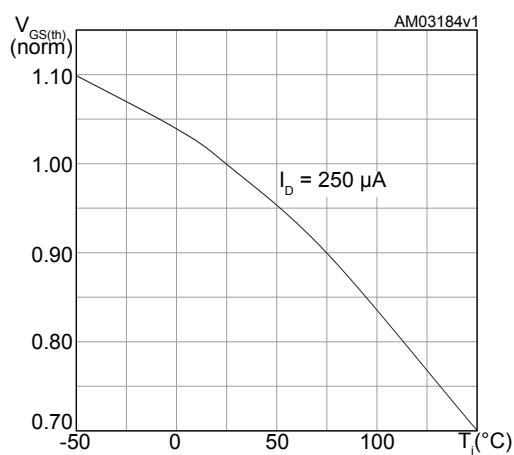


Figure 6. Normalized V(BR)DSS vs temperature

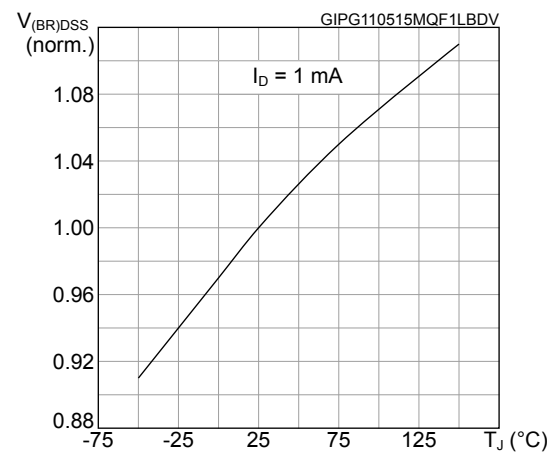
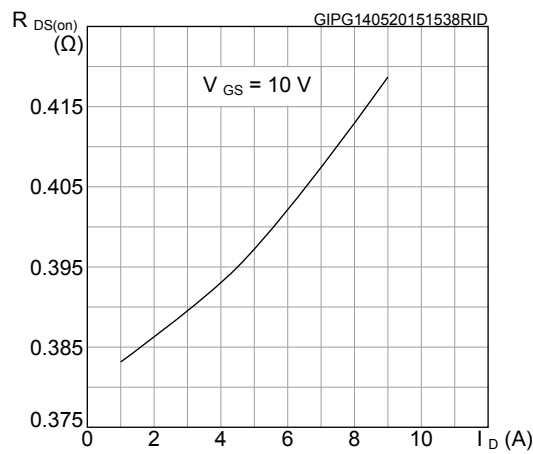
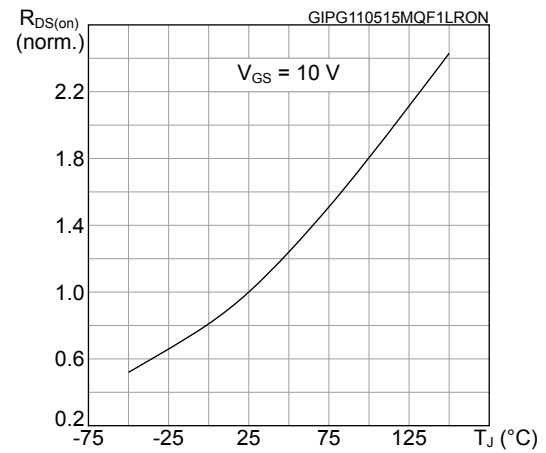
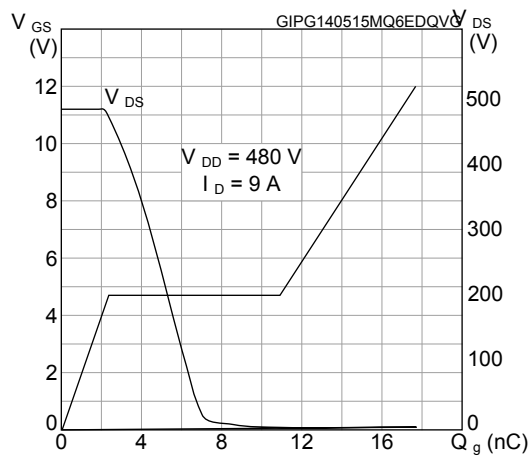
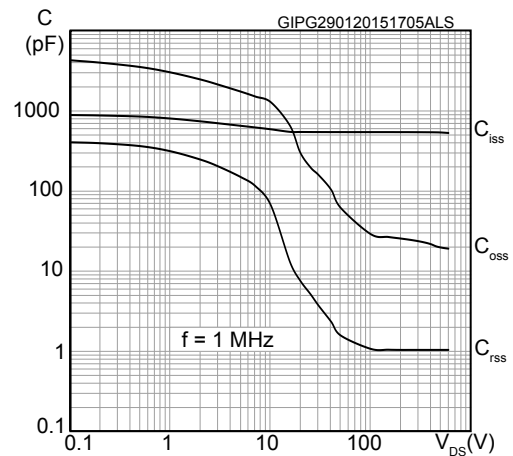
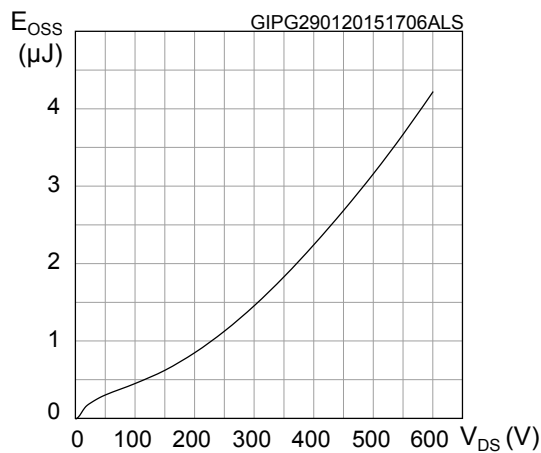
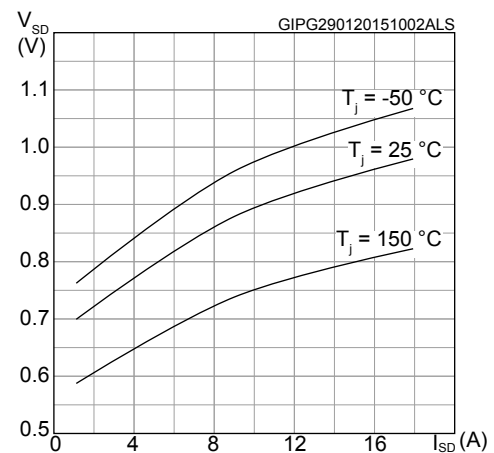
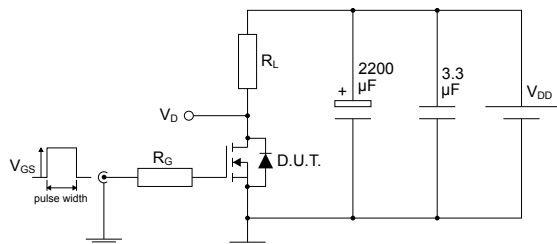


Figure 7. Static drain-source on-resistance

Figure 8. Normalized on-resistance vs temperature

Figure 9. Gate charge vs. gate-source voltage

Figure 10. Capacitance variations

Figure 11. Output capacitance stored energy

Figure 12. Source-drain diode forward characteristics


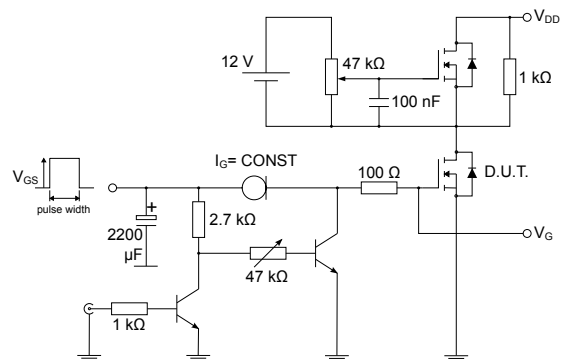
3 Test circuits

Figure 13. Test circuit for resistive load switching times



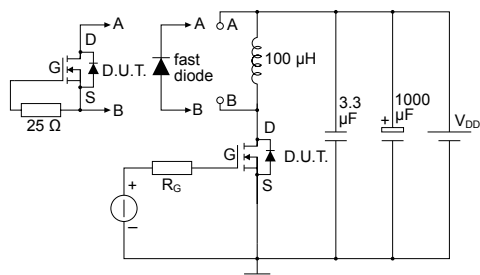
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Figure 14. Test circuit for gate charge behavior



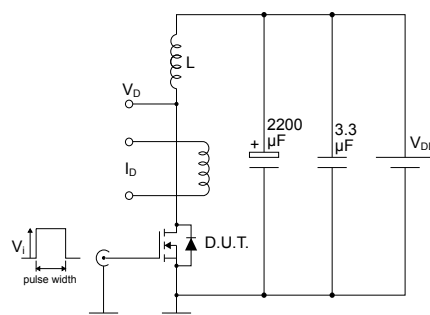
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Figure 15. Test circuit for inductive load switching and diode recovery times



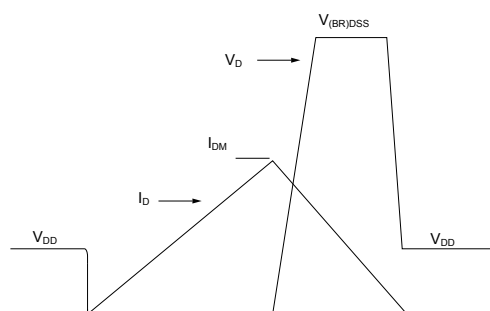
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Figure 16. Unclamped inductive load test circuit



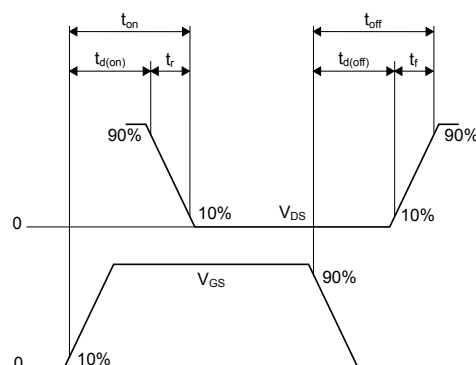
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



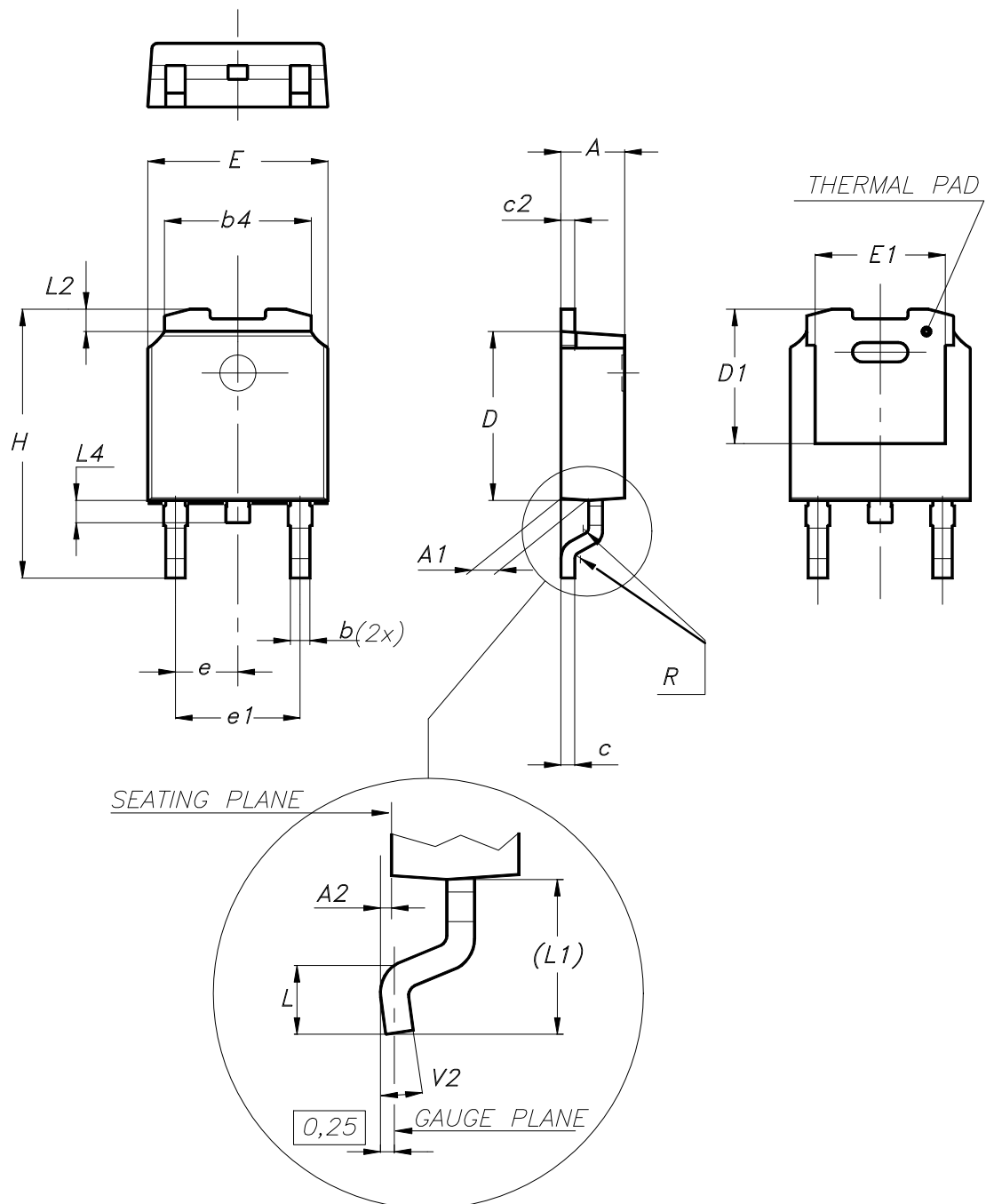
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



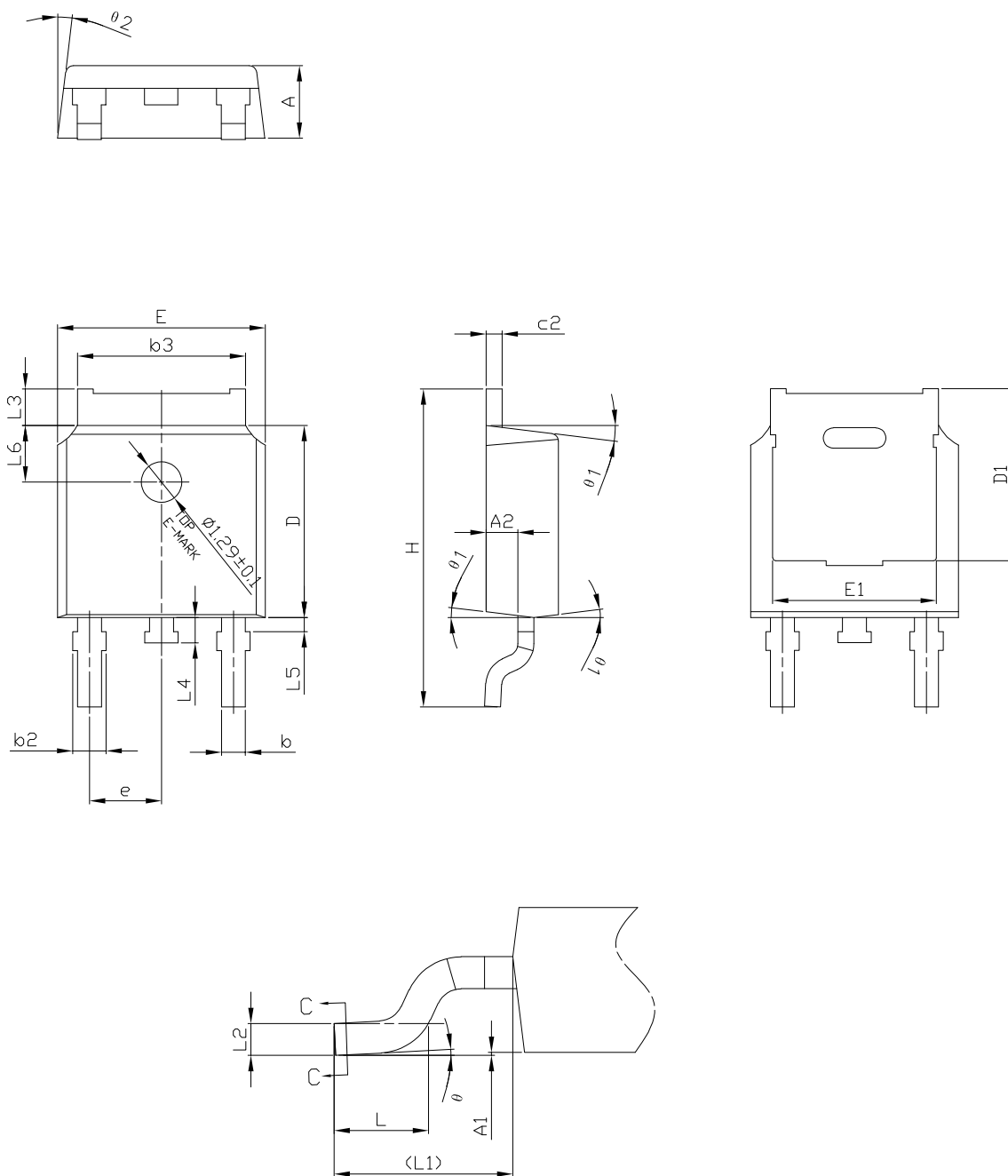
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Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C3 package information

Figure 20. DPAK (TO-252) type C3 package outline



0068772_type-C3_rev34

Table 9. DPAK (TO-252) type C3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

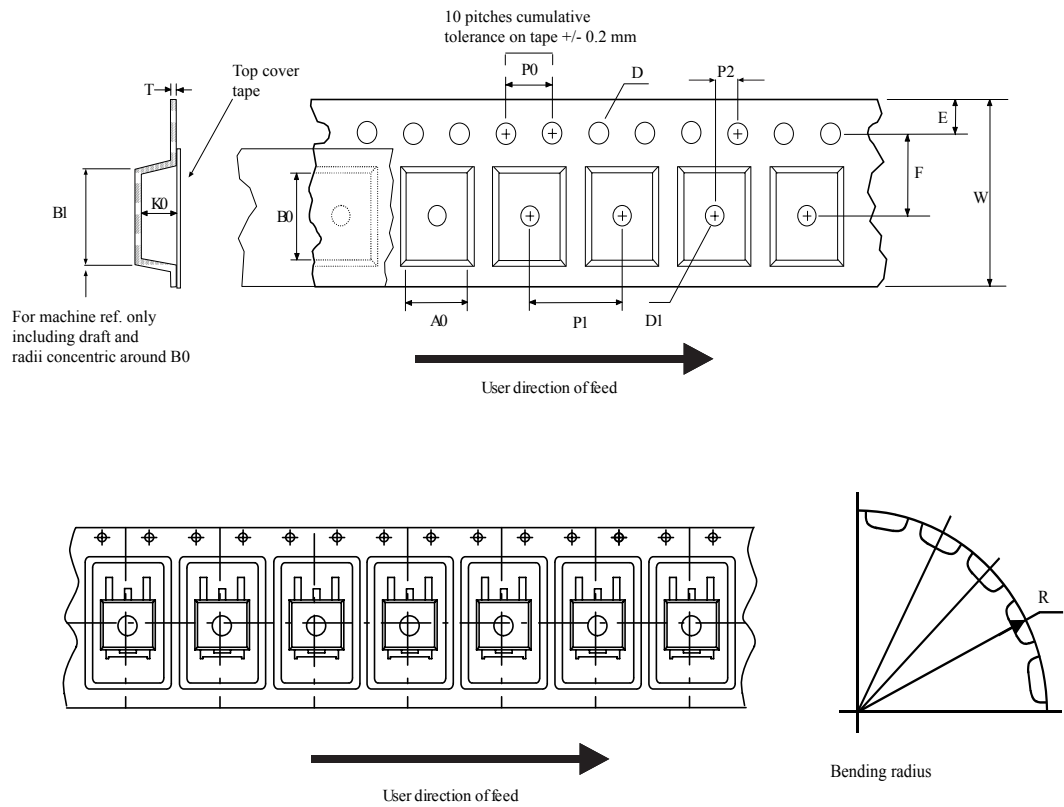
Technical drawing of a mechanical part. The drawing shows a top view and a side view. The top view is a rectangle with a width of 6.3 and a height of 6.5. The side view is a rectangle with a width of 11.2 and a height of 1.8 MIN. The part has two rectangular features on the top surface, each with a width of 1.5 and a height of 2.9. The distance between the centers of these features is 4.572. The drawing includes section lines (hatching) and dimension lines with arrows. A section line A-A is shown at the bottom, and a section line B-B is shown on the right.

2) The device must be positioned within $\oplus 0.05 \text{ A B}$

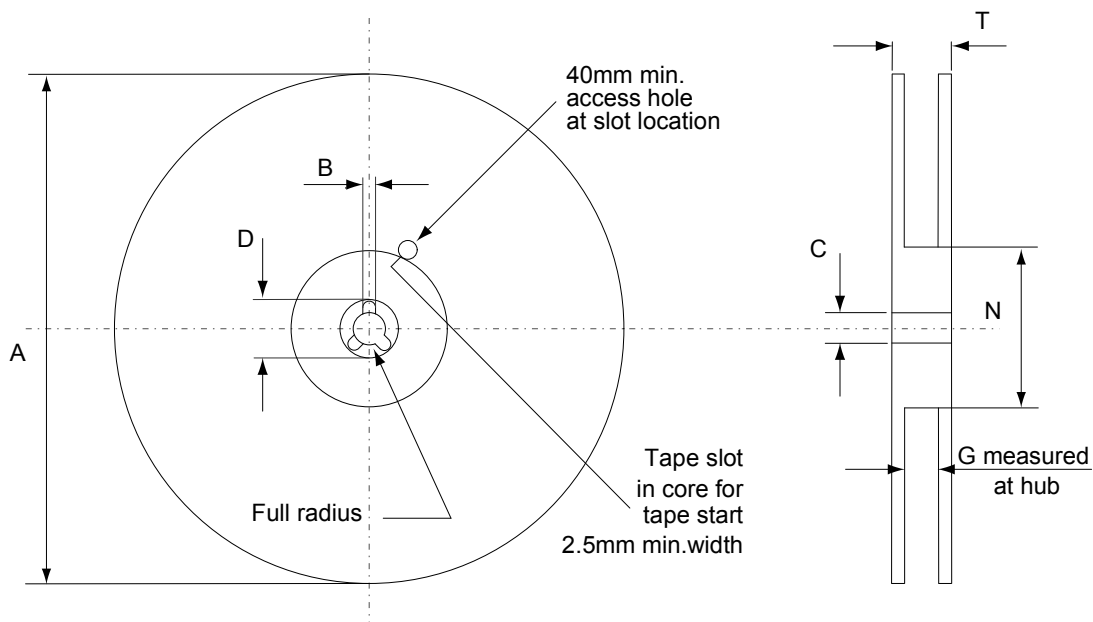
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4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



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Figure 23. DPAK (TO-252) reel outline


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Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. Document revision history

Date	Revision	Changes
30-Jan-2014	1	First release.
12-Apr-2019	2	Added <i>Section 4.2 DPAK (TO-252) type C2 package information</i> .
17-May-2023	3	Updated <i>Section 4.1 DPAK (TO-252) type A package information</i> . Added <i>Section 4.2 DPAK (TO-252) type C3 package information</i> . Minor text changes.

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