Low Noise, Switched Capacitor Regulated Voltage Inverters

FEATURES

- **Regulated Negative Voltage from a Single Positive Supply**
- **Low Output Ripple: Less Than 1mV$_{P-P}$ Typ**
- **High Charge Pump Frequency: 900kHz Typ**
- Small Charge Pump Capacitors: 0.1µF
- Requires Only Four External Capacitors
- Fixed –4.1V or Adjustable Output
- Shutdown Mode Drops Supply Current to < 1µA
- High Output Current: Up to 10mA, V_{CC} = 5V
- Output Regulation: 5%
- Available in SO-8 and 16-Lead SSOP

APPLICATIONS

- GaAs FET Bias Generators
- Negative Supply Generators
- Battery-Powered Systems
- Single Supply Applications

DESCRIPTION

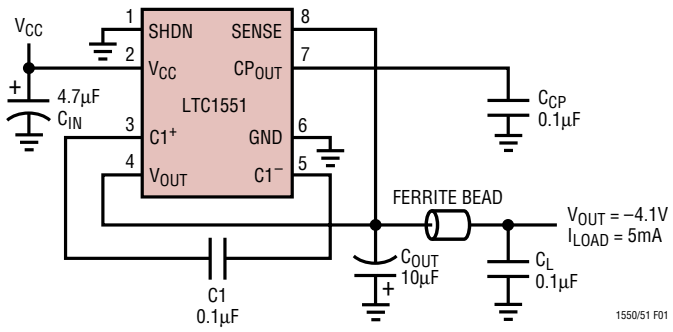
The LTC®1550/LTC1551 are switched capacitor charge pump voltage inverters which include internal linear post-regulators to minimize output ripple. Output voltages are fixed at –4.1V, with ripple voltages typically below 1mV$_{P-P}$. The LTC1550 is also available in an adjustable output voltage version. The LTC1550/LTC1551 are ideal for use as bias voltage generators for GaAs transmitter FETs in portable RF and cellular telephone applications.

The LTC1550/LTC1551 operate from single 4.5V to 6.5V supplies and draw typical quiescent currents of 4.25mA with a 5V supply. Each device includes a TTL compatible Shutdown pin which drops supply current to 0.2µA typically. The LTC1550 Shutdown pin is active low ($\overline{SHDN}$), while the LTC1551 Shutdown pin is active high (SHDN). Only four external components are required: an input bypass capacitor, two 0.1µF charge pump capacitors and a filter capacitor at the linear regulator output. The adjustable LTC1550 requires two additional resistors to set the output voltage. The LTC1550/LTC1551 will supply up to 10mA output current with a 5V supply, while maintaining guaranteed output regulation of ±5%.

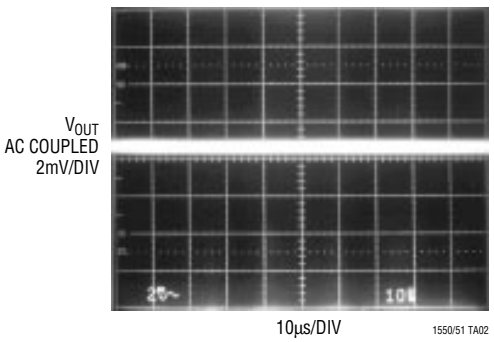
The fixed voltage LTC1550/LTC1551 are available in S0-8 plastic packages. The adjustable LTC1550 is available in a 16-pin SSOP.

TYPICAL APPLICATION

–4.1V Generator with 1mV$_{P-P}$ Noise



V_{OUT} Output Noise and Ripple

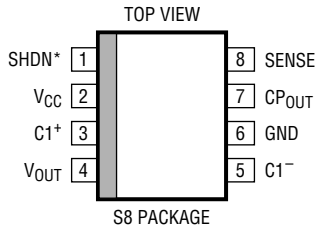


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 7V
Output Voltage ..... 0.3V to (V_{CC} – 14V)
Total Voltage, V_{CC} to CP_{OUT} 14V
Input Voltage (SHDN Pin) ..... –0.3V to (V_{CC} + 0.3V)
Input Voltage (REG Pin) ..... –0.3V to 12V
Output Short-Circuit Duration ..... 30 sec

Commercial Temperature Range ..... 0°C to 70°C
Extended Commercial Operating
Temperature Range (Note 3) ..... –40°C to 85°C
Industrial Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

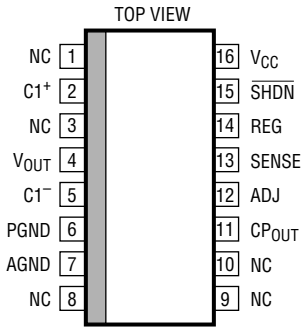


S8 PACKAGE
8-LEAD PLASTIC SO

*$\overline{SHDN}$ FOR LTC1550, SHDN FOR LTC1551

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1550CS8-4.1 LTC1551CS8-4.1



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1550CGN LTC1550IGN
GN PART MARKING
1550

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 6.5V, C1 = C2 = 0.1µF, C_{OUT} = 10µF, T_A = 25°C unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (LTC1550CGN/LTC1550IGN) (LTC1550CS8-4.1/LTC1551CS8-4.1)		 ● ●	 2.7 4.5		 6.5 6.5	 V V
V_{REF}	Reference Voltage		●		1.24		V
I_S	Supply Current	V_{CC} = 5V, V_{SHDN} = V_{CC} (LTC1550) or GND (LTC1551) V_{CC} = 5V, V_{SHDN} = GND (LTC1550) or V_{CC} (LTC1551)	● ●		4.25 0.2	7 10	mA µA
f_{OSC}	Internal Oscillator Frequency				900		kHz
V_{OL}	REG Output Low Voltage	I_{REG} = 1mA, V_{CC} = 5V	●		0.1	0.8	V
I_{REG}	REG Sink Current	V_{REG} = 0.8V, V_{CC} = 5V	●	7	15		mA
V_{IH}	SHDN Input High Voltage	V_{CC} = 5V	●	2			V
V_{IL}	SHDN Input Low Voltage	V_{CC} = 5V	●			0.8	V
I_{IN}	SHDN Input Current	V_{SHDN} = V_{CC}	●		0.1	1	µA
t_{ON}	Turn-On Time	I_{OUT} = 10mA			1		ms
V_{OUT}	Output Regulation (LTC1550CGN/LTC1550IGN)	2.7V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA 2.8V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA 3.5V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	● ● ●	–1.575 –1.575 –1.575	–1.5 –1.5 –1.5	–1.425 –1.425 –1.425	V V V
V_{OUT}	Output Regulation (LTC1550CGN/LTC1550IGN)	2.7V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA 3.1V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA 3.75V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	● ● ●	–2.1 –2.1 –2.1	–2.0 –2.0 –2.0	–1.9 –1.9 –1.9	V V V

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 6.5V, C1 = C2 = 0.1µF, C_{OUT} = 10µF, T_A = 25°C unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Regulation (LTC1550CGN/LTC1550IGN)	3.05V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA	●	–2.625	–2.5	–2.375	V
		3.45V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–2.625	–2.5	–2.375	V
		4.1V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	●	–2.625	–2.5	–2.375	V
V_{OUT}	Output Regulation (LTC1550CGN/LTC1550IGN)	3.45V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA	●	–3.15	–3.0	–2.85	V
		3.85V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–3.15	–3.0	–2.85	V
		4.5V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	●	–3.15	–3.0	–2.85	V
V_{OUT}	Output Regulation (LTC1550CGN/LTC1550IGN)	3.9V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA	●	–3.675	–3.5	–3.325	V
		4.2V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–3.675	–3.5	–3.325	V
		4.85V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	●	–3.675	–3.5	–3.325	V
V_{OUT}	Output Regulation (LTC1550CGN/LTC1550IGN)	4.5V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA	●	–4.3	–4.1	–3.9	V
		4.75V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–4.3	–4.1	–3.9	V
		5.35V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	●	–4.3	–4.1	–3.9	V
V_{OUT}	Output Regulation (LTC1550CGN/LTC1550IGN)	4.8V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA	●	–4.725	–4.5	–4.275	V
		5.1V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–4.725	–4.5	–4.275	V
		5.7V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	●	–4.725	–4.5	–4.275	V
V_{OUT}	Output Regulation (LTC1550CS8-4.1/LTC1551CS8-4.1)	4.5V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 5mA	●	–4.3	–4.1	–3.9	V
		4.75V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–4.3	–4.1	–3.9	V
		5.35V ≤ V_{CC} ≤ 6.5V, 0 ≤ I_{OUT} ≤ 20mA	●	–4.3	–4.1	–3.9	V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 5V	●		50	150	mA
		V_{OUT} = 0V, V_{CC} = 6.5V	●		80	200	mA
V_{RIPPLE}	Output Ripple Voltage				1		mV

The ● denotes specifications which apply over the specified temperature range.

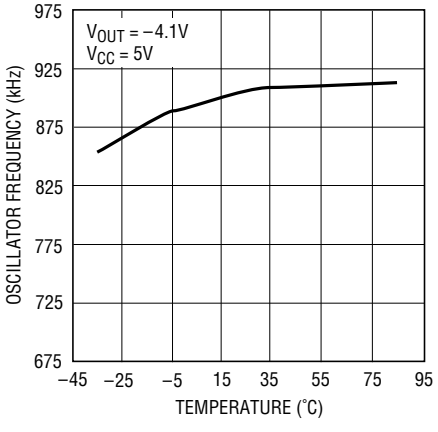
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified. All typicals are given at T_A = 25°C.

Note 3: C-grade device specifications are guaranteed over the 0°C to 70°C temperature range. In addition, C-grade device specifications are assured over the –40°C to 85°C temperature range by design or correlation, but are not production tested.

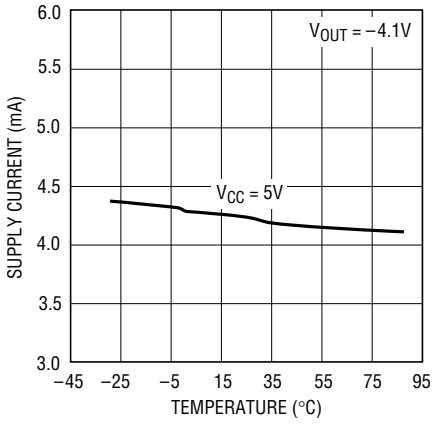
TYPICAL PERFORMANCE CHARACTERISTICS

Oscillator Frequency vs Temperature



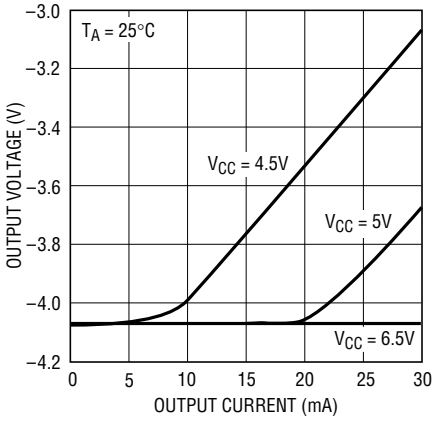
LTC1550/51 G01

Supply Current vs Temperature



LTC1550/51 G02

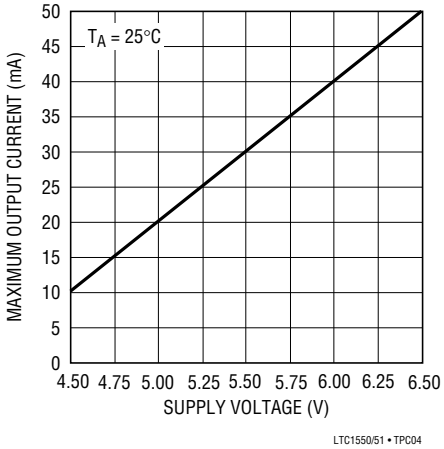
Output Voltage vs Output Current (LTC1550CS8-4.1/LTC1551CS8-4.1)



LTC1550/51 G03

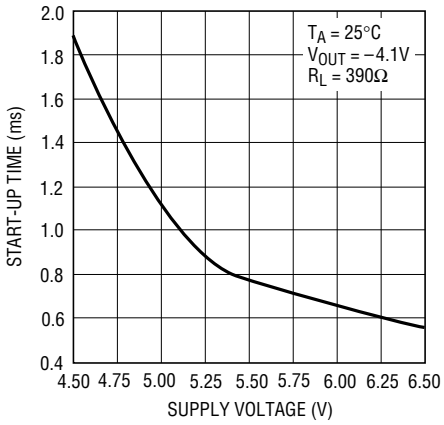
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Output Current vs Supply Voltage



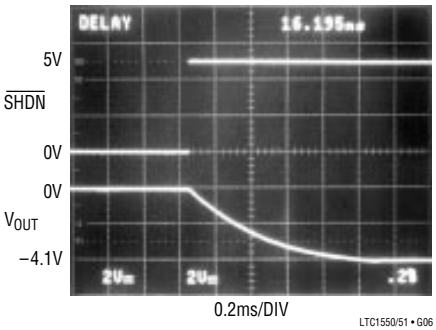
LTC1550/51 • TPC04

Start-Up Time vs Supply Voltage



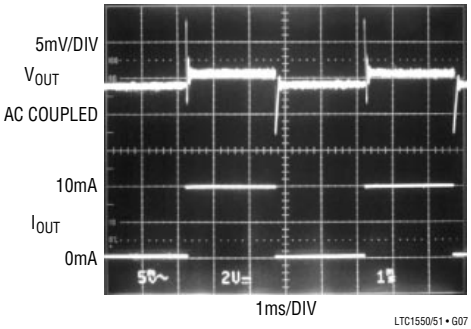
LTC1550/51 G05

Startup Time (LTC1550 Shown)



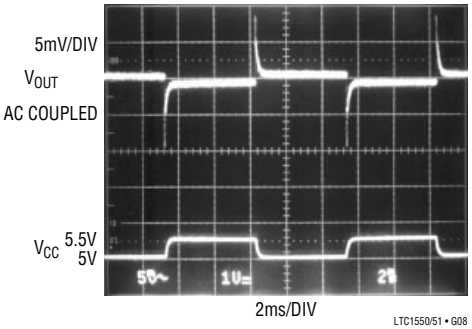
LTC1550/51 • G06

Load Transient Response (See Figure 2, V_{CC} = 5V)



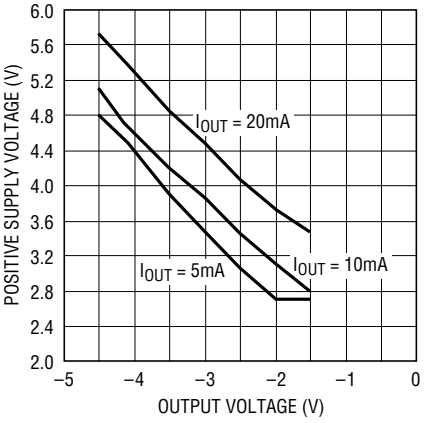
LTC1550/51 • G07

Line Transient Response (See Figure 2, I_L = 10mA)



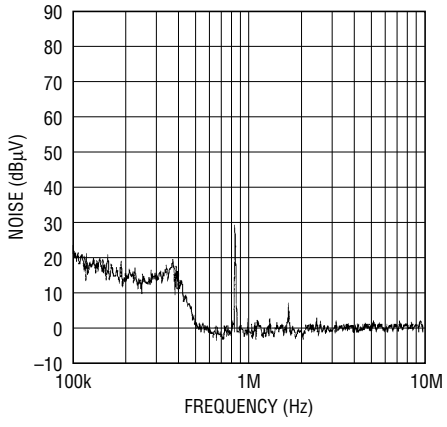
LTC1550/51 • G08

Minimum Required V_{CC} vs V_{OUT} and I_{OUT}



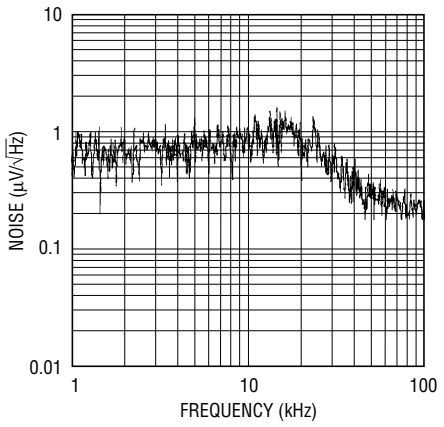
LTC1550/51 • G08.5

Output Spectrum (*See Typical Application)



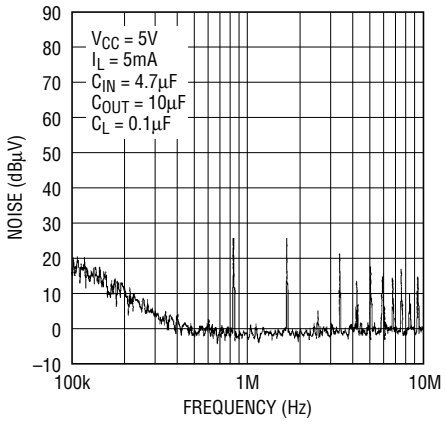
LTC1550/51 • G09

Spot Noise (*See Typical Application)



LTC1550/51 • G10

Output Spectrum (See Figure 2, C_{OUT} = 10μF)

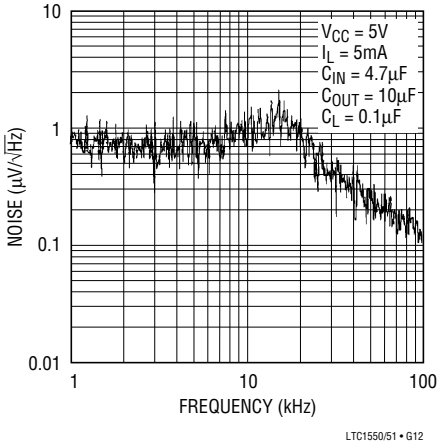


LTC1550/51 • G11

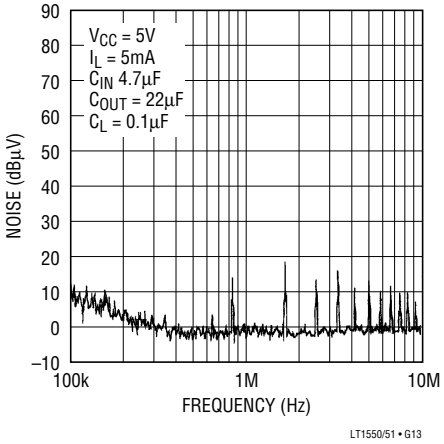
* On first page of data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

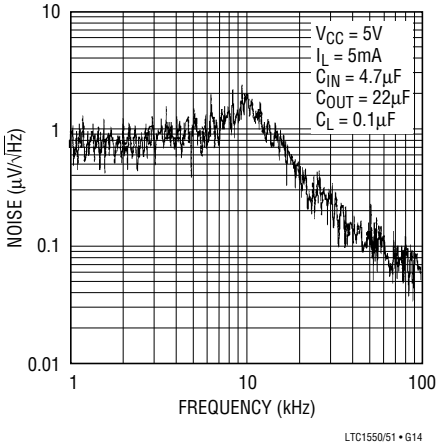
Spot Noise
(See Figure 2, C_{OUT} = 10µF)



Output Spectrum
(See Figure 2, C_{OUT} = 22µF)



Spot Noise
(See Figure 2, C_{OUT} = 22µF)



PIN FUNCTIONS

SHDN: Shutdown (TTL Compatible). This pin is active low (SHDN) for the LTC1550 and active high (SHDN) for the LTC1551. When this pin is at V_{CC} (GND for LTC1551), the LTC1550 operates normally. When SHDN is pulled low (high for LTC1551), the LTC1550 enters shutdown mode. In shutdown, the charge pump stops, the output collapses to 0V, and the quiescent current drops typically to 0.2µA.

V_{CC}: Power Supply. V_{CC} requires an input voltage between 4.5V and 6.5V for the fixed voltage LTC1550CS8-4.1/ LTC1551CS8-4.1. The adjustable voltage LTC1550CGN/ LTC1550IGN operates with a VCC range of 2.7V to 6.5V. Output voltage and output load current conditions depend on the VCC supply voltage. Consult the Electrical Characteristics table and Typical Performance Characteristics for guaranteed test points. The difference between the input voltage and output should never be set to exceed 14V or damage to the chip may occur. V_{CC} must be bypassed to PGND (GND for 8-pin packages) with at least a 0.1µF capacitor placed in close proximity to the chip. A 4.7µF or larger bypass capacitor is recommended to minimize noise and ripple at the output.

$C1^+$: C1 Positive Input. Connect a 0.1µF capacitor between $C1^+$ and $C1^-$.

V_{OUT}: Negative Voltage Output. This pin must be bypassed to ground with a 4.7µF or larger capacitor to ensure regulator loop stability. At least 10µF is recommended to provide specified output ripple. An additional 0.1µF low ESR capacitor is recommended to minimize high frequency spikes at the output.

$C1^-$: C1 Negative Input. Connect a 0.1µF capacitor from $C1^+$ to $C1^-$.

GND: Ground. Connect to a low impedance ground. A ground plane will help minimize regulation errors.

CP_{OUT}: Negative Charge Pump Output. This pin requires a 0.1µF storage capacitor to ground.

SENSE: Connect to V_{OUT}. The LTC1550/LTC1551 internal regulator uses this pin to sense the output voltage. For optimum regulation, SENSE should be connected close to the output load.

SSOP PACKAGE ONLY

PGND: Power Ground. Connect to a low impedance ground. PGND should be connected to the same potential as AGND.

AGND: Analog Ground. Connect to a low impedance ground. AGND should be connected to a ground plane to minimize regulation errors.

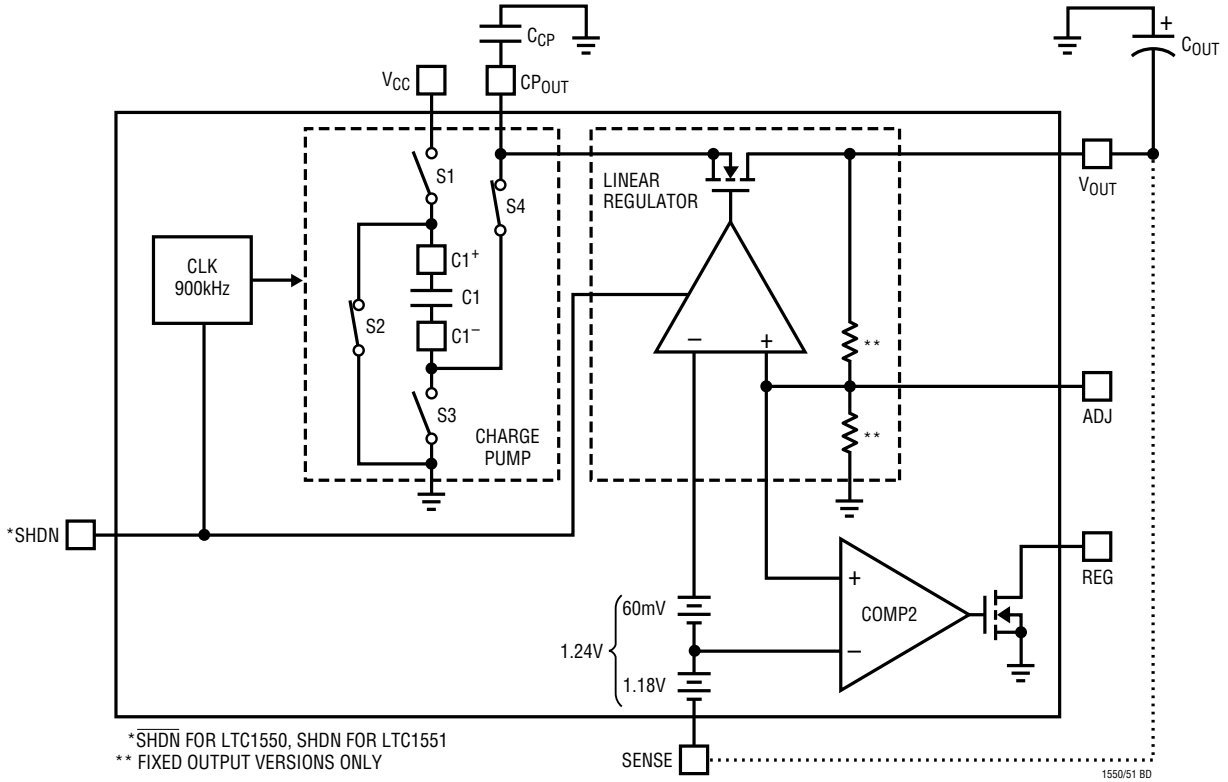
PIN FUNCTIONS

REG: This is an open-drain output that pulls low when the output voltage is within 5% of the set value. It will sink 7mA to ground with a 5V supply. The external circuitry must provide a pull-up or REG will not swing high. The voltage at REG may exceed V_{CC} and can be pulled up to 12V above ground without damage.

ADJ: For adjustable versions only, this is the feedback point for the external resistor divider string. Connect a divider string from AGND to V_{OUT} with the divided tap connected to ADJ. Note that the resistor string needs to be connected "upside-down" from a traditional negative regulator. See the Applications Information section for hook-up details.

NC: No Internal Connection.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

The LTC1550/LTC1551 are switched capacitor, inverting charge pumps with internal linear post-regulators. The LTC1550CS8/LTC1551CS8 provide a regulated, low ripple –4.1V output at up to 10mA load current from a single 5V supply. The LTC1550CGN provides a regulated, low ripple adjustable output. Output load current for the adjustable version depends on the input/output voltage combination. Consult the graph provided in the Typical Performance Characteristics section and the Electrical Characteristics table for guaranteed test points. The LTC1550/LTC1551 are ideal for use as bias voltage generators for GaAs transmitter FETs in portable RF and cellular telephone applications. The LTC1550 features an active-low Shutdown pin ($\overline{SHDN}$) that drops quiescent current to below 1μA. The LTC1551 is identical to the LTC1550,

APPLICATIONS INFORMATION

except that the Shutdown pin is active-high (SHDN). All members of the LTC1550 family feature a 900kHz charge pump frequency. The LTC1550/ LTC1551 come standard with fixed –4.1V output voltages and the LTC1550 is available with an adjustable output voltage. Both devices can be configured with other fixed output voltages; contact Linear Technology for more information.

The LTC1550 consists of two major blocks (see Block Diagram): an inverting charge pump and a negative linear regulator. The charge pump uses two external capacitors, C1 and C_{CP} to generate a negative voltage at CP_{OUT}. It operates by charging and discharging C1 on alternate phases of the internal 900kHz clock. C1 is initially charged to V_{CC} through switches S1 and S3. When the internal clock changes phase, S1 and S3 open and S2 and S4 close, shorting the positive side of C1 to ground. This forces the negative side of C1 below ground, and charge is transferred to C_{CP} through S4. As this cycle repeats, the magnitude of the negative voltage approaches V_{CC}. The 900kHz internal clock frequency helps keep noise out of 400kHz to 600kHz IF bands commonly used by portable radio frequency systems and reduces the size of the external capacitors required. Most applications can use standard 0.1µF ceramic capacitors for C1 and C_{CP}. Increasing C1 and C_{CP} beyond 0.1µF has little effect on the output ripple or the output current capacity of the LTC1550/LTC1551.

The negative voltage at CP_{OUT} supplies the input to the negative regulator block. This block consists of an N-channel MOSFET pass device and a feedback amplifier that monitors the output voltage and compares it to the internal reference. The regulated output appears at the V_{OUT} pin. The regulation loop is optimized for fast transient response, enabling it to remove most of the switching artifacts present at the CP_{OUT} pin. Output ripple is typically below $1mV_{P-P}$ with output loads between 0mA and 10mA. The output voltage is set to –4.1V by a pair of internal divider resistors. The N-channel pass device minimizes dropout, allowing the output to remain in regulation with supply voltages as low as 4.5V. An output capacitor of at least 4.7µF from V_{OUT} to ground is required to keep the regulator loop stable; for optimum stability and minimum output ripple, at least 10µF is recommended.

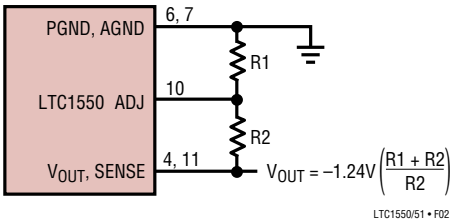


Figure 1. External Resistor Connections

Adjustable Hook-Up

The LTC1550CGN is available in an adjustable output version in a 16-pin SSOP package. The output voltage is set with a resistor divider from GND to SENSE/V_{OUT} (Figure 1). Note that the internal reference and the internal feedback amplifier are set up as a positive-output regulator referenced to the SENSE pin, not a negative regulator referenced to ground. The output resistor divider must be set to provide a 1.24V at the ADJ pin with respect to V_{OUT}. For example, a –3V output would require a 13k resistor from GND to ADJ, and a 9.1k resistor to SENSE/V_{OUT}. If, after connecting the divider resistors, the output voltage is not what you expected, try swapping them.

CAPACITOR SELECTION

The LTC1550/LTC1551 requires four external capacitors: an input bypass capacitor, two 0.1µF charge pump capacitors and an output filter capacitor. The overall behavior of the LTC1550/LTC1551 is strongly affected by the capacitors used. In particular, the output capacitor has a significant effect on the output ripple and noise performance. Proper capacitor selection is critical for optimum performance of the LTC1550/LTC1551.

Output Ripple vs Output Capacitor

Figure 3 shows the effect of using different output capacitor values on LTC1550/LTC1551 output ripple. These curves are taken using the circuit in Figure 2, with C_{IN} = 4.7µF and I_{LOAD} = 5mA. The upper curve shows the performance with a standard tantalum capacitor alone and the lower curve shows the tantalum capacitor in parallel with a 0.1µF ceramic capacitor. As a general rule, larger

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output capacitors provide lower output ripple. To keep ripple below 1mV$_{P-P}$, 10µF or greater, with a 0.1µF ceramic capacitor in parallel, is required. At least 4.7µF is required at the output under all conditions to guarantee loop stability.

Figure 3 shows a marked decrease in peak-to-peak output ripple when a 0.1µF ceramic capacitor added in parallel with the tantalum output capacitor. The additional ripple with the tantalum output capacitor alone is mostly very high order harmonics of the 900kHz clock, which appear as sharp "spikes" at the output. The energy in these spikes is very small and they do not contribute to the RMS output voltage, but their peak-to-peak amplitude can be several millivolts under some conditions. A garden variety 0.1µF ceramic capacitor has significantly lower impedance at the spike frequency than even a large tantalum capacitor, and helps eliminate most of these left-over switching spikes that the tantalum capacitor leaves behind. Figure 4 and 5 show scope photos of the output of Figure 3 with and without the additional ceramic capacitor at the output.

A series RC or LC filter can reduce high frequency output noise even further. Due to the high 900kHz switching frequency, not much R or L is required; a ferrite bead or a relatively long PC board trace in series with 0.1µF ceramic capacitor will usually keep the output ripple well below 1mV$_{P-P}$. The cover page shows an example of an ultralow

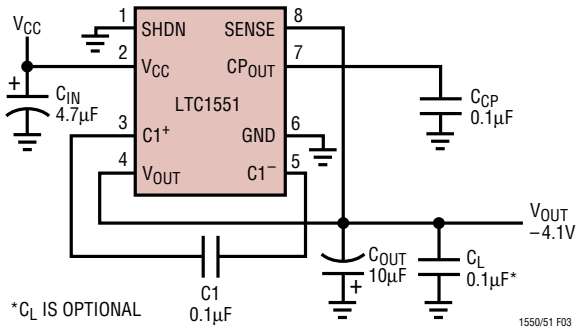


Figure 2. Output Ripple Test Circuit

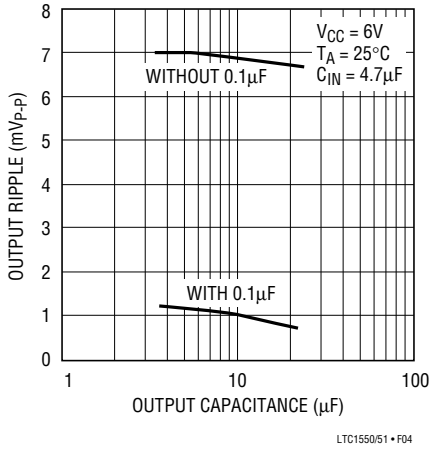


Figure 3. Output Ripple vs Output Capacitance

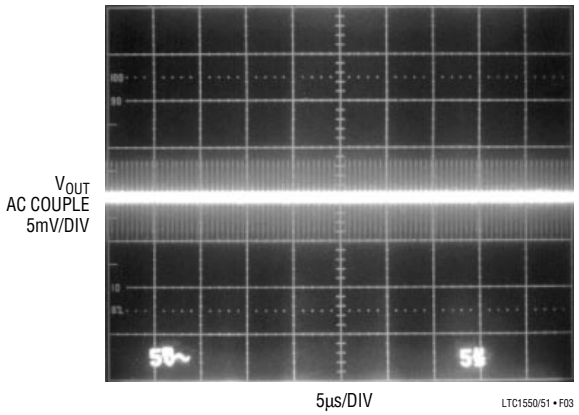


Figure 4. Output Ripple with 10µF Tantalum Capacitor

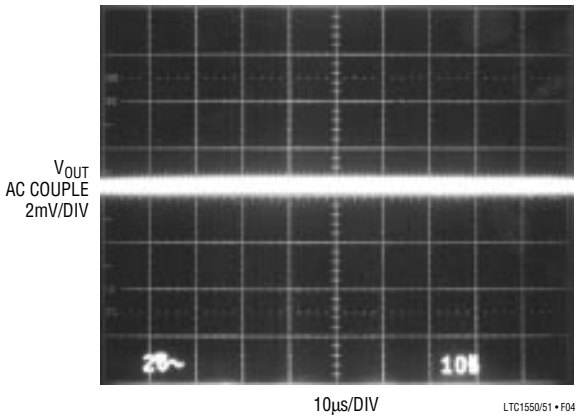


Figure 5. Output Ripple with 10µF Tantalum Capacitor Paralleled with 0.1µF Ceramic Capacitor

APPLICATIONS INFORMATION

noise –4.1V generator which uses a ferrite bead output filter to achieve better than 1mV$_{P-P}$ noise and output ripple. The corresponding spectrum and spot noise plots for this circuit are shown in the Typical Performance Characteristics section.

Output Ripple vs Input Bypass Capacitor

The input bypass capacitor (C_{IN}) can also have a fairly significant impact on the output ripple. C_{IN} provides most of the LTC1550/LTC1551's supply current while it is charging the flying capacitor (C1). Inadequate input bypass can cause the V_{CC} supply to dip when the charge pump switches, causing the output linear regulator to momentarily stop regulating. C_{IN} should be mounted as close to the LTC1550/LTC1551 as possible and its value should be significantly larger than C1. Tantalum capacitors with low ESR generally provide adequate performance. Figure 6 shows the LTC1550/LTC1551 peak-to-peak output ripple vs C_{IN}, taken using the test circuit in Figure 2 with I_{LOAD} set at 5mA. C_{OUT} is a 10µF in parallel with a 0.1µF ceramic capacitor.

A 4.7µF tantalum capacitor at V_{CC} generally provides adequate output ripple performance for most applications.

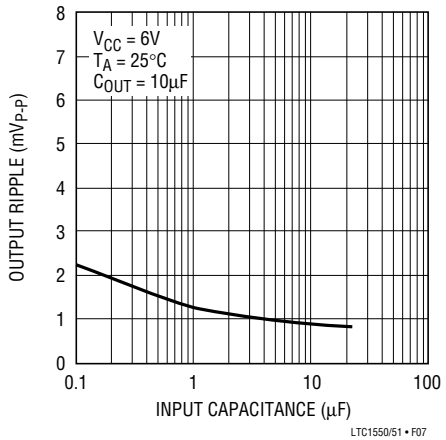
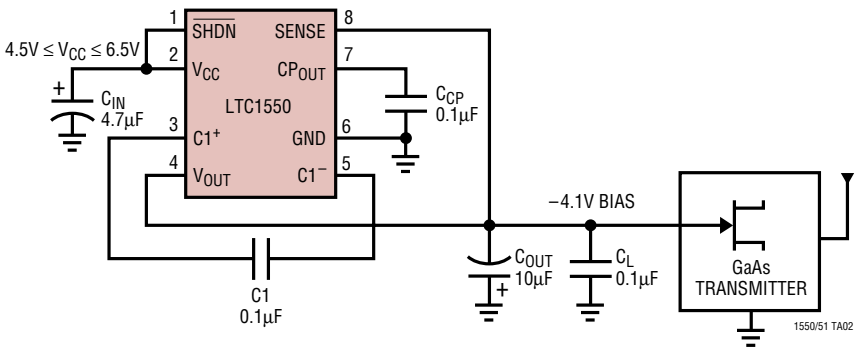


Figure 6. Output Ripple vs Input Bypass Capacitance

TYPICAL APPLICATION

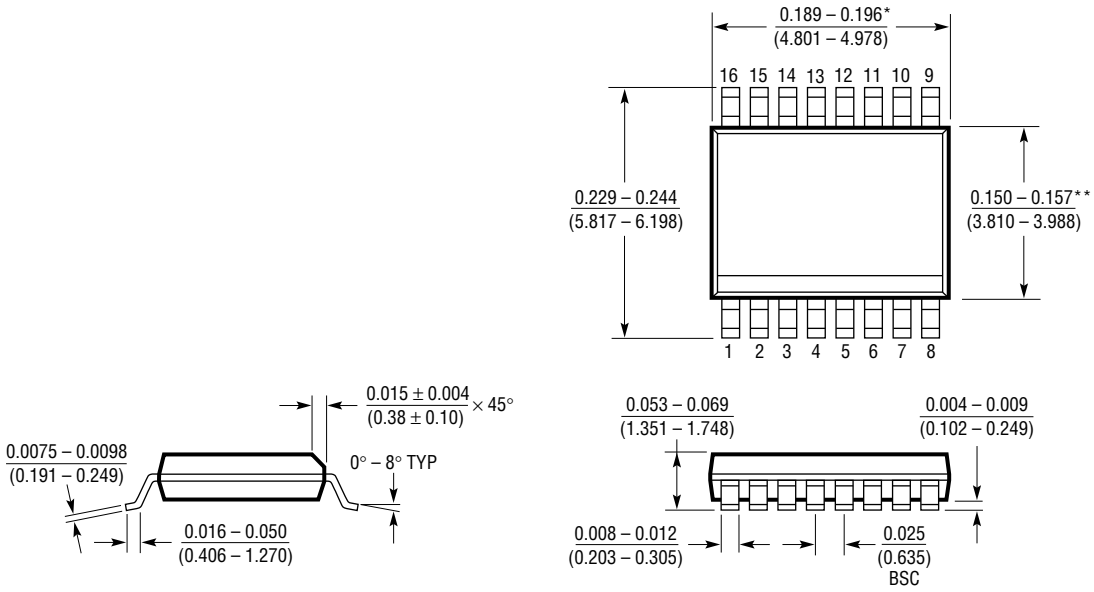
–4.1V Output GaAs FET Bias Generator



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

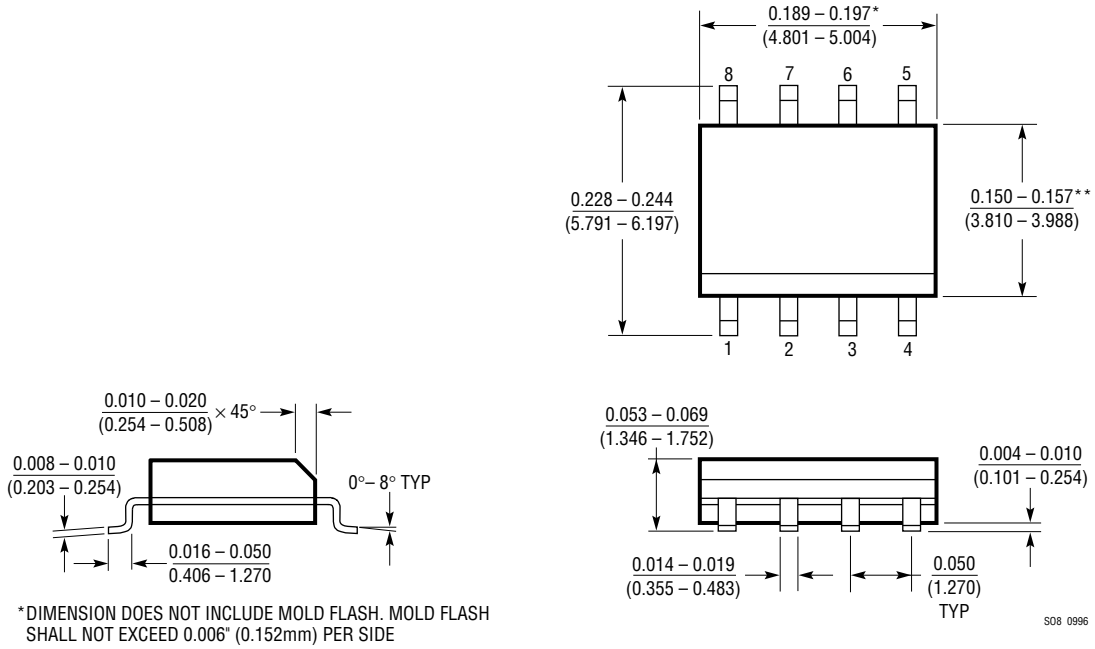
** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0895

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

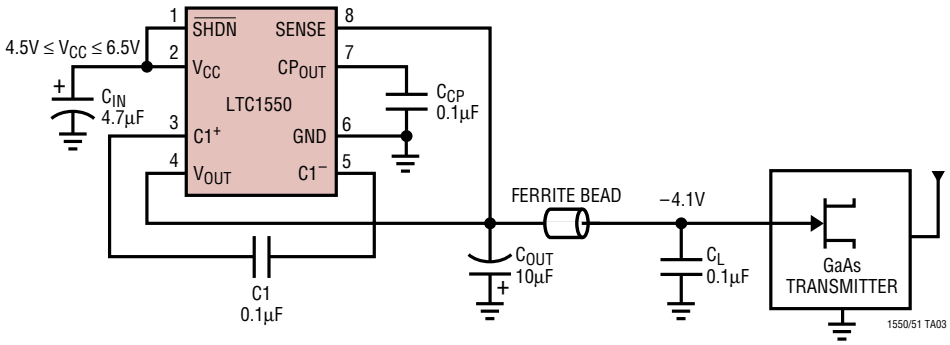


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

< 1mV$_{P-P}$ Ripple, –4.1V Output GaAs FET Bias Generator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1054	Switched-Capacitor Voltage Converter with Regulator	100mA Switched-Capacitor Converter
LTC1261	Switched-Capacitor Regulated Voltage Inverter	Selectable Fixed Output Voltages
LTC1429	Clock-Synchronized Switched-Capacitor Voltage Inverter	Synchronizable Up to 2MHz System Clock

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