HIGHLY INTEGRATED ACTIVE CLAMP FLYBACK PWM CONTROLLER

Description

The DIODES™ AP3306 is a highly integrated Active Clamp Flyback (ACF) controller optimally designed for offline power supplies to meet ultra-low standby power, high power density, and comprehensive protection requirements. The controller realizes non-complimentary high-low-side control mechanisms to achieve Leakage Energy Recycling and Zero Voltage Switching (ZVS) for supreme-efficiency performance.

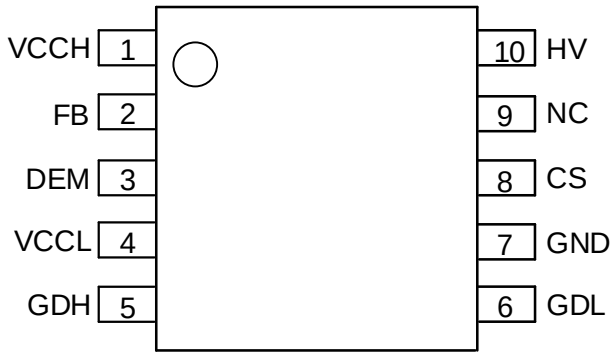
The AP3306 provides a high-voltage start-up function through the HV pin, reducing standby loss. Moreover, the AP3306 integrates a VCCL LDO circuit, allowing the LDO to regulate the wide range VCCL to an acceptable value. This makes the AP3306 an ideal candidate for wide-range output-voltage applications, such as USB-PD. The built-in frequency dithering function greatly eases EMI design as well.

At no load or light load, the IC will enter burst mode to minimize standby power consumption. The minimum switching frequency (about 22kHz) is set to avoid audible noise. When the load increases, the IC will enter ACF mode with frequency foldback to improve system efficiency and EMI performance. The maximum switching frequency (about 130kHz or 200kHz optional) is set to clamp the switching frequency to reduce switching power loss.

Comprehensive protection features are included, such as Brown-Out Protection (BNO), Cycle-by-Cycle Overcurrent Protection (OCP), VCC Overvoltage Protection (VOVP), Secondary-Side Output OVP (SOVP) and UVP (SUVP), internal Overtemperature Protection (OTP), Overload Protection (OLP), and Pin Fault Protection.

Pin Assignments

(Top View)



SO-10 (Type A1)

Features

- Active Clamp Flyback Topology with Recycled Leakage Energy and Pseudo Zero Voltage Switching Functions
- High-Voltage Startup
- Embedded VCC LDO for VCCL Pin to Guarantee Wide Range Output Voltage
- Non-Audible-Noise Quasi-Resonant Control
- Soft Start During Startup Process
- Frequency Foldback for High Average Efficiency
- Secondary Winding Short Protection with FOCP
- Frequency Dithering for Reducing EMI
- X-CAP Discharge Function
- Useful Pin Fault Protection
- CS Pin Floating Protection
- FB/Opto-Coupler Open/Short Protection
- Comprehensive System Protection Features:
  - VCC Overvoltage Protection (VOVP)
  - Overload Protection (OLP)
  - Brown-Out Protection (BNO)
  - Secondary-Side OVP (SOVP) and UVP (SUVP)
- Packaged in the SO-10 (Type A1)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Smartphone quick chargers
- Notebook computer adapters
- High-Power density adapters/chargers: 30W/inch^3
- Compact switching AC-DC adapter/charger
- Suitable for variable output voltage applications (USB PD, QC, SCP, VSCP, VOOC, AFC, etc.)
- ATX/BTX auxiliary power applications
- Set-top box (STB) power supplies
- Open-frame switching power supplies

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

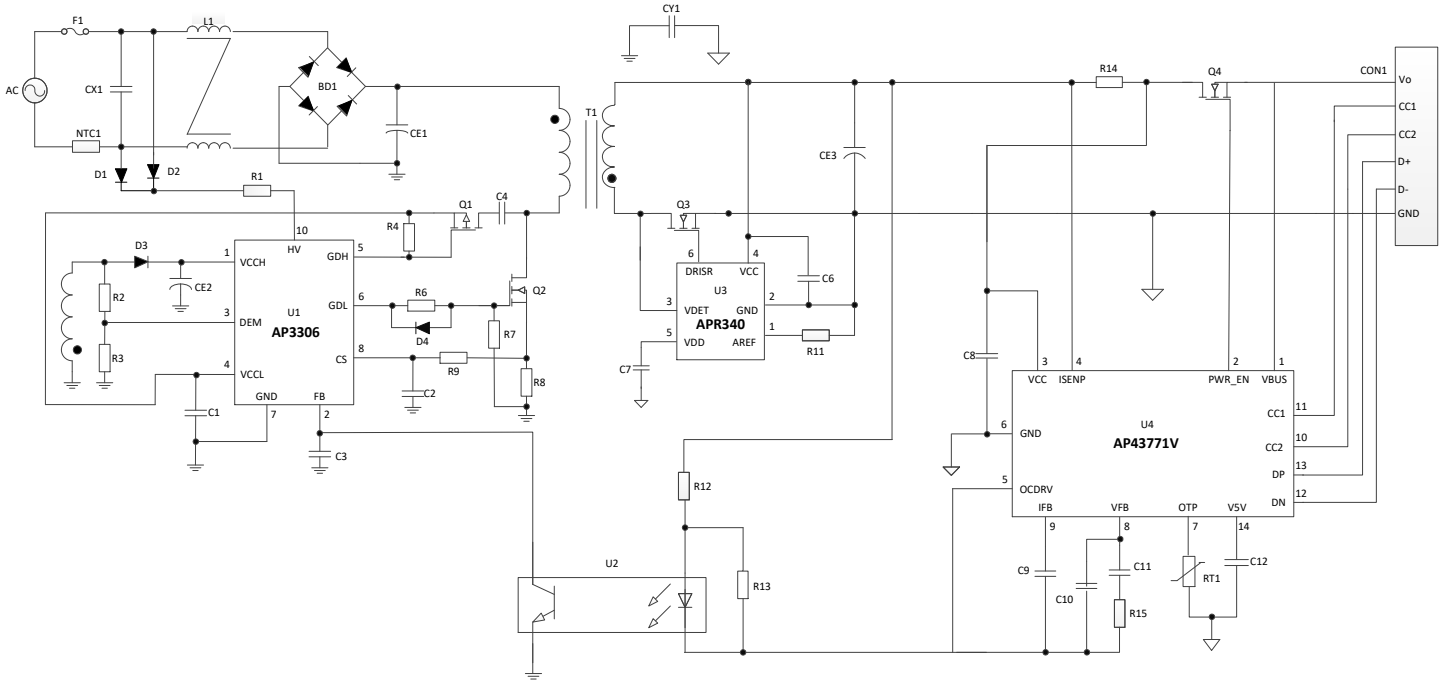


Figure 1. Typical Application Circuit of AP3306 for PD3.0 PPS Charger

Pin Descriptions

Pin Name	Pin Number	Function
VCCH	1	Wide range input supply voltage to produce V_{CC}
FB	2	Feedback. Directly connected to the opto-coupler
DEM	3	Peak and valley detection for ZVS control, sample output voltage for SOVP and SUVP, set OCP line compensation current.
VCCL	4	Supply voltage of driver and control circuits
GDH	5	Gate driver output to drive high side P MOSFET
GDL	6	Gate driver output to drive low side N MOSFET
GND	7	Signal ground. Current return for driver and control circuits
CS	8	Current sense
NC	9	Not connected
HV	10	High voltage input. Sense line voltage and provide startup current to V_{CC}

Functional Block Diagram

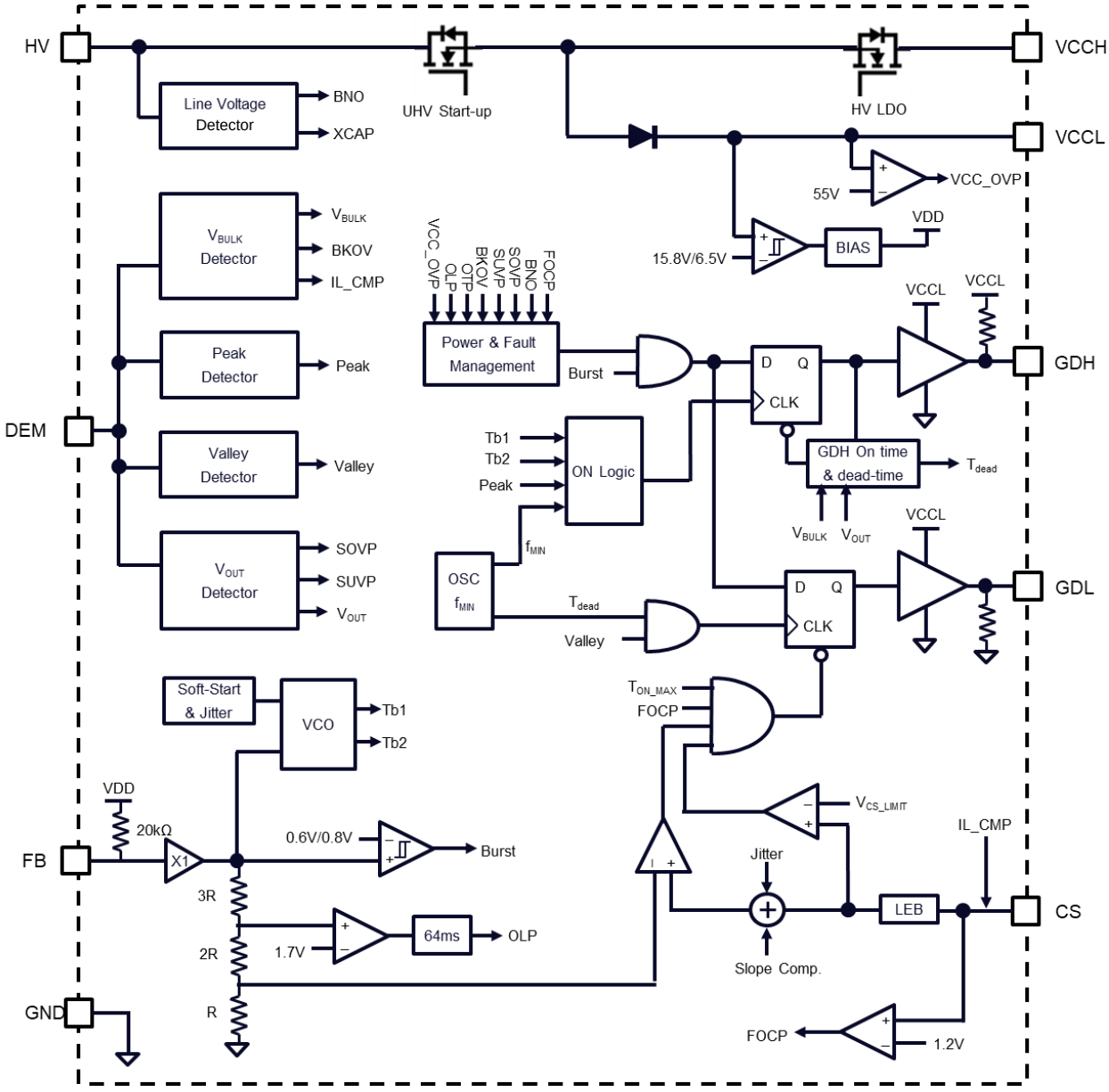


Figure 2. Functional Block Diagram of AP3306

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{HT}	HV Pin Input Voltage	700	V
V_{CCH}	LDO Supply Voltage	120	V
V_{CCL}	Power Supply Voltage	60	V
I_O	Gate Output Current	-800 to +300	mA
V_{FB}, V_{CS}, V_{DEM}	Input Voltage to FB, CS, DEM	-0.3 to 6.5	V
θ_{JA}	Thermal Resistance (Junction to Ambient)	165	°C/W
P_D	Power Dissipation at T_A < +25°C	550	mW
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature Range	+150	°C
ESD	Human Body Model	2000	V
ESD	Charged Device Model	1250	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CCL}	Power Supply Voltage	10	50	V
T_A	Ambient Temperature	-40	+85	°C

Electrical Characteristics (@ T_A = +25°C, V_{CCL} = 18V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltage (VCCL Pin)						
I_{ST}	Startup Current	V_{CCL} = 14.8V	—	1	10	μA
I_{CC}	Operating Supply Current	V_{FB} = 2.5V, C_{GDL} = 1nF, C_{GDH} = 0.47nF	1.5	2.2	2.9	mA
I_{BURST}	Operating Current at Burst	V_{FB} = 0V, C_{GDL} = 1nF, C_{GDH} = 0.47nF	—	0.33	—	mA
V_{ST}	Turn-On Threshold Voltage	—	14.8	15.8	16.8	V
$V_{CCL-UVLO}$	VCCL UVLO Voltage	—	—	6.5	7	V
$V_{CCL-OVP}$	VCCL OVP Threshold Voltage	—	50	55	—	V
HV Section (HV Pin)						
I_{CHARGE}	Charge Current	V_{CCL} = 10V, V_{HV} = 50V	—	2	—	mA
V_{BR-IN}	Brown-In Voltage	—	92	102	112	V
V_{BR-HYS}	Voltage Gap Between Brown-In and Brown-Out Voltage	—	7	8.5	—	V
t_{BR-OUT}	Delay of Brown Out	—	—	64	—	ms
$I_{DISCH-X}$	X-CAP Discharge Current	V_{CCL} = 10V, V_{HV} = 50V	—	2	—	mA
PWM Section/Oscillator Section						
t_{ON-MAX}	Maximum Duty Cycle	—	—	14	—	μs
$f_{PWM-MAX}$	Maximum Clamp Frequency (Non-Jitter)	—	110	125	140	kHz
$f_{OSC-MIN}$	Minimum Clamp Frequency (Non-Jitter)	—	20	22	—	kHz
$f_{OSC-JITTER}$	Frequency Dithering (Note 5)	—	—	±3	—	%
Current Sense Section (CS Pin)						
V_{CS-MAX}	Maximum Sense Voltage	—	0.51	0.56	0.61	V
$V_{TH-FOCP}$	FOCP Voltage	—	1.0	1.2	1.4	V
$t_{DELAY-FOCP}$	FOCP Debounce Time	—	—	7	—	Cycles
t_{LEB}	LEB Time Of Sense	—	—	500	600	ns
Feedback Input Section (FB Pin)						
K_{FB-CS}	The Ratio of FB Input Voltage to Current Sense Voltage	—	—	6	—	V/V
R_{FB}	Input Impedance	—	—	22	—	kΩ
$t_{DELAY-OLP}$	Delay of OLP Protection	—	—	64	—	ms
$I_{FB-SOURCE}$	Source Current	V_{FB} = 0V	—	0.2	—	mA
$V_{BURST-ET}$	Threshold for Entering Burst Mode	—	0.54	0.6	0.66	V
$V_{BURST-ED}$	Threshold for Ending Burst Mode	—	0.72	0.8	0.88	V

Note: 5. Guaranteed by design.

Electrical Characteristics (@ T_A = +25°C, V_{CCL} = 18V, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Output Section (GDH/GDL Pin)						
V_{GDL-L}	Output Low-Level Voltage	I_O = 10mA, V_{CCL} = 18V	—	—	0.8	V
V_{GDL-H}	Output High-Level Voltage	I_O = 10mA, V_{CCL} = 18V	7	—	—	V
$V_{GDL-CLP}$	High-Level Clamping Voltage	V_{CCL} = 18V	8	9.5	11	V
$t_{GDL-RISE}$	Rising Time (Note 5)	C_L = 1nF, V_{CCL} = 18V	—	70	200	ns
$t_{GDL-FALL}$	Falling Time (Note 5)	C_L = 1nF, V_{CCL} = 18V	—	20	80	ns
V_{GDH-L}	Output Low-Level Voltage (Note 6)	I_O = 10mA, V_{CCL} = 18V	—	—	0.8	V
V_{GDH-H}	Output High-Level Voltage (Note 6)	I_O = 10mA, V_{CCL} = 18V	7	—	—	V
$V_{GDH-CLP}$	High-Level Clamping Voltage (Note 6)	V_{CCL} = 18V	8	9.5	11	V
$t_{GDH-RISE}$	Rising Time (Note 5)	C_L = 0.5nF, V_{CCL} = 18V	—	100	250	ns
$t_{GDH-FALL}$	Falling Time (Note 5)	C_L = 0.5nF, V_{CCL} = 18V	—	30	100	ns
De-Magnetization Section (DEM Pin)						
V_{QR}	Demagnetization Voltage	—	—	100	—	mV
I_{TH-ZVS}	ZVS Mode Thershold.		—	315	—	μA
$V_{TH-SOVP}$	SOVP Threshold	—	3.0	3.2	3.4	V
$V_{TH-SUVP}$	SUVP Threshold	—	0.34	0.4	0.46	V
t_{SAMPLE}	Sample Delay Time (Note 5)	—	—	1.8	—	μs
LDO Section (VCCH Pin/VCCL Pin)						
$V_{THLDO-ON}$	LDO turn-on threshold	V_{CCH} = 20V	8.5	9.5	—	V
$V_{THLDO-OFF}$	LDO turn-off threshold	V_{CCH} = 30V	—	—	20	V
I_{LDO}	Operating Current	V_{CCL} = 8V, V_{CCH} = 12.5V	4	—	—	mA
Internal OTP Section						
T_{OTP}	OTP Threshold	—	—	+150	—	°C
T_{HYS}	OTP Recovery Hysteresis	—	—	+25	—	°C

Note: 5. Guaranteed by design.
6. AP3306 controls a PMOS switch by driving the gate of the PMOS with GDH and connecting the source of the PMOS to VCCL. Thus, the spec. V_{GDH-L} shows the small voltage difference between VCCL pin and GDH pin for turning off the PMOS, and the spec. V_{GDH-H} shows the large voltage difference for turning on. Furthermore, the $t_{GDH-RISE}$ measures the increasing of voltage difference between VCCL pin and GDH pin and the $t_{GDH-FALL}$ measures the decreasing of voltage difference between VCCL pin and GDH pin.

Operation Description

Diodes Incorporated's Smart Active Clamp Control Strategy: Valley Switching & Zero Voltage Switch (ZVS) Multiple Operation Modes.

The AP3306's patented control strategy allows the Active Clamp Fly-back system to operate on valley switching or ZVS according to the input voltage. When operating under low line input, the valley switching can naturally achieve ZVS and the leakage inductance energy will be transferred to output through the high side PMOSFET and C_{SN}. When operating under high line input, the ZVS mode activated with perfect jitter whilst balancing system efficiency and EMI performance. The ZVS with jitter operation is regarded as a quasi-soft switching technology, which always turns on the primary PMOSFET at the peak status of the Drain-to-Source voltage (V_{DS}) and uses leakage inductance to achieve ZVS with jitter.

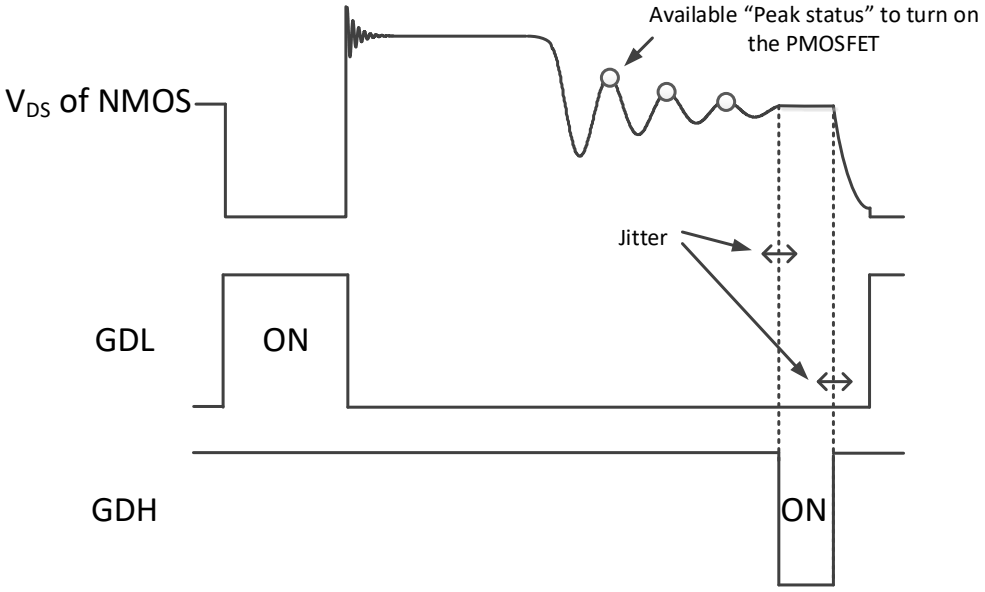


Figure 3. ZVS with Jitter Operation

PMOS Driving

Figure 4 shows the AP3306's easily built-in PMOS control method. The GDH pin connects to the PMOS's gate, the PMOS's source pin connects to VCCL, and the PMOS's drain pin connects to C_{SN}. The AP3306 drives PMOS on by pulling down the GDH pin voltage, and turns off PMOS by pulling up on the GDH pin to VCCL.

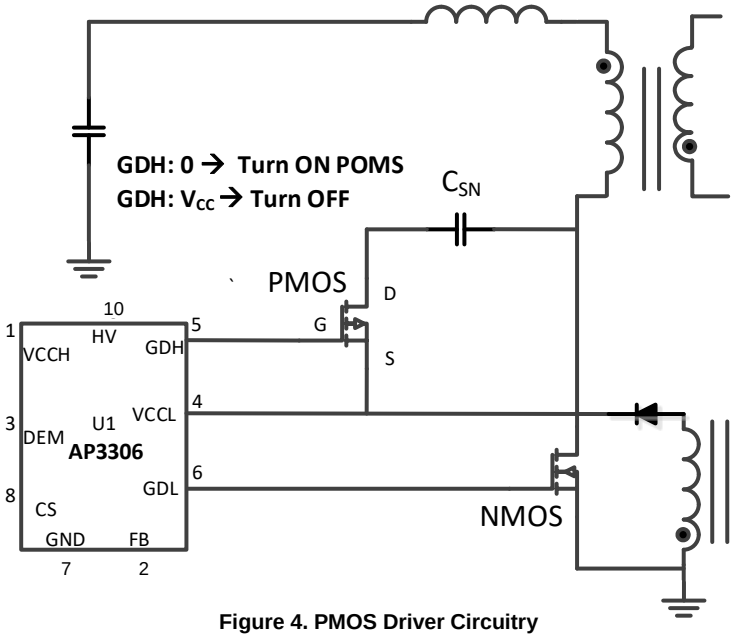


Figure 4. PMOS Driver Circuitry

Operation Description (continued)

Frequency Modulation Strategy

The AP3306 operates with valley switching, ZVS mode, green mode, and burst mode to achieve high-efficiency performance.

In general, the AP3306 power system operates with first “valley status” under low-line and full-load conditions, where the maximum primary peak current and transformer flux density can occur. The power system designer is thus required to choose the transformer size and switching frequency according to this worst-case condition.

With output load decreasing from full load in the first “valley status”, the switching frequency of the AP3306 increases accordingly. In order to avoid performance degradation at very high switching frequency operation, there is a fixed 125kHz maximum frequency limitation in the AP3306. Since a too high switching frequency will lead to worsening performance, the AP3306 has a built-in reference in the FB pin voltage to adjust “peak status” for green-mode operation, as shown in Figure 5. When the FB pin voltage decreases to a modulating reference, the first “valley status” is forced to shift to another available “valley status”.

The AP3306 has a minimum switching frequency limit of 22kHz to avoid audible noise issues. When the switching frequency decreases to 22kHz with output load decreasing, the switching frequency will remain at 22kHz. When the FB pin voltage is lower than V_{BURST}, the power system enters burst mode to reduce power dissipation under very light load conditions.

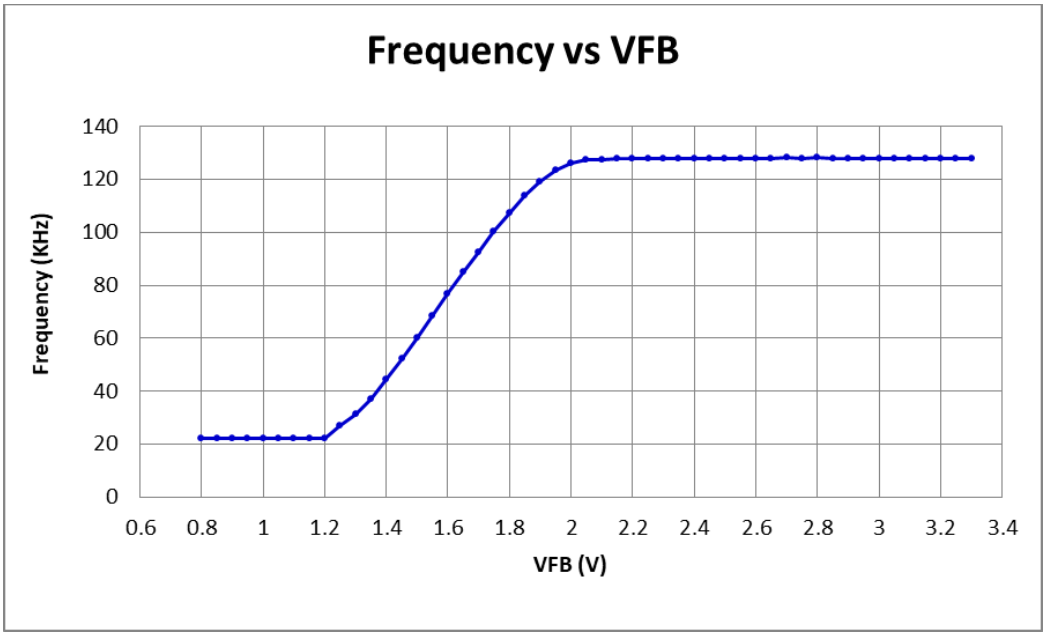


Figure 5. Frequency Curve

HV Start-Up Circuit for AP3306 Only

A built-in HV start-up circuit in the AP3306 can help to simplify the power system design for ultra-low standby application. For AP3306, there are two HV start-up charging currents: the $I_{CHARGE-L}$ when V_{CC} is lower than 6V; and the $I_{CHARGE-H}$ when the V_{CC} voltage rises above 6V, which can prevent the IC from overheating when V_{CC} short-to-GND fault occurs. The HV start-up circuit will stop working with no additional power dissipation when the V_{CC} voltage reaches the V_{ST}, at which point the AP3306 will begin working and will supply energy to V_{CC} from auxiliary winding.

However, the charging process described above is only for the normal system startup condition. Once some system faults occur and the protection process triggers, the AP3306 will shut down and V_{CC} voltage will begin to decrease. The HV start-up circuit starts working again when the V_{CC} voltage decreases below $V_{CC-UVLO}$, and charges the V_{CC} capacitor with the current of $I_{CHARGE-FAULT}$. This special design can hugely reduce the input power dissipation when system faults occur, especially for output short conditions. The HV start-up circuit-working processes are illustrated in Figure 6.

Operation Description (continued)

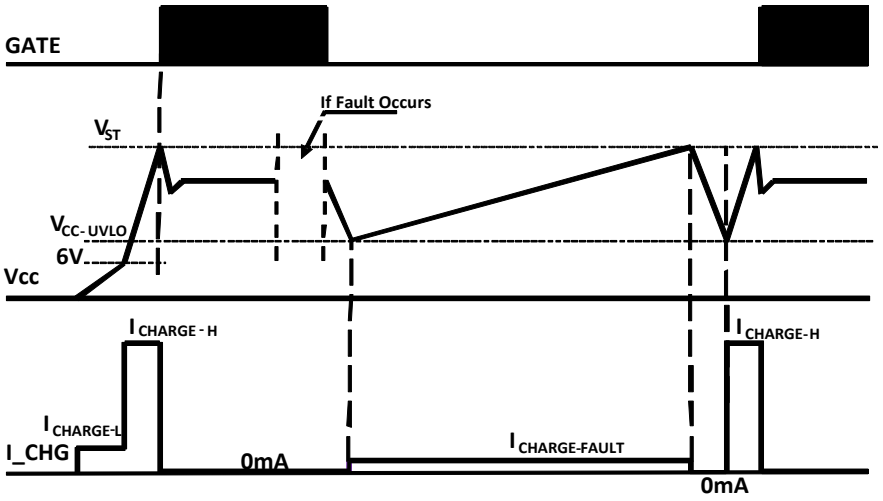


Figure 6. HV to VCCL Charge Current

X-CAP Discharge Function

To attenuate the differential-mode noise for higher power applications, an X-CAP is used before the rectifier bridge. Also present are paralleled resistors to discharge the X-CAP for safety consideration when the AC line is off. The paralleled resistors have large power dissipation and will increase standby power. The AP3306 integrates an X-CAP discharge function to replace discharge resistors and decrease the standby power.

This function contains two processes; the first process detects the condition of the AC line through the HV pin, with the detected voltage named V_B. When the system is plugged in, an inner timer of 40ms within the AP3306 begins to work. Meanwhile, a phase-drifted and filtered signal V_C is generated based on V_B, compared to V_B with V_C, as shown in Figure 7.

Whenever signal V_C crosses over with signal V_B, the inner 40ms timer will reset, representing that the AC line is on. If the system is disconnected from the AC line, the cross-over signal of V_C and V_B will disappear and the 40ms timer will continue to count until it reaches 40ms. At this moment, the second process (discharge process) will come into effect and a 1.7mA discharge current will flow through the HV pin to GND, lasting for 40ms. After the AC line is off, the first process and the second process will act alternately until the HV pin voltage is discharged below 10V, even when the V_{CC} voltage is lower than $V_{CC-UVLO}$.

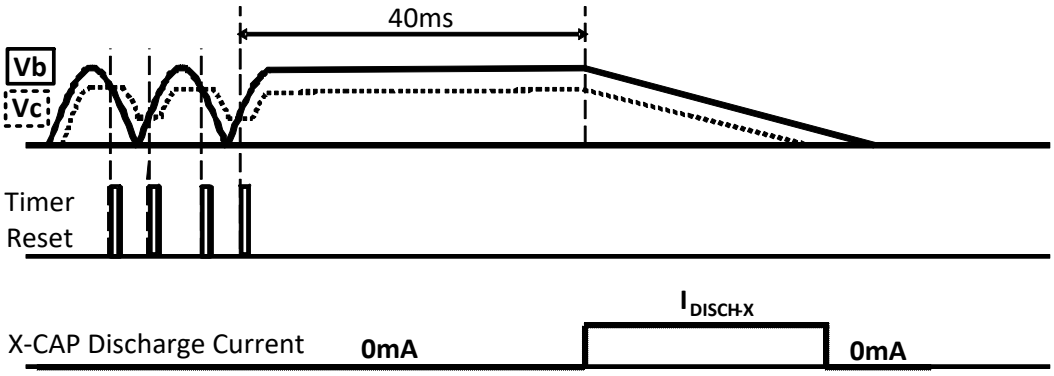


Figure 7. X-CAP Discharge

Built-In V_{CC} LDO

The AP3306 integrates a V_{CC} LDO circuitry. The LDO regulates the wide-range V_{CC_IN}, which is rectified from auxiliary winding to an acceptable value. This makes the AP3306 a good choice in wide-range output-voltage applications.

Operation Description (continued)

Brown-In/Out Protection

To avoid potential high-current stress at low-line voltage, the AP3306 introduces a reliable brown-out protection. The AC line voltage is detected through the HV pin. A pair of high-voltage diodes are connected to the AC line, which will rectify the AC input voltage to a double-frequency positive voltage referring to GND. A 20kΩ resistor is recommended to be added to improve surge immunity. When the voltage across the HV pin is higher than V_{BR-IN} for about 100μs once t_{BR-IN} and V_{CC} reaches V_{ST}, the GDL pin will output drive signals and the system will start to work. If the HV pin voltage falls below V_{BR-OUT} and lasts for 50ms of t_{BR-OUT}, the GDL pin will turn off and the system will shut down until the line voltage rises over its brown-in voltage again.

SOVP/SUVP Protection

The AP3306 provides output OVP and UVP protection functions. The auxiliary winding voltage during the secondary rectifier conducting period reflects the output voltage. A voltage divide network is connected to the auxiliary winding and DEM pin. The DEM pin will detect the equivalent output voltage with a delay of t_{SAMPLE} from the falling edge of the GATE driver signal, as shown in Figure 8. The detected voltage will be compared to the SOVP and SUVP threshold voltage $V_{TH-SOVP}$ and $V_{TH-SUVP}$. If the SOVP threshold is reached continuously by seven switching cycles, SOVP protection will trigger. If the SUVP threshold is reached continuously and the FB voltage is pulled high, SUVP protection will trigger. The AP3306 will shut down after protection is triggered and the system will restart when the V_{CC} voltage falls below the UVLO voltage.

To prevent a false-trigger of SUVP during the start-up process, a blank time of $t_{BLANK-SUVP}$ is set, during which the SUVP protection function is ignored.

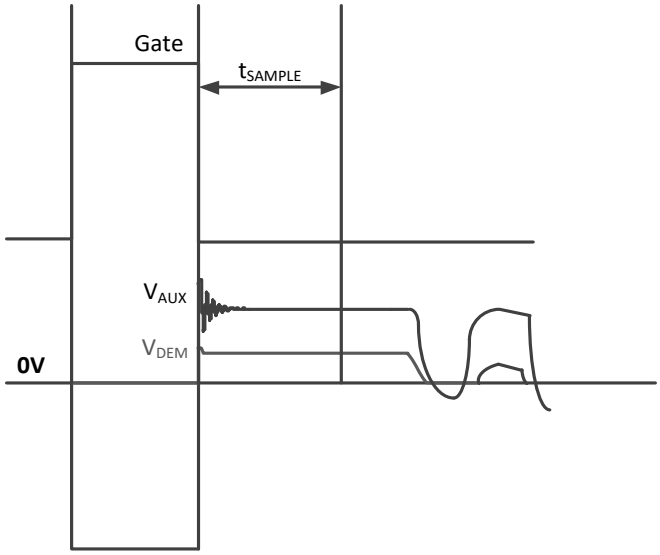


Figure 8. Secondary-Side Voltage Sampling

System Protection

LOVP, FOCP, SSCP, VCC OVP, OTP

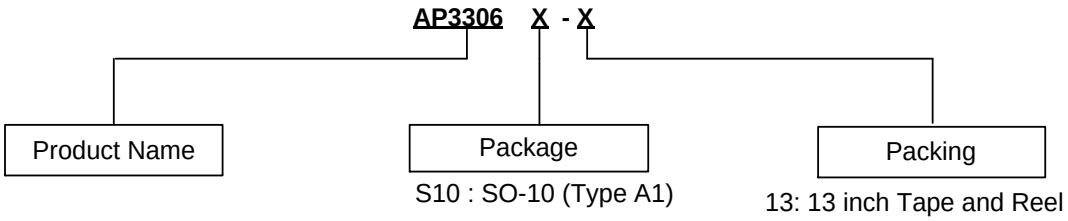
The AP3306 provides versatile protections to ensure the reliability of the power system. LOVP achieves line-voltage overvoltage protection. If the detected AC line voltage is higher than V_{LOVP} for seven switching cycles, the LOVP protection will trigger.

FOCP protection is an ultra-fast short-current protection, which is helpful to avoid catastrophic damage of the system when the secondary rectifier is short. The primary peak current will be monitored by the CS pin through a primary sense resistor. Whenever the sampled voltage reaches the threshold of $V_{TH-FOCP}$ for seven switching cycles continuously, FOCP protection will activate to shut down the switching pulse.

SSCP may trigger at ultra-low DC bus voltage conditions or other failure conditions that short the CS pin to ground. The SSCP module senses the voltage across the primary sense resistor with a delay of 3μs after the rising edge of primary GATE signal. This sensed signal is compared with $V_{TH-SSCP}$. If it is lower than $V_{TH-SSCP}$ for seven switching cycles, the SSCP protection will trigger and the driving signal will disable.

All the protections described above will restart the system when the V_{CC} voltage falls below UVLO.

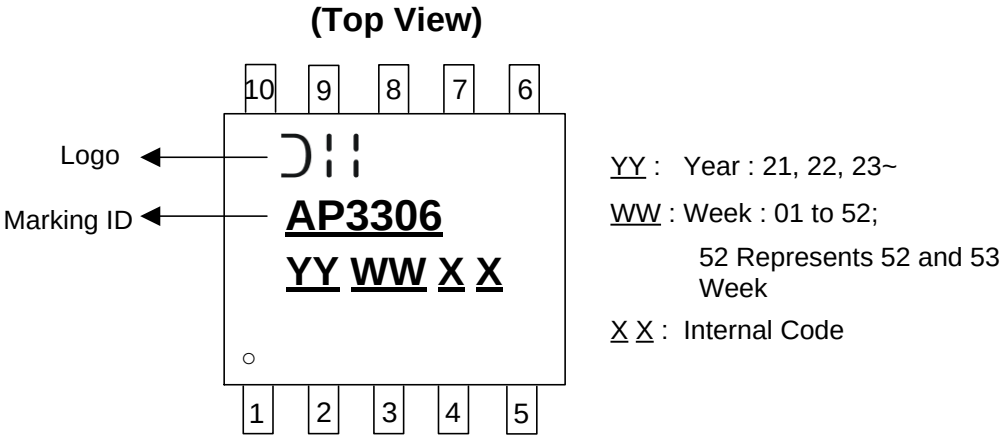
Ordering Information



Part Number	Marking ID	Package	Packing
AP3306S10-13	AP3306	SO-10 (Type A1)	2,500/13" Tape and Reel

Marking Information

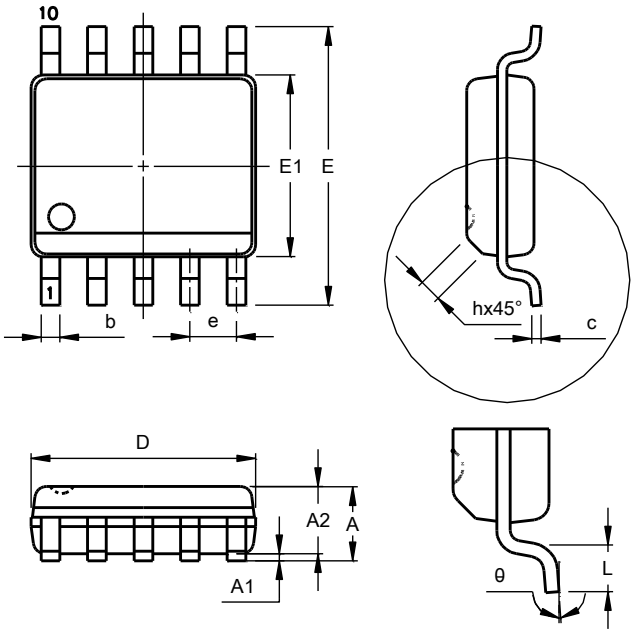
SO-10 (Type A1)



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-10 (Type A1)

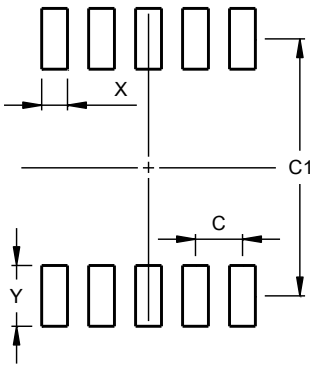


SO-10 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	--	1.75	--
A1	0.10	0.25	--
A2	1.25	--	--
b	0.30	0.45	--
c	0.10	0.25	--
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.00 BSC		
h	0.25	0.50	--
L	0.40	1.27	--
θ	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-10 (Type A1)



Dimensions	Value (in mm)
C	1.00
C1	5.50
X	0.55
Y	1.30

Mechanical Data

- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Finish—Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.079 grams (Approximate)

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