THIS SPEC IS OBSOLETE

Spec No: 38-05392

Spec Title: CY62157DV30 MOBL(R) 8-MBIT (512K X 16) MOBL(R) STATIC RAM

Sunset Owner: Ramesh Raghavan (rame)

Replaced by: NONE

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CY62157DV30 MoBL®

8-Mbit (512K x 16) MoBL® Static RAM

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Features

- Temperature ranges
  - Industrial: –40 °C to 85 °C
- Very high speed: 55 ns
- Wide voltage range: 2.20 V–3.60 V
- Pin-compatible with CY62157CV25, CY62157CV30, and CY62157CV33
- Ultra-low active power
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 12 mA @ f = f_{max}
- Ultra-low standby power
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Available in Pb-free and non Pb-free 48-ball fine ball grid array (FBGA), and Pb-free 44-pin thin small outline package (TSOPII) package

Functional Description

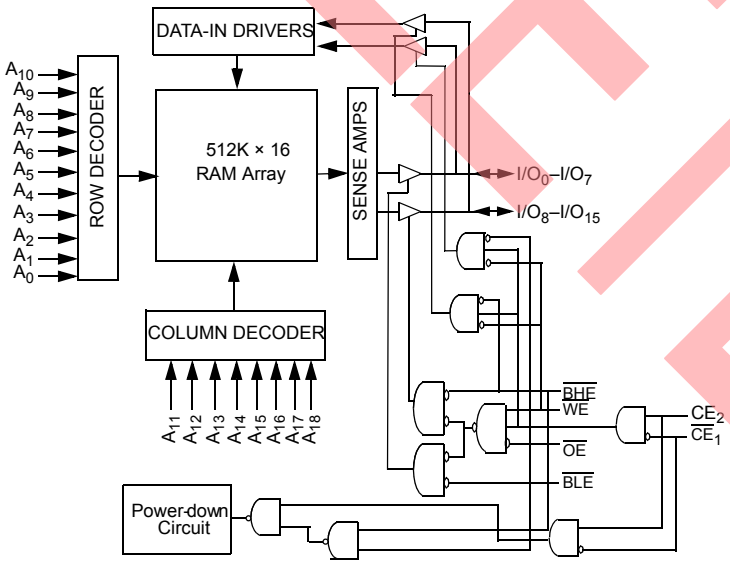
The CY62157DV30 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones.The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



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Contents

Product Portfolio **3**
Pin Configuration **3**
Maximum Ratings **4**
Operating Range **4**
Electrical Characteristics **4**
Capacitance **4**
Thermal Resistance **5**
AC Test Loads and Waveforms **5**
Data Retention Characteristics 5
Data Retention Waveform **5**
Switching Waveforms **7**
Truth Table **10**
Ordering Information **11**
Ordering Code Definition 11
Package Diagram **12**
Acronyms **13**
Document Conventions **13**
Units of Measure 13
Document History Page **14**
Sales, Solutions, and Legal Information **15**
Worldwide Sales and Design Support 15
Products 15
PSoC Solutions 15

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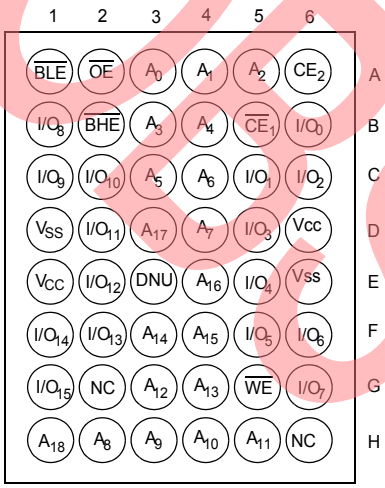
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Product Portfolio

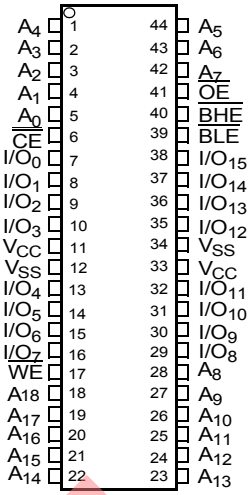
Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby I_{SB2}, (µA)	
						f = 1MHz		f = f_{max}			
		Min	Typ[1]	Max		Typ[1]	Max	Typ[1]	Max	Typ[1]	Max
CY62157DV30LL	Industrial	2.2	3.0	3.6	55, 70	1.5	3	12	15	2	8

Pin Configuration[2, 3, 4]

48-Ball FBGA Pinout
Top View



44-pin TSOP II Pinout
Top View



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Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, T_A = 25 °C.
2. NC pins are not internally connected on the die.
3. DNU pins have to be left floating.
4. The 44-TSOPII package device has only one chip enable pin ($\overline{CE}$).

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Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High-Z State[5, 6] ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage[5, 6] ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... >2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature (T_A)	V_{CC}[7]
CY62157DV30LL	Industrial	–40 °C to +85 °C	2.20 V to 3.60 V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			-55 Min	-55 Typ[8]	-55 Max	Unit
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20 V		2.0	–	–	V
		I_{OH} = –1.0 mA	V_{CC} = 2.70 V		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20 V		–	–	0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70 V		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V			1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V			2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V			–0.3	–	0.6	V
		V_{CC} = 2.7 V to 3.6 V			–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	Ind'l		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled	Ind'l		–1	–	+1	µA
I_{CC}	V_{CC} Operating supply current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels	LL	–	12	15	mA
		f = 1 MHz		LL		1.5	3	mA
I_{SB1}	Automatic Power-down current — CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$), V_{CC} = 3.60V	Ind'l	LL	–	2	8	µA
I_{SB2}	Automatic Power-down current -CMOS inputs	$\overline{CE_1}$ ≥ V_{CC}– 0.2 V or CE_2 ≤ 0.2 V, ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.60 V	Ind'l	LL	–	2	8	µA

Capacitance

Parameter[9, 10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Notes

5. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC}+0.75 V for pulse duration less than 20 ns.
7. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VCC = VCC(typ), TA = 25 °C
9. Tested initially and after any design or process changes that may affect these parameters.
10. The input capacitance on the CE_2 pin of the FBGA package and on the $\overline{BHE}$ pin of the 44TSOPII package is 15 pF.

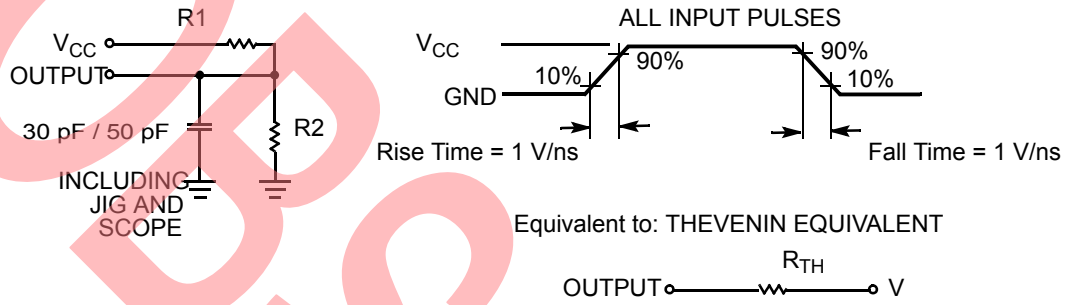
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Thermal Resistance

Parameter[11]	Description	Test Conditions	FBGA	TSOP II	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	39.3	35.62	°C / W
Θ_{JC}	Thermal resistance (Junction to case)		9.69	9.13	°C / W

AC Test Loads and Waveforms

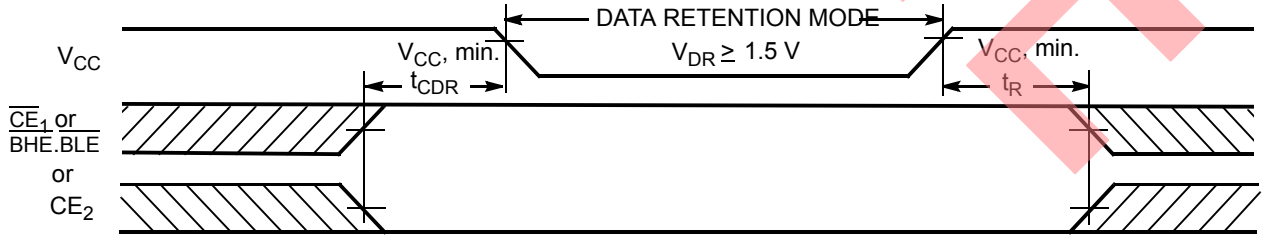


Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min	Typ[12]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}	Data retention current	V_{CC}= 1.5 V $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Ind'l	–	–	4	µA
t_{CDR}[11]	Chip deselect to data retention time			0	–	–	ns
t_R[13]	Operation recovery time			55	–	–	ns

Data Retention Waveform[14]



Notes
11. Tested initially and after any design or process changes that may affect these parameters
12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VCC = VCC(typ), TA = 25 °C
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

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Switching Characteristics Over the Operating Range

Parameter[15]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16, 17]	–	20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[16]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[16, 17]	–	20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-down	–	55	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	55	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[16]	10	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH Z[16, 17]	–	20	ns
Write Cycle[18]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	40	–	ns
t_{AW}	Address set-up to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	40	–	ns
t_{SD}	Data set-up to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[16, 17]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[16]	10	–	ns

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Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
18. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

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Switching Waveforms

Figure 1. Read Cycle 1 (Address Transition Controlled)[19, 20]

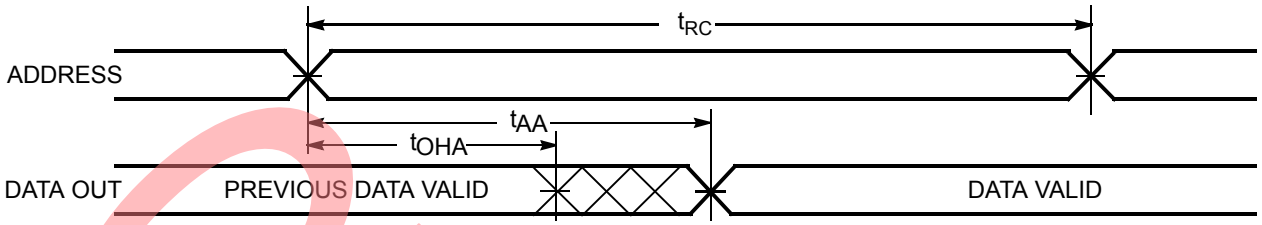
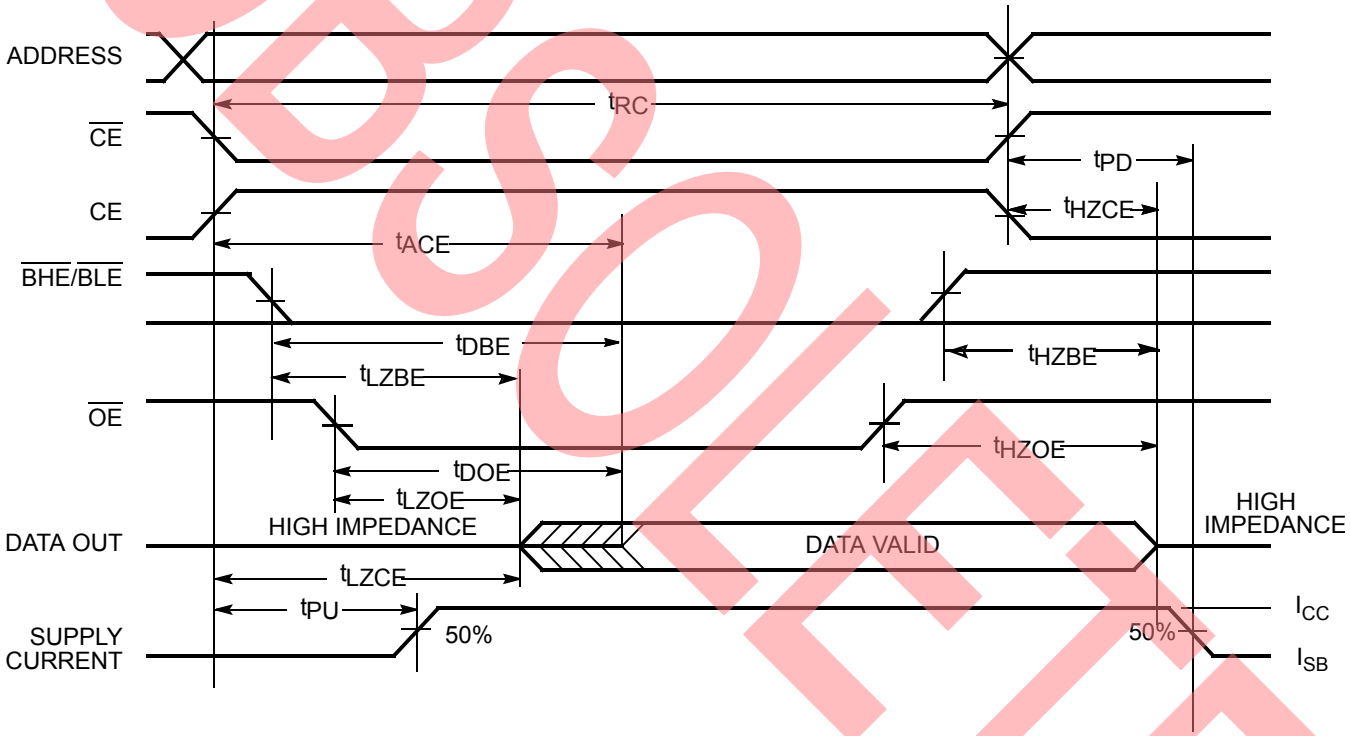


Figure 2. Read Cycle 2 ($\overline{OE}$ Controlled)[20, 21]



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Notes
19. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

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Switching Waveforms (continued)

Figure 3. Write Cycle 1 ($\overline{WE}$ Controlled)[22, 23, 24]

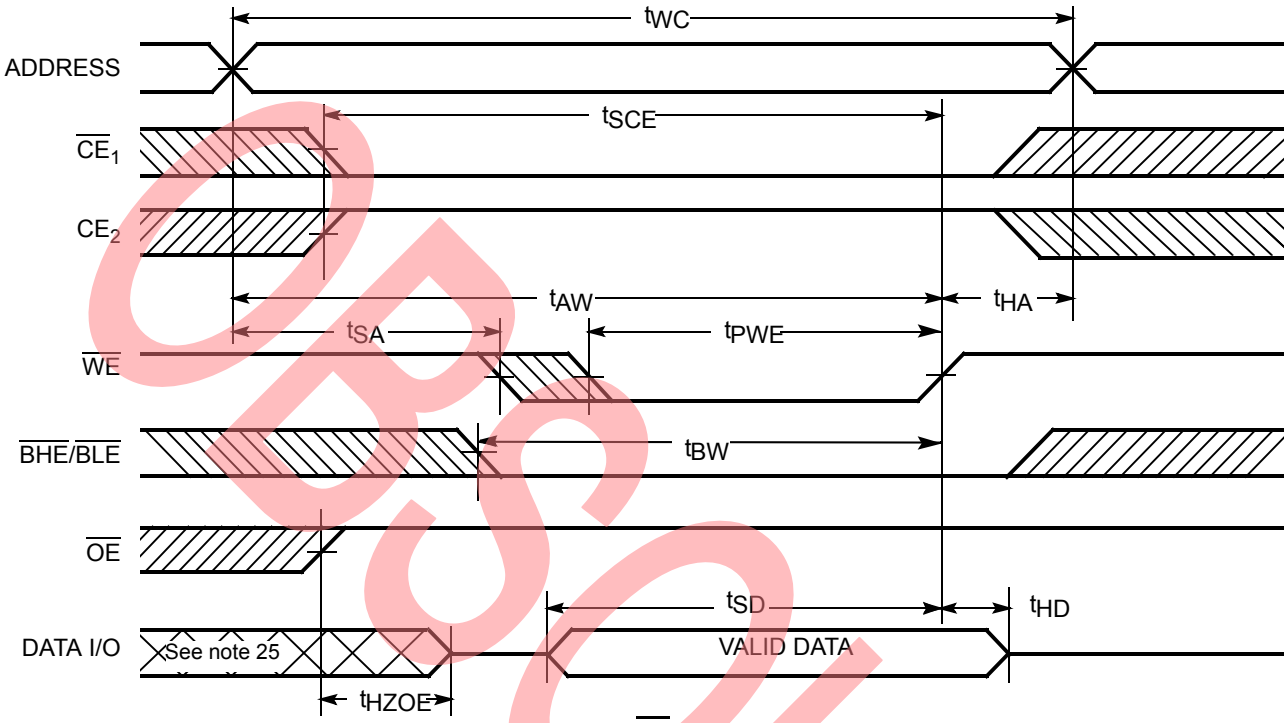
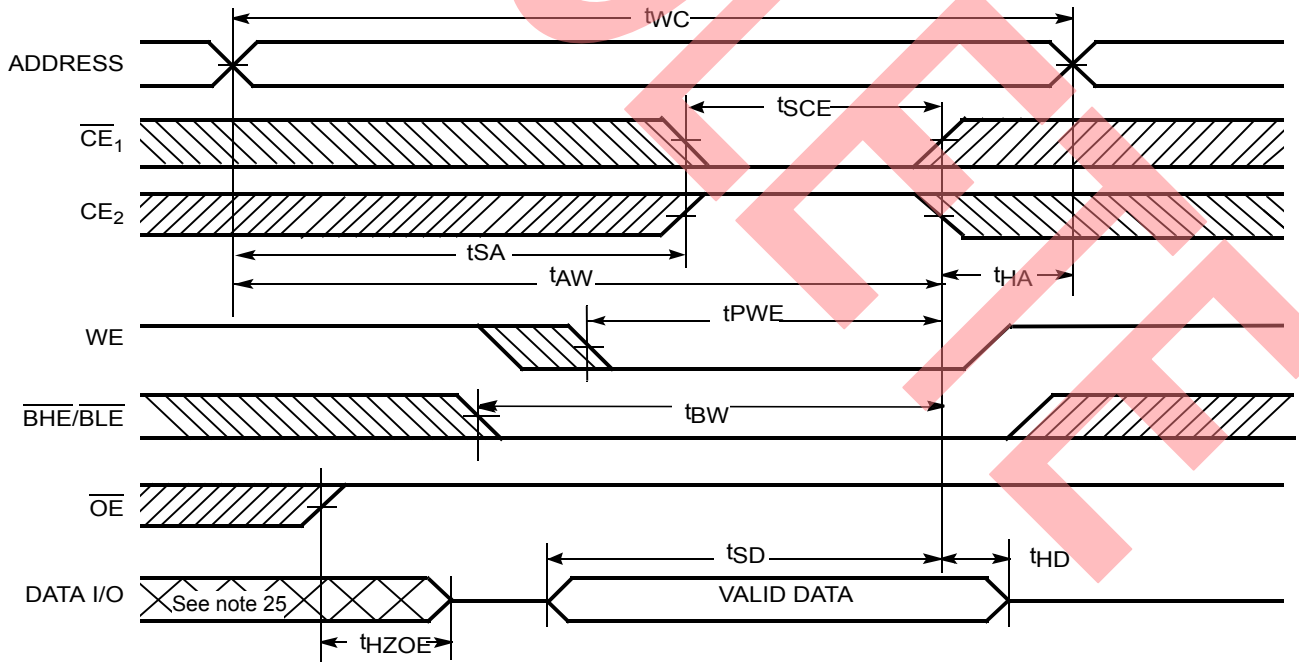


Figure 4. Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled)[22, 23, 24]



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Notes

22. The internal Write time of the memory is defined by the overlap of WE, $\overline{CE_1}$ = VIL, $\overline{BHE}$ and/or $\overline{BLE}$ = VIL, and CE_2 = VIH. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write
23. Data I/O is high-impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
25. During this period, the I/Os are in output state and input signals should not be applied.

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Switching Waveforms (continued)

Figure 5. Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[26]

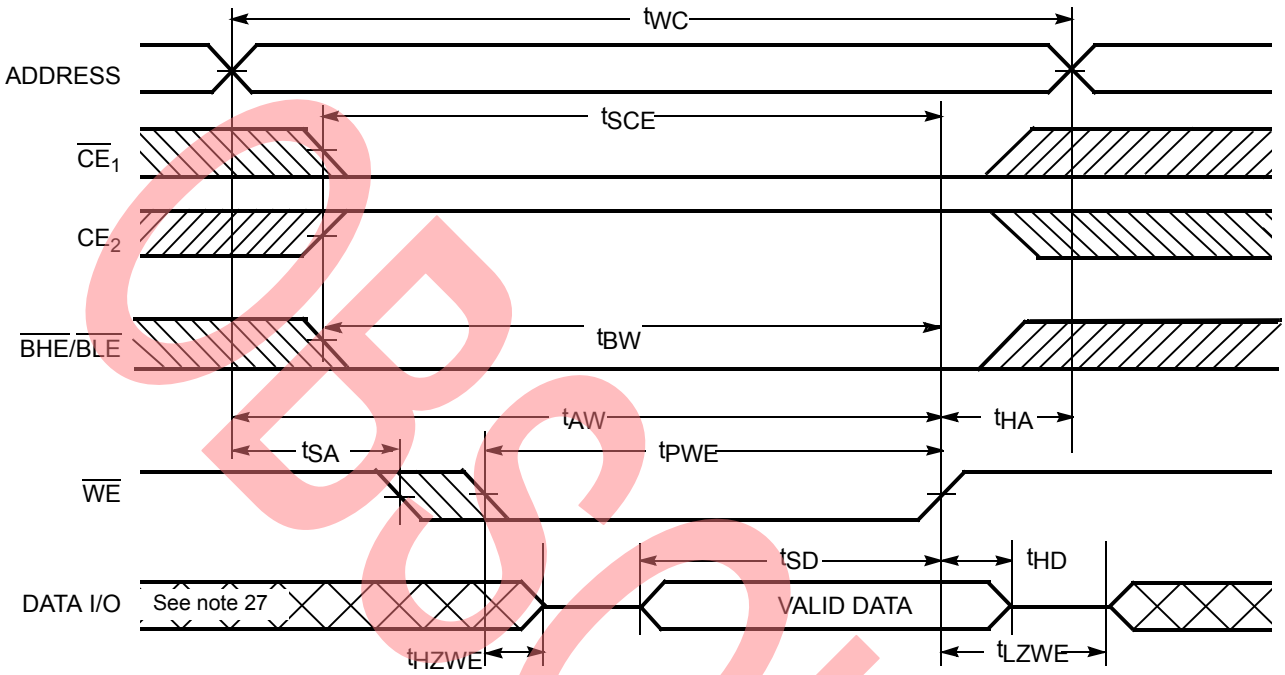
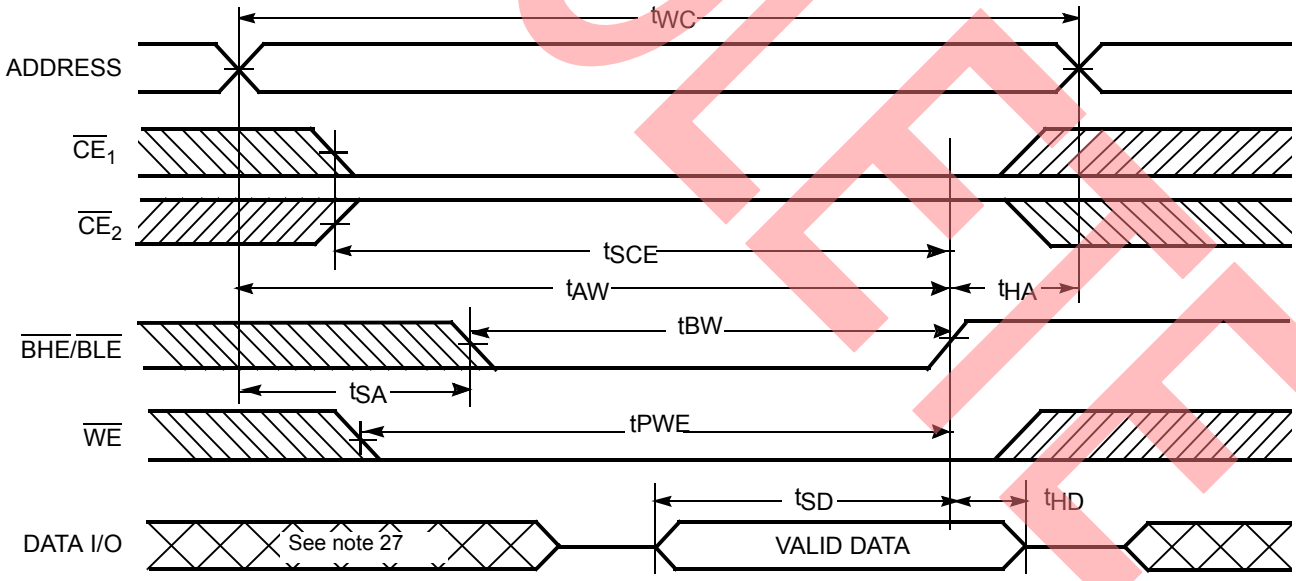


Figure 6. Write Cycle 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[26]



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Notes
26. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state
27. During this period, the I/Os are in output state and input signals should not be applied

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Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O_0–I/O_{15})	Read (upper byte and Lower byte)	Active (I_{CC})
L	H	H	L	H	L	Data out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read (lower byte only)	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data out (I/O_8–I/O_{15})	Read (upper byte only)	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O_0–I/O_{15})	Write (upper byte and Lower byte)	Active (I_{CC})
L	H	L	X	H	L	Data in (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write (lower byte only)	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data in (I/O_8–I/O_{15})	Write (upper byte only)	Active (I_{CC})

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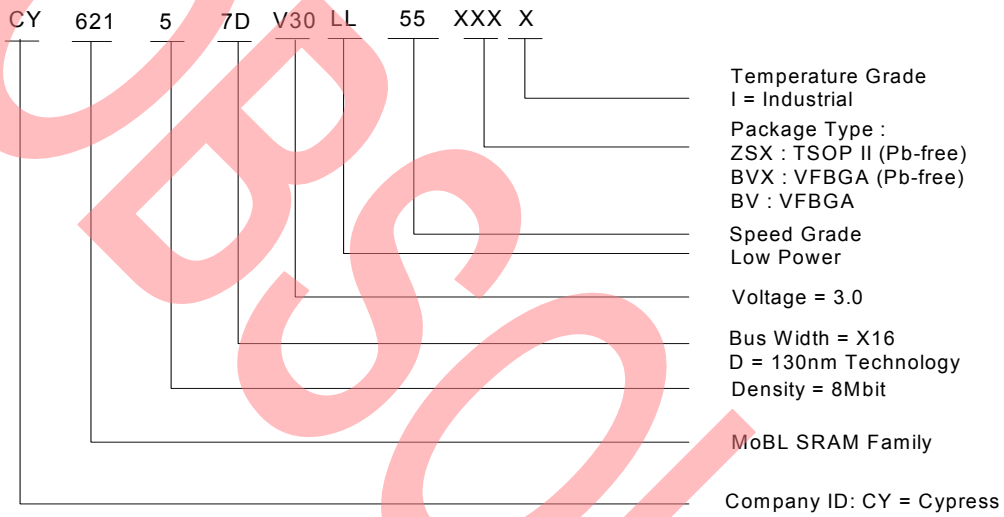
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Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62157DV30LL-55BVI	51-85150	48-ball (6 x 8 x 1 mm) FBGA	Industrial
	CY62157DV30LL-55BVXI		48-ball (6 x 8 x 1 mm) FBGA (Pb-free)	
	CY62157DV30LL-55ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Ordering Code Definition

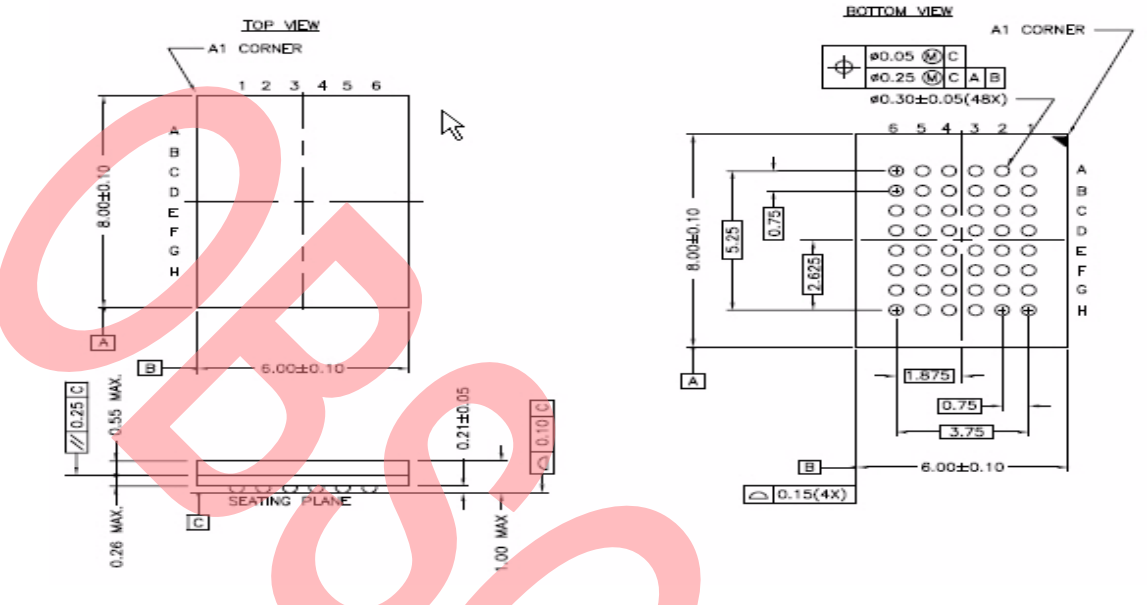


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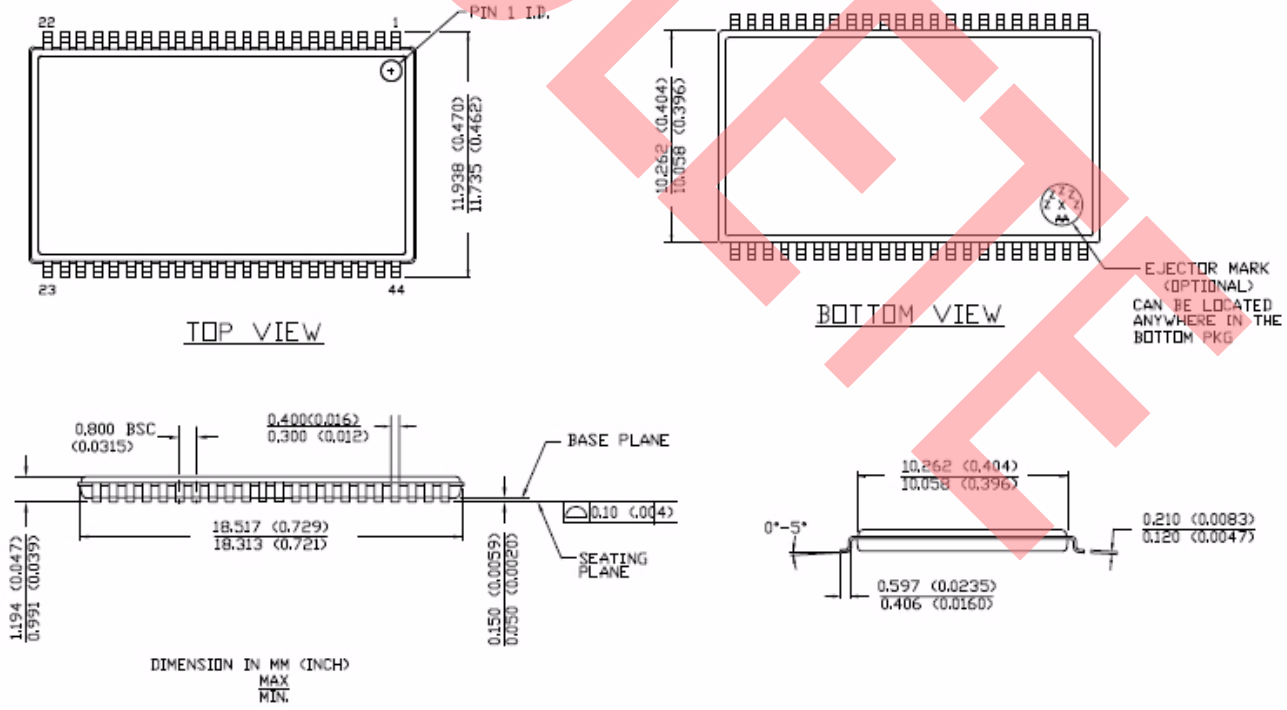
Package Diagram

Figure 7. 48-Pin VFBGA (51-85150)



51-85150 *F

Figure 8. 44-pin TSOP II (51-85087)



51-85087 *C

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Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball grid array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

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Document History Page

Document Title: CY62157DV30 MoBL® 8-Mbit (512K x 16) MoBL® Static RAM Document Number: 38-05392				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	126316	05/22/03	HRT	New Data Sheet
*A	131013	11/19/03	CBD/LDZ	Change from Advance to Preliminary
*B	133115	01/24/04	CBD	Minor Change: Change MPN and upload.
*C	211601	See ECN	AJU	Change from Preliminary to Final Changed Marketing part number from CY62157DV to CY62157DV30 in the title and in the Ordering Information table Added footnotes 4, 5 and 11 Modified footnote 8 to include ramp time and wait time Removed MAX value for VDR on Data Retention Characteristics table Changed ordering code for Pb-free parts Modified voltage limits in Maximum Ratings section
*D	236628	See ECN	SYT/AJU	Added 45-ns and 70-ns Speed Bins Added Automotive product information
*E	257349	See ECN	PCI	Added test condition for 45 ns part (footnote #13 on page 4)
*F	372074	See ECN	SYT	Added Pb-Free Automotive Part in the Ordering Information Removed 'Preliminary' tag from Automotive Information
*G	433838	See ECN	ZSD	Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Updated the thermal resistance table Updated the ordering information table and changed the package name column to package diagram
*H	488954	See ECN	VKN	Added Automotive-A product Updated ordering Information table
*I	2897932	03/23/2010	VKN	Removed 45ns speed bin Removed Auto-A/Auto-E information Removed 48-Pin TSOP I information Updated ordering Information table Updated package diagrams.
*J	3068300	10/25/2010	RAME	Removed CY62157DV30LL-70BVXI part related info Updated I_{SB1}/I_{SB2}/I_{CCDR} test conditions to reflect byte power down feature Updated datasheet as per new template Added Acronyms and Units of Measure table Added Ordering Code Definition Updated Package Diagram to 51-85150 *F Converted all tablenotes into footnotes
*K	3094203	11/24/2010	RAME	The specified parts in the ordering information table are being pruned. Obsolete datasheet.

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