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January 2008

74LVT240, 74LVTH240 Low Voltage Octal Buffer/Line Driver with 3-STATE Outputs

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH240), also available without bushold feature (74LVT240)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32mA/+64mA
- Functionally compatible with the 74 series 240
- Latch-up performance exceeds 500mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

General Description

The LVT240 and LVTH240 are inverting octal buffers and line drivers designed to be er leved as memory address drivers, clock drivers are ous conted transmitters or receivers which provide improved PC board density.

The LVTH240 dat inp.clude bushold, aliminating the need for extern put o sistors to hold unused inputs.

The plock of the prime drivers are designed for low-rolts. The VCC applications, but with the capability to vious Tile merface to a 5V environment. The LVT240 are LV. 1240 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissination.

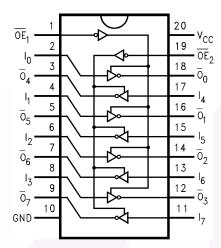
Ordering Informa on

Order N. 1ber	Çkaye N mber	Package Description
VIZ W.	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
VT24 J	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74L JMSA	iMSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LVT240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm
74LV 711240WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH240MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LVTH240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

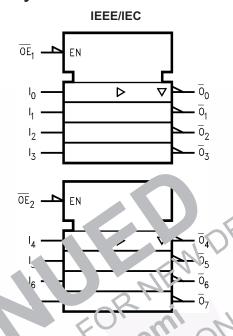
Connection Diagrams



Pin Descriptions

Pin Names	Description
\overline{OE}_1 , \overline{OE}_2	3-STATE Output Enable Inputs
I ₀ –I ₇	Inputs
$\overline{O}_0 - \overline{O}_7$	3-STATE Outputs

Logic Symbols



Tru 'n Tables

$\overline{OE}_1 \qquad I_n$	Outputs (Pins 12, 14, 16, 18)
10 150	Н
L	L
Н	Z

Inp	uts	Outputs
OE ₂	In	(Pins 3, 5, 7, 9)
L	L	Н
L	Н	L
Н	Х	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5V to +4.6V
V _I	DC Input Voltage	-0.5V to +7.0V
Vo	DC Output Voltage	
	Output in 3-STATE	-0.5V to +7.0V
	Output in HIGH or LOW State ⁽¹⁾	-0.5V to +7.0V
I _{IK}	DC Input Diode Current, V _I < GND	-50mA
I _{OK}	DC Output Diode Current, V _O < GND	-50mA
Io	DC Output Current, V _O > V _{CC}	
	Output at HIGH State	64mA
	Output at LOW State	128mA
I _{CC}	DC Supply Current per Supply Pin	±64mA
I _{GND}	DC Ground Current per Ground Pin	±128mA
T _{STG}	Storage Temperature	-65° C tc → 150° C

Note:

1. In Absolute Maximum Rating must be of a ved.

Recommended Operation Corditions

The Recommended Oproving Conditions able defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend excretely a more signing to assolute maximum ratings.

Symb	Pararieter	Min	Max	Units
~	Single oltage	2.7	3.6	V
VI	nput Voltage	0	5.5	V
Гон	HIGH Level Output Current		-32	mA
JL J	LOV/-Level Output Current		64	mA
TA	T _A Free-Air Cperating 1 mperature		85	°C
Δ+/ ΔV	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$		10	ns/V

DC Electrical Characteristics

		Vcc	T A =-	T _A =-40°C to +85°C		
Parameter	(V)	Conditions	Min.	Typ. ⁽²⁾	Max.	Units
Input Clamp Diode Voltage	2.7	I _I = -18mA			-1.2	V
Input HIGH Voltage	2.7–3.6	$V_0 \le 0.1V$ or	2.0			V
Input LOW Voltage	2.7–3.6	$V_O \ge V_{CC} - 0.1V$			0.8	V
Output HIGH Voltage	2.7–3.6	$I_{OH} = -100 \mu A$	V _{CC} -0.2			V
	2.7	$I_{OH} = -8mA$	2.4			
	3.0	$I_{OH} = -32mA$	2.0			
Output LOW Voltage	2.7	$I_{OL} = 100 \mu A$			0.2	V
		I _{OL} = 24mA			0.5	
	3.0	I _{OL} = 16mA			0.4	5
		$I_{OL} = 32mA$			0.5	
		I _{OL} = 64mA			0.55	
Bushold Input Minimum	3.0	V _I = 0.8V	75		1	μA
Drive		V _I = 2.0V	-75	190		
Bushold Input Over-Drive	3.0	(4)	500			μA
Current to Change State			-5υύ	9(1)		7
Input Current	3.5	- 5.5V		5 1	10	μA
Control Pins	3.0	V _I = V or V _{CC}	0/	10	±1	
Data Pins		$V_I = 0V$	2	5/4	-5	
		V _I = V _{C()}	Z.0		1	
Power Off Leakage Irrent	U	$uV \le V_1 \text{ or } V_0 \le 5.5V$	71		±100	μA
Power up/ Jwn 3-STA	0-1.5V	$V_0 = 0.5 \text{V to } 3.0 \text{V},$			±100	μA
	6					
STATE O. ut lakage	3.6	$V_0 = 0.5V$			– 5	μA
2 CTATE vutnut l 2 vara	(30)	W 10V			-	
	3.6	V _C = 3.0V			5	μA
	3.6	$V_{CC} \leq V_O \leq 5.5V$			10	μA
Current	W.					
Power Supply Current	3.6	Outputs HIGH			0.19	mA
Power Supply Cur ent	3.6	Outputs LOW			5	mA
Power Supply Current	3.6	Outputs Disabled			0.19	mA
Power Surply Current	3.6	$V_{CC} \le V_O \le 5.5V$,			0.19	mA
		Outputs Disabled				
Increase in Power Supply	3.6	One Input at V _{CC} – 0.6V,			0.2	mA
Current		Other Inputs at V _{CC} or GND				
	Input Clamp Diode Voltage Input HIGH Voltage Input LOW Voltage Output HIGH Voltage Output LOW Voltage Bushold Input Minimum Drive Bushold Input Over-Drive Current to Change State Input Current Control Pins Data Pins Power Off Leakage Irrent Power up/ Jwn 3-STA Output C 'ent STATE Output Leakage Unitent 3-STATE Jutput Leakage Current Power Supply Current	Input Clamp Diode Voltage Input HIGH Voltage Input LOW Voltage Output HIGH Voltage 2.7–3.6 2.7 3.0 Output LOW Voltage 2.7 3.0 Output LOW Voltage 2.7 3.0 Output LOW Voltage 2.7 3.0 Bushold Input Minimum Drive Bushold Input Over-Drive Current to Change State Input Current Control Pins Data Pins Power Up Dwn 3-STA Output C ent STATE Output Leakage Turrent 3.6 3-STATE Output Leakage Current Power Supply Current 3.6 Increase in Power Supply 3.6 Increase in Power Supply 3.6 Increase in Power Supply 3.6	$ \begin{array}{ c c c c } \hline \textbf{Parameter} & \textbf{(V)} & \textbf{Conditions} \\ \hline \textbf{Input Clamp Diode Voltage} & 2.7 & \textbf{I}_{1} = -18 \text{mA} \\ \hline \textbf{Input HIGH Voltage} & 2.7-3.6 & \textbf{V}_{O} \leq 0.1 \text{V or} \\ \hline \textbf{Input LOW Voltage} & 2.7-3.6 & \textbf{I}_{OH} = -100 \mu \text{A} \\ \hline \textbf{2.7} & \textbf{I}_{OH} = -8 \text{mA} \\ \hline \textbf{3.0} & \textbf{I}_{OH} = -32 \text{mA} \\ \hline \textbf{3.0} & \textbf{I}_{OH} = -32 \text{mA} \\ \hline \textbf{3.0} & \textbf{I}_{OL} = 24 \text{mA} \\ \hline \textbf{3.0} & \textbf{I}_{OL} = 16 \text{mA} \\ \hline \textbf{I}_{OL} = 32 \text{mA} \\ \hline \textbf{I}_{OL} = 30 \text{mA} \\ \hline \textbf{I}_{OL} = 32 \text{mA} \\ \hline \textbf{I}_$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Parameter	Parameter

Notes:

- 2. All typical values are at $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$.
- 3. Applies to bushold versions only (74LVTH240).
- 4. An external driver must source at least the specified current to switch from LOW-to-HIGH.
- 5. An external driver must sink at least the specified current to switch from HIGH-to-LOW.
- 6. This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics⁽⁷⁾

			Conditions	1	T _A = 25°0	C	
Symbol	Parameter	V _{CC} (V)	$C_L = 50 pF, R_L = 500 \Omega$	Min.	Тур.	Max.	Units
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	(8)		0.8		V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	(8)		-0.8		V

Notes:

- 7. Characterized in SOIC package. Guaranteed parameter, but not tested.
- 8. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

		$T_A = -40^{\circ}$ to $C_L = 50$ pF, =	C 100	D
		V _{CC} = 3. V ± 3V	$V_{CC} = 2.7V$	
Symbol	Parameter	Min. Tyo	Min. Max.	Units
t _{PLH}	Propagation Delay, Data to Output	1.1 3.8	1.1 4.6	ns
t _{PHL}		1.3	1.3	
t _{PZH}	Output Enable Time	1 4.6	1.1 5.6	ns
t _{PZL}		1 4.4	1.4 5.1	
t _{PHZ}	Output Disable Tim	2.0 4.5	2.0 4.7	ns
t _{PLZ}		4.3	1.8 4.3	
t _{OSHL} , t _{OSLH}	Output tr Junjut & W(10)	7.0	1.0	ns

Notes:

- 9. All typical values are $\frac{1}{2}$ 3.3V T_A = 25°C.
- 10. Skew de as absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, output to to be with the contraction of the difference between the actual propagation delay for any two separate outputs of the same direction, outputs switching in the same direction, outputs to be the difference between the actual propagation delay for any two separate outputs of the difference between the actual propagation delay for any two separate outputs of the difference between the actual propagation delay for any two separates outputs of the difference between the actual propagation delay for any two separates outputs of the difference between the actual propagation delay for any two separates outputs of the difference between the actual propagation delay for any two separates outputs of the difference between the actual propagation delay for any two separates outputs of the difference between the actual propagation delay for any two separates of the difference between the actual propagation delay for any two separates of the difference between the actual propagation delay for any two separates of the difference between the actual propagation delay for any two separates of the difference between the delay for a separate output separates of the difference between the delay for a separate output separates of the delay for a separate output separates output separates of the delay for a separate output separates outpu

Cap Litange (11)

Symbol	Pararieter	Conditions	Typical	Units
CIN	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	3	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_{O} = 0V$ or V_{CC}	6	pF

Note:

11. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

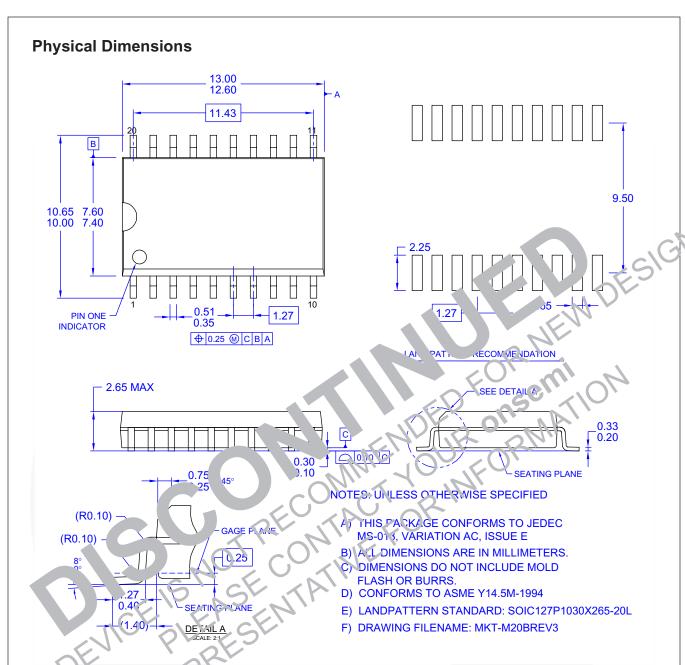


Figure 1. 20-Levi Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued) 12.6±0.10 0.40 TYP -A-20 11 12 11 5.01 TYP 5.3±0.10 9.27 TYP 7.8 -B-3.9 (2.13)△ 0.2 C B A ALL LEAD TIPS 10 PIN #1 IDENT. J.6 TYP 1.27 ALL LEAD TIPS △ 0.1 C 2.1 MAX.--C-0.15 - 0.250.35-0.51 1.27 TYP 7° TYP ARE IN MILLIMATER GAGE PLANE 0.25 0°-8° TYP CONFORMS TO LIAU EDG-7320 REGISTRATION ESTABLISHED IN DECEMBER, 1998. D.Y.L.NSIONS ARE EXCLUSIVE OF TURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. 0.60 ± 0.15 SEATING PLANE 1.25 -DETAIL A

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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M20DREVC

Physical Dimensions (Continued) 7.2±0.30 0.68 TYP В 9.12 5.58 5.3±0.30 7.8 10 3.9 ○ 0.2 C A B PIN #1 IDENT. RECOMMENDATIONS △ 0.10 C ALL LEAD TIPS 1.75±0 2.0 MAX. 0.65 TYP 0.15M L GAGE PLANE NOTES 0.25 NFORMS TO JEDIC REGISTRATION ARIATION AC, LATE 1/94. DIMENSIONS ARE IN MILLINIZIERS. 0.75±0.2 DIMENSIONS ARE FACLUSIVE CF DURRS, MOLD FLASH, AND THE BAR EXTRUSIONS SEATING PLANE (1.25)CIMENSIONS AND TOLERAILC'S PER ASME Y14.5M - 1994. DETAIL A

Figure 3. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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SA20REVB

Physical Dimensions (Continued) 5.5±0.1 -A--0.20 وحا 4.16 6,4 4.4±0.1 -B-3,2 0.2 C B A 0.65 ALL LEAD PIN #1 IDENT. O.1 C -0.90 1.2 -C-0.09-0.20 0.05 0.65 -12.00° GAGE PLANE 0.25 SEATING PLANE CONFORMS TO JEDEC RESISTRATION MIL-133 REF NOTE 6, DATE 7/33. VARIATION AC, -0.6±0.1-R0.09min DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS

MTC20REVD1

D. DIMENSIONS AND TO ERANCES PER ANSI Y14.5M, 1982.

Figure 4. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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DETAIL A





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