# UPC451, UPC324

## Single Power Supply Quad Operational Amplifiers

### DESCRIPTION

UPC451, UPC324 are quad operational amplifiers designed to operate on a single power supply. The features include low-voltage operation, a common-mode input voltage that range from $V^-$ (GND) level, an output from a $V^-$ (GND) level that is determined by the output stage of class C push-pull circuit and a 50 μA(TYP.) constant current, and a low current consumption.

In addition to that, this amplifier can also operate in both positive and negative power supply and can be used extensively in various amplifier circuits.

The UPC451 is suited for wide operating ambient temperature use due to its temperature expansion type, while UPC324 is for general purposes usage.

A DC parameter selection that is compatible to operational amplifiers is also available.

UPC1251, UPC358 which are dual types with the same circuit configuration are also available under this series of operational amplifiers.

### FEATURES

- Input Offset Voltage ±2 mV (TYP.)
- Input Offset Current ±5 nA (TYP.)
- Large Signal Voltage Gain 100000 (TYP.)
- Internal Frequency Compensation
- Output Short-Circuit Protection

### ORDERING INFORMATION

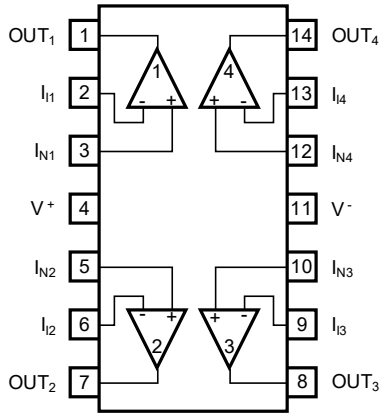
| Order Name (1) | Selected Grade | Package |
|---|---|---|
| UPC451G2-AP | Standard | 14-Pin plastic SOP ( 5.72 mm ( 225 )) |
| UPC451G2(5)-AP | DC parameter selection | 14-Pin plastic SOP ( 5.72 mm ( 225 )) |
| UPC324G2-AP | Standard | 14-Pin plastic SOP ( 5.72 mm ( 225 )) |
| UPC324G2(5)-AP | DC parameter selection | 14-Pin plastic SOP ( 5.72 mm ( 225 )) |
| UPC451GR-9LG-A | Standard | 14-Pin plastic TSSOP ( 5.72 mm ( 225 )) |
| UPC451GR(5)-9LG-A | DC parameter selection | 14-Pin plastic TSSOP ( 5.72 mm ( 225 )) |
| UPC324GR-9LG-A | Standard | 14-Pin plastic TSSOP ( 5.72 mm ( 225 )) |
| UPC324GR(5)-9LG-A | DC parameter selection | 14-Pin plastic TSSOP ( 5.72 mm ( 225 )) |

(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

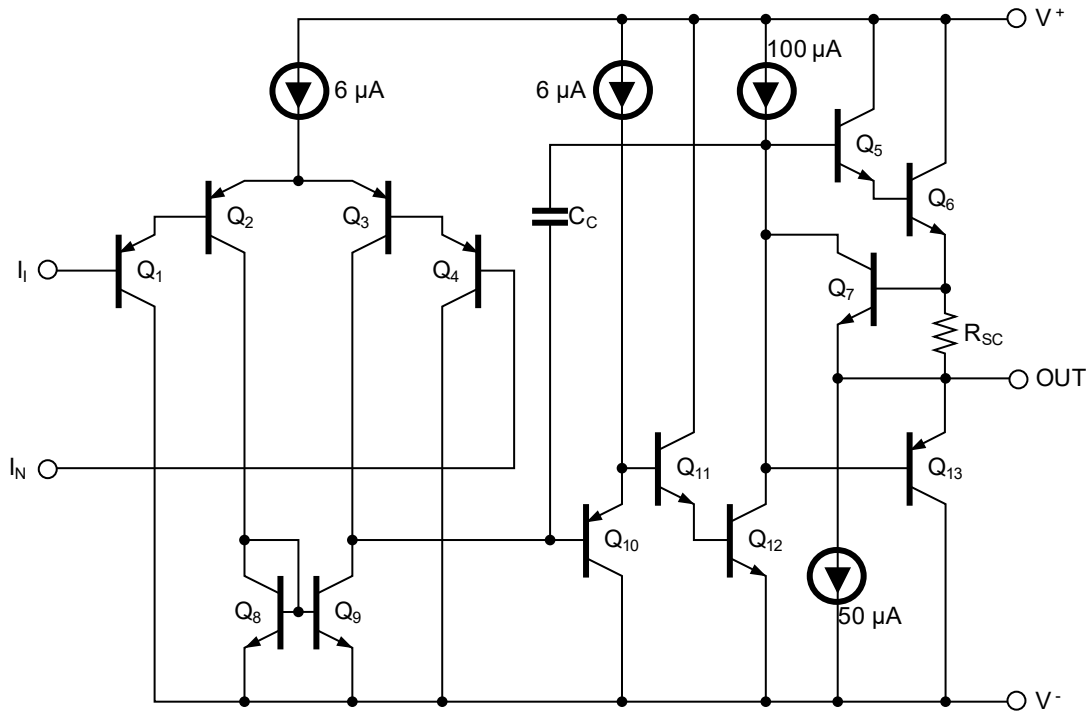


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## PIN CONFIGURATION (Marking side)




## EQUIVALENT CIRCUIT (1/2 Circuit)






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## ABSOLUTE MAXIMUM RATINGS

($T_A$ = 25 °C)

| Parameter | Symbol | UPC451G2, UPC451G2(5) | UPC324G2, UPC324G2(5) | UPC451GR, UPC451GR(5) | UPC324GR, UPC324GR(5) | Unit |
|---|---|---|---|---|---|---|
| Voltage between $V^+$ and $V^-$ Note1 | $V^+$ - $V^-$ | -0.3 ~ +32 | | | | V |
| Differential Input Voltage | $V_{ID}$ | ±32 | | | | V |
| Input Voltage Note 2 | $V_I$ | $V^-$ -0.3 ~ $V^-$ +32 | | | | V |
| Output applied Voltage Note3 | $V_O$ | $V^-$ -0.3 ~ $V^+$ +0.3 | | | | V |
| Total Power Dissipation Note4 | $P_T$ | 550 | | | | mW |
| Output Short Circuit Duration Note5 | $t_S$ | Indefinite | | | | s |
| Operating Ambient Temperature | $T_A$ | -40 ~ +85 | -20 ~ +80 | -40 ~ +125 | -40 ~ +85 | °C |
| Storage Temperature | $T_{stg}$ | -55 ~ +125 | | -55 ~ +150 | -55 ~ +125 | °C |

【Note】 **1.** Note that reverse connections of the power supply may damage the ICs.

**2.** The input voltage is allowed to input without damage or destruction independent of the magnitude of $V^+$. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

**3.** A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

**4.** This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.
Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

UPC451G2, 324G2 : Derate at -5.5 mW/°C when $T_A$ > 25 °C
UPC451GR-9LG : Derate at -7.0 mW/°C when $T_A$ > 71°C
(Junction − ambient thermal resistance $R_{th(J-A)}$ = 144°C/W)
UPC324GR-9LG : Derate at -7.0 mW/°C when $T_A$ > 46 °C
(Junction − ambient thermal resistance $R_{th(J-A)}$ = 144°C/W)

**5.** Short circuits from the output to $V^+$ can cause destruction. ($V^+$ ≤ +15V, for any one channel only) Pay careful attention to the total power dissipation by not exceeding the absolute maximum ratings, **Note 4**.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage (Dual) | $V^±$ | ±1.5 | | ±15 | V |
| Power Supply Voltage ($V^-$ = GND) | $V^+$ | +3 | | +30 | V |



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## ELECTRICAL CHARACTERISTICS

UPC451, UPC324 ($T_A$ = 25 °C, $V^+$ = +5 V, $V^-$ = GND)

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | | ±2 | ±7 | mV | $R_S$ = 0 Ω |
| Input Offset Current | $I_{IO}$ | | ±5 | ±50 | nA | |
| Input Bias Current Note 6 | $I_B$ | | 15 | 250 | nA | |
| Large Signal Voltage Gain | $A_V$ | 25000 | 100000 | | | $R_L$ ≥ 2 kΩ |
| Circuit Current Note 7 | $I_{CC}$ | | 1.2 | 2.0 | mA | $R_L$ = ∞, $I_O$ = 0 A |
| Common Mode Rejection Ratio | CMR | 65 | 85 | | dB | |
| Supply Voltage Rejection Ratio | SVR | 65 | 100 | | dB | |
| Output Voltage Swing | $V_O$ | 0 | | $V^+$ -1.5 | V | $R_L$ = 2 kΩ (Connected to GND) |
| Common Mode Input Voltage Range | $V_{ICM}$ | 0 | | $V^+$ -1.5 | V | |
| Output Source Current | $I_{O\ SOURCE}$ | 20 | 40 | | mA | $V_{IN\ (+)}$ = +1 V, $V_{IN\ (-)}$ = 0 V |
| Output Sink Current | $I_{O\ SINK1}$ | 10 | 20 | | mA | $V_{IN\ (-)}$ = +1 V, $V_{IN\ (+)}$ = 0 V |
| | $I_{O\ SINK2}$ | 12 | 50 | | μA | $V_{IN\ (-)}$ = +1 V, $V_{IN\ (+)}$ = 0 V, $V_O$ = 200 mV |
| Channel Separation | | | 120 | | dB | f = 1 ~ 20 kHz |

UPC451 (5), UPC324 (5) ($T_A$ = 25 °C, $V^+$ = +5 V, $V^-$ = GND)

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | | ±2 | ±3 | mV | $R_S$ = 0 Ω |
| Input Offset Current | $I_{IO}$ | | ±5 | ±50 | nA | |
| Input Bias Current Note 6 | $I_B$ | | 15 | 60 | nA | |
| Large Signal Voltage Gain | $A_V$ | 50000 | 100000 | | | $R_L$ ≥ 2 kΩ |
| Circuit Current Note7 | $I_{CC}$ | | 1.2 | 1.5 | mA | $R_L$ = ∞, $I_O$ = 0 A |
| Common Mode Rejection Ratio | CMR | 65 | 85 | | dB | |
| Supply Voltage Rejection Ratio | SVR | 65 | 100 | | dB | |
| Output Voltage Swing | $V_O$ | 0 | | $V^+$ -1.5 | V | $R_L$ = 2 kΩ (Connected to GND) |
| Common Mode Input Voltage Range | $V_{ICM}$ | 0 | | $V^+$ -1.4 | V | |
| Output Source Current | $I_{O\ SOURCE}$ | 30 | 40 | | mA | $V_{IN\ (+)}$ = +1 V, $V_{IN\ (-)}$ = 0 V |
| Output Sink Current | $I_{O\ SINK1}$ | 15 | 20 | | mA | $V_{IN\ (-)}$ = +1 V, $V_{IN\ (+)}$ = 0 V |
| | $I_{O\ SINK2}$ | 30 | 50 | 70 | μA | $V_{IN\ (-)}$ = +1 V, $V_{IN\ (+)}$ = 0 V, $V_O$ = 200 mV |
| Channel Separation | | | 120 | | dB | f = 1 ~ 20 kHz |

【Note】 **6.** The absolute value of the input bias current is small, thus the direction of the current flowing from the inside of the IC may be reversed due to variations in the product during high temperature.

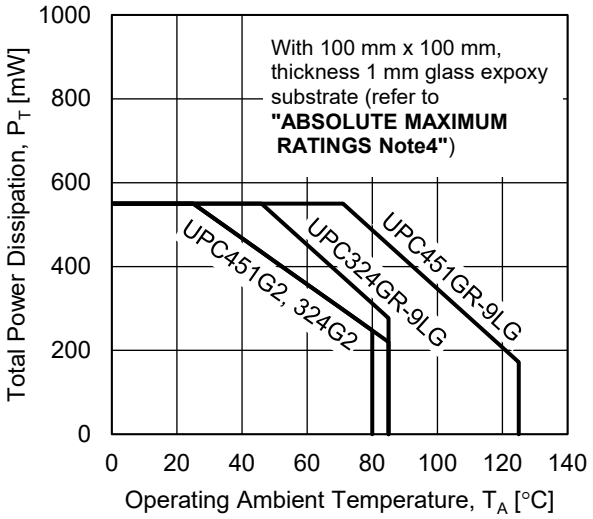
**7.** This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.



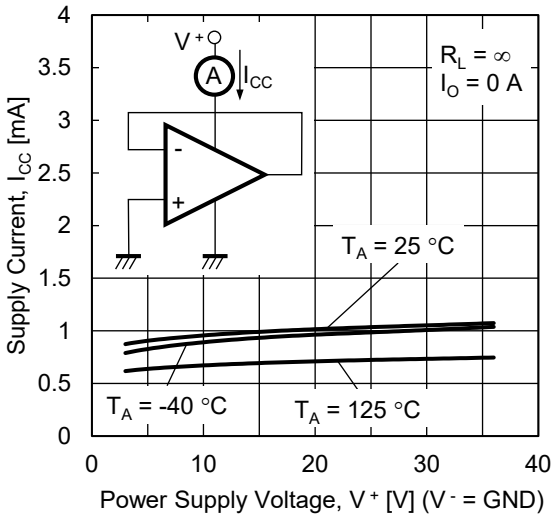
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## TYPICAL PERFORMANCE CHARACTERISTICS ($T_A$ = 25 °C, TYP.) (Reference value)

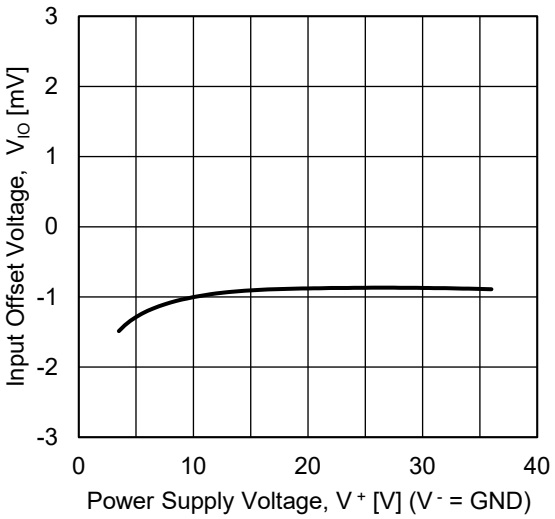
$P_T$ vs. $T_A$



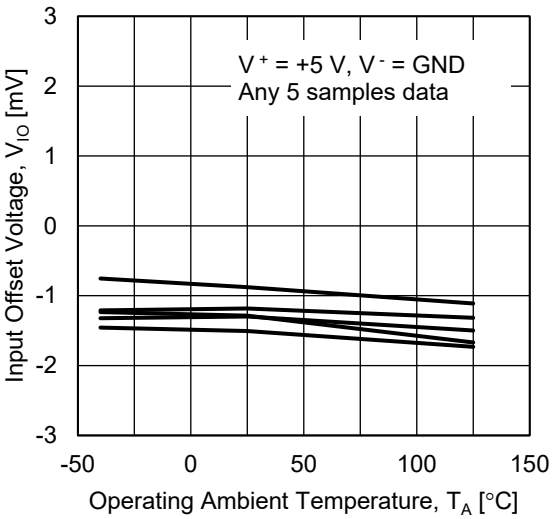

$I_{CC}$ vs. $V^+$



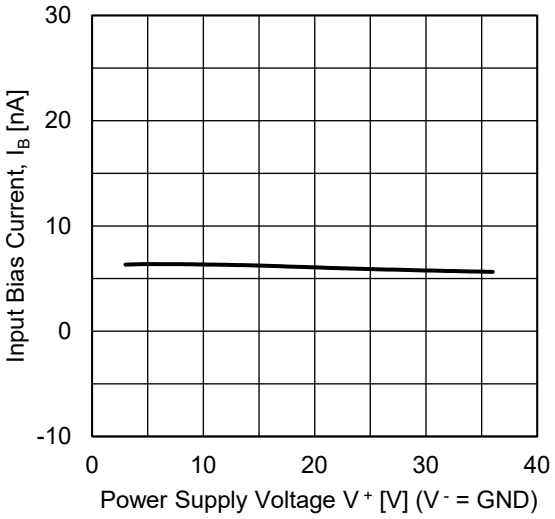

$V_{IO}$ vs. $V^+$



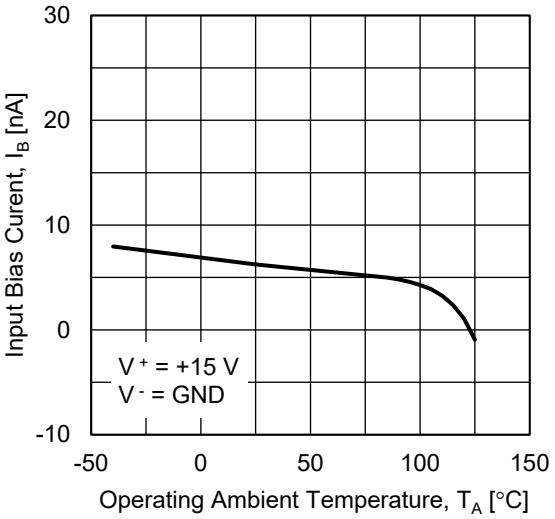

$V_{IO}$ vs. $T_A$




$I_B$ vs. $V^+$



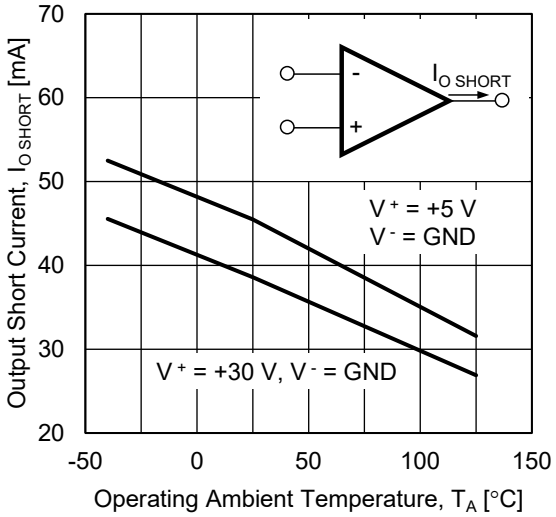

$I_B$ vs. $T_A$



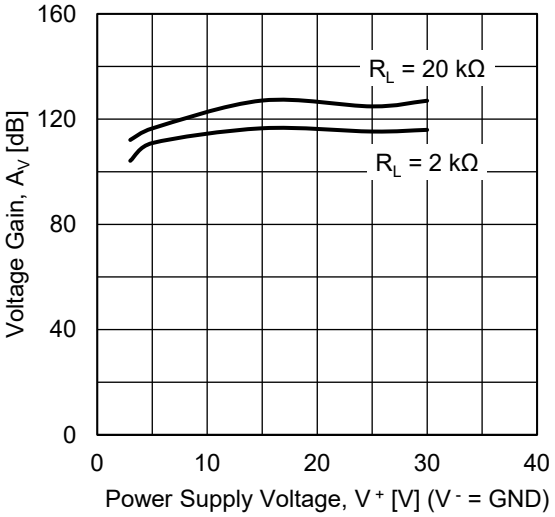



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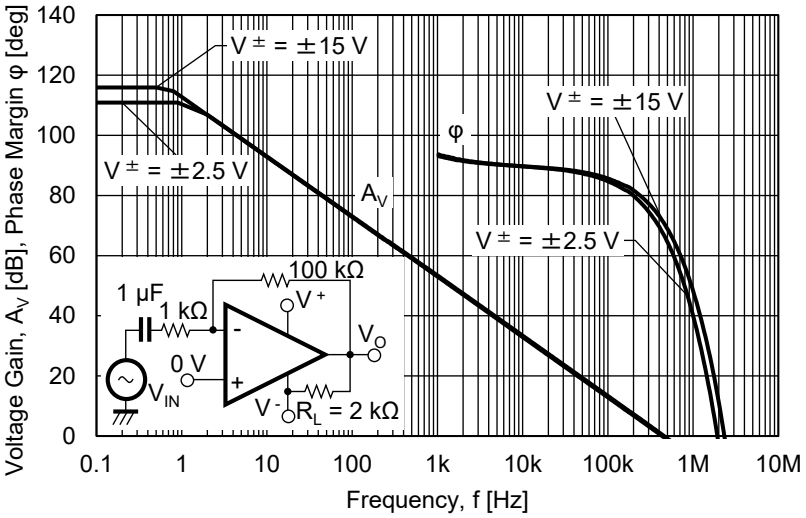
$I_{O\ SHORT}$ vs. $T_A$



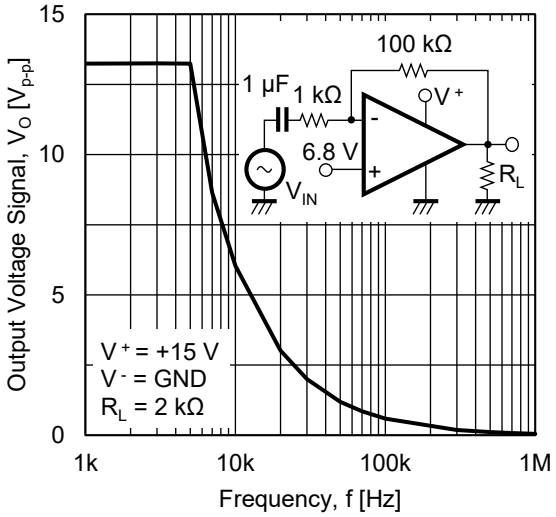

$A_V$ vs. $V^+$



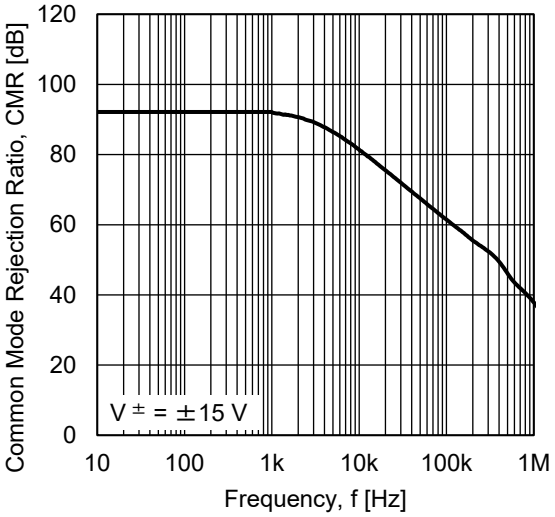

$A_V$, φ vs. f




$V_O$ vs. f

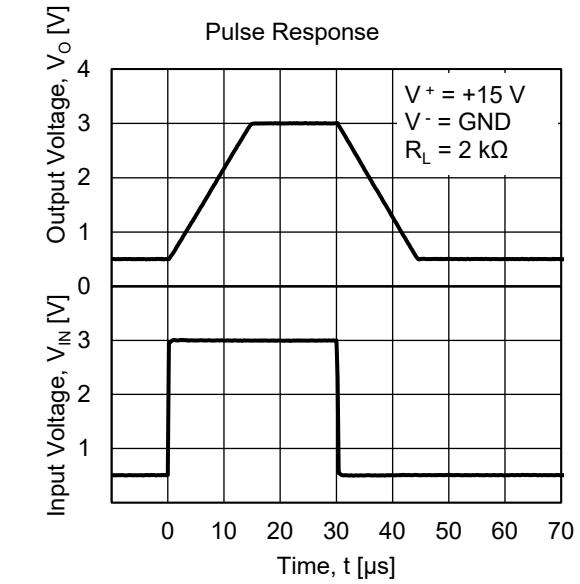


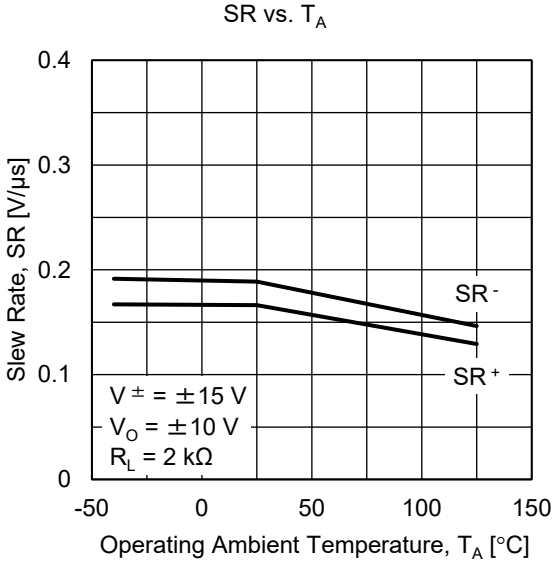

CMR vs. f

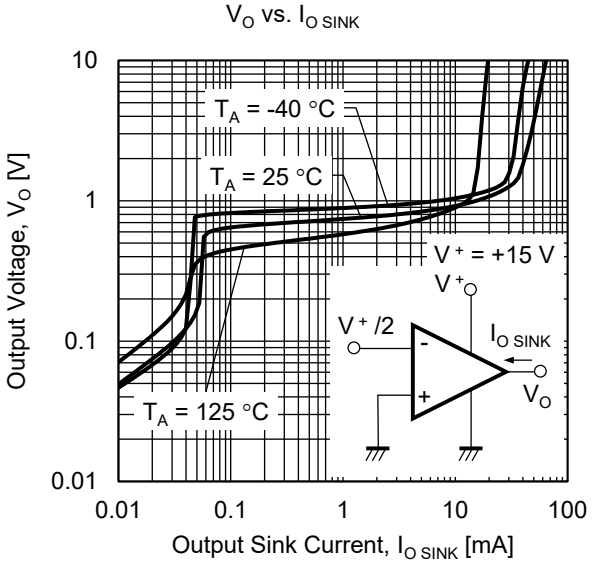


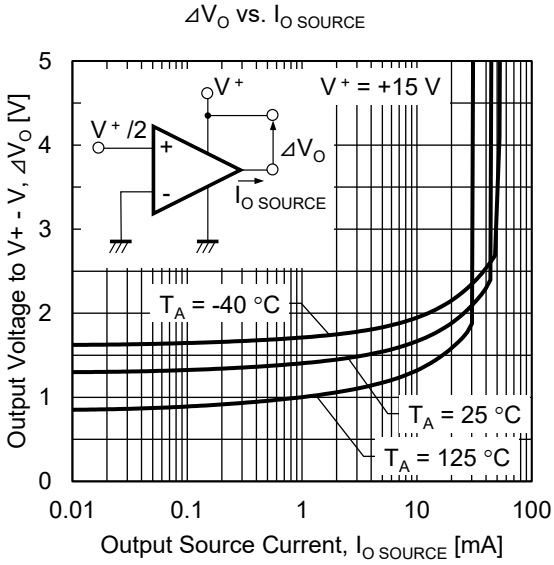



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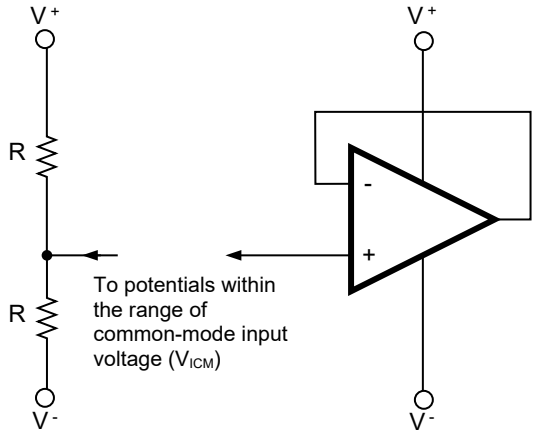

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## PRECAUTIONS

- **The process of unused circuits**

  If there is an unused circuit, the following connection is recommended.

**Process example of unused circuits**




**Remark** A midpoint potential of $V^+$ and $V^-$ is applied to this example.

- **Ratings of input/output pin voltage**

  When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damage, by a conduction of a parasitic diode within an IC. In addition, if the input pin is lower than $V^-$, or the output pin may exceed the power supply voltage, it is recommended to make a clump circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

  $V_{ICM}$ (TYP.): $V^-$ to $V^+ - 1.5$ (V) ($T_A$ = 25°C).

  During designing, do include some tolerance by considering temperature characteristics and etc.

- **Maximum output voltage**

  The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

  $V_{om}^+$ (TYP.): $V^+ - 1.5$ [V] ($T_A$ = 25°C), $V_{om}^-$ (TYP.) ($I_{O\ SINK} \leq 50$ µA): Approx. $V^-$ (V) ($T_A$ = 25°C)

  During designing, include some tolerance such as characteristics variation and temperature characteristics consideration and so forth. In addition, also note that the output voltage range ($V_{om}^+ - V_{om}^-$) will become narrow when an output current increases.

- **Operation of output**

  This IC output level consist of a class C push-pull. Therefore, when a load resistance is connected to the midpoint potential of $V^+$, $V^-$, a crossover distortion occurs during the transition state of output current flow direction (source, sink).

- **Handling of ICs**

  When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

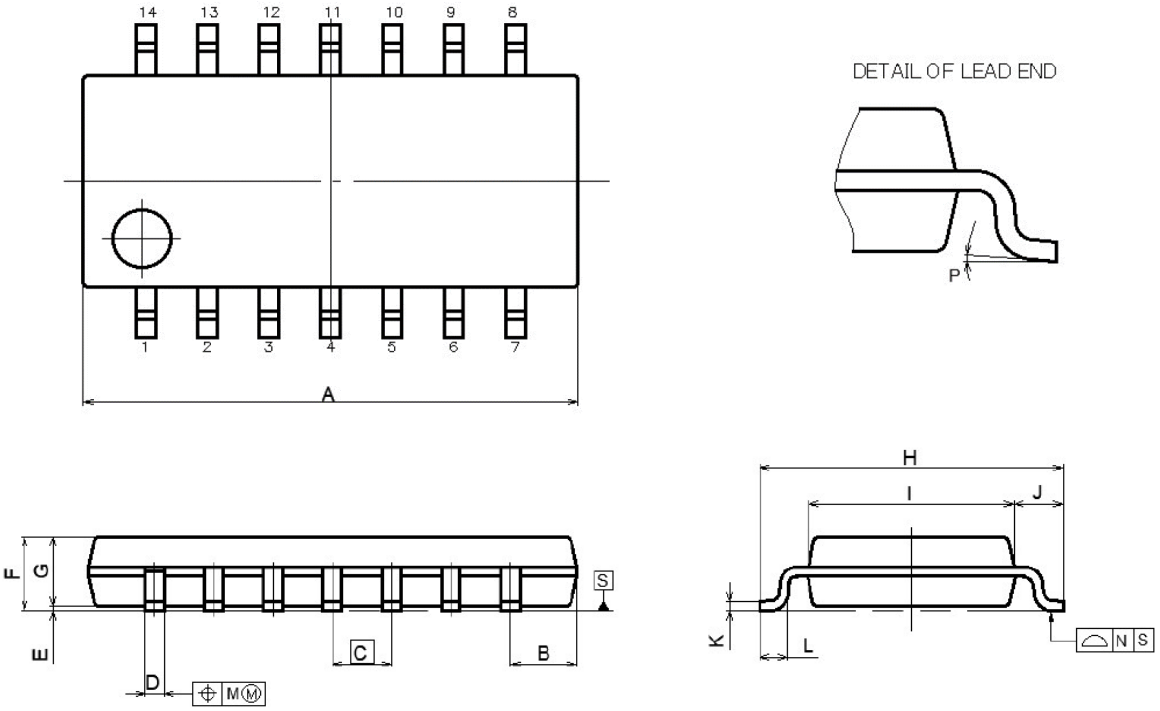


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## PACKAGE DRAWINGS

### 14-Pin PLASTIC SOP

| JEITA Package code | RENESAS code | MASS (TYP.) [g] |
|---|---|---|
| P-LSOP14-4.4×10.2-1.27 | PLSP0014DB-A | 0.17[g] |




NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF
ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

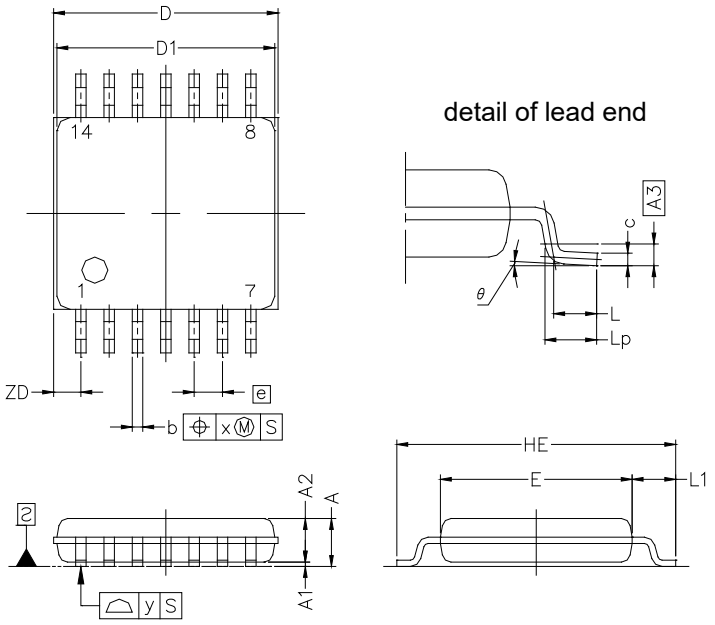
| ITEM | DIMENSIONS |
|---|---|
| A | 10.2±0.2 |
| B | 1.42MAX |
| C | 1.27(T.P) |
| D | 0.40±0.05 |
| E | 0.1±0.1 |
| F | 1.59±0.20 |
| G | 1.49±0.1 |
| H | 6.5±0.2 |
| I | 4.4±0.1 |
| J | 1.05±0.15 |
| K | 0.2±0.07 |
| L | 0.6±0.20 |
| M | 0.1MAX |
| N | 0.1MAX |
| P | 4°±4° |



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**14-Pin PLASTIC TSSOP**

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.) [g] |
|---|---|---|---|
| P-TSSOP14-0225-0.65 | PTSP0014JB-A | P14GR-65-9LG-1 | — |




Unit : mm

| ITEM | MILLIMETERS |
|---|---|
| D | 5.15 ±0.15 |
| D1 | 5.00 ±0.10 |
| E | 4.40 ±0.10 |
| HE | 6.40 ±0.20 |
| A | 1.20 MAX. |
| A1 | 0.10 ±0.05 |
| A2 | 1.00 ±0.05 |
| A3 | 0.25 |
| b | 0.24 +0.06 -0.05 |
| c | 0.145 ±0.055 |
| L | 0.5 |
| Lp | 0.60 ±0.15 |
| L1 | 1.00 ±0.20 |
| θ | 3° +5° -3° |
| e | 0.65 |
| x | 0.10 |
| y | 0.10 |
| ZD | 0.625 |

**NOTE**

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.



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